TLE4675

Low Drop Out Linear Voltage Regulator
5V Fixed Output Voltage

Automotive Power

Never stop thinking

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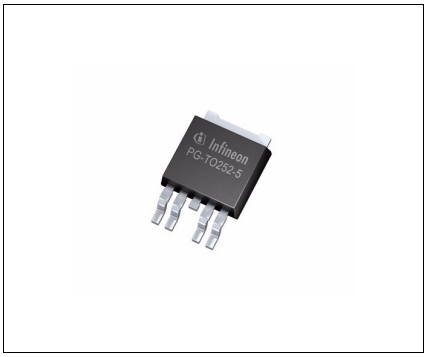
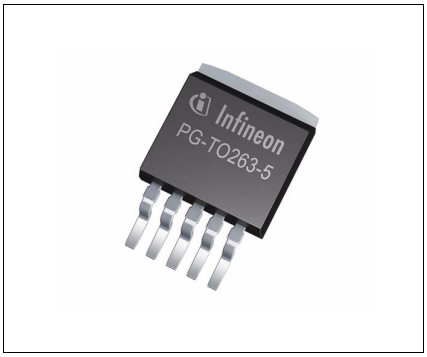
Low Drop Out Linear Voltage Regulator **TLE4675**
5V Fixed Output Voltage

1 Overview



PG-TO252-5



PG-TO263-5

Features

- Output Voltage 5 V ± 2%
- Output Current Capability 400 mA
- Ultra Low Current Consumption
- Very Low Drop Out Voltage
- Reset Circuit Sensing the Output Voltage with Programmable Delay Time
- Reset Output Active Low Down to V_Q = 1 V
- Excellent Line Transient Robustness
- Maximum Input Voltage -42 V ≤ V_I ≤ +45 V
- Reverse Polarity Protection
- Short Circuit Protected
- Overtemperature Shutdown
- Automotive Temperature Range -40 °C ≤ T_j ≤ 150 °C
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE4675 is a monolithic integrated low drop out fixed output voltage regulator for loads up to 400 mA. An input voltage up to 45 V is regulated to an output voltage of 5 V. The integrated reset function, as well as several protection circuits combined with the wide operating temperature range offered by the TLE4675 make it suitable for supplying microprocessor system in automotive environments.

Type	Package	Marking
TLE4675D	PG-TO252-5	TLE4675
TLE4675G	PG-TO263-5	TLE4675

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2 Block Diagram

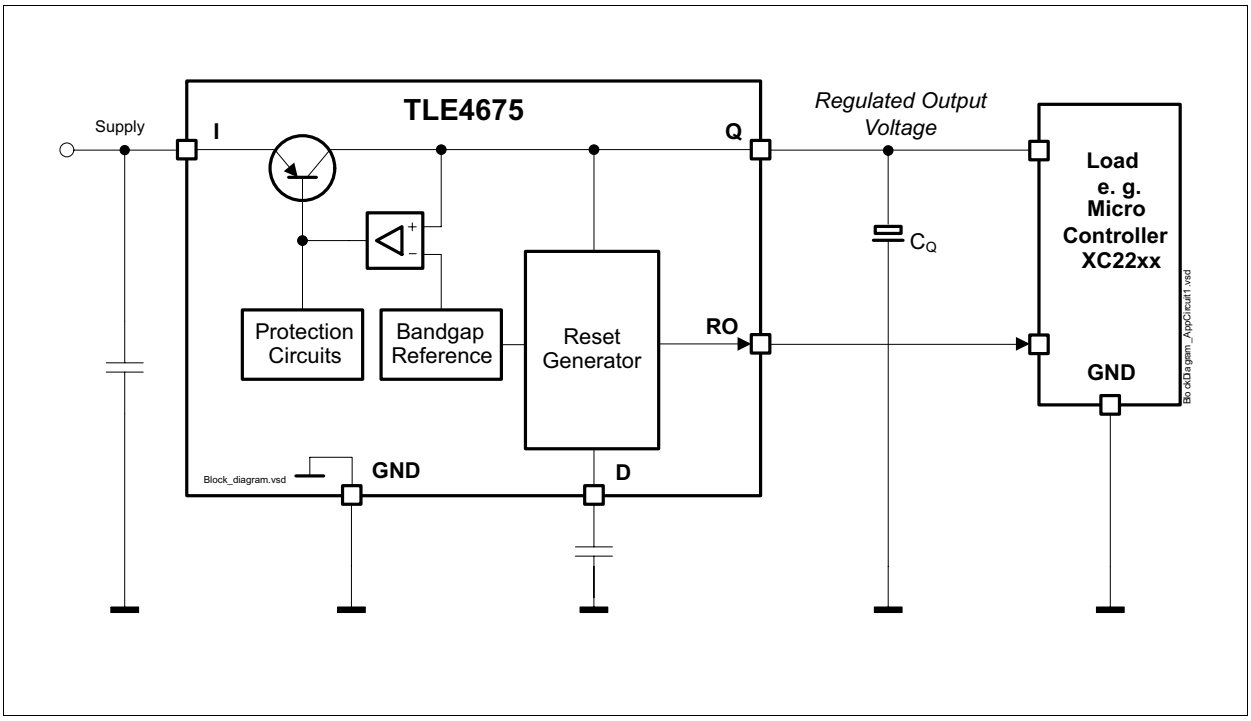

Figure 1 Block Diagram and Simplified Application Circuit

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3 Pin Configuration

3.1 Pin Assignment TLE4675D (PG-TO252-5)

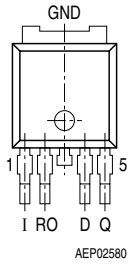

Figure 2 Pin Assignment (top view) TLE4675D

3.2 Pin Definitions and Functions TLE4675D

Pin	Symbol	Function
1	I	**Regulator Input and IC Supply** For compensating line influences, a capacitor to GND close to the IC pin is recommended.
2	RO	**Reset Output** Open collector output; external pull up resistor required; Leave open if the reset function is not needed.
3		Internally connected to TAB
4	D	**Reset Delay Timing** Connect a ceramic capacitor from D (Pin 4) to GND for the reset delay timing adjustment; Leave open, if reset functionality is not used.
5	Q	**5 V Regulator Output** Connect a capacitor between Q (Pin 5) and GND close to the IC pins, respecting capacitance and ESR requirements given in the **Chapter 4.2 Functional Range**.
TAB	GND	**Ground, Cooling TAB** Connect to heatsink area

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3.3 Pin Assignment TLE4675G (PG-TO263-5)

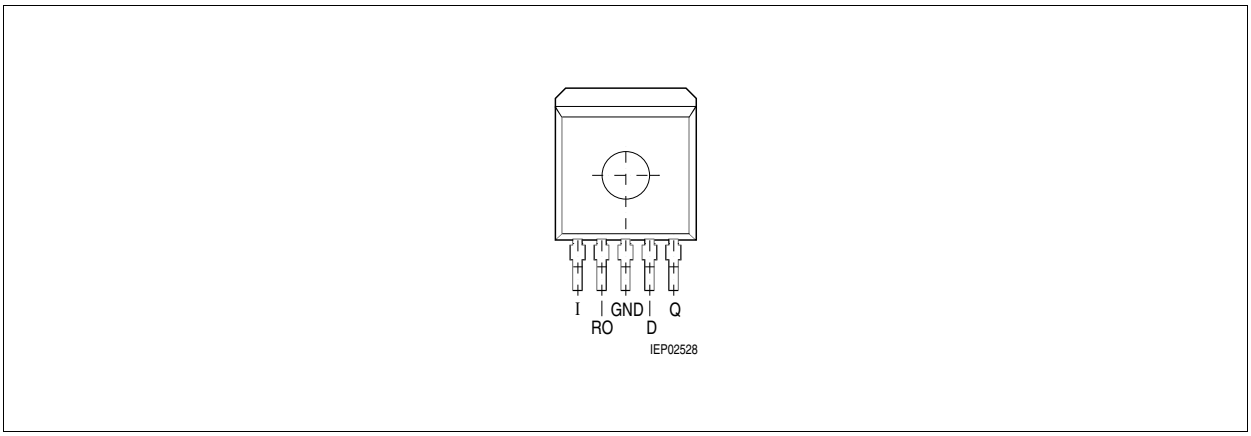

Figure 3 Pin Assignment (top view) TLE4675G

3.4 Pin Definitions and Functions TLE4675G

Pin	Symbol	Function
1	I	**Regulator Input and IC Supply** For compensating line influences, a capacitor to GND close to the IC pin is recommended
2	RO	**Reset Output** Open collector output; external pull up resistor required; Leave open if the reset function is not needed
3	GND	**Ground** Internally connected to TAB
4	D	**Reset Delay Timing** Connect a ceramic capacitor from D (Pin 4) to GND for the reset delay timing adjustment; leave open, if reset functionality is not used
5	Q	**5 V Regulator Output** Connect a capacitor between Q (Pin 5) and GND close to the IC pins, respecting capacitance and ESR requirements given in the **Chapter 4.2 Functional Range**
TAB		**Cooling TAB** Connect to heatsink area and Ground

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4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Regulator Input and IC Supply I	V_I	-42	45	V	–
4.1.2	Regulator Output Q	V_Q	-1	7	V	–
4.1.3	Reset Output RO	V_{RO}	-0.3	7	V	–
4.1.4	Reset Delay Timing D	V_D	-0.3	7	V	–
Temperatures						
4.1.5	Junction Temperature	T_j	-40	150	°C	–
4.1.6	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.7	ESD Resistivity	$V_{ESD,HBM}$	-4	4	kV	Human Body Model [2)]
4.1.8		$V_{ESD,CDM}$	-1	1	kV	Charged Device Model [3)]

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to AEC-Q100-002 - JESD22-A114

3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

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4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input Voltage Range for Normal Operation	$V_{I(nor)}$	$V_Q + V_{dr}$	45	V	1)
4.2.2	Extended Input Voltage Range	$V_{I(ext)}$	3.3	45	V	2)
4.2.3	Input Voltage Transient Immunity	dV_I/dt	-10	20	V/µs	$dV_I \leq 10$ V; $V_I > 9$ V; No trigger of RO.3)
4.2.4	Junction Temperature	T_j	-40	150	°C	–
4.2.5	Output Capacitor Requirements	C_Q	22	–	µF	–4)
4.2.6		ESR_{CQ}	–	2.5	Ω	–5)

1) For specification of the input voltage V_Q and the drop out voltage V_{dr} see **Chapter 5 Voltage Regulator**.
2) The output voltage VQ will follow the input voltage, but is outside the specified range. For details see **Chapter 5 Voltage Regulator**.
3) Transient measured directly at the input pin. Not subject to production test, specified by design.
4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%
5) Relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

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4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
TLE4675D Package PG-TO252-5							
4.3.1	Junction to Case	R_{thJC}	–	3.7	–	K/W	1)
4.3.2	Junction to Ambient	R_{thJA}	–	110	–	K/W	Footprint only 1)2)
4.3.3			–	57	–	K/W	300 mm² heatsink area on PCB 1)2)
4.3.4			–	42	–	K/W	600 mm² heatsink area on PCB 1)2)
4.3.5			–	27	–	K/W	2s2p PCB 1)3)
TLE4675G Package PG-TO263-5							
4.3.6	Junction to Case	R_{thJC}	–	3.7	–	K/W	1)
4.3.7	Junction to Ambient	R_{thJA}	–	123	–	K/W	Footprint only 1)2)
4.3.8			–	42	–	K/W	300 mm² PCB heatsink area 1)2)
4.3.9			–	33	–	K/W	600 mm² PCB heatsink area 1)2)
4.3.10			–	22	–	K/W	2s2p PCB 1)3)

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm3 board with 1 copper layer (1 x 70µm Cu).

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

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5 Voltage Regulator

5.1 Description Voltage Regulator

The output voltage V_Q is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. Saturation control as a function of the load current prevents any oversaturation of the pass element. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table "Operating Range" have to be maintained. For details see also the typical performance graph "Output Capacitor Series Resistor ESR_{CQ} vs. Output Current I_Q". Also, the output capacitor shall be sized to buffer load transients.

An input capacitor C_I is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above V_I = 22 V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore reduce the IC lifetime.

The TLE4675 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

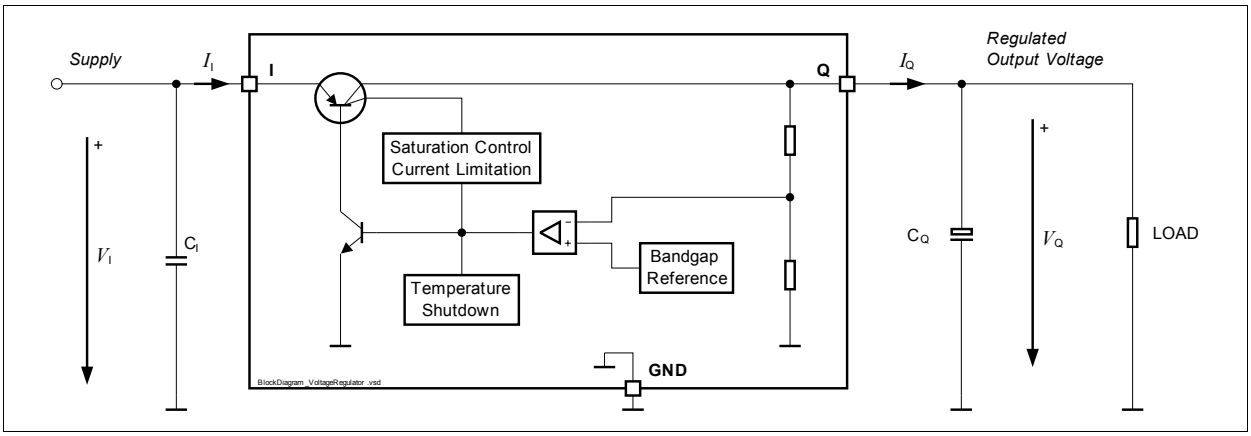

Figure 4 Block Diagram Voltage Regulator Circuit

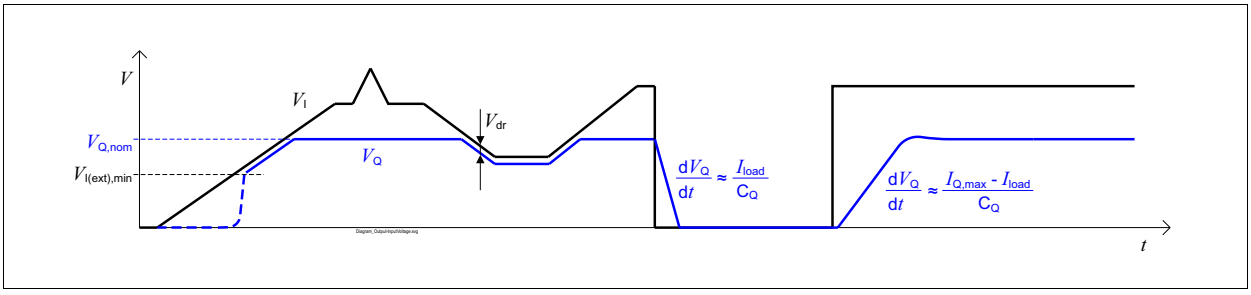

Figure 5 Output Voltage vs. Input Voltage

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5.2 Electrical Characteristics Voltage Regulator

Electrical Characteristics: Voltage Regulator

V_I = 13.5 V, T_j = -40 °C to +150 °C,

all voltages with respect to ground, direction of currents as shown in **Figure** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Output Voltage	V_Q	4.9	5.0	5.1	V	200 µA ≤ I_Q ≤ 400 mA; 8 V ≤ V_I ≤ 18 V
5.2.2			4.9	5.0	5.1	V	200 µA ≤ I_Q ≤ 300 mA; 6 V ≤ V_I ≤ 18V
5.2.3			4.9	5.0	5.1	V	200 µA ≤ I_Q ≤ 200 mA; 18 V ≤ V_I ≤ 32 V[1)]
5.2.4			4.9	5.0	5.1	V	200 µA ≤ I_Q ≤ 20 mA; 32 V ≤ V_I ≤ 45 V[1)]
5.2.5	Load Regulation steady-state	$dV_{Q,load}$	-30	-5	–	mV	I_Q = 1 mA to 300 mA; V_I = 6 V
5.2.6	Line Regulation steady-state	$dV_{Q,line}$	–	5	20	mV	V_I = 6 V to 32 V; I_Q = 5 mA
5.2.7	Power Supply Ripple Rejection	$PSRR$	60	65	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp[2)]
5.2.8	Drop Out Voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	120	250	mV	I_Q = 100 mA[3)]
5.2.9			–	250	500	mV	I_Q = 300 mA[3)]
5.2.10	Output Current Limitation	$I_{Q,max}$	401	550	850	mA	0 V ≤ V_Q ≤ 4.8 V
5.2.11	Reverse Current	I_Q	-2	-1	–	mA	V_I = 0 V; V_Q = 5 V
5.2.12	Reverse Current at Negative Input Voltage	I_I	-5	-2	–	mA	V_I = -16 V; V_Q = 0 V
5.2.13			-10	-3	–	mA	V_I = -42 V; V_Q = 0 V
5.2.14	Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing[2)]
5.2.15	Overtemperature Shutdown Threshold Hysteresis	$T_{j,hy}$	–	25	–	K	T_j decreasing[2)]

1) See typical performance graph for details.

2) Parameter not subject to production test; specified by design.

3) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

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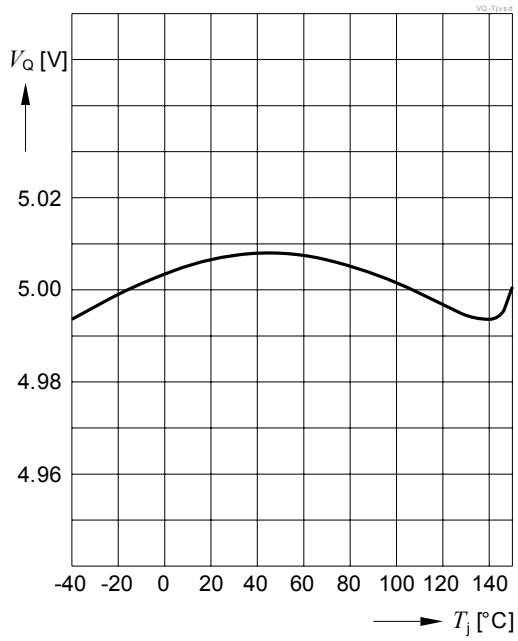
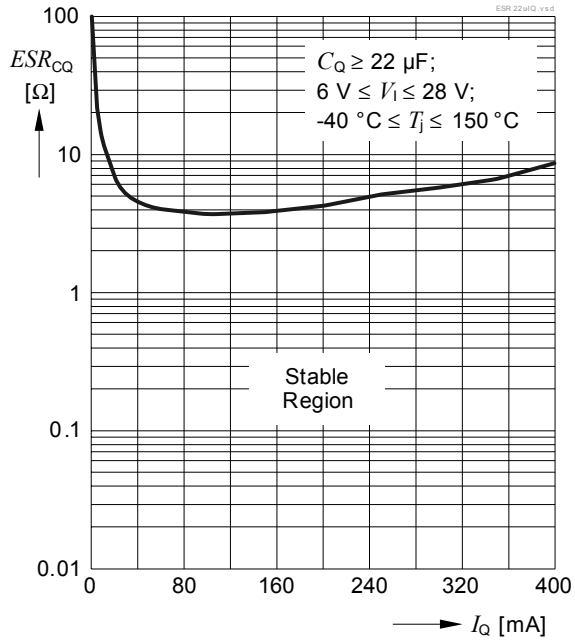
5.3 Typical Performance Characteristics Voltage Regulator

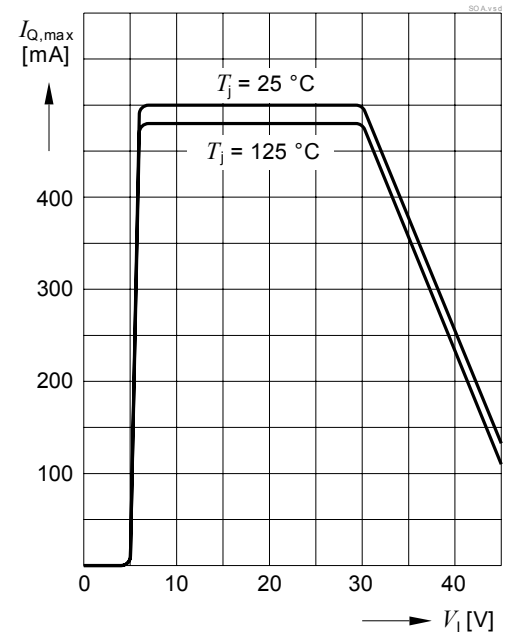
Output Voltage V_Q vs. Junction Temperature T_j



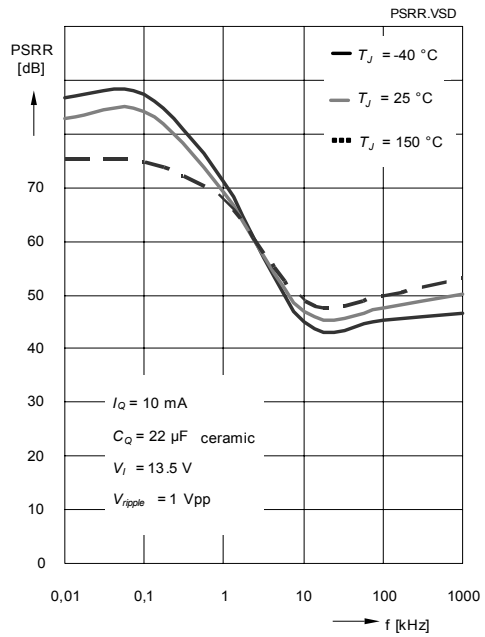
Output Capacitor Series Resistor ESR_{CQ} vs. Output Current I_Q



Output Current Limitation $I_{Q,max}$ vs. Input Voltage V_I



Power Supply Ripple Rejection $PSRR$



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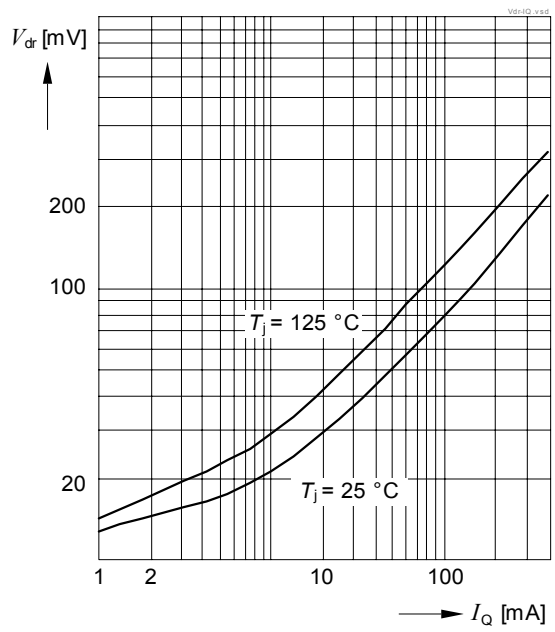
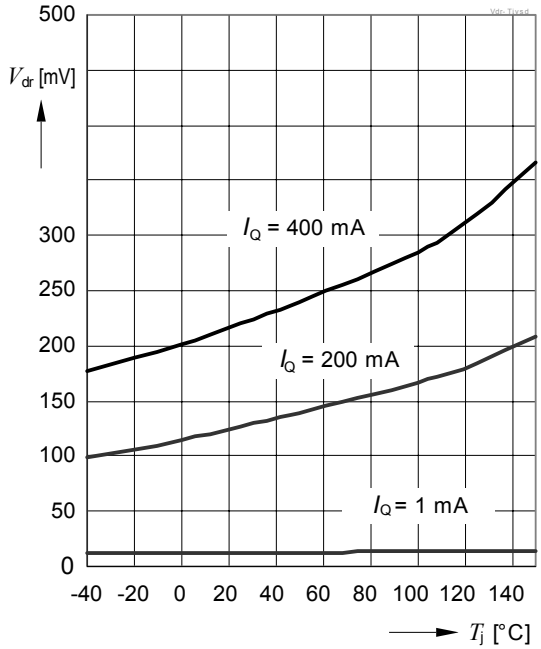
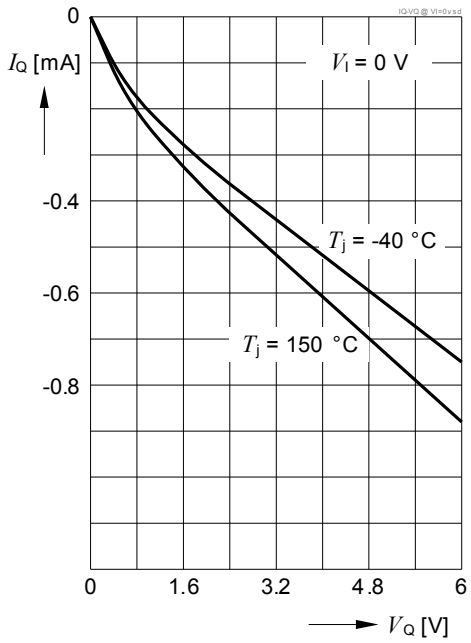
**Dropout Voltage V_{dr} vs.
Output Current I_Q**



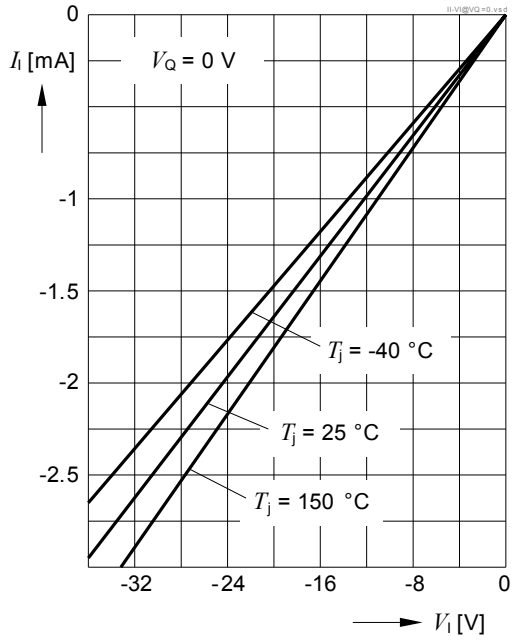
**Dropout Voltage V_{dr} vs.
Junction Temperature T_j**



**Reverse Output Current I_Q vs.
Input Voltage V_Q**



**Reverse Current I_I vs.
Input Voltage V_I**



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6 Current Consumption

6.1 Electrical Characteristics Current Consumption

Electrical Characteristics: Current Consumption

V_I = 13.5 V, T_j = -40 °C to +150 °C,

all voltages with respect to ground, directions of currents as shown in **Figure 6** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.1.1	Current Consumption $I_q = I_I - I_Q$	I_q	–	65	80	µA	$I_Q \leq 200$ µA; $T_j \leq 25$ °C
6.1.2			–	70	85	µA	$I_Q \leq 200$ µA; $T_j \leq 85$ °C
6.1.3			–	6	10	mA	I_Q = 250 mA
6.1.4			–	15	25	mA	I_Q = 400 mA

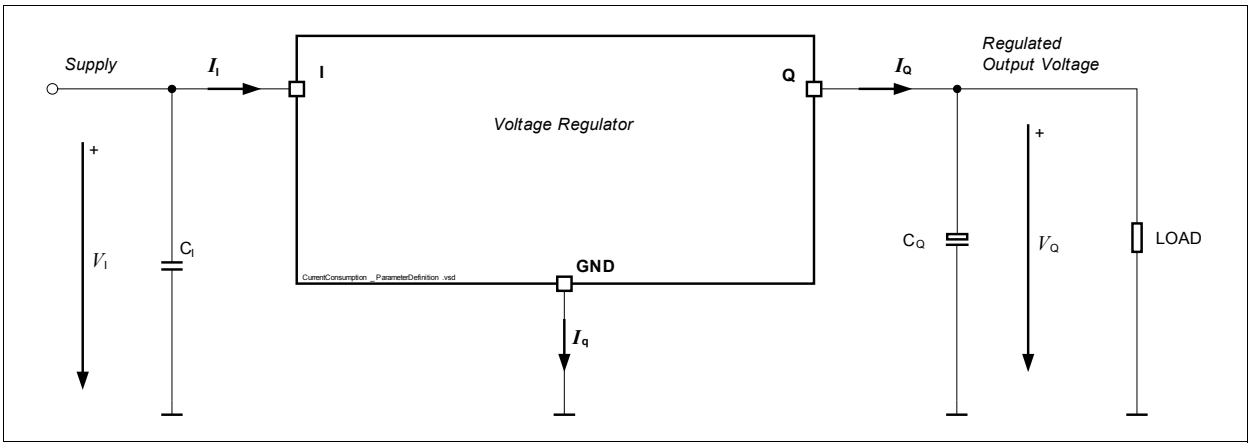

Figure 6 Parameter Definition

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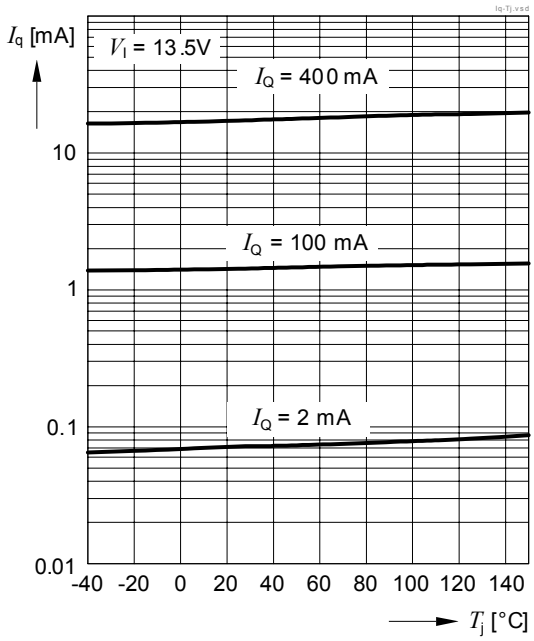
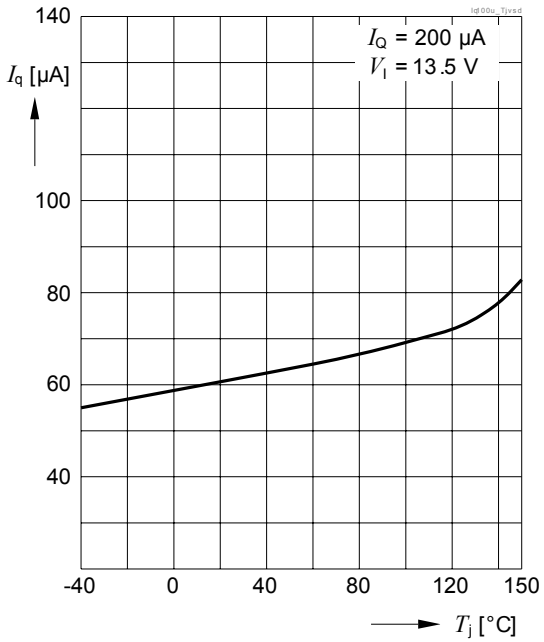
6.2 Typical Performance Characteristics Current Consumption

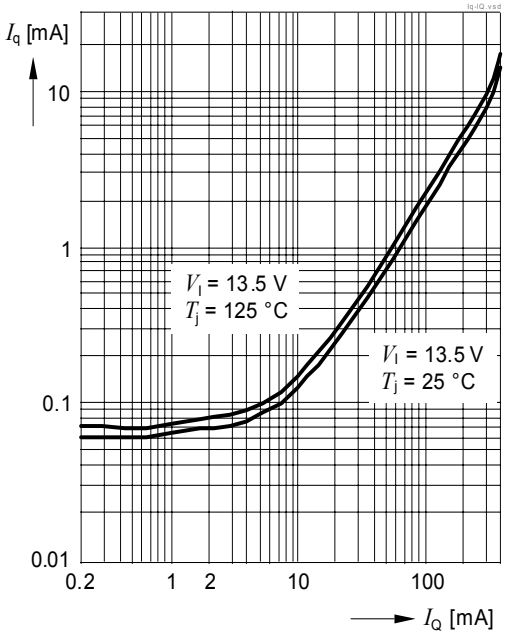
Current Consumption I_q vs. Junction Temperature T_j



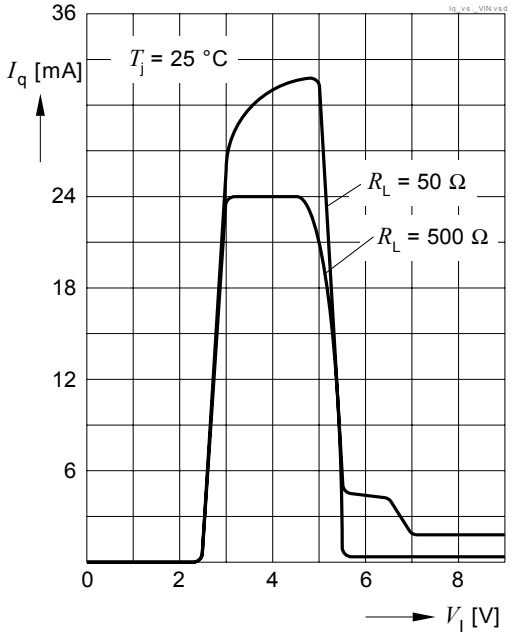
Current Consumption I_q vs. Junction Temperature T_{jl}



Current Consumption I_q vs. Output Current I_Q



Current Consumption I_q vs. Input Voltage V_I



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7 Reset Function

7.1 Description Reset Function

The reset function contains several features:

Output Undervoltage Reset:

An output undervoltage condition is indicated by setting the reset output “RO” to “low”. This signal might be used to reset a microcontroller during a low supply voltage condition.

Power-On Reset Delay Time

The power-on reset delay time $t_{d,PWR-ON}$ allows a microcontroller and oscillator to start up. This delay time is the time period from exceeding the upper reset switching threshold $V_{RT,hi}$ until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time $t_{d,PWR-ON}$ is defined by an external delay capacitor C_D connected to pin “D”, which is charged up by the delay capacitor charge current $I_{D,ch}$ starting from V_D = 0 V.

In case a power-on reset delay time $t_{d,PWR-ON}$ different from the value for C_D = 100nF is required, the delay capacitor’s value can be derived from the specified value given in **Item 7.2.15**:

$$C_D = \frac{t_{d,PWR-ON}}{t_{d,PWR-ON,100nF}} \times 100nF$$

with

- $t_{d,PWR-ON}$: Desired power-on reset delay time
- $t_{d,PWR-ON,100nF}$: Power-on reset delay time specified in **Item 7.2.15**
- C_D: Delay capacitor required

The formula is valid for $C_D \geq$ 10nF.For a precise calculation consider also the delay capacitor’s tolerance.

Undervoltage Reset Delay Time

Unlike the power-on reset delay time, the undervoltage reset delay t_d time considers a short output undervoltage event, where the delay capacitor C_D is assumed to be discharged to $V_D = V_{DST,lo}$ only before the charging sequence starts. Therefore, the undervoltage reset delay time t_d is defined by the delay capacitor charge current $I_{D,ch}$ starting from $V_D = V_{DST,lo}$ and the external delay capacitor C_D.

A delay capacitor CD for a different undervoltage reset delay time as specified in **Item 7.2.14** can be calculated similar as above:

$$C_D = \frac{t_d}{t_{d,100nF}} \times 100nF$$

with

- t_d: Desired reset delay time
- $t_{d,100nF}$: Reset delay time specified in **Item 7.2.14**
- C_D: Delay capacitor required

The formula is valid for $C_D \geq$ 10nF.For a precise calculation consider also the delay capacitor’s tolerance.

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Reset Reaction Time

In case the output voltage of the regulator drops below the output undervoltage lower reset threshold $V_{RT,lo}$, the delay capacitor CD is discharged rapidly. Once the delay capacitor's voltage has reached the lower delay switching threshold $V_{DST,lo}$, the reset output RO will be set to "low".

Additionally to the delay capacitor discharge time $t_{rr,d}$ an internal time $t_{rr,int}$ applies. Hence the total reset reaction time $t_{rr,total}$ becomes:

$$t_{rr,total} = t_{rr,int} + t_{rr,d}$$

with

- $t_{rr,total}$: total reset reaction time
- $t_{rr,int}$: Internal reset reaction time; see **Item 7.2.16**
- $t_{rr,d}$: Delay capacitor discharge time. For a capacitor C_D different from the value specified in **Item 7.2.17**, see typical performance graphs.

Reset Output Pull-Up Resistor R_{RO}:

The Reset Output RO is an open collector output requiring an external pull-up resistor to a voltage V_{IO}, e.g. V_Q. In **Item 7.2.7** a minimum value for the external resistor R_{RO} is given for the case it is connected to V_Q.

For applications, where the external pull-up resistor R_{RO} has to be connected to a different voltage rail V_{IO} than V_Q, the minimum pull-up resistor R_{RO} can be calculated out of the minimum sink current capability given in **Item 7.2.6**:

$$R_{RO} = \frac{V_{IO} - V_{RO,low}}{I_{RO,max}}$$

with

- R_{RO}: Reset pull up resistor
- V_{IO}: Voltage rail, where the pull up resistor is connected
- $V_{RO,low}$: Maximum allowed voltage level for a logic "Low" signal inside the application

Please be aware, that V_{IO} should not exceed the ratings for the RO pin given in **Item 4.1.3**.

Reset Output "RO" Low for $V_Q \geq 1$ V

In case of an undervoltage reset condition reset output "RO" is held "low" for $V_Q \geq 1$ V, even if the input voltage V_I is 0 V. This is achieved by supplying the reset circuit from the output capacitor.

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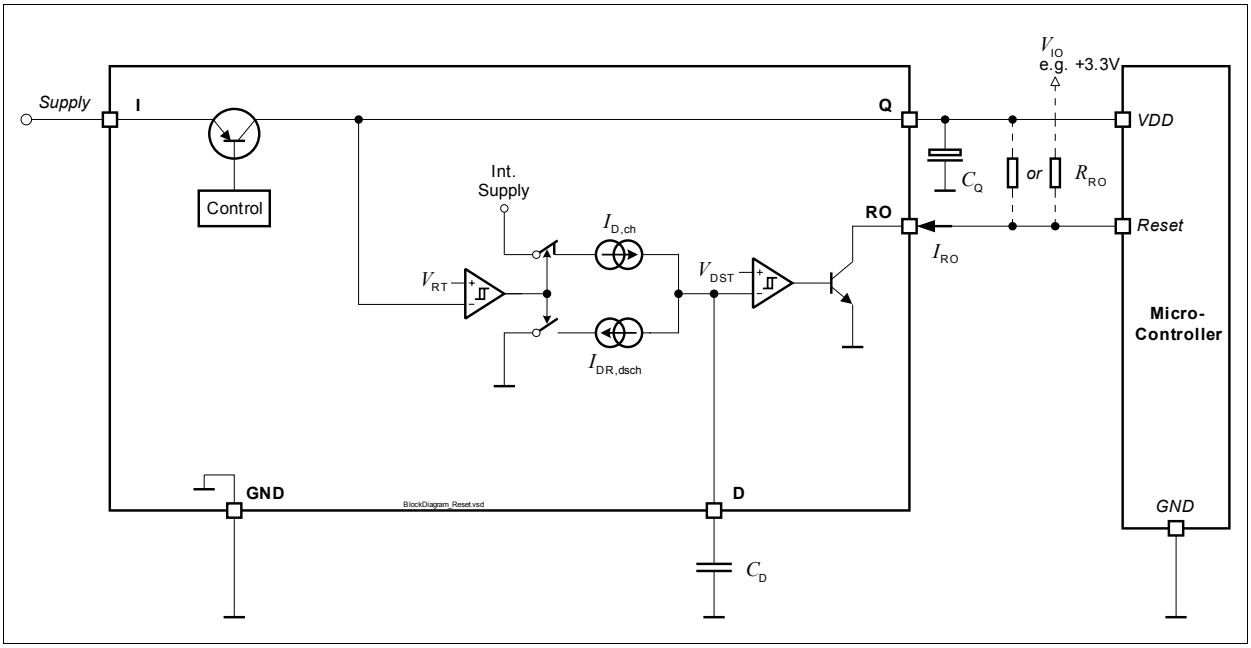

Figure 7 Block Diagram Reset Circuit

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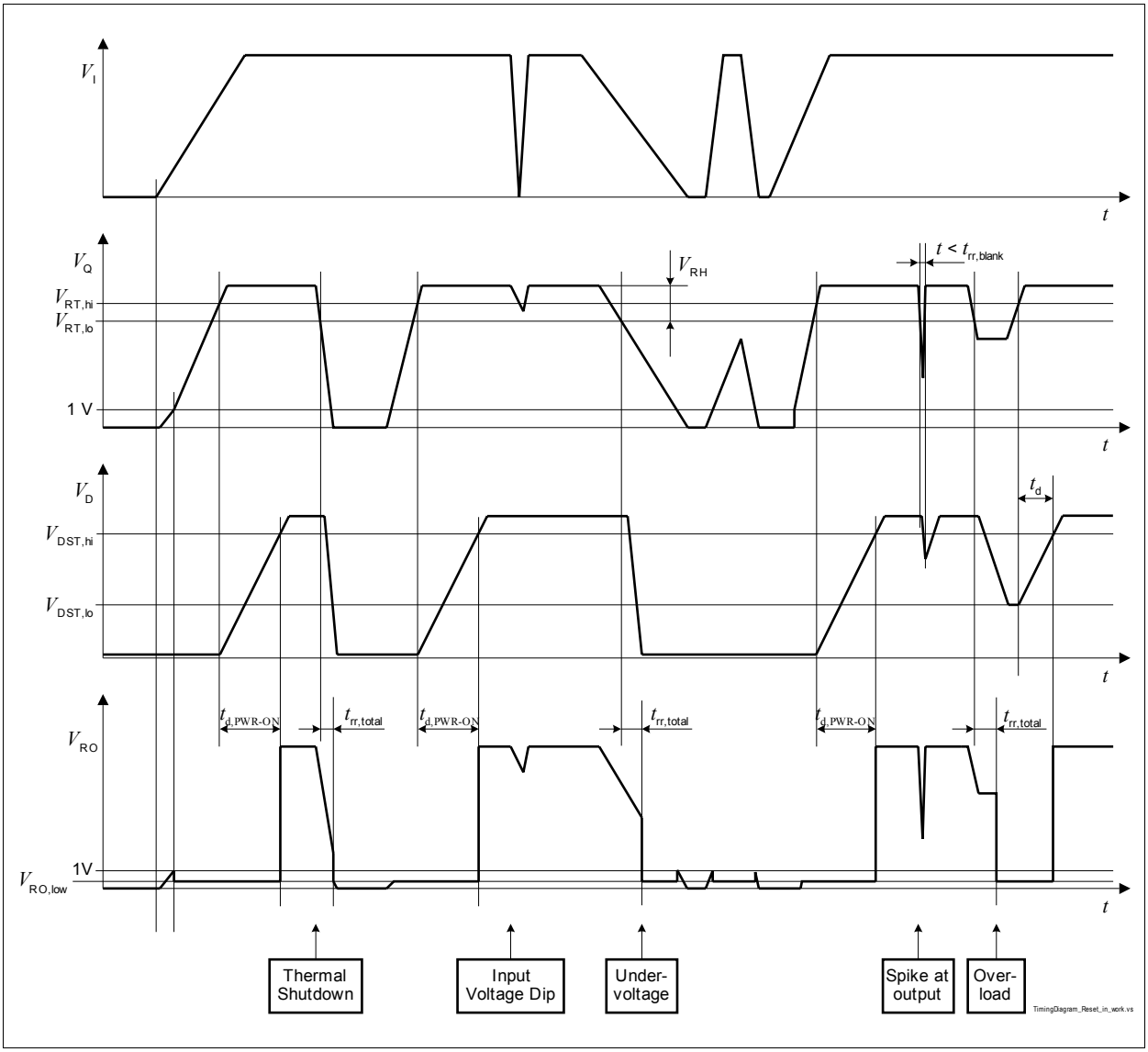

Figure 8 Timing Diagram Reset

The timing diagram assumes that the external pull up resistor R_{RO} is connected to the output voltage V_Q.

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7.2 Electrical Characteristics Reset Function

Electrical Characteristics: Reset Function

V_I = 13.5 V, T_j = -40 °C to +150 °C,

all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output Undervoltage Reset Comparator Default Values							
7.2.1	Output Undervoltage Reset Lower Switching Threshold	$V_{RT,lo}$	4.6	4.7	4.8	V	V_I = 0 V V_Q decreasing
7.2.2	Output Undervoltage Reset Upper Switching Threshold	$V_{RT,hi}$	4.7	4.8	4.9	V	V_I within operating range V_Q increasing
7.2.3	Output Undervoltage Reset Switching Hysteresis	$V_{RT,hy}$	50	100	–	mV	V_I within operating range
7.2.4	Output Undervoltage Reset Headroom	V_{RH}	250	300	–	mV	Calculated Value: V_Q - $V_{RT,lo}$ V_I within operating range I_Q = 50 mA
Reset Output RO							
7.2.5	Reset Output Low Voltage	$V_{RO,low}$	–	0.2	0.8	V	V_I = 0V 1 V ≤ V_Q < $V_{RT,low}$; I_{RO} = 0.3 mA
7.2.6	Reset Output Sink Current Capability	$I_{RO,max}$	0.3	–	–	mA	V_I = 0V; 1 V ≤ V_Q < $V_{RT,low}$; V_{RO} = 5V
7.2.7	Reset Output External Pull-up Resistor to V_Q	R_{RO}	3.0	–	–	kΩ	1 V ≤ V_Q < V_{RT}; V_{RO} ≤ 0.4V [1]
7.2.8	Reset Output Leakage Current	$I_{RO,leak}$	–	5	10	µA	V_{RO} = 5 V
Reset Delay Timing							
7.2.9	Delay Pin Output Voltage	V_D	–	–	5	V	–
7.2.10	Upper Delay Switching Threshold	$V_{DST,hi}$	–	1.1	–	V	–
7.2.11	Lower Delay Switching Threshold	$V_{DST,lo}$	–	0.3	–	V	–
7.2.12	Delay Capacitor Charge Current	$I_{D,ch}$	–	3.5	–	µA	V_D = 1 V
7.2.13	Delay Capacitor Reset Discharge Current	$I_{DR,dsch}$	–	70	–	mA	V_D = 1 V
7.2.14	Undervoltage Reset Delay Time	$t_{d,100nF}$	16	23	30	ms	Calculated value; C_D = 100 nF[2] C_D discharged to $V_{DST,lo}$

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Electrical Characteristics: Reset Function (cont'd)

V_I = 13.5 V, T_j = -40 °C to +150 °C,

all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

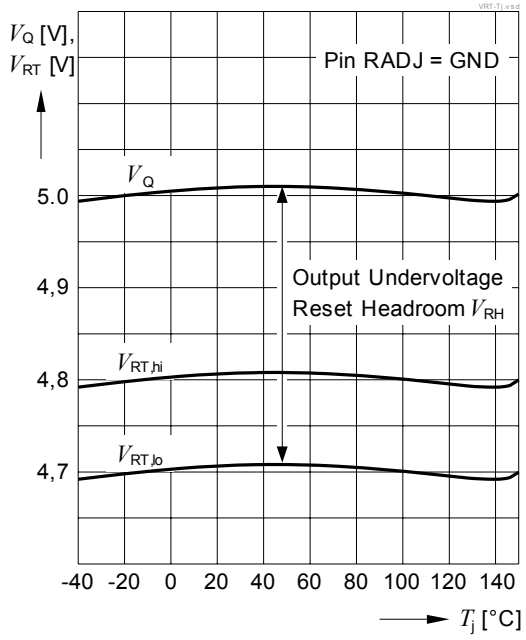
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.2.15	Power-on Reset Delay Time	$t_{d,PWR-ON,100nF}$	23	33	43	ms	Calculated value; C_D = 100 nF[2)] C_D discharged to 0 V
7.2.16	Internal Reset Reaction Time	$t_{rr,int}$	–	10	15	µs	C_D = 0 nF
7.2.17	Delay Capacitor Discharge Time	$t_{rr,d}$	–	1	2	µs	C_D = 100 nF
7.2.18	Total Reset Reaction Time	$t_{rr,total}$	–	11	17	µs	Calculated Value: $t_{rr,total} = t_{rr,d} + t_{rr,int}$ C_D = 100 nF[2)]

1) Parameter not subject of production test.

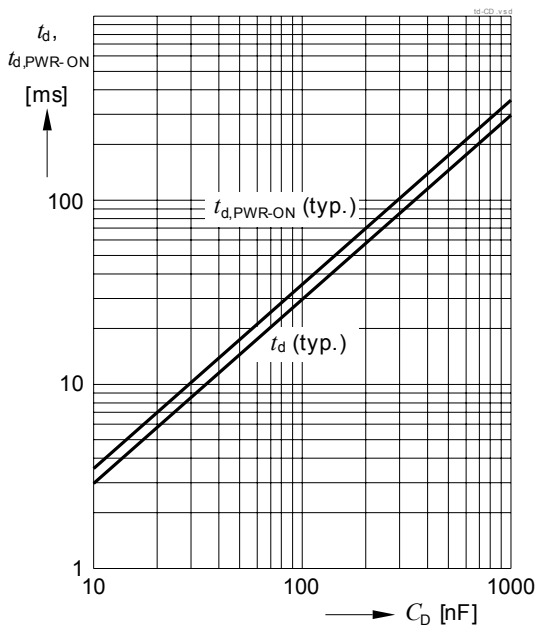
2) For programming a different delay and reset reaction time, see **Chapter 7.1** for calculation.

7.3 Typical Performance Characteristics Reset Function

Undervoltage Reset Switching Thresholds $V_{RO,lo}$, $V_{RO,hi}$ versus T_j



Reset Delay Time t_d, t_{d,PWR_ON} versus Delay Capacitor C_D



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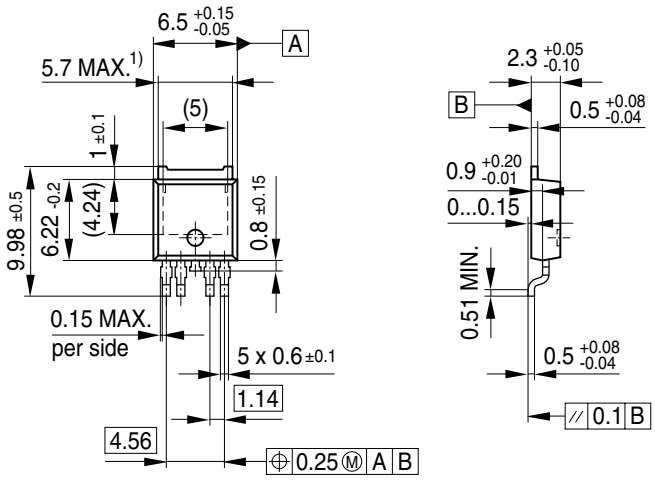
8 Package Outlines

8.1 PG-TO252-5 Package



1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

Figure 9 Package Outline PG-TO252-5

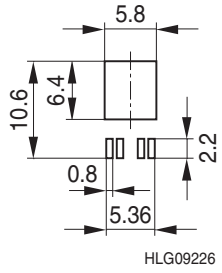


Figure 10 Footprint PG-TO252-5, Reflow Soldering Type

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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8.2 PG-TO263-5 Package

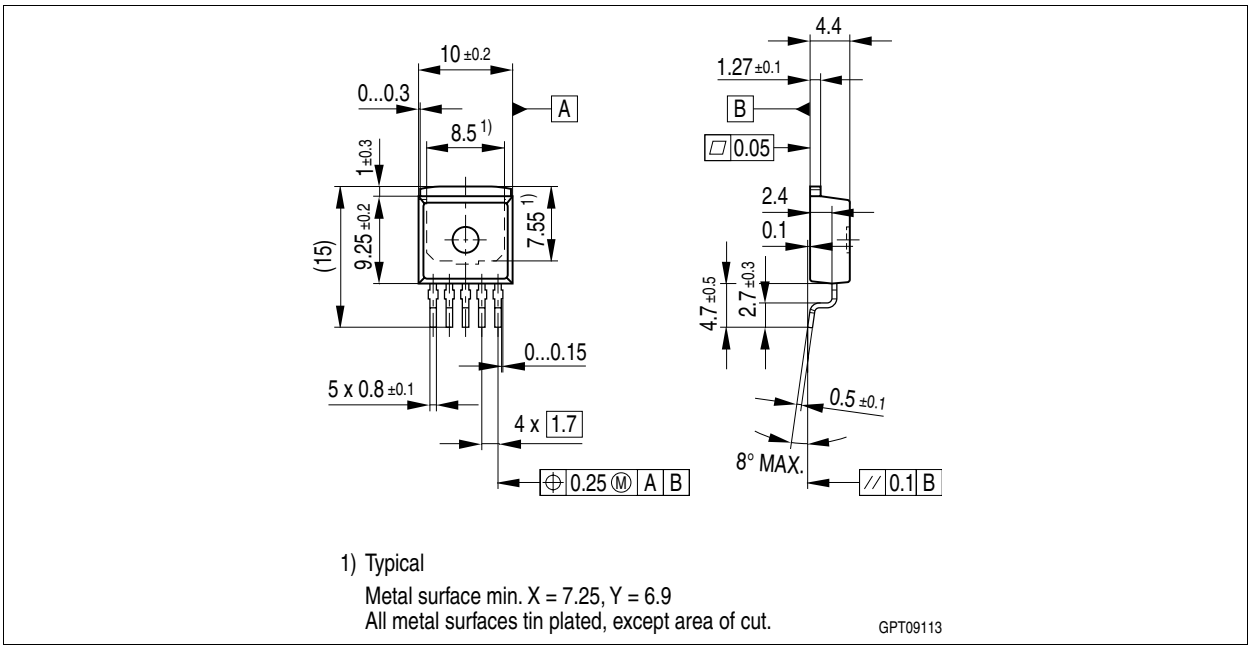

Figure 11 Package Outline PG-TO263-5

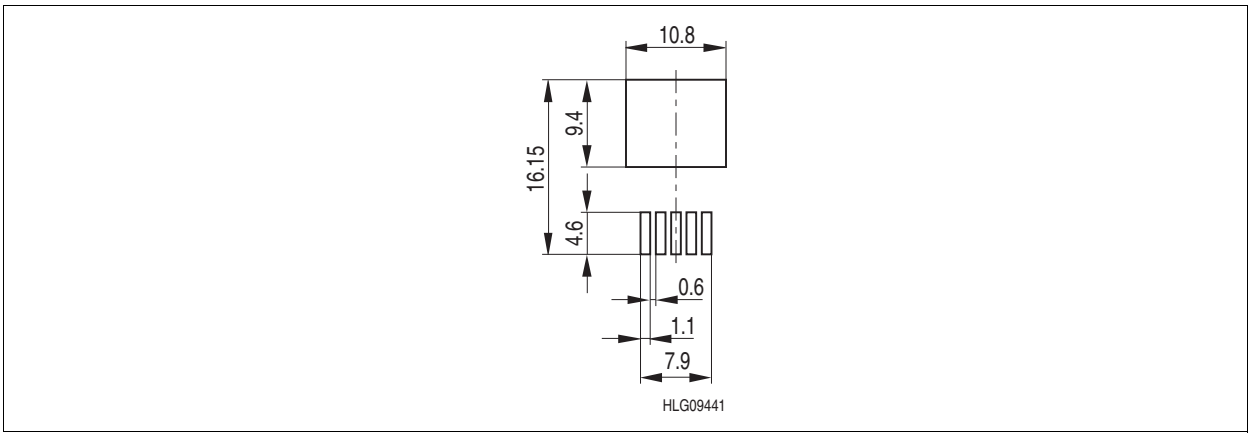

Figure 12 Footprint PG-TO263-5, Reflow Soldering Type

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on packages, please visit our website:
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Dimensions in mm

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9 Revision History

Revision	Date	Changes
1.0	2009-09-30	Final Data Sheet

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