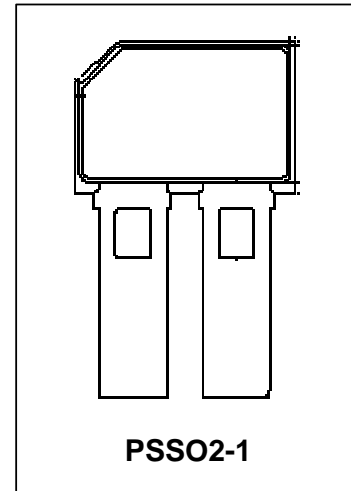


## Differential Two-Wire Hall Effect Sensor IC

**TLE4942**  
**TLE4942C**

### Features

- Two-wire PWM current interface
- Detection of rotation direction
- Airgap diagnosis
- Assembly position diagnosis
- Dynamic self-calibration principle
- Single chip solution
- No external components needed
- High sensitivity
- South and north pole pre-induction possible
- High resistance to piezo effects
- Large operating air-gaps
- Wide operating temperature range
- TLE4942C: 1.8nF overmolded capacitor



Type	Marking	Ordering Code	Package
TLE 4942	4200E4	Q62705-K428	PSSO2-1
TLE 4942C	42C0E4	Q62705-K437	PSSO2-2

The Hall Effect sensor IC TLE4942 is designed to provide information about rotational speed, direction of rotation, assembly position and limit airgap to modern vehicle dynamics control systems and ABS. The output has been designed as a two wire current interface based on a Pulse Width Modulation principle. The sensor operates without external components and combines a fast power-up time with a low cut-off frequency. Excellent accuracy and sensitivity is specified for harsh automotive requirements as a wide temperature range, high ESD robustness and high EMC resilience. State-of-the-art BiCMOS technology is used for monolithic integration of the active sensor areas and the signal conditioning.

Finally, the optimised piezo compensation and the integrated dynamic offset compensation enable easy manufacturing and elimination of magnet offsets.

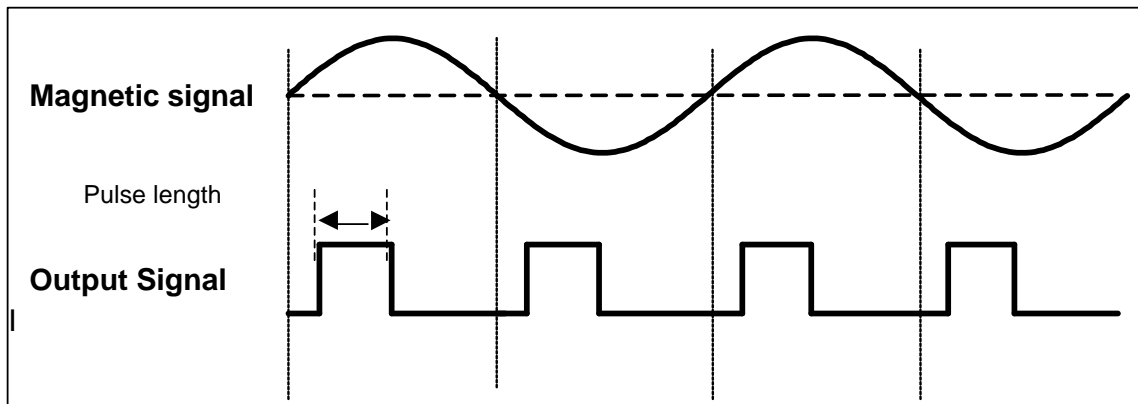
The TLE4942C is additionally provided with an overmolded 1.8nF capacitor for improved EMI performance.

## Functional Description

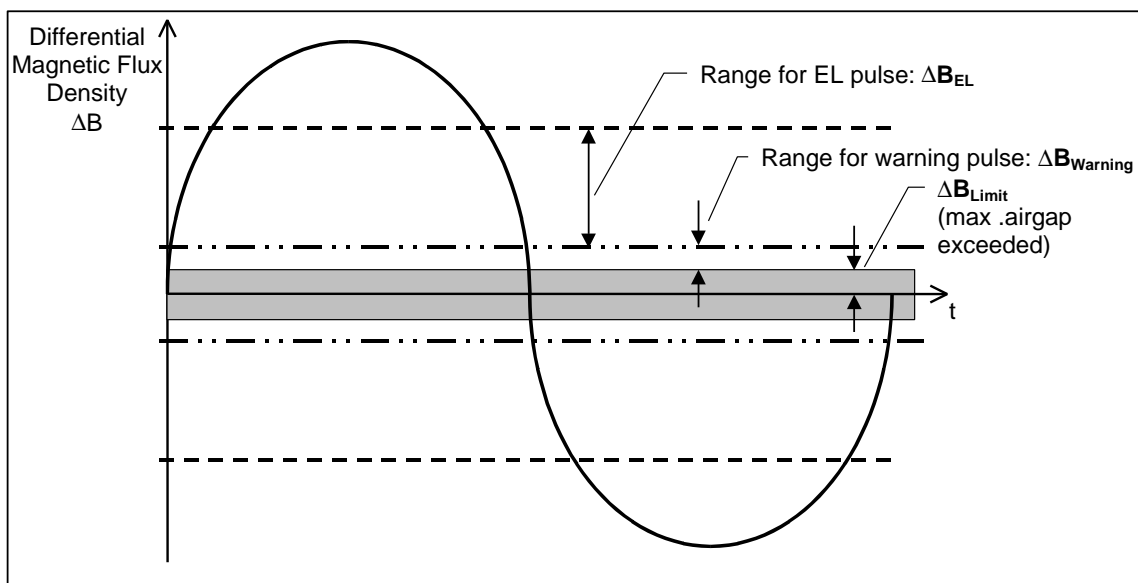
The differential Hall Effect IC detects the motion of ferromagnetic or permanent magnet structures by measuring the differential flux density of the magnetic field. To detect the motion of ferromagnetic objects the magnetic field must be provided by a backbiasing permanent magnet. Either the South or North pole of the magnet can be attached to the rear, unmarked side of the IC package.

Magnetic offsets of up to  $\pm 20\text{mT}$  and mechanical offsets are cancelled out through a self-calibration algorithm. Only a few transitions are necessary for the self-calibration procedure. After the initial self-calibration sequence switching occurs when the input signal crosses the arithmetic mean of its max. and min. values (e.g. zero-crossing for sinusoidal signals).

The ON and OFF state of the IC are indicated by **High** and **Low** current consumption. Each zero crossing of the magnetic input signal triggers an output pulse.

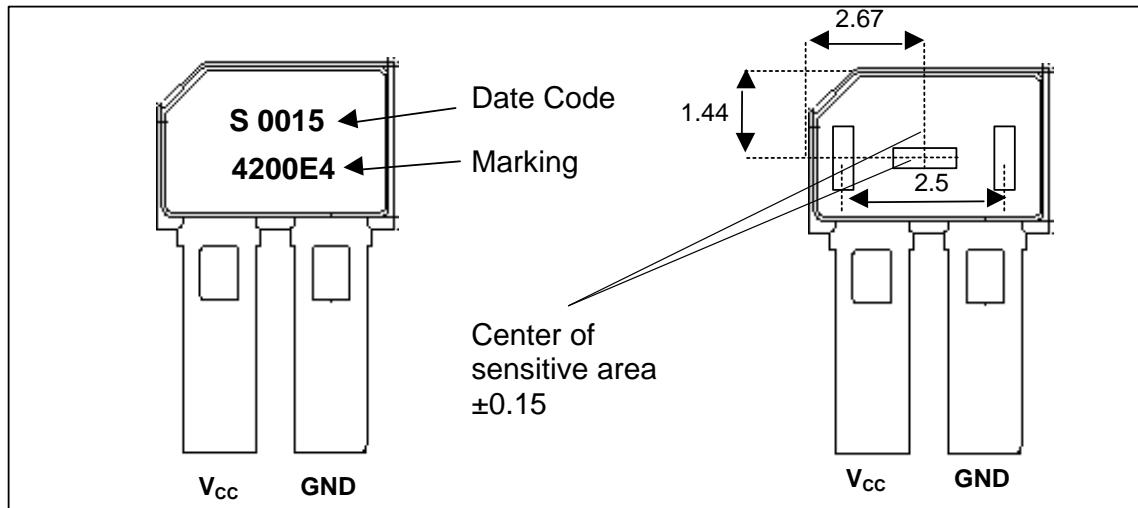


**Figure 3** Zero-crossing principle and corresponding output pulses

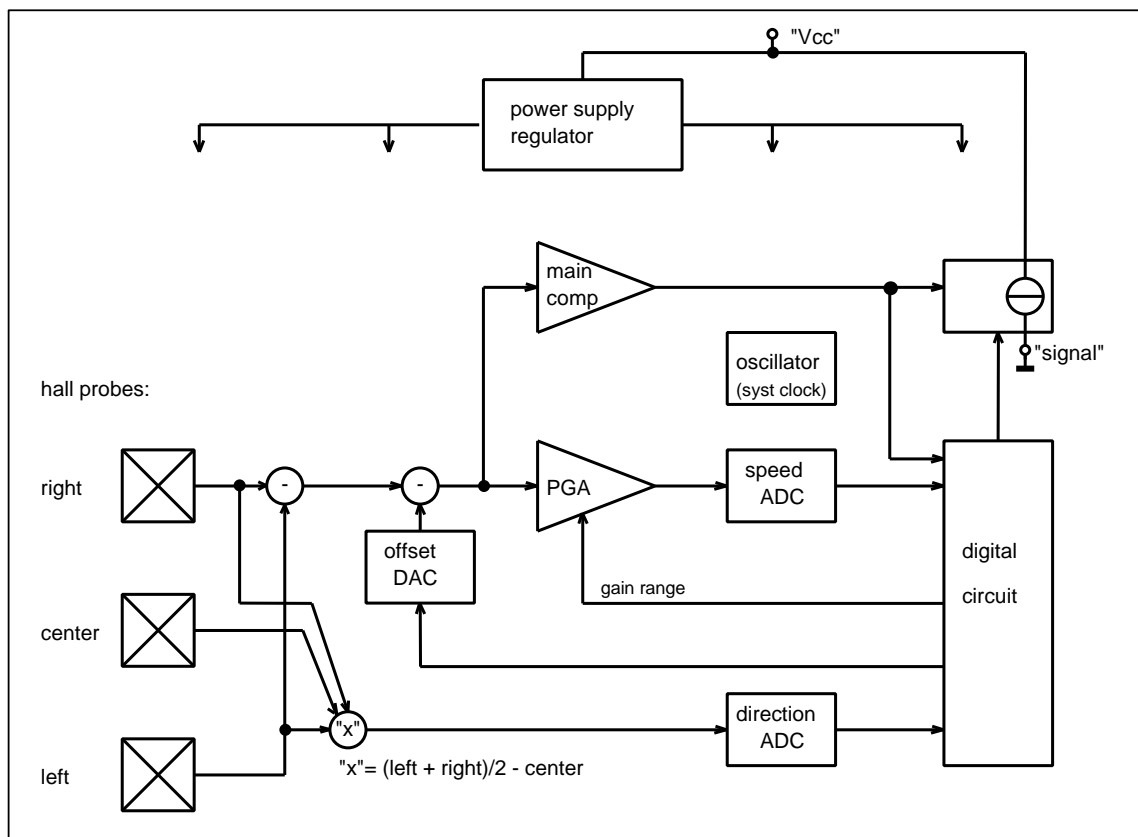


**Figure 4** Definition of differential magnetic flux density ranges

**Pin Configuration**  
(view on branded side of component)



**Figure 1**



**Figure 2 Block diagram**

In addition to the speed signal, the following information is provided by varying the length of the output pulses in Figure 3 (PWM modulation):

*Airgap Warning range = Warning*

Warning information is issued in the output pulse length when the magnetic field is below a critical value. (E. g. the airgap between the Hall Effect IC and the target wheel exceeds a critical value). The device works with reduced functionality.

*Assembly position range = EL*

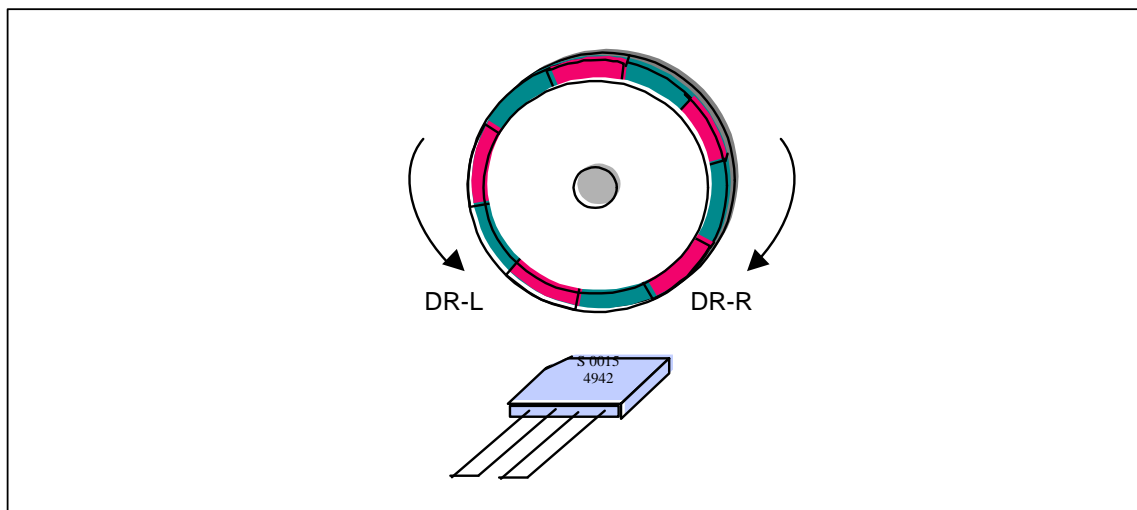
EL information is issued in the output pulse length when the magnetic field is below a predefined value (the airgap between the Hall Effect IC and the target wheel exceeds a predefined value). The device works with full functionality.

*Direction of rotation right = DR-R*

DR-R information is issued in the output pulse length when the target wheel in front of the Hall Effect IC moves from the pin GND to the pin V<sub>CC</sub>.

*Direction of rotation left = DR-L*

DR-L information is issued in the output pulse length when the target wheel in front of the Hall Effect IC moves from the pin V<sub>CC</sub> to the pin GND.



**Figure 5** Definition of rotation direction

## Circuit Description

The circuit is supplied internally by a voltage regulator. An on-chip oscillator serves as a clock generator for the DSP and the output encoder.

### *Speed signal circuitry:*

TLE4942 speed signal path comprises of a pair of Hall Effect probes, separated from each other by 2.5mm, a differential amplifier including noise limiting low-pass filter, and a comparator triggering a switched current output stage. An offset cancellation feedback loop is provided through a signal-tracking A/D converter, a digital signal processor (DSP), and an offset cancellation D/A converter.

During the power-up phase (uncalibrated mode) the output is disabled. The differential input signal is digitized in the speed A/D converter and fed into the DSP part of the circuit. The minimum and maximum values of the input signal are extracted and their corresponding arithmetic mean value is calculated. The offset of this mean value is determined and fed into the offset cancellation DAC. After successful correction of the offset, the output switching is enabled.

In running mode (calibrated mode) the offset correction algorithm of the DSP is switched into a low-jitter mode, thereby avoiding oscillation of the offset DAC LSB. Switching occurs at zero-crossover. It is only affected by the small residual offset of the comparator and by the propagation delay time of the signal path, which is mainly determined by the noise limiting filter. Signals which are below a predefined threshold  $\Delta B_{\text{Limit}}$  are not detected. This prevents unwanted switching.

The comparator also detects whether the signal amplitude exceeds  $\Delta B_{\text{Warning}}$  or  $\Delta B_{\text{EL}}$ . This information is fed into the DSP and the output encoder. The pulse length of the **High** output current is generated according to the rotational speed, the direction of rotation and the magnetic field strength.

### *Direction signal circuitry:*

The differential signal between a third Hall probe and the mean of the differential Hall probe pair is obtained from the direction input amplifier. This signal is digitized by the direction ADC and fed into the DSP circuitry. There, the phase of the signal referring to the speed signal is analyzed and the direction information is forwarded to the output encoder.

### Absolute Maximum Ratings

 $T_j = -40 \text{ to } 150^\circ\text{C}, 4.5\text{V} \leq V_{cc} \leq 16.5\text{V}$ 

Parameter	Symbol	Limit values		Unit	Remarks
		Min	Max		
Supply voltage	$V_{cc}$	-0.3			$T_j < 80^\circ\text{C}$
Supply voltage	$V_{cc}$		16.5	V	$T_j = 170^\circ\text{C}$
Supply voltage	$V_{cc}$		20	V	$T_j = 150^\circ\text{C}$
Supply voltage	$V_{cc}$		22	V	$t = 10 * 5 \text{ min}$
Supply voltage	$V_{cc}$		24	V	$t = 10 * 5 \text{ min}, R_{M \geq 75\Omega}$
Supply voltage	$V_{cc}$		27	V	$t = 400 \text{ ms}, R_{M \geq 75\Omega}$
Reverse polarity current	$I_{rev}$		200	mA	External current limitation required, $t < 4\text{h}$
Junction temperature	$T_j$		150	$^\circ\text{C}$	5000 h, $V_{cc} < 16.5\text{V}$
Junction temperature	$T_j$		160	$^\circ\text{C}$	2500 h, $V_{cc} < 16.5\text{V}$
Junction temperature	$T_j$		170	$^\circ\text{C}$	500 h, $V_{cc} < 16.5\text{V}$
Junction temperature	$T_j$		190	$^\circ\text{C}$	4 h, $V_{cc} < 16.5\text{V}$
Active lifetime	$t_{B,active}$	10000		h	
Storage Temperature	$T_s$	-40	150	$^\circ\text{C}$	
Thermal Resistance PSSO2-1	$R_{thJA}$		190	K/W	1)
ESD	$U_{ESD}$		$\pm 2$	kV	According to standard EIA/JESD22-A114-B HBM <sup>2)</sup> $R=1500 \Omega, C=100\text{pF}$

1) can be improved significantly by further processing like overmolding

2) covers MIL STD 883D

**Note:** Stresses in excess of those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Operating Range

Parameter	Symbol	Limit values		Unit	Remarks
		Min	Max		
Supply voltage	$V_{CC}$	4.5	20	V	
Supply voltage ripple	$V_{AC}$		6	$V_{pp}$	$V_{CC}=13V$ $0 < f < 50kHz$
Junction temperature	$T_j$	-40	150	°C	
Junction temperature	$T_j$		170	°C	$V_{CC} \leq 16.5V$ , increased jitter permissible
Pre-induction	$B_0$	-500	+500	mT	
Pre-induction offset between outer probes	$\Delta B_{stat., l/r}$	-20	+20	mT	
Pre-induction offset between mean of outer probes and center probe	$\Delta B_{stat., m/o}$	-20	+20	mT	
Differential Induction	$\Delta B$	-120	+120	mT	

**Note:** Within the operating range the functions given in the circuit description are fulfilled.



### AC/DC Characteristics

All values specified at constant amplitude and offset of input signal

Parameter	Symbol	Limit values			Unit	Remarks
		Min	Typ	Max		
Supply current	$I_{Low}$	5.9	7	8.4	mA	
Supply current	$I_{High}$	11.8	14	16.8	mA	
Supply current ratio	$I_{High}/I_{Low}$	1.9				
Output rise/fall slew rate TLE4942	$t_r, t_f$	12 7.5		26 24	mA/ $\mu$ s	$R_M \leq 150 \Omega$ $R_M \leq 750 \Omega$ See Figure 6.
Output rise/fall slew rate TLE4942C	$t_r, t_f$	8 8		22 26	mA/ $\mu$ s	$R_M = 75 \Omega$ $T < 125^\circ\text{C}$ $T < 170^\circ\text{C}$ See Figure 6.
Current ripple $dI_X/dV_{CC}$	$I_X$			90	$\mu\text{A}/\text{V}$	
Limit threshold	$\Delta B_{Limit}$	0.35	0.8	1.5	mT	Amplitude values
Airgap warning threshold	$\Delta B_{Warning}$	0.9	1.4	2.6	mT	Amplitude values
Limit - Airgap warning threshold ratio	$\Delta B_{Warning} / \Delta B_{Limit}$	1.3	1.75	2.7		Amplitude values
Assembly position threshold	$\Delta B_{EL}$	5.2	7.2	9.6	mT	at room temp

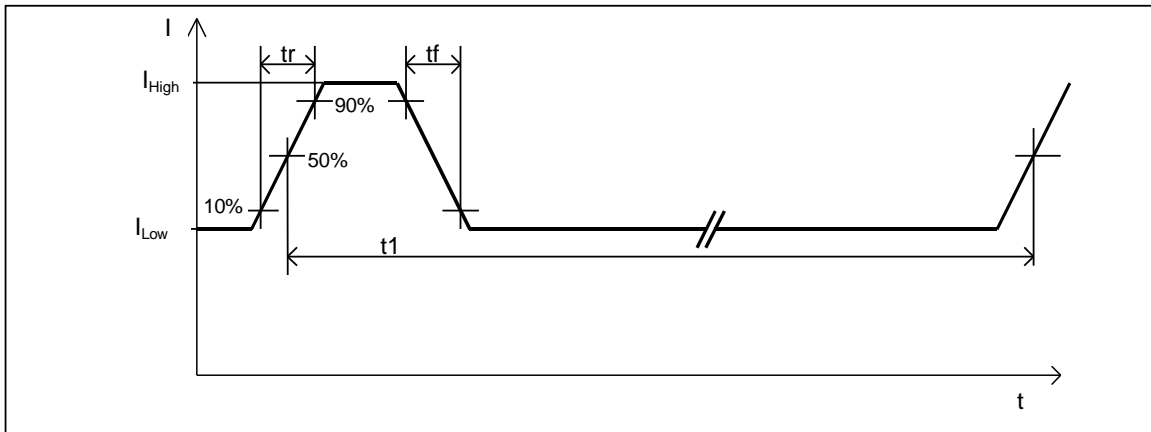
Initial calibration delay time	$t_{d,input}$			300	$\mu s$	Additional to $n_{start}$
Magnetic edges required for initial calibration <sup>1)</sup>	$n_{start}$			6 *	magn. edges	
Number of emitted pulses with invalid supplementary information <sup>2)</sup>	$n_{DR-Start}$			3 *	magn. edges	
Frequency	f	1		2500	Hz	
Frequency changes	df/dt			$\pm 100$	Hz/ms	
Duty cycle	duty	40	50	60	%	<sup>3)</sup> Measured @ $\Delta B = 2mT$ sine wave Def. Figure 7
Jitter, $T_j < 150^\circ C$ $T_j < 170^\circ C$	$S_{Jit-close}$			$\pm 2$ $\pm 3$	% %	1 s value $V_{CC} = 12 V$ $\Delta B \geq 2mT$
Jitter, $T_j < 150^\circ C$ $T_j < 170^\circ C$	$S_{Jit-far}$			$\pm 4$ $\pm 6$	% %	1 s value $V_{CC} = 12 V$ ( $2mT \geq$ ) $\Delta B > \Delta B_{Limit}$
Jitter at board net ripple	$S_{Jit-AC}$			$\pm 2$	%	$V_{CC} = 13V \pm 6V_{pp}$ $0 < f < 50kHz$ $\Delta B = 15 mT$

\* See Appendix B

<sup>1)</sup> The sensor requires up to  $n_{start}$  magnetic switching edges for valid speed information after power-up or after a stand still condition. During that phase the output is disabled.

<sup>2)</sup> The first 3 pulses containing direction information can have the wrong rotation information. (The first pulse after starting with the speed signal can have any length  $< t_{stop}$ . At  $\Delta B_{Limit}$  output pulses might have any length  $< t_{stop}$ ).

<sup>3)</sup> During fast offset alterations, due to the calibration algorithm, exceeding the specified duty cycle is permitted for short time periods.

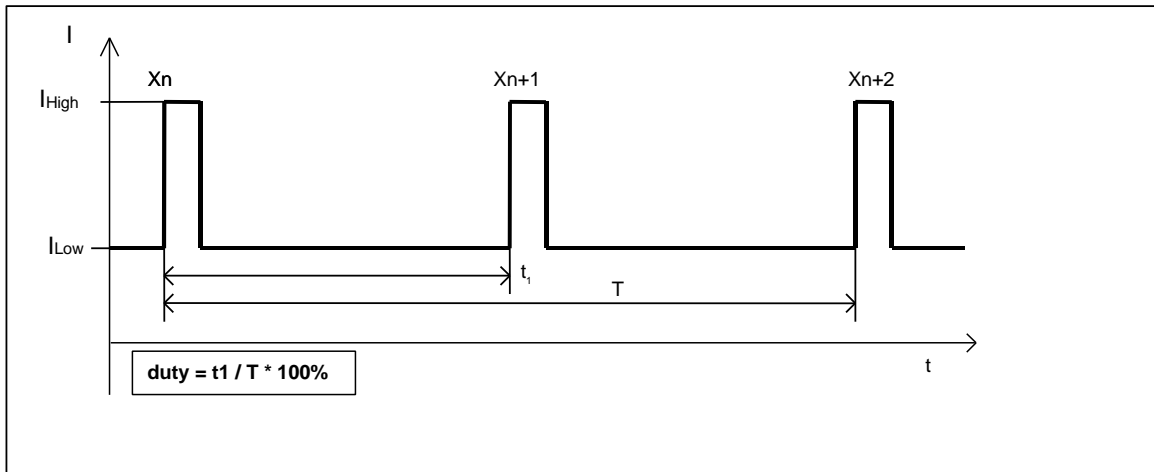


**Figure 6** Definition of rise and fall time

### Timing Characteristics

Parameter	Symbol	Limit values			Unit	Remarks
		Min	Typ	Max		
Pre-low length	$t_{\text{pre-low}}$	38	45	52	$\mu\text{s}$	
Length of Warning pulse	$t_{\text{Warning}}$	38	45	52	$\mu\text{s}$	
Length of DR-L pulse	$t_{\text{DR-L}}$	76	90	104	$\mu\text{s}$	
Length of DR-R pulse	$t_{\text{DR-R}}$	153	180	207	$\mu\text{s}$	
Length of DR-L & EL pulse	$t_{\text{DR-L\&EL}}$	306	360	414	$\mu\text{s}$	
Length of DR-R & EL pulse	$t_{\text{DR-R\&EL}}$	616	720	828	$\mu\text{s}$	
Output of EL pulse, maximum frequency	$f_{\text{EL, max}}$		117		Hz	
Length of stand still pulse	$t_{\text{stop}}$	1.232	1.44	1.656	ms	Def. Fig.9
Stand still period <sup>1)</sup>	$T_{\text{stop}}$	590	737	848	ms	Def. Fig. 9

<sup>1)</sup> If no magnetic switching edge is detected for a period longer than  $T_{\text{stop}}$ , the stand still pulse is issued.



**Figure 7** Definition of duty cycle

### PWM Current Interface

Between each magnetic transition and the rising edge of the corresponding output pulse the output current is **Low** for  $t_{\text{pre-low}}$  in order to allow reliable internal conveyance. Following the signal pulse (current is **High**) is output.

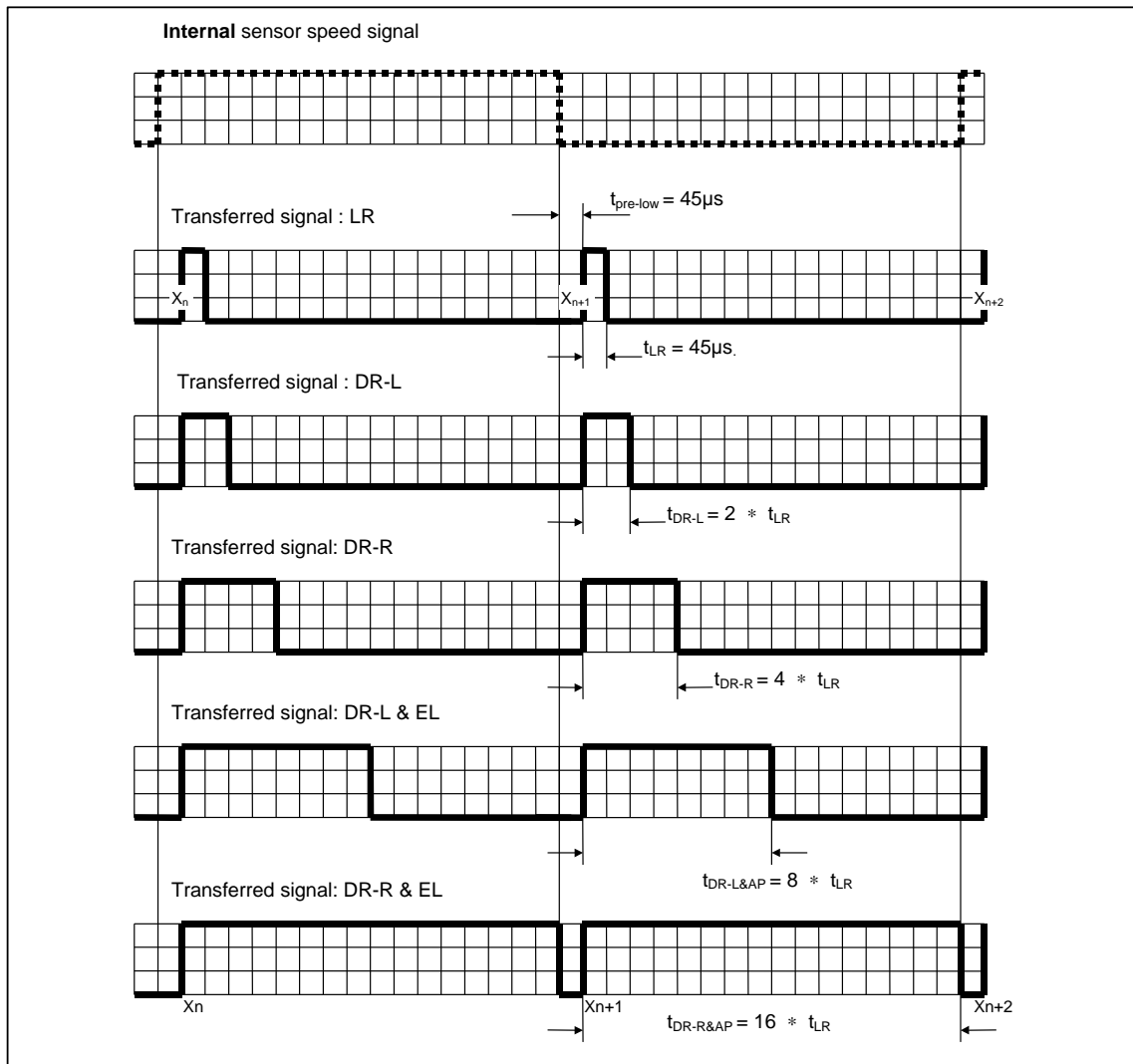
If the magnetic differential field exceeds  $\Delta B_{\text{EL}}$ , the output pulse lengths are  $90\mu\text{s}$  or  $180\mu\text{s}$  respectively, depending on the direction of rotation.

When the magnitude of the magnetic differential field is below  $\Delta B_{\text{EL}}$ , the output pulse lengths are  $360\mu\text{s}$  and  $720\mu\text{s}$  respectively, depending on left or right rotation. Due to decreasing cycle times at higher frequencies, these longer pulses are only output up to frequencies of approximately  $117\text{Hz}$ . For higher frequencies and differential magnetic fields below  $\Delta B_{\text{EL}}$ , the output pulse lengths are  $90\mu\text{s}$  or  $180\mu\text{s}$  respectively.

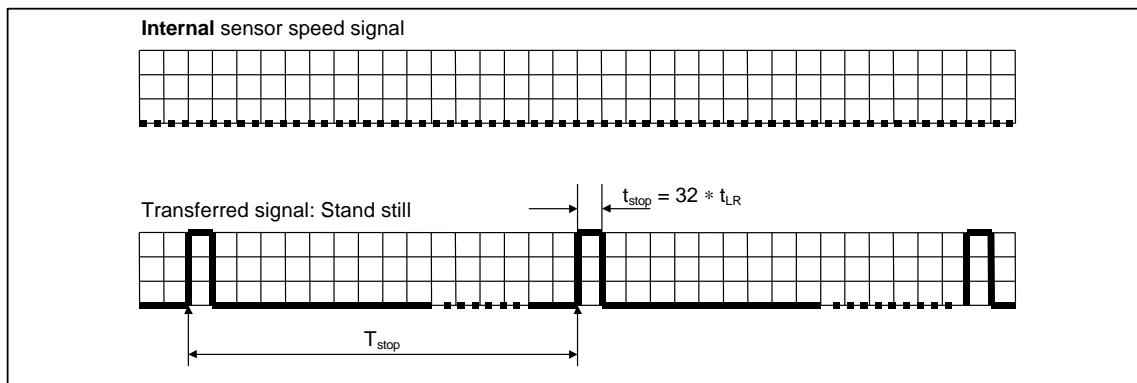
If the magnitude of the magnetic differential field is below  $\Delta B_{\text{Warning}}$ , the output pulse length is  $45\mu\text{s}$ . The warning output is dominant, this means that close to the limit airgap the direction and the assembly position information are disabled.

For magnitudes of the magnetic differential field below  $\Delta B_{\text{Limit}}$ , signal is lost.

In case no magnetic differential signal is detected for a time longer than the stand still period  $T_{\text{stop}}$ , the stop pulse is output. Typically with the first output stop pulse, the circuitry reverts to the uncalibrated mode.



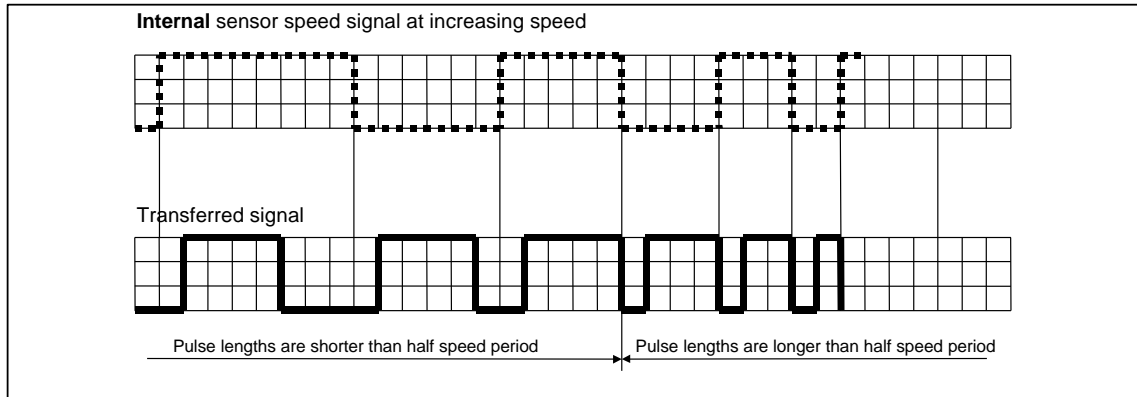
**Figure 8 Definition of PWM current interface**



**Figure 9 Definition of stand still output pulse**

### Duty cycle at fast changing frequencies

*If the duty cycle deviates from 50%, it is possible that the present pulse length is output entirely once and cut once, within the same period, see Figure 10.*



**Figure 10** Deviation of duty cycle at fast changing frequencies

### Electro Magnetic Compatibility - (values depend on $R_M$ !)

Ref. ISO 7637-1; test circuit 1;

$\Delta B = 2\text{mT}$  (amplitude of sinus signal);  $V_{CC}=13.5\text{ V}$ ,  $f_B= 100\text{ Hz}$ ;  $T= 25^\circ\text{C}$ ;  $R_M \geq 75\ \Omega$

No.	Parameter	Symbol	Level/typ.	Status
1.1.1	Testpulse 1	$V_{LD}$	IV / -100 V	C <sup>(1)</sup>
	Testpulse 2		IV / 100 V	C <sup>(1)</sup>
	Testpulse 3a		IV / -150 V	A
	Testpulse 3b		IV / +100 V	A
	Testpulse 4		IV / -7 V	B <sup>(3)</sup>
	Testpulse 5		IV / +86,5 V <sup>(2)</sup>	C

<sup>(1)</sup> According to 7637-1 the supply switched „OFF“ for  $t=200\text{ms}$ . For battery „ON“ is valid status „A“.

<sup>(2)</sup> Applying in the board net a suppressor diode with sufficient energy absorption capability.

<sup>(3)</sup> According to 7637-1 for test pulse 4 the test voltage shall be  $12\text{V} \pm 0,2\text{V}$

#### Values are valid for all TLE4941/42 types!

Ref. ISO 7637-3; test circuit 1;

$\Delta B = 2\text{mT}$  (amplitude of sinus signal);  $V_{CC}=13.5\text{ V}$ ,  $f_B= 100\text{ Hz}$ ;  $T= 25^\circ\text{C}$ ;  $R_M \geq 75\ \Omega$

No.	Parameter	Symbol	Level/typ.	Status
1.2.1	Testpulse 1	$V_{LD}$	IV / -30 V	A
	Testpulse 2		IV / 30 V	A
	Testpulse 3a		IV / -60 V	A
	Testpulse 3b		IV / 40 V	A

#### Values are valid for all TLE4941/42 types!

Ref. ISO 11452-3; test circuit 1; measured in TEM-cell

$\Delta B = 2\text{mT}$ ;  $V_{CC}=13.5\text{V}$ ,  $f_B= 100\text{ Hz}$ ;  $T= 25^\circ\text{C}$

No.	Parameter	Symbol	Level/Max.	Remarks
1.2.2	EMC field strength	$E_{\text{TEM-Cell}}$	IV / 200 V/m	AM=80%, $f=1\text{kHz}$ ;

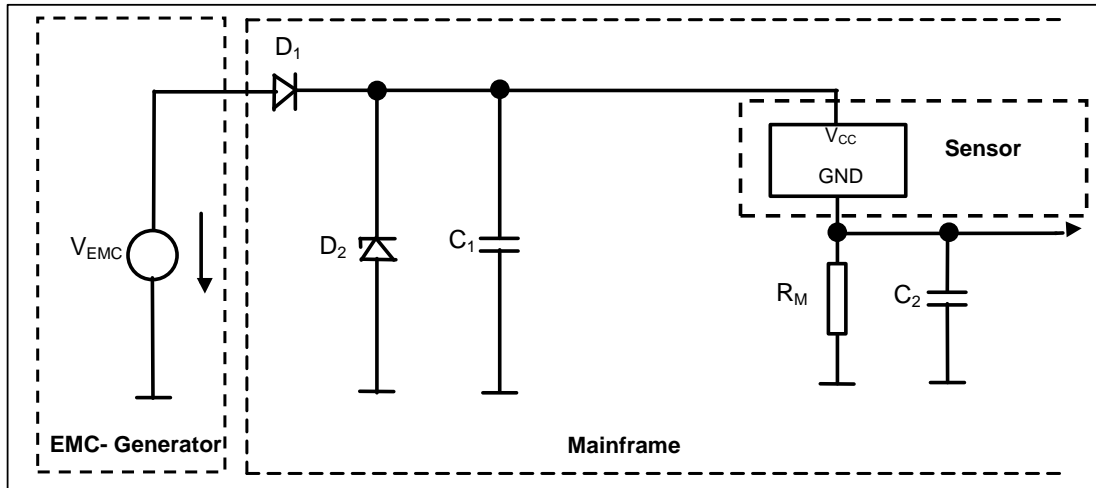
#### Only valid for non C- types!

Ref. ISO 11452-3; test circuit 1; measured in TEM-cell

$\Delta B = 2\text{mT}$ ;  $V_{CC}=13.5\text{V}$ ,  $f_B= 100\text{ Hz}$ ;  $T= 25^\circ\text{C}$

No.	Parameter	Symbol	Level/Max.	Remarks
1.2.2	EMC field strength	$E_{\text{TEM-Cell}}$	IV / 250 V/m	AM=80%, $f=1\text{kHz}$ ;

#### Only valid for C-types!



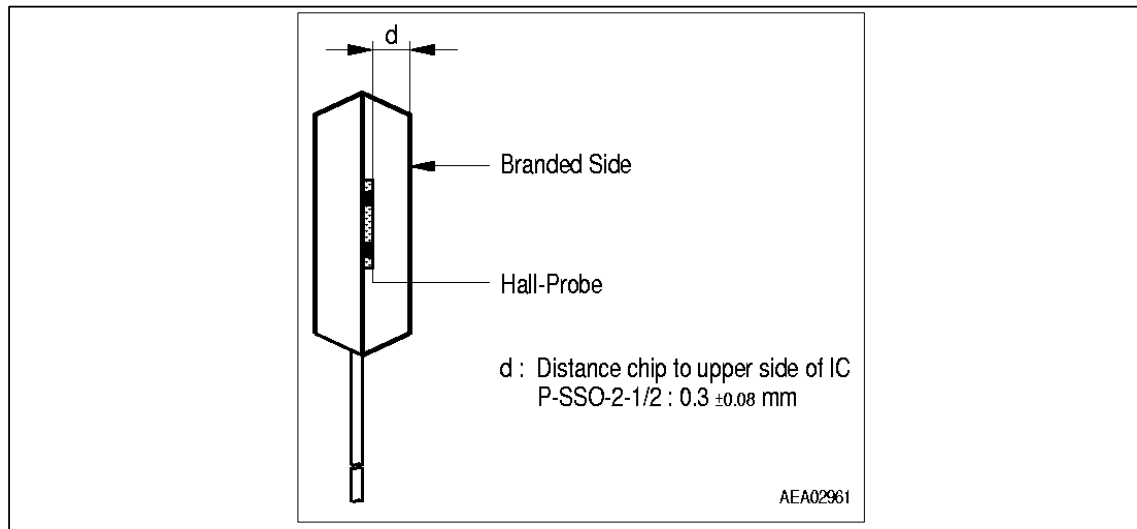
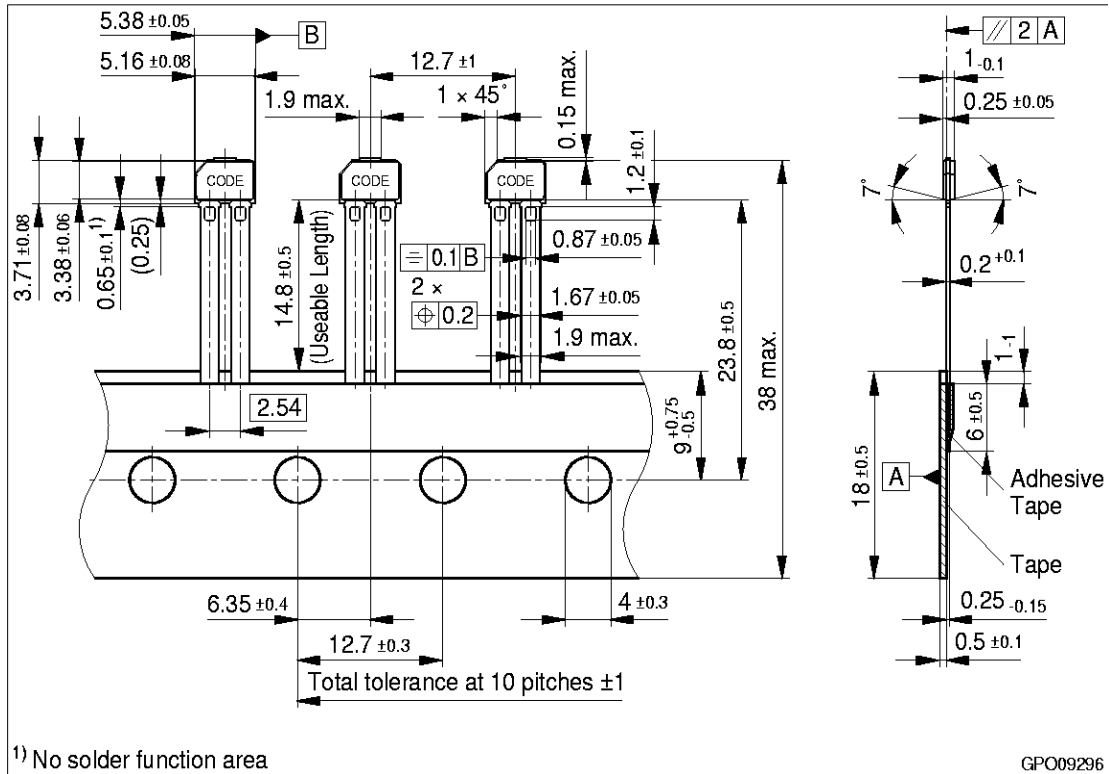
- Components:**
- D1: 1N4007
  - D2: T 5Z27 1J
  - C1: 10 $\mu$ F/35V
  - C2: 1nF/1000V
  - R<sub>M</sub>: 75 $\Omega$ /5W

**Figure 11 Test Circuit 1**



Package Outlines

**PSSO2-1**  
(Plastic Single Small Outline Package)



**PSSO2-2**  
(Plastic Single Small Outline Package)

