TLE42754

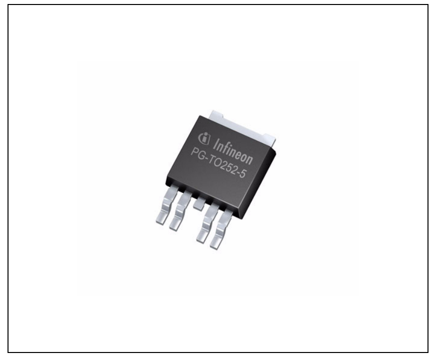
Low Dropout Linear Fixed Voltage Regulator

Automotive Power

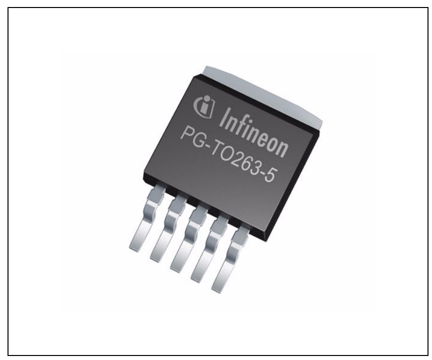
Never stop thinking

Low Dropout Linear Fixed Voltage Regulator **TLE42754**

1 Overview



PG-TO252-5



PG-TO263-5

Features

- Output Voltage 5 V ± 2%
- Ouput Current up to 450 mA
- Very low Current Consumption
- Power-on and Undervoltage Reset with Programmable Delay Time
- Reset Low Down to V_Q = 1 V
- Very Low Dropout Voltage
- Output Current Limitation
- Reverse Polarity Protection
- Overtemperature Protection
- Suitable for Use in Automotive Electronics
- Wide Temperature Range from -40 °C up to 150 °C
- Input Voltage Range from -42 V to 45 V
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE42754 is a monolithic integrated low-dropout voltage regulator in a 5-pin TO-package, especially designed for automotive applications. An input voltage up to 42 V is regulated to an output voltage of 5.0 V. The component is able to drive loads up to 450 mA. It is short-circuit proof by the implemented current limitation and has an integrated overtemperature shutdown. A reset signal is generated for an output voltage $V_{Q,rt}$ of typically 4.65 V. The power-on reset delay time can be programmed by the external delay capacitor.

Dimensioning Information on External Components

An input capacitor C_I is recommended for compensation of line influences. An output capacitor C_Q is necessary for the stability of the control loop.

Type	Package	Marking
TLE42754D	PG-TO252-5	TLE42754D
TLE42754G	PG-TO263-5	TLE42754G

Circuit Description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The component also has a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

2 Block Diagram

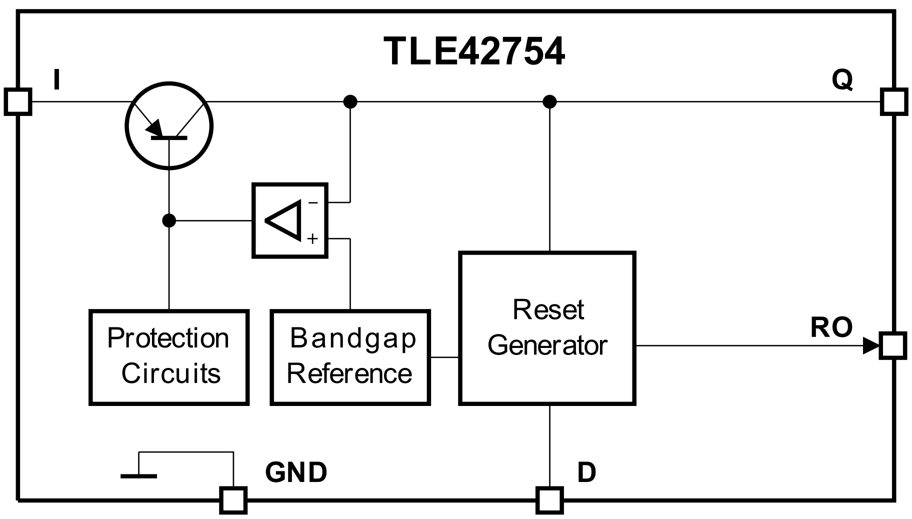


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment TLE42754D (PG-TO252-5) and TLE42754G (PG-TO263-5)

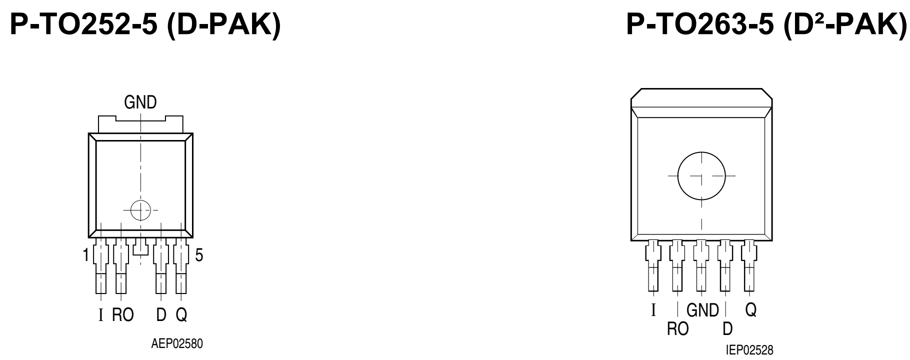


Figure 2 Pin Configuration (top view)

3.2 Pin Definitions and Functions TLE42754D (PG-TO252-5) and TLE42754G (PG-TO263-5)

Pin	Symbol	Function
1	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended
2	RO	**Reset Output** open collector output; external pull-up resistor to a positive potential required; leave open if the reset function is not needed
3	GND	**TLE42754G (PG-TO263-5) only: Ground** internally connected to tab
4	D	**Reset Delay Timing** connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
5	Q	**Output** block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in the table **"Functional Range" on Page 7**
TAB	GND	**Ground** connect to heatsink area

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

-40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Input						
4.1.1	Voltage	V_I	-42	45	V	–
Output						
4.1.2	Voltage	V_Q	-0.3	7	V	–
Reset Output						
4.1.3	Voltage	V_{RO}	-0.3	25	V	–
Reset Delay						
4.1.4	Voltage	V_D	-0.3	7	V	–
Temperature						
4.1.5	Junction Temperature	T_j	-40	150	°C	–
4.1.6	Storage Temperature	T_{stg}	-50	150	°C	–
ESD Absorption						
4.1.7	ESD Absorption	$V_{ESD,HBM}$	-2	2	kV	Human Body Model (HBM)[2)]
4.1.8		$V_{ESD,CDM}$	-500	500	V	Charge Device Model (CDM)[3)]
4.1.9			-750	750	V	Charge Device Model (CDM)[3)] at corner pins

1) Not subject to production test, specified by design.
2) ESD HBM Test according JEDEC JESD22-A114
3) ESD CDM Test according AEC/ESDA ESD-STM5.3.1-1999

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input Voltage	V_I	5.5	42	V	–
4.2.2	Output Capacitor's Requirements for Stability	C_Q	22	–	µF	–[1]
		$ESR(C_Q)$	–	3	Ω	–[2]
4.2.3	Junction Temperature	T_j	-40	150	°C	–

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%
2) relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Value			Unit	Conditions
			Min.	Typ.	Max.		
TLE42754D (PG-TO252-5)							
4.3.4	Junction to Case[1]	R_{thJC}	–	3.7	–	K/W	–
4.3.5	Junction to Ambient[1]	R_{thJA}	–	27	–	K/W	[2]
4.3.6			–	110	–	K/W	footprint only[3]
4.3.7			–	57	–	K/W	300 mm^2 heatsink area on PCB[3]
4.3.8			–	42	–	K/W	600 mm^2 heatsink area on PCB[3]
TLE42754G (PG-TO263-5)							
4.3.9	Junction to Case[1]	R_{thJC}	–	3.7	–	K/W	–
4.3.10	Junction to Ambient[1]	R_{thJA}	–	27	–	K/W	[2]
4.3.11			–	70	–	K/W	footprint only[3]
4.3.12			–	42	–	K/W	300 mm^2 heatsink area on PCB[3]
4.3.13			–	33	–	K/W	600 mm^2 heatsink area on PCB[3]

1) not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a $76.2 \times 114.3 \times 1.5$ mm^3 board with 1 copper layer (1 x 70µm Cu).

5 Block Description and Electrical Characteristics

5.1 Voltage Regulator

The output voltage V_Q is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table **"Functional Range" on Page 7** have to be maintained. For details see also the typical performance graph **"Output Capacitor Series Resistor ESR(CQ) versus Output Current IQ" on Page 12**. As the output capacitor also has to buffer load steps it should be sized according to the application's needs.

An input capacitor C_I is strongly recommended to compensate line influences. Connect the capacitors close to the component's terminals.

A protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain an output current limitation, a reverse polarity protection as well as a thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above V_I = 28 V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behaviour of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

The TLE42754 allows a negative supply voltage. In this fault condition, small currents are flowing into the IC, increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity conditions.

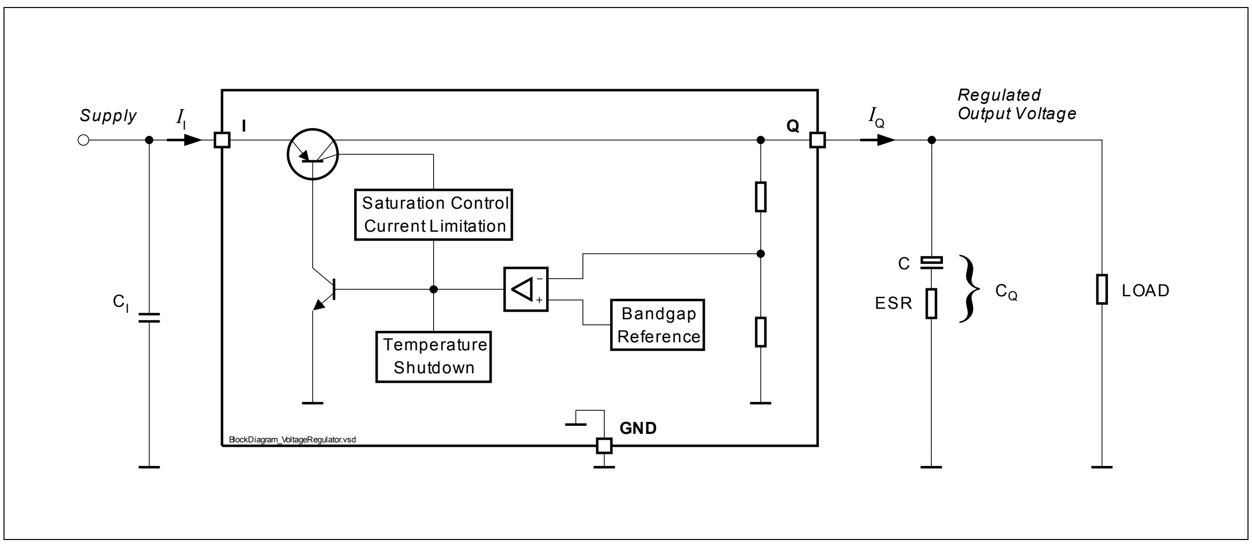


Figure 3 Voltage Regulator

Electrical Characteristics Voltage Regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

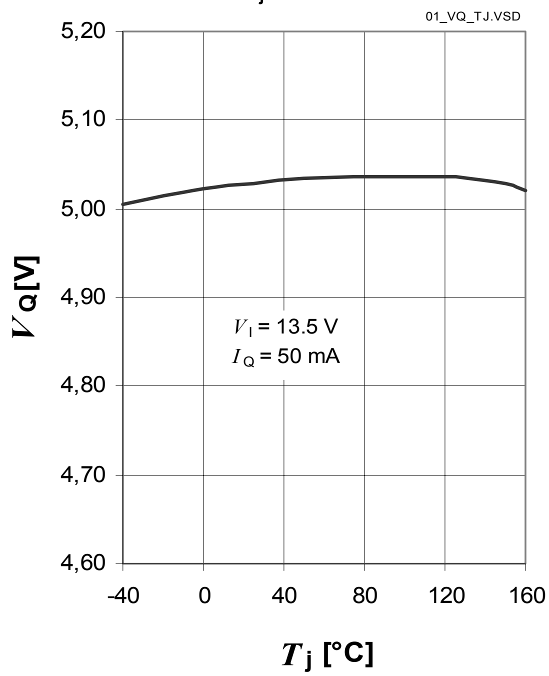
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Output Voltage	V_Q	4.9	5.0	5.1	V	1 mA < I_Q < 450 mA 9 V < V_I < 28 V
5.1.2	Output Voltage	V_Q	4.9	5.0	5.1	V	1 mA < I_Q < 400 mA 6 V < V_I < 28 V
5.1.3	Output Voltage	V_Q	4.9	5.0	5.1	V	1 mA < I_Q < 200 mA 6 V < V_I < 40 V
5.1.4	Output Current Limitation	$I_{Q,max}$	450	–	1100	mA	V_Q = 4.8V
5.1.5	Load Regulation steady-state	$\Delta V_{Q,load}$	-30	-15	–	mV	I_Q = 5 mA to 400 mA V_I = 8 V
5.1.6	Line Regulation steady-state	$\Delta V_{Q,line}$	–	5	15	mV	V_I = 8 V to 32 V I_Q = 5 mA
5.1.7	Dropout Voltage[1)] $V_{dr} = V_I - V_Q$	V_{dr}	–	250	500	mV	I_Q = 300 mA
5.1.8	Power Supply Ripple Rejection[2)]	$PSRR$	–	60	–	dB	f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp
5.1.9	Temperature Output Voltage Drift	dV_Q/dT	–	0.5	–	mV/K	–
5.1.10	Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing[2)]
5.1.11	Overtemperature Shutdown Threshold Hysteresis	$T_{j,sdh}$	–	20	–	°C	T_j decreasing[2)]

1) measured when the output voltage V_Q has dropped 100mV from the nominal value obtained at V_I = 13.5V

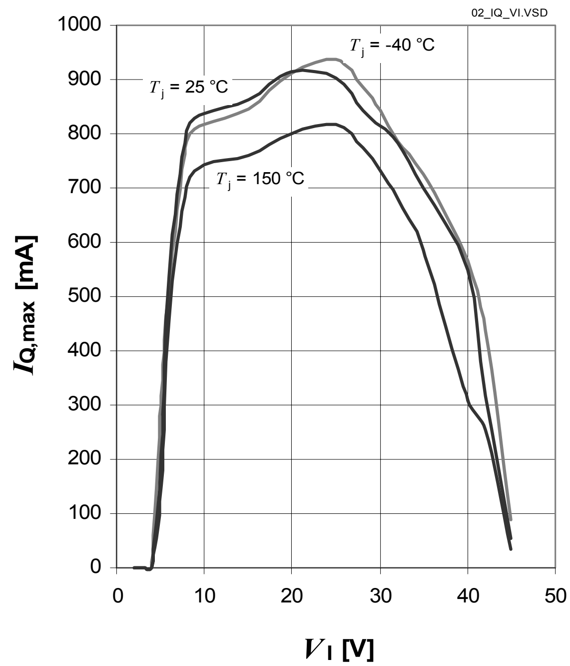
2) not subject to production test, specified by design

Typical Performance Characteristics Voltage Regulator

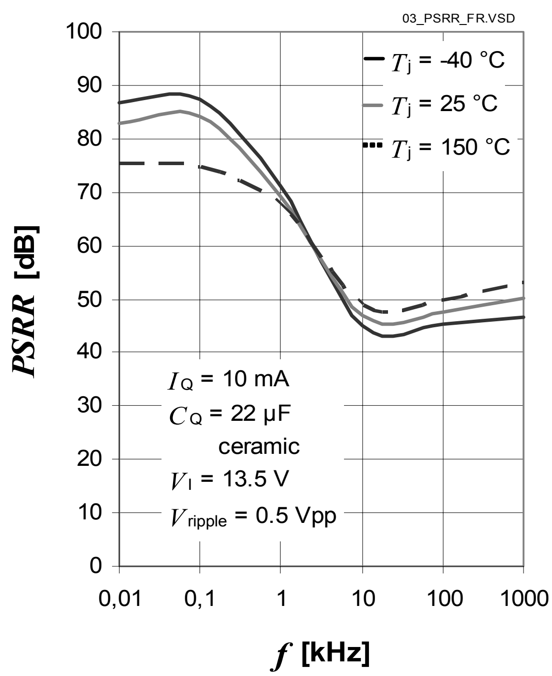
Output Voltage V_Q versus Junction Temperature T_j



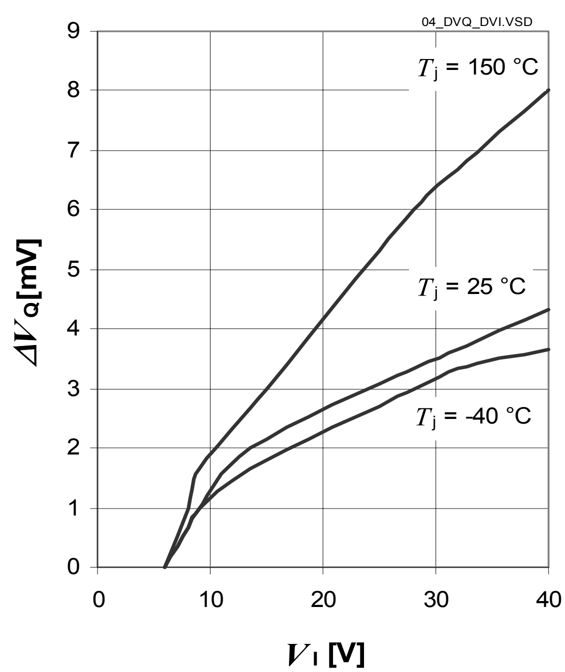
Output Current I_Q versus Input Voltage V_I



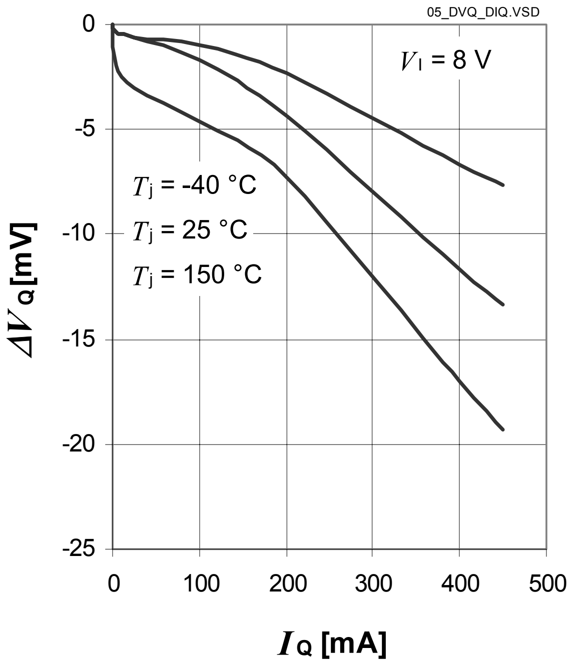
Power Supply Ripple Rejection *PSRR* versus ripple frequency f_r)



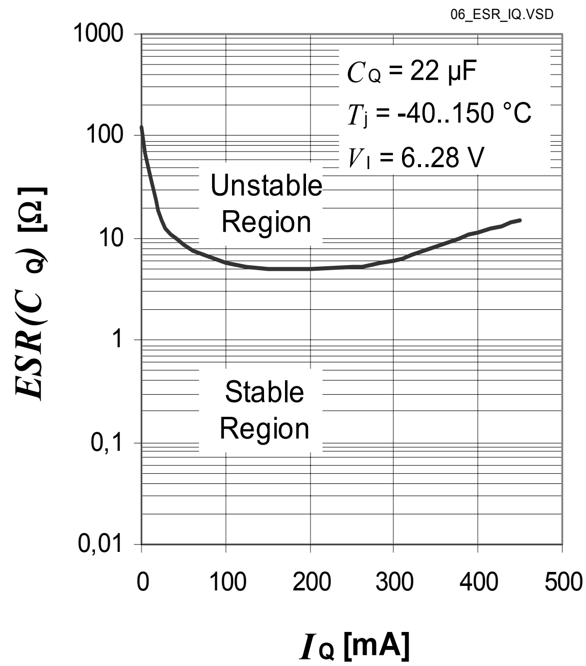
Line Regulation $\Delta V_{Q,line}$ versus Input Voltage Change ΔV_I)



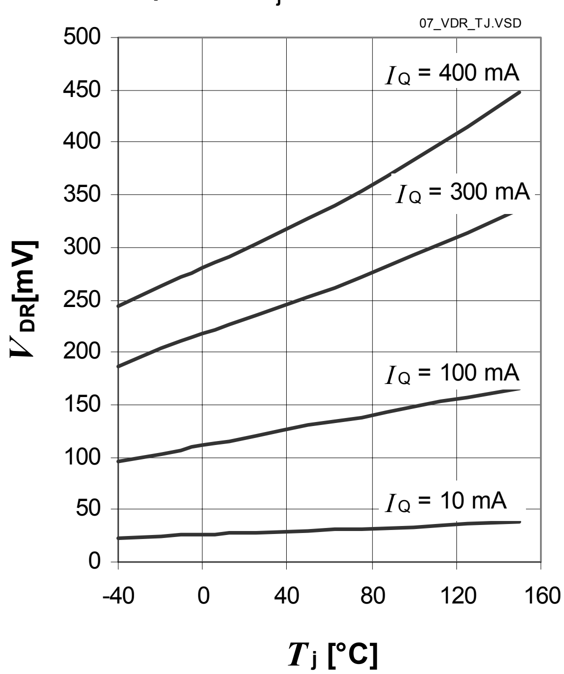
Load Regulation $\Delta V_{Q,load}$ versus Output Current Change ΔI_Q



Output Capacitor Series Resistor $ESR(C_Q)$ versus Output Current I_Q



Dropout Voltage V_{dr} versus Junction Temperature T_j



5.2 Current Consumption

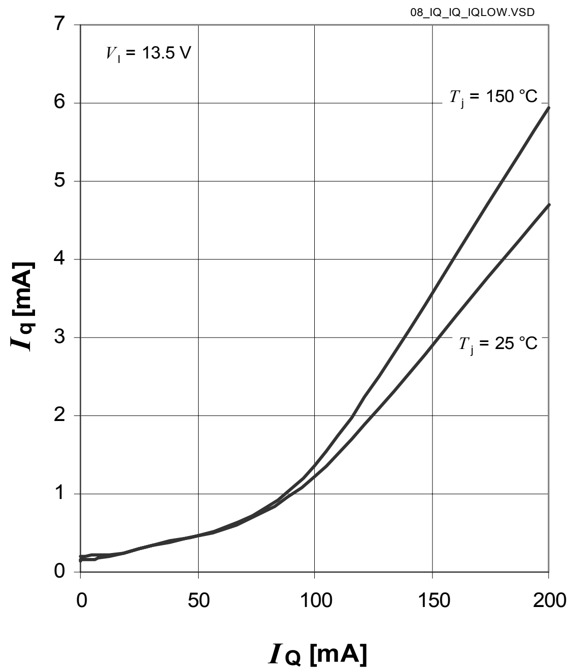
Electrical Characteristics Current Consumption

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, positive current flowing into pin
(unless otherwise specified)

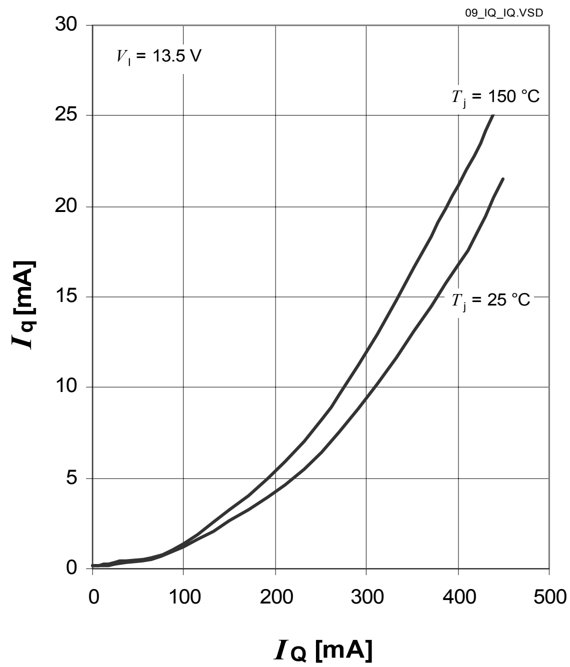
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Current Consumption $I_q = I_I - I_Q$	I_q	–	150	200	µA	I_Q = 1 mA T_j = 25 °C
5.2.2			–	150	220	µA	I_Q = 1 mA T_j = 85 °C
5.2.3			–	5	10	mA	I_Q = 250 mA
5.2.4			–	15	25	mA	I_Q = 400 mA

Typical Performance Characteristics Current Copnsumption

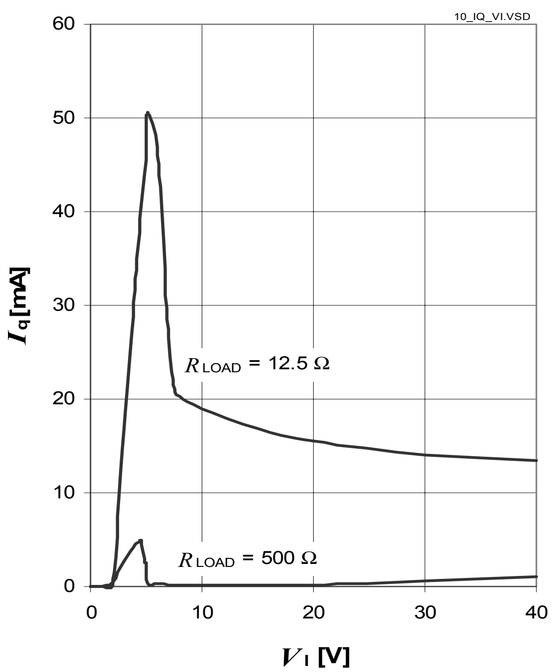
Current Consumption I_q versus Output Current I_Q (I_Q low)



Current Consumption I_q versus Output Current I_Q



Current Consumption I_q versus Input Voltage V_I



5.3 Reset Function

The reset function provides several features:

Output Undervoltage Reset:

An output undervoltage condition is indicated by setting the Reset Output RO to “low”. This signal might be used to reset a microcontroller during low supply voltage.

Power-On Reset Delay Time:

The power-on reset delay time t_{rd} allows a microcontoller and oscillator to start up. This delay time is the time frame from exceeding the reset switching threshold V_{RT} until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time t_{rd} is defined by an external delay capacitor C_D connected to pin D charged by the delay capacitor charge current $I_{D,ch}$ starting from V_D = 0 V.

If the application needs a power-on reset delay time t_{rd} different from the value given in **Item 5.3.6**, the delay capacitor’s value can be derived from the specified values in **Item 5.3.6** and the desired power-on delay time:

$$C_D = \frac{t_{rd,\,new}}{t_{rd}} \times 47\text{nF}$$

with

- C_D: capacitance of the delay capacitor to be chosen
- $t_{rd,new}$: desired power-on reset delay time
- t_{rd}: power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor’s tolerance into consideration.

Reset Reaction Time:

The reset reaction time avoids that short undervoltage spikes trigger an unwanted reset “low” signal. The reset reaction rime t_{rr} considers the internal reaction time $t_{rr,int}$ and the discharge time $t_{rr,d}$ defined by the external delay capacitor C_D (see typical performance graph for details). Hence, the total reset reaction time becomes:

$$t_{rr} = t_{rd,\,int} + t_{rr,\,d}$$

with

- t_{rr}: reset reaction time
- $t_{rr,int}$: internal reset reaction time
- $t_{rr,d}$: reset discharge

Reset Output Pull-Up Resistor R_{RO}:

The Reset Output RO is an open collector output requiring an external pull-up resistor to a voltage V_{IO}, e.g. V_Q. In **Table “Electrical Characteristics Reset Function” on Page 18** a minimum value for the external resistor R_{RO} is given for the case it is connected to V_Q or to a voltage $V_{IO} < V_Q$. If the pull-up resistor shall be connected to a voltage $V_{IO} > V_Q$, use the following formula:

$$R_{RO} = \frac{5\text{k}\Omega}{V_Q} \times V_{IO}$$

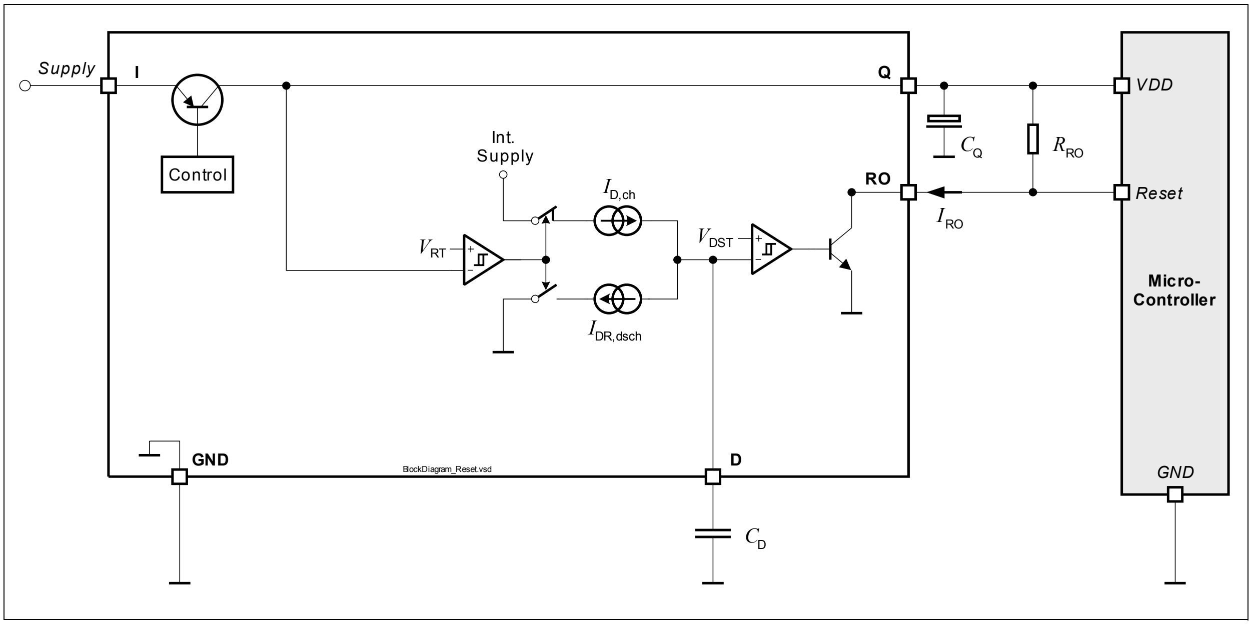


Figure 4 Block Diagram Reset Function

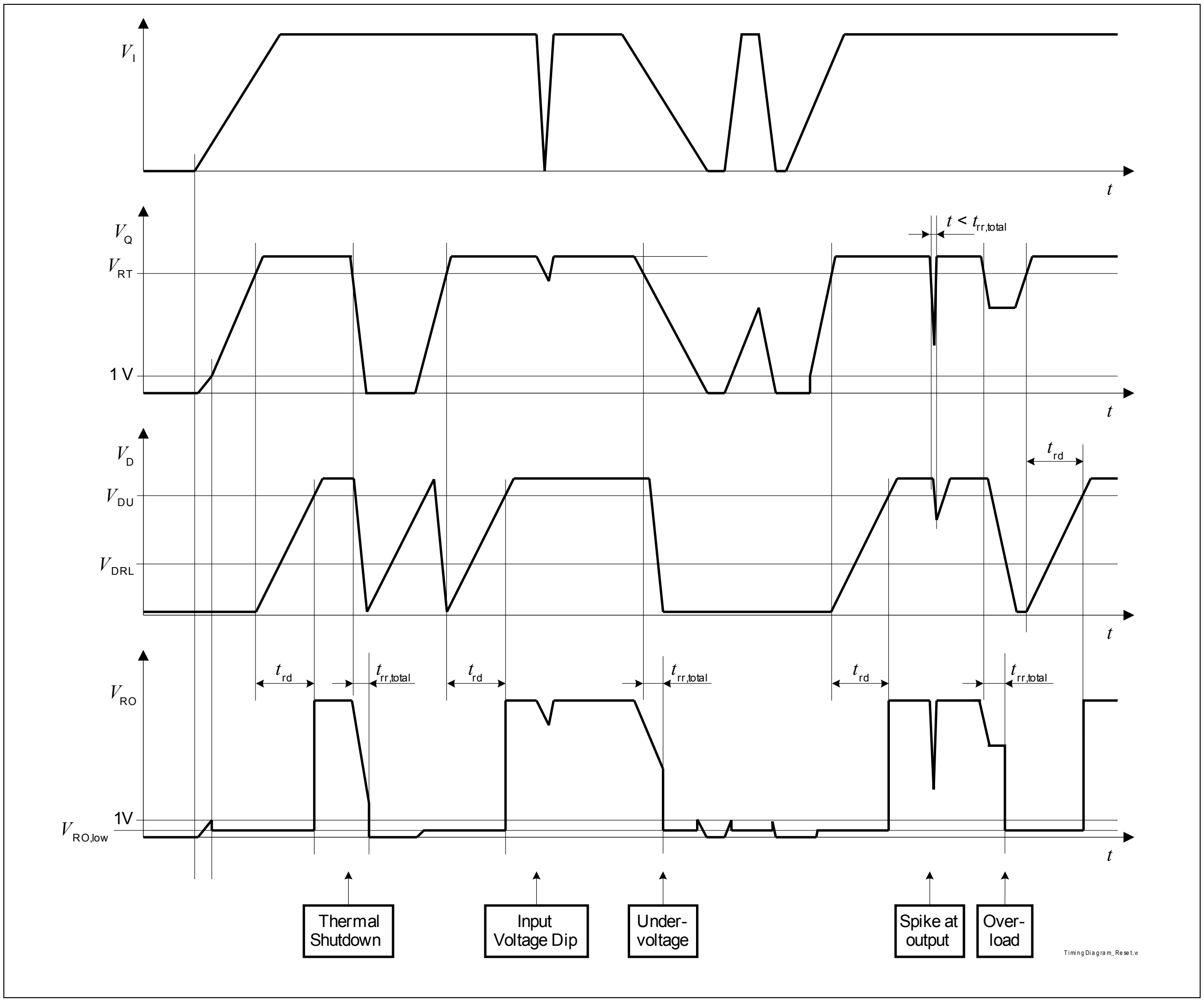


Figure 5 Timing Diagram Reset

Electrical Characteristics Reset Function

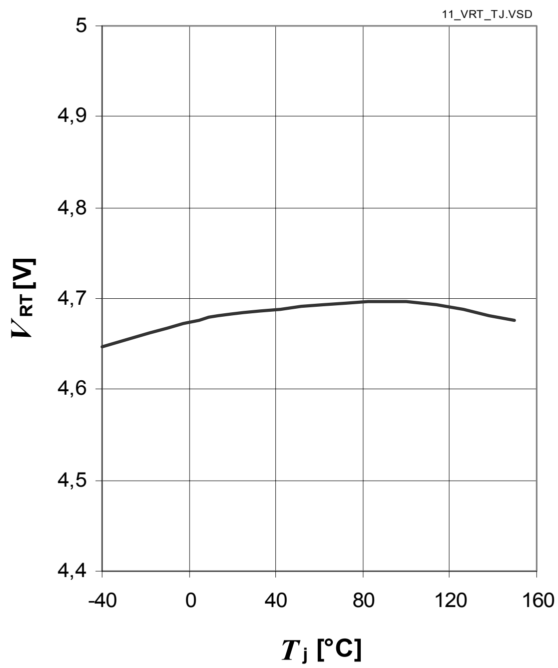
V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output Undervoltage Reset							
5.3.1	Output Undervoltage Reset Switching Thresholds	V_{RT}	4.5	4.65	4.8	V	V_Q decreasing
Reset Output RO							
5.3.2	Reset Output Low Voltage	$V_{RO,low}$	–	0.2	0.4	V	1 V ≤ V_Q ≤ V_{RT} ; I_{RO} = 0.2 mA
5.3.3	Reset Output Sink Current Capability	$I_{RO,max}$	0.2	–	–	mA	1 V ≤ V_Q ≤ V_{RT} ; V_{RO} = 5 V
5.3.4	Reset Output Leakage Current	$I_{RO,leak}$	–	0	10	µA	V_{RO} = 5 V
5.3.5	Reset Output External Pull-up Resistor to V_Q	R_{RO}	5	–	–	kΩ	1 V ≤ V_Q ≤ V_{RT} ; V_{RO} ≤ 0.4 V
Reset Delay Timing							
5.3.6	Power On Reset Delay Time	t_{rd}	10	16	22	ms	C_D = 47 nF
5.3.7	Upper Delay Switching Threshold	V_{DU}	–	1.8	–	V	–
5.3.8	Lower Delay Switching Threshold	V_{DRL}	–	0.65	–	V	–
5.3.9	Delay Capacitor Charge Current	$I_{D,ch}$	–	5.5	–	µA	V_D = 1 V
5.3.10	Delay Capacitor Reset Discharge Current	$I_{D,dch}$	–	100	–	mA	V_D = 1 V
5.3.11	Delay Capacitor Discharge Time	$t_{rr,d}$	–	0.5	1	µs	Calculated Value: $t_{rr,d} = C_D*(V_{DU} - V_{DRL})/ I_{D,dch}$ C_D = 47 nF
5.3.12	Internal Reset Reaction Time	$t_{rr,int}$	–	4	7	µs	C_D = 0 nF[1)]
5.3.13	Reset Reaction Time	$t_{rr,total}$	–	4.5	8	µs	Calculated Value: $t_{rr,total} = t_{rr,int} + t_{rr,d}$ C_D = 47 nF

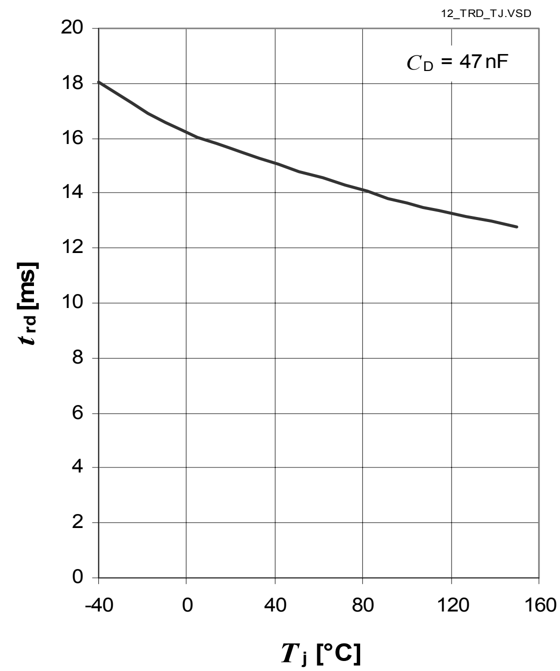
1) parameter not subject to production test; specified by design

Typical Performance Characteristics

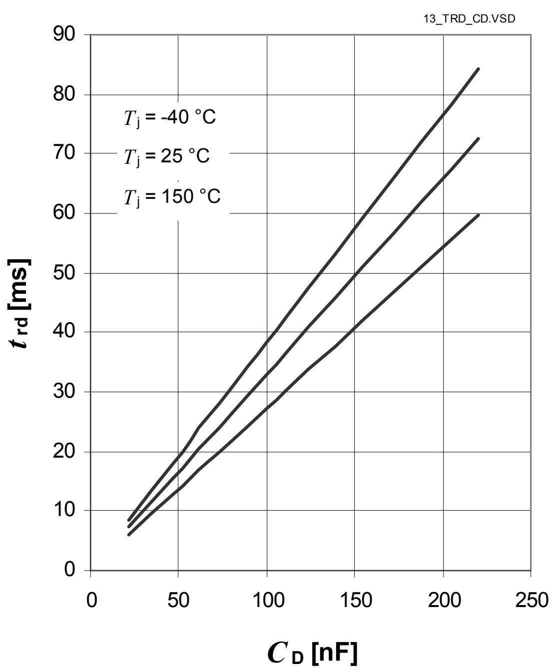
Undervoltage Reset Switching Threshold V_{RT} versus T_j



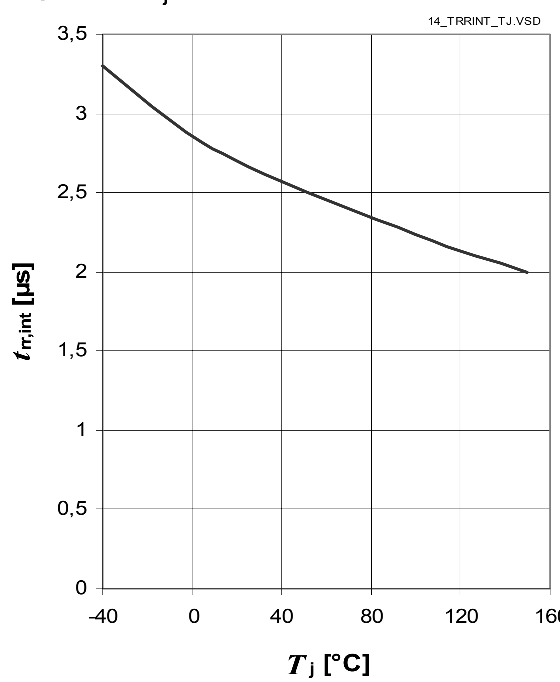
Power On Reset Delay Time t_{rd} versus Junction Temperature T_j



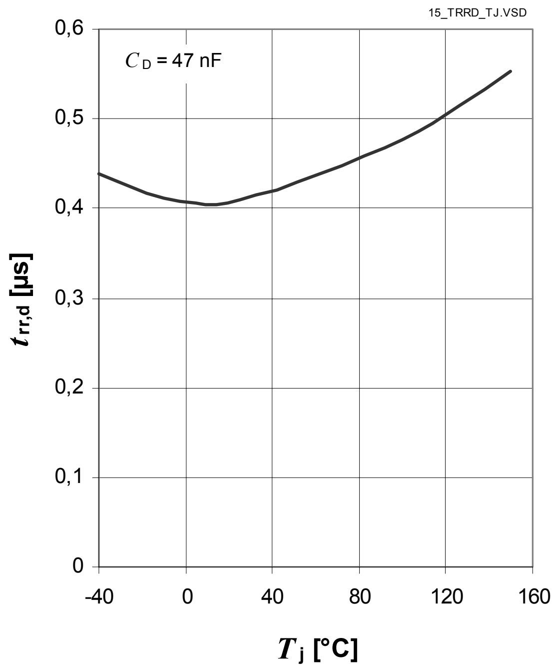
Power On Reset DelayTime t_{rd} versus Capacitance C_D



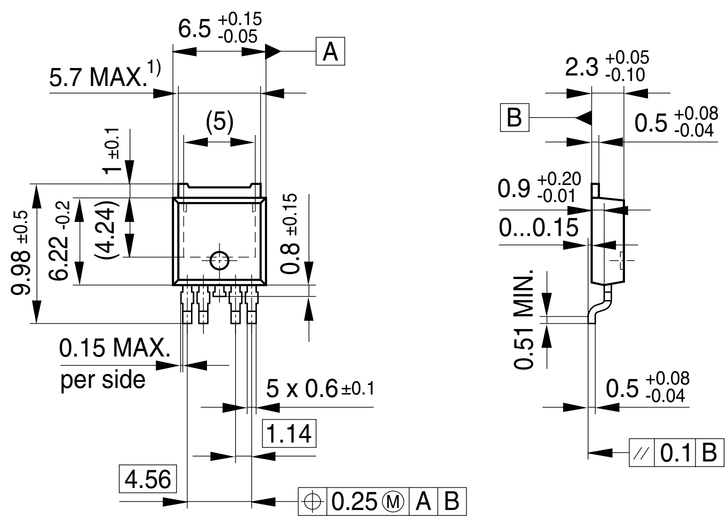
Internal Reset Reaction Time $t_{rr,int}$ versus Junction Temperature T_j



Delay Capacitor Discharge Time $t_{rr,d}$ versus Junction Temperature T_j



6 Package Outlines



1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

Figure 6 PG-TO252-5

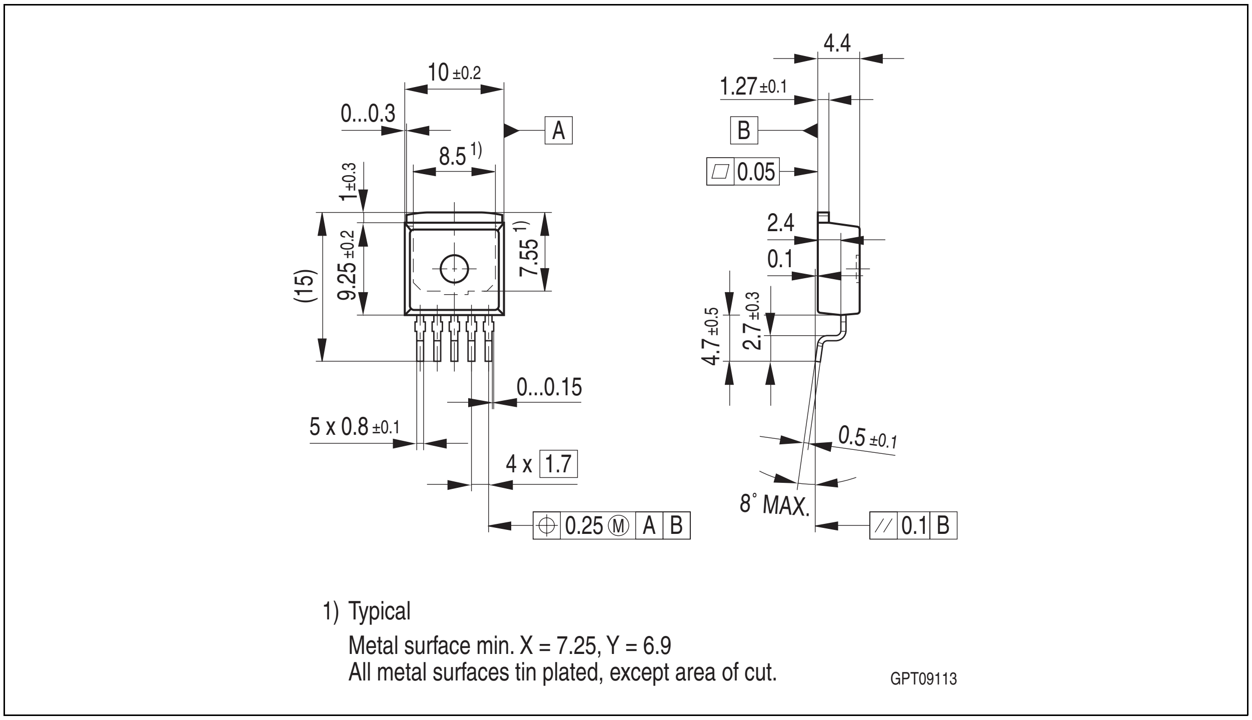


Figure 7 PG-TO263-5

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **http://www.infineon.com/products**.

Dimensions in mm

7 Revision History

Version	Date	Changes
1.0	2008-05-29	final data sheet

Edition 2008-05-29

Published by
Infineon Technologies AG
81726 Munich, Germany

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