NUD4330MN

Advance Information

Three Channel Linear LED Driver

The NUD4330 device is an integrated LED driver designed to replace discrete solutions for driving multiple LED arrays in DC high voltage applications (up to 200 V).

It contains three independent channels capable to drive three independent LED arrays of up to 100 mA. The LED current setting for each of the channels is made through an external low power resistor.

It also has three enable pins that control each of the channels independently for PWM or on/off purposes.

The device is packaged in a space saving 18 pins 6x5 mm DFN package.

Features

- Independent PWM (On/Off) Control for Each of the Channels
- Internal Thermal Protection
- Independent LED current setting up to 100 mA for each channel
- Settable Low Quiescent Current Circuit for Battery Based Applications
- This is a Pb-Free Device

Typical Applications

- LED General Lighting
- LED Backlighting

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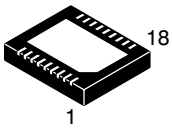
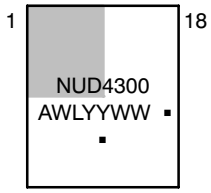
MARKING DIAGRAM



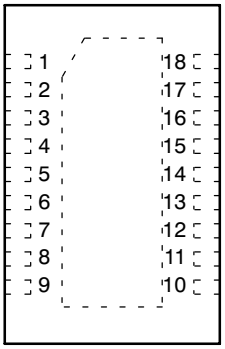


18-LEAD DFN
MN SUFFIX
CASE 505

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
E	= Automotive Grade
▪	= Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NUD4330MNTXG	DFN18 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

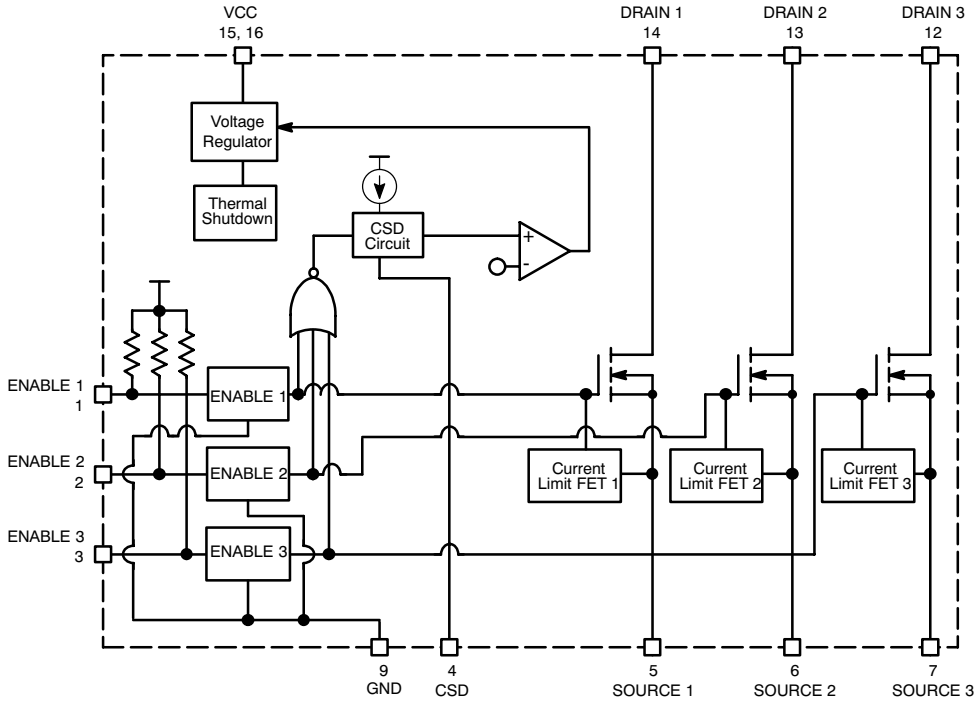


Figure 1. Block Diagram

Table 1. FUNCTIONAL PIN DESCRIPTION

Pin	Function	Description
1	Enable 1	This pin is used for enable or PWM dimming control of channel 1. A positive voltage signal at this pin enables channel 1. A PWM signal with greater amplitude than 2.2 V is required for dimming control.
2	Enable 2	This pin is used for enable or PWM dimming control of channel 2. A positive voltage signal at this pin enables channel 2. A PWM signal with greater amplitude than 2.2 V is required for dimming control.
3	Enable 3	This pin is used for enable or PWM dimming control of channel 3. A positive voltage signal at this pin enables channel 3. A PWM signal with greater amplitude than 2.2 V is required for dimming control.
4	CSD	This pin is the circuit shutdown delay and can be used to set the non-operational IBias to a low value. See applications info for more details about this circuit.
5	Source 1	Source terminal of the FET 1. A resistor from this pin to ground is used to set the ILimit for channel 1.
6	Source 2	Source terminal of the FET 2. A resistor from this pin to ground is used to set the ILimit for channel 2.
7	Source 3	Source terminal of the FET 3. A resistor from this pin to ground is used to set the ILimit for channel 3.
8,10,11 17, 18	N/C	No Connection
9	GND	The ground reference to the device.
12	Drain 3	Drain terminal of the FET 3, which is also the switching node of the load 3.
13	Drain 2	Drain terminal of the FET 2, which is also the switching node of the load 2.
14	Drain 1	Drain terminal of the FET 1, which is also the switching node of the load 1.
15,16	VCC	Input voltage to the LED driver. This voltage can be between 20 V and 80 V dc.
19		This pin is the center flag of the package. Although it does not have direct contact with the ground potential, it is still recommended to ground it.

Table 2. MAXIMUM RATINGS (Maximum ratings are those, that, if exceeded, may cause damage to the device. Electrical Characteristics are not guaranteed over this range)

Rating	Symbol	Value	Unit
Control Circuitry Input Voltage, Operating (V_{CC} to Ground)	V_{CC}	20 to 80	V
Drain Voltage, Operating (Drain to Ground) Steady-State Transient (1 ms)	V_{DD}	 200 220	V
Maximum Enable Voltage, Operating	V_{EN}	12	V
Maximum Voltage at CSD pin	V_{CSD}	10	V
Drain Current, Peak	I_{Dpk}	200	mA
Drain Current, Continuous	$I_{D(avg)}$	100	mA
Human Body Model (HBM) Machine Model (MM) According to EIA/JESD22/A114, A115 Specifications	ESD	2000 200	V

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Operating Temperature Range	T_J	-40 to 125	°C
Non-Operating Temperature Range	T_J	-55 to 150	°C
Lead Temperature, Soldering (1/8 in from case for 10 sec)	T_L	260	°C
Thermal Resistance, Junction-to-Air Mounted onto the Minimum Recommended Pad Mounted onto FR-4 Board, 1.0 in^2 Pad, 1 oz Coverage	Q_{JA}	 240 65	 °C/W °C/W
Thermal Resistance, Junction-to-Lead	Q_{JL}	12	°C/W
Power Dissipation (T_A = 25°C) Mounted onto the Minimum Recommended Pad Mounted onto FR-4 Board, 1.0 in^2 Pad, 1 oz Coverage	P_{max}	 0.52 1.92	W

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = 25°C, Rsense = 16.5 Ω 1%)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET (Each Channel)					
ON Resistance (V_{CC} = 24V, I_D = 20 mA, R_{sense} = 16.5 Ω, Enable = 3.3 V)	$R_{DS(ON)}$	-	20	-	Ω
Zero Enable Voltage Drain Current (V_{DD} = 200 V, Enable Low)	I_{DSS}	-	-	10	μA
Drain-to-Source Sustaining Voltage (I_D = 1 mA)	$V_{(BR)}$	200	-	-	V
Output Capacitance (V_{DD} = 40 V, Enable Low, f = 1 kHz)		-	330	-	pF
Voltage drop (Notes 1 and 2) (I_D = 30 mA, R_{sense} = 16.5 Ω, Enable = 3.3 V)	V_{drop}	-	-	1.5	V
CURRENT REGULATION CIRCUIT (Each Channel)					
Line LED Current Regulation, (T_J = -20°C to 85°C) (V_{in} = 0.8 V_{DD} to V_{DD}max; V_{CC} = 24 V; R_{sense} = 16.5 Ω, V_{LEDs} = 0.8 V_{DD} - 2 V ; Enable = 3.3 V)	I_{out1}	28.5	30	31.5	mA
Load LED Current Regulation, (T_J = -20 to 85°C) (V_{in} = rated V_{DD}, V_{CC} = 24 V, V_{LEDs} = 0.8 V_{in} to (V_{in} - 2 V), R_{sense} =16.5 Ω; Enable = 3.3 V)	I_{out2}	28.5	30	31.5	mA
THERMAL LIMIT					
Shutdown Junction Temperature (Notes 3 and 4)	T_{SD}	140	150	160	°C
Hysteresis (Note 4)	T_{hyst}	-	10	-	°C
ENABLE CIRCUIT (Each Channel)					
Logic Level High (Unit Operational)	V_{ENhigh}	2.2	-	-	V
Logic Level Low (Unit Shutdown)	V_{ENlow}	-	-	1.6	V
PWM Frequency	f_{PWM}	100	-	1000	Hz
Internal Pullup Resistor (Connected to an Internal 9 V Source)	R_{pullup}	-	600	-	kΩ
CSD CIRCUIT					
Charging Current (Into External Capacitor) (V_{CC} = 24 V, CSD Pin Grounded)	I_{Charge}	9.0	10	11	μA
Maximum Capacitor Voltage	V_{Cmax}	-	-	10	V
TOTAL DEVICE					
Bias Current, Operational (All Enables = 3.3 V, V_{CC} = 40 V)	I_{BIAS1}	-	1	2.5	mA
Bias Current, Non-Operational (All Enables Low, CSD Pin Open, V_{CC} = 40 V)	I_{BIAS2}	-	100	200	μA
Bias Current, Non-Operational (All Enables Low, CSD Pin Grounded, V_{CC} = 40 V)	I_{BIAS3}	-	600	800	μA
Minimum Operating Voltage	V_{CCmin}	20	-	-	V
SWITCHING CHARACTERISTICS					
Propagation Delay Times (V_{EN} = 3.3V, V_{CC} = 24V, V_{in} = 60 V, R_L = 1.5 kΩ, R_{sense} = 10 Ω, CSD Pin Shorted) High to Low Propagation Delay Low to High Propagation Delay	 t_{PHL} t_{PLH}	 - -	 2960 96	 - -	ns
Transition Times (V_{EN} = 3.3 V, V_{CC} = 24 V, Vin = 60 V, R_L = 1.5 kΩ, R_{sense} = 10 Ω, CSD Pin Shorted) Rise Time; Fall Time;	 tr tf	 - -	 90 620	 - -	ns

1. V_{drop} = V_{DS} + V_{Rsense} (This is the minimum voltage needed across the device and R_{sense} for operation)
2. The max voltage drop is limited by the device's power dissipation for given conditions of ambient temperature and board copper area.
3. The typical thermal limit is set to 150°C so that the device shuts down when its lead temperature reaches 138°C for 1.0 W of power dissipation and 12°C/W of junction-to-lead thermal resistance.
4. Guaranteed by design

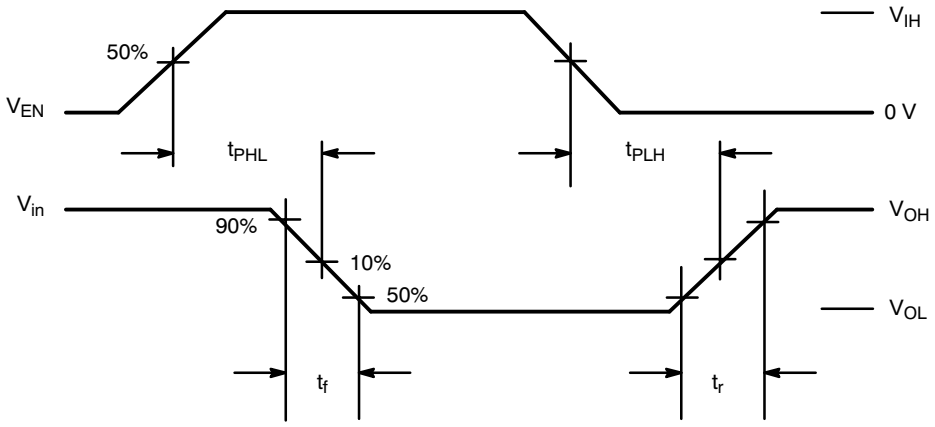


Figure 2. Switching Waveforms

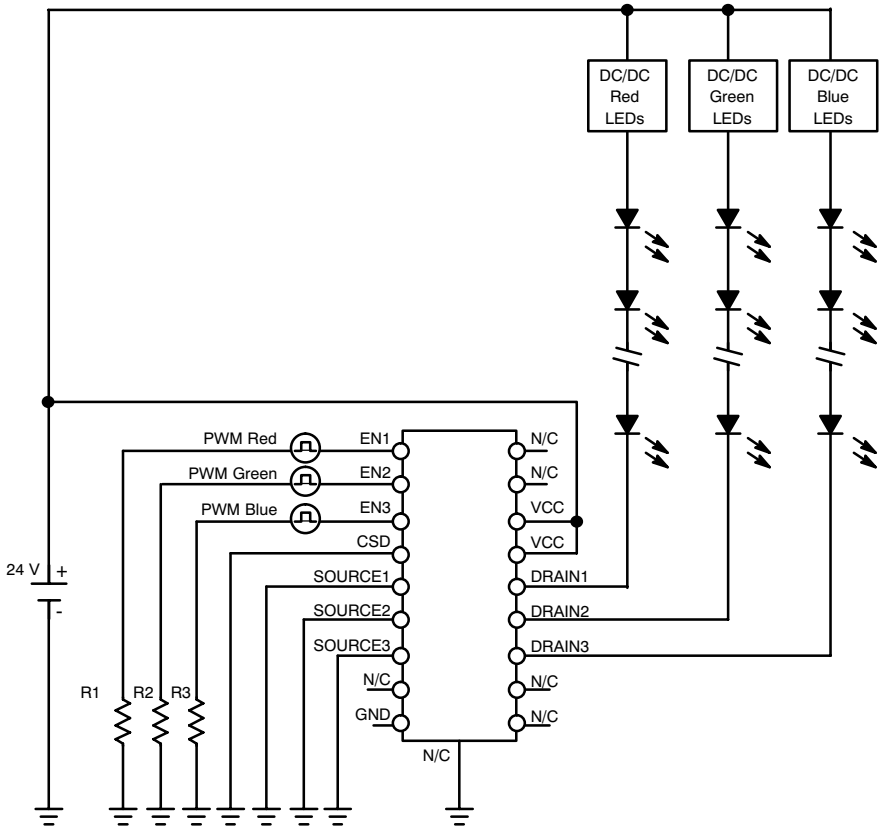


Figure 3. Typical Application Circuit

TYPICAL PERFORMANCE CURVES (T_A = 25°C unless otherwise noted)

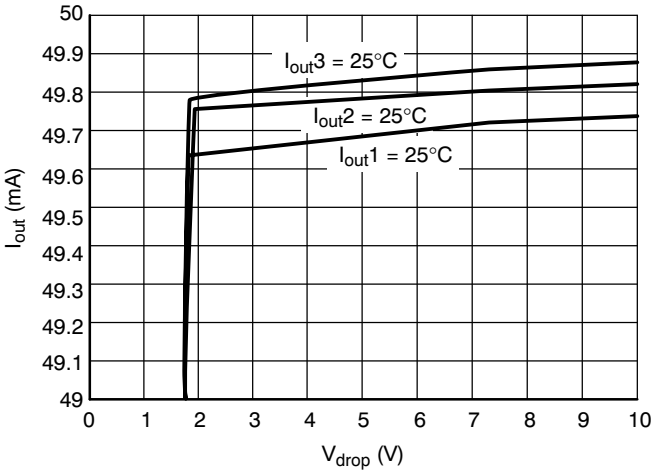


Figure 4. Line Regulation (V_{CC} = 24 V, R_{sense} = 10 Ω, 1%, V_{drop} Changing)

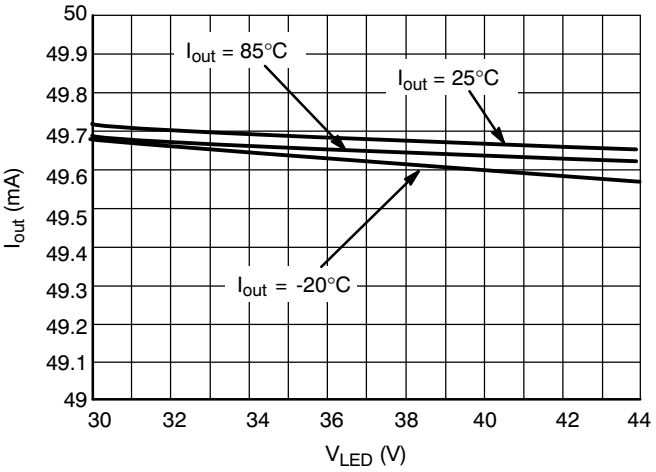


Figure 5. Load Regulation (V_{CC} = 24 V, R_{sense} = 10 Ω, 1%, V_{in} = 50 V)

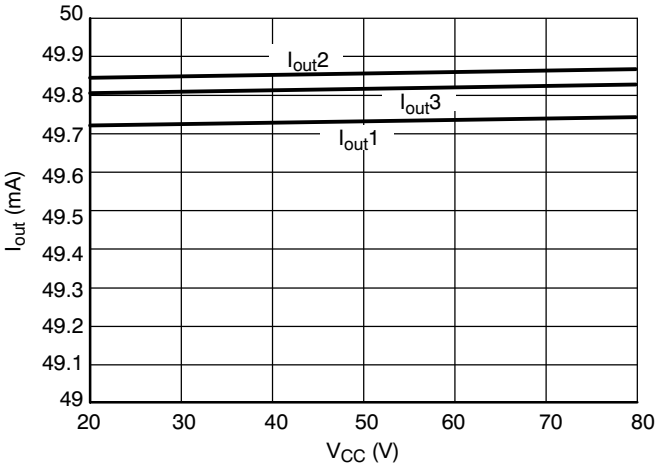


Figure 6. V_{CC} Regulation (V_{in} = 60 V, V_{LED}s = 56 V, R_{sense} = 10 Ω, 1%)

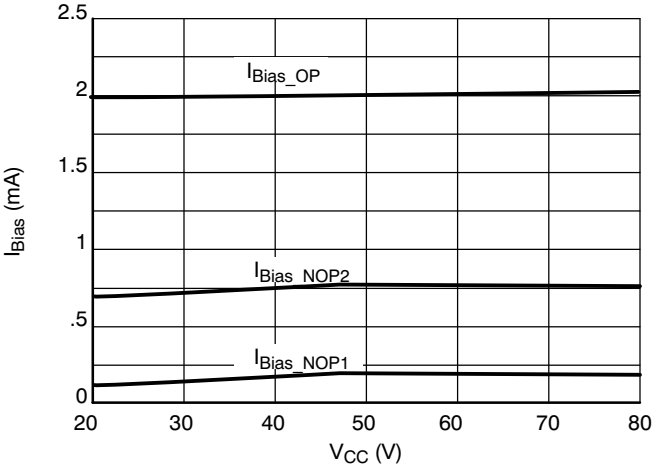


Figure 7. I_{Bias} vs V_{CC} Voltage

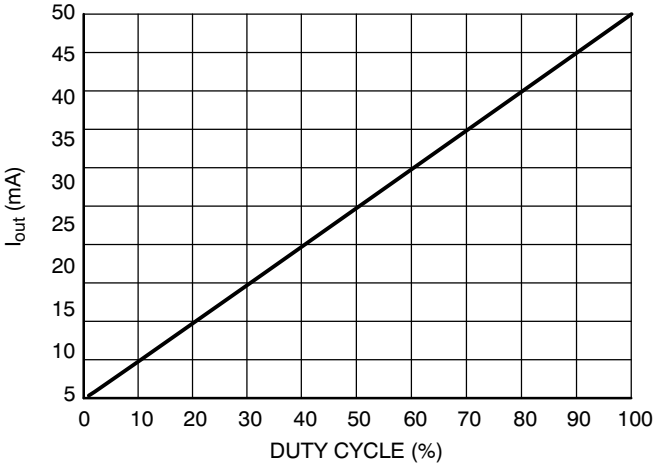


Figure 8. PWM Performance (V_{CC} = 24 V, R_{sense} = 10 Ω, 1%)

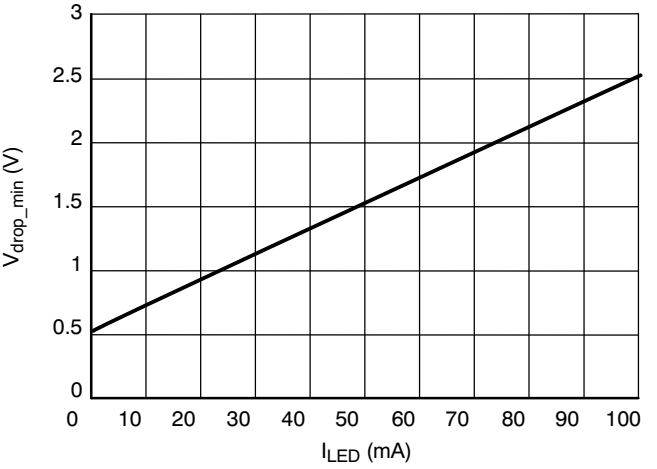


Figure 9. Typical I_{LED} vs V_{drop_min}

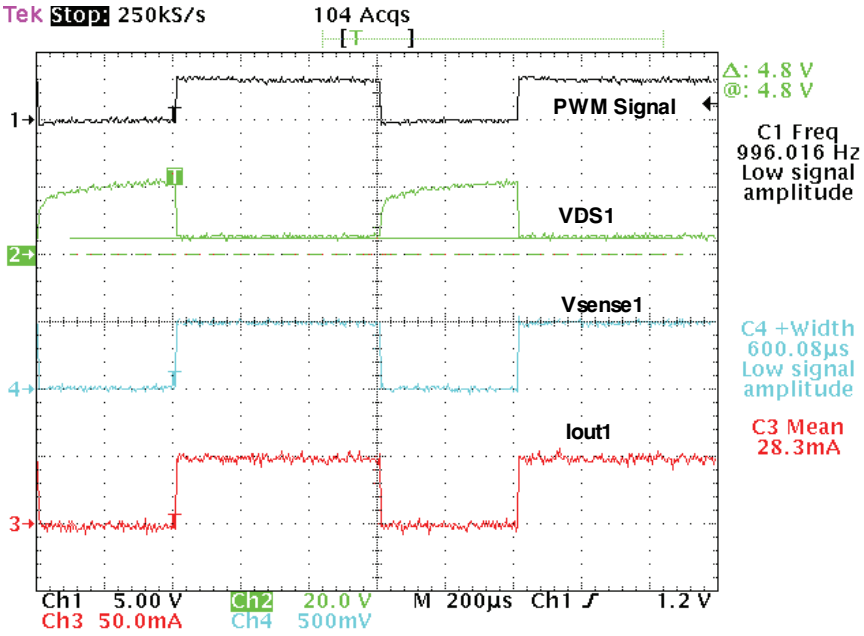


Figure 10. PWM Waveforms (V_{CC} = 24 V, R_{sense} = 10 Ω, 1%)

APPLICATIONS INFORMATION

Theory of Operation

This device contains three linear LED current sources. Each channel is comprised of a FET controlled by a current limit circuit that senses the voltage drop across the Rsense resistor and compares it with an internal bandgap voltage reference (0.5 V) to provide the current regulation.

Current Limit Circuit

The current limit circuit contains a bandgap voltage reference of 0.5 V. Then the value of the sense resistor (R_{sense}) is calculated by simply using the ohms law formula:

$$R_{sense} = \frac{0.5\ V}{I_{LED}} \qquad \text{(eq. 1)}$$

Each of the three channels can be set independently for I_{LED} using the same formula.

CSD Circuit

The circuit shutdown delay (CSD) allows for low quiescent current when the device is in its non-operational state (all enables low). This is extremely important in particular for Li-Ion battery based applications (LapTops and portables). Figure 11 shows the equivalent circuit for CSD

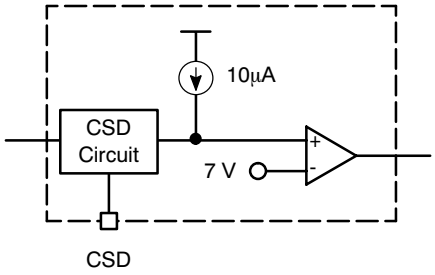


Figure 11. CSD Circuit

Depending on how the CSD pin is connected, the CSD circuit can be configured for three different options:

- CSD pin open = immediate shutdown
- CSD pin grounded = No shutdown
- External capacitor = Delay before shutdown

The delay capacitor is connected between CSD pin and ground and is calculated using the following formula:

$$C_{delay} = \frac{\left(t_{delay} \times 10^{E-6}\ A\right)}{7.0\ V} \qquad \text{(eq. 2)}$$

Where:

T_{delay} = Wanted delay time (seconds)

C_{delay} = Delay capacitor (Farads)

Thermal Shutdown

The temperature limit circuit senses the temperature of the junction and removes the gate drive of all FETs if the maximum level (150°C) is exceeded. There is a nominal hysteresis of 10°C for this circuit. After a thermal shutdown, the device will automatically restart when the temperature drops to a safe level as determined by the hysteresis.

Minimum Vdrop

There is a minimum voltage drop required to have across the drain-to-source terminals of each of the FETs and R_{sense} for operation. Since $V_{drop} = V_{DS} + V_{Rsense}$, the minimum V_{drop} required will change for different I_{LED} currents according the following formula:

$$Vdrop_{min} = \left(I_{LED} \times R_{DS(on)}\right) + 0.5\ V \qquad \text{(eq. 3)}$$

This will be the minimum voltage required across the drain-to-source terminals of each of the FETs and its respective Rsense for regulation.

Maximum Vdrop

The maximum voltage drop in each of the channels will be limited by the device's max power dissipation. That is, the voltage drop across each of the internal FETs should be taken into account for the calculation of the device's total power dissipation. The following formula is used to calculate the device's total power dissipation:

$$P_{Dtotal} = P_{Dcontrol} + P_{Dch1} + P_{Dch2} + P_{Dch3} \qquad \text{(eq. 4)}$$

$$P_{Dtotal} = \left(V_{CC} * 2.5\ mA\right) + \left(V_{DS1} * I_{LED1}\right) + \left(V_{DS2} * I_{LED2}\right) + \left(V_{DS3} * I_{LED3}\right) \qquad \text{(eq. 5)}$$

Where $V_{DS(n)} = V_{DD(n)} - V_{LEDs(n)} - 0.5V$

The resulting total power dissipation should not exceed the PD value shown on the maximum ratings table.

Power Dissipation

Since the NUD4330 device is a linear device, power dissipation considerations should be taken into account. That is, the device's power dissipation listed on the maximum ratings table is for T_A = 25°C. So the device's power dissipation capability will be derated for higher temperatures than 25°C. The following formula may be used for those purposes:

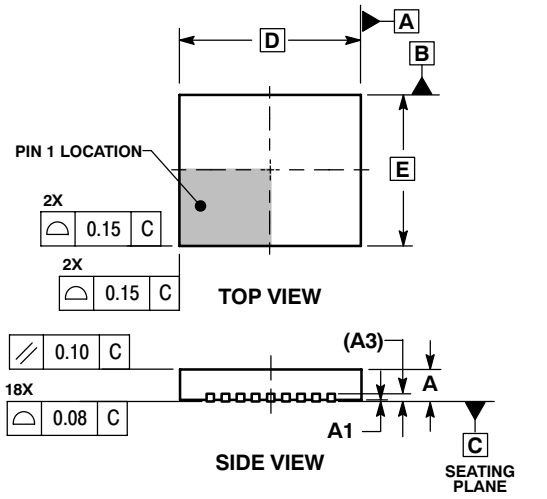
$$T_J = T_A + R_{\theta JA} \times P_D \qquad \text{(eq. 6)}$$

Enable Circuit

The enable circuit can be used to enable/disable the channels or for PWM dimming purposes. The PWM frequency is recommended to be between 100 Hz and 1 kHz. Each of the enable circuits have an internal 0.6 MΩ pullup resistor connected to an internal 9 V voltage source. So if left open, the channel will automatically be enabled.

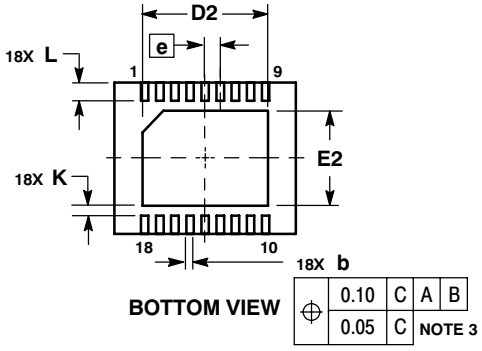
PACKAGE DIMENSIONS

DFN18 6x5, 0.5P
CASE 505-01
ISSUE D

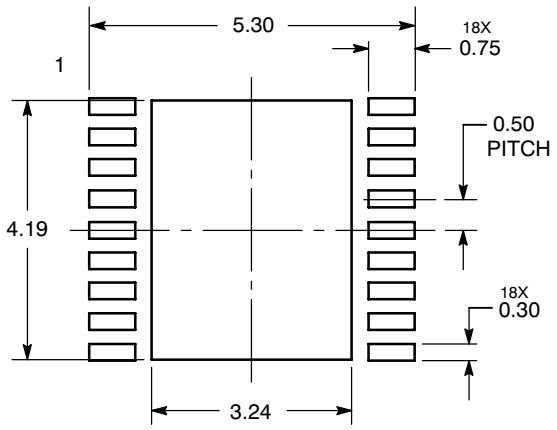


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	---
L	0.45	0.65



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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NUD4330/D