National Semiconductor

June 2007

LP5521
Programmable Three Channel LED Driver

General Description

The LP5521 is a three channel LED driver designed to produce variety of lighting effects for mobile devices. High efficiency charge pump enables LED driving over full Li-Ion battery voltage range. The device has a program memory for creating variety of lighting sequences. When program memory has been loaded, LP5521 can operate independently without processor control.

LP5521 maintains excellent efficiency over a wide operating range by automatically selecting proper charge pump gain based on LED forward voltage requirements. LP5521 is able to automatically enter power-save mode, when LED outputs are not active and thus lowering current consumption.

Three independent LED channels have accurate programmable current sources and PWM control. Each channel has program memory for creating desired lighting sequences with PWM control.

LP5521 has a flexible digital interface. Trigger I/O and 32 kHz clock input allow synchronization between multiple devices. Interrupt output can be used to notify processor, when LED sequence has ended. LP5521 has four pin selectable I²C addresses. This allows connecting up to four parallel devices in one I²C bus. GPO and INT pins can be used as a digital control pin for other devices.

LP5521 requires only four small and low cost ceramic capacitors.

LP5521 is available in tiny 2.1x1.7x0.6 mm microSMD-20 package and in 4.0x5.0x0.8 mm bumped LLP-24 package.

Comprehensive application tools are available, including command compiler for easy LED sequence programming.

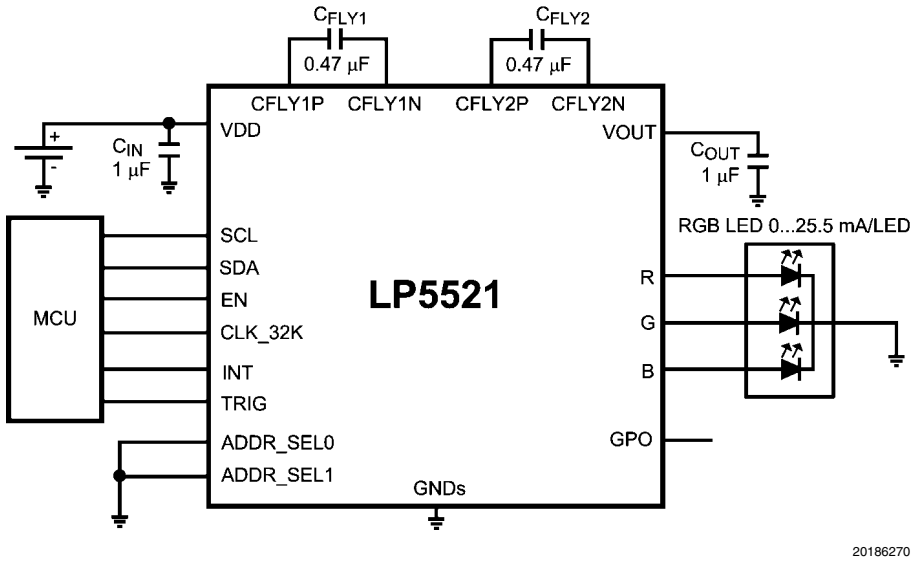
Features

- Adaptive charge pump with 1x and 1.5x gain provides up to 95% LED drive efficiency
- Charge pump with soft start and overcurrent/short circuit protection
- Low input ripple and EMI
- Very small solution size, no inductor or resistors required
- 200 nA typical shutdown current
- Automatic power save mode
- I²C compatible interface
- Independently programmable constant current outputs with 8-bit current setting and 8-bit PWM control
- Typical LED output saturation voltage 50 mV and current matching 1%
- Three program execution engines with flexible instruction set
- Autonomous operation without external control
- Large SRAM program memory
- Two general purpose digital outputs
- microSMD-20 package, 0.4 mm pitch
- Bumped LLP-24 package, 0.5 mm pitch

Applications

- Fun / indicator lights
- LCD sub-display backlighting
- Keypad RGB backlighting and phone cosmetics
- Vibra, speakers, waveform generator

Typical Application



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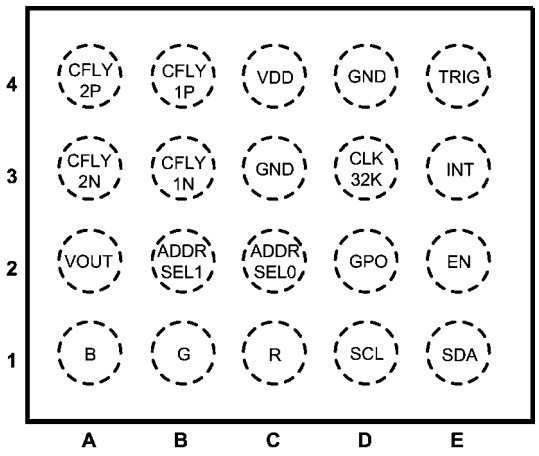
Connection Diagrams and Package Mark Information

Thin microSMD-20 Package (2.1 x 1.7 x 0.6 mm, 0.4 mm pitch)
NS Package Number TMD20ECA



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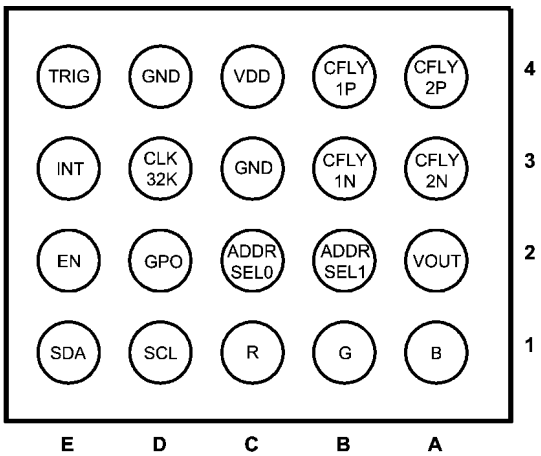
Top View



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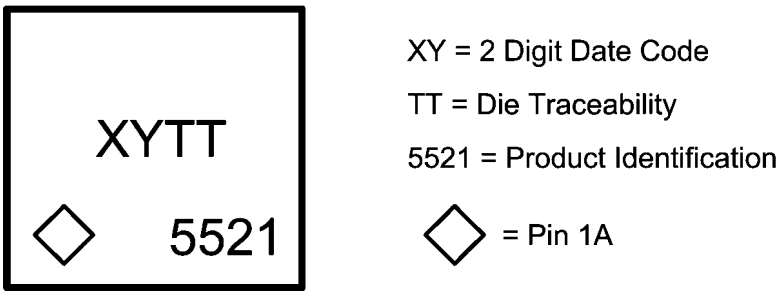
Bottom View

Package Mark



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Package Mark - Top View

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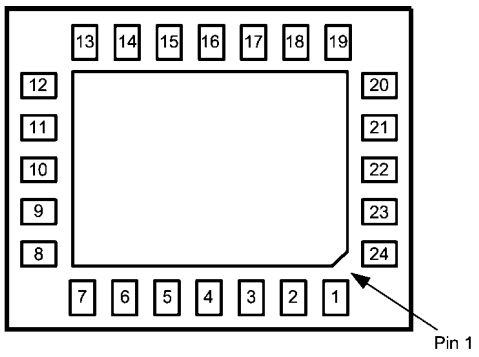
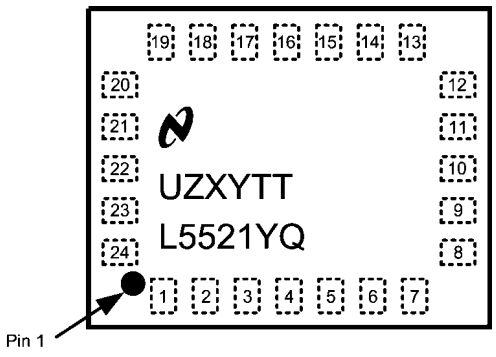
Connection Diagrams and Package Mark Information

Bumped LLP-24 Package (5 x 4 x 0.8 mm, 0.5 mm pitch)
NS Package Number YQA24A



Bottom View



Package Mark - Top View

U = Fab
Z = Assembly
XY = 2 Digit Date Code
TT = Die Traceability
L5521YQ = Product Identification

Ordering Information

Order Number	Package	Package Marking	Supplied As	Spec/Flow
LP5521TM	µSMD	5521	250 units, Tape-and-Reel	NoPb
LP5521TM X	µSMD	5521	3000 units, Tape-and-Reel	NoPb
LP5521YQ	bumped LLP	L5521YQ	1000 units, Tape-and-Reel	NoPb
LP5521YQ X	bumped LLP	L5521YQ	4500 units, Tape-and-Reel	NoPb

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Pin Descriptions LP5521TM

Pin #	Name	Type	Description
1A	B	A	Current source output
1B	G	A	Current source output
1C	R	A	Current source output
1D	SCL	I	I²C Serial interface clock input
1E	SDA	I/OD	I²C Serial interface data input/output
2A	VOUT	A	Charge pump output
2B	ADDR_SEL1	I	I²C address select input
2C	ADDR_SEL0	I	I²C address select input
2D	GPO	O	General purpose output
2E	EN	I	Chip enable
3A	CFLY2N	A	Negative terminal of charge pump fly capacitor 2
3B	CFLY1N	A	Negative terminal of charge pump fly capacitor 1
3C	GND	G	Ground
3D	CLK_32K	I	32 kHz clock input
3E	INT	OD/O	Interrupt output / General Purpose Output
4A	CFLY2P	A	Positive terminal of charge pump fly capacitor 2
4B	CFLY1P	A	Positive terminal of charge pump fly capacitor 1
4C	VDD	P	Power supply pin
4D	GND	G	Ground
4E	TRIG	I/OD	Trigger input/output

A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, I/O: Input/Output Pin, O: Output Pin, OD: Open Drain Pin

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Pin Descriptions LP5521YQ

Pin #	Name	Type	Description
1	CFLY2P	A	Positive terminal of charge pump fly capacitor 2
2	CFLY1P	A	Positive terminal of charge pump fly capacitor 1
3	VDD	P	Power supply pin
4	GND	G	Ground
5	CLK_32K	I	32 kHz clock input
6	INT	OD/O	Interrupt output / General purpose output
7	TRIG	I/OD	Trigger input/output
8		N/C	
9		N/C	
10		N/C	
11		N/C	
12		N/C	
13	SDA	I/OD	I²C Serial interface data input/output
14	EN	I	Chip enable
15	SCL	I	I²C Serial interface clock input
16	GPO	O	General purpose output
17	R	A	Current source output
18	G	A	Current source output
19	B	A	Current source output
20	ADDR_SEL0	I	I²C address select input
21	ADDR_SEL1	I	I²C address select input
22	VOUT	A	Charge pump output
23	CFLY2N	A	Negative terminal of charge pump fly capacitor 2
24	CFLY1N	A	Negative terminal of charge pump fly capacitor 1

A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, I/O: Input/Output Pin, O: Output Pin, OD: Open Drain Pin, N/C: Not Connected

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Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

$V(V_{DD}$, V_{OUT}, R, G, B)	-0.3V to +6.0V
Voltage on Logic Pins	-0.3V to V_{DD} +0.3V with 6.0V max
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{J-MAX})	125°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering)	(Note 4)
ESD Rating (Note 5)	
Human Body Model:	2 kV
Machine Model:	200V

Operating Ratings (Notes 1, 2)

V_{DD}	2.7 to 5.5V
Recommended Charge Pump Load Current I_{OUT}	0 to 100 mA
Junction Temperature (T_J) Range	-30°C to +125°C
Ambient Temperature (T_A) Range (Note 6)	-30°C to +85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), TMD20 Package (Note 7)	50 - 90°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}), YQA24A Package (Note 7)	37 - 90°C/W

Electrical Characteristics (Notes 2, 8)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (-30°C < T_A < +85°C). Unless otherwise noted, specifications apply to the LP5521 Block Diagram with: 2.7V ≤ V_{DD} ≤ 5.5V, C_{OUT}= C_{IN} = 1 µF, C_{FLY1} = C_{FLY2} = 0.47 µF. (Note 9).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{VDD}	Standby supply current	EN = 0 (pin), CHIP_EN = 0 (bit), external 32 kHz clock running or not running		0.2	**2**	µA
		EN = 1 (pin), CHIP_EN = 0 (bit), external 32 kHz clock not running		1.0		µA
		EN = 1 (pin), CHIP_EN = 0 (bit), external 32 kHz clock running		1.4		µA
	Normal mode supply current	Charge pump and LED drivers disabled		0.25		mA
		Charge pump in 1x mode, no load, LED drivers disabled		0.70		mA
		Charge pump in 1.5x mode, no load, LED drivers disabled		1.5		mA
		Charge pump in 1x mode, no load, LED drivers enabled		1.2		mA
	Powersave mode supply current	External 32 kHz clock running		10		µA
		Internal oscillator running		0.25		mA
f_{OSC}	Internal oscillator frequency accuracy		-4 **-7**		4 **7**	%

Charge Pump Electrical Characteristics (Note 10)

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{OUT}	Charge pump output resistance	Gain = 1.5x		3.5		Ω
		Gain = 1x		1		Ω
f_{SW}	Switching frequency		 **-7**	1.25	 **7**	MHz %
I_{GND}	Ground current	Gain = 1.5x		1.2		mA
		Gain = 1x		0.5		mA
t_{ON}	V_{OUT} turn-on time from charge pump off to 1.5x mode	V_{DD} = 3.6V, CHIP_EN = H I_{OUT} = 60 mA		100		µs
V_{OUT}	Charge pump output voltage	V_{DD} = 3.6V, no load, Gain = 1.5x		4.55		V

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LED Driver Electrical Characteristics (R, G, B Outputs)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LEAKAGE}$	R, G, B pin leakage current			0.1	**1**	µA
I_{MAX}	Maximum Source Current	Outputs R, G, B		25.5		mA
I_{OUT}	Accuracy of output current	Output current set to 17.5 mA, V_{DD} = 3.6V	-4 **-5**		4 **5**	%
I_{MATCH}	Matching (Note 11)	I_{OUT} = 17.5 mA, V_{DD} = 3.6V		1	2	%
f_{LED}	LED PWM switching frequency	PWM_HF = 1 Frequency defined by internal oscillator		558		Hz
		PWM_HF = 0 Frequency defined by 32 kHz clock (internal or external)		256		Hz
V_{SAT}	Saturation voltage (Note 12)	I_{OUT} set to 17.5 mA		50	100	mV

Logic Interface Characteristics

(V(EN) = 1.65V...V_{DD} unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOGIC INPUT EN						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**1.2**			V
I_I	Logic Input Current		**–1.0**		**1.0**	µA
t_{DELAY}	Input delay			2		µs
LOGIC INPUT SCL, SDA, TRIG, CLK_32K						
V_{IL}	Input Low Level				**0.2xV(EN)**	V
V_{IH}	Input High Level		**0.8xV(EN)**			V
I_I	Input Current		**-1.0**		**1.0**	µA
f_{CLK_32K}	Clock frequency			32		kHz
f_{SCL}	Clock frequency				**400**	kHz
LOGIC OUTPUT SDA, TRIG, INT						
V_{OL}	Output Low Level	I_{OUT} = 3 mA (pull-up current)		0.3	**0.5**	V
I_L	Output Leakage Current				**1.0**	µA
LOGIC INPUT ADDR_SEL0, ADDR_SEL1						
V_{IL}	Input Low Level				**0.2xV_{DD}**	V
V_{IH}	Input High Level		**0.8xV_{DD}**			V
I_I	Input Current		**–1.0**		**1.0**	µA
LOGIC OUTPUT GPO, INT (in GPO state)						
V_{OL}	Output Low Level	I_{OUT} = 3 mA		0.3	**0.5**	V
V_{OH}	Output High Level	I_{OUT} = -2 mA	**V_{DD} - 0.5**	V_{DD} - 0.3		V
I_L	Output leakage current				**1.0**	µA

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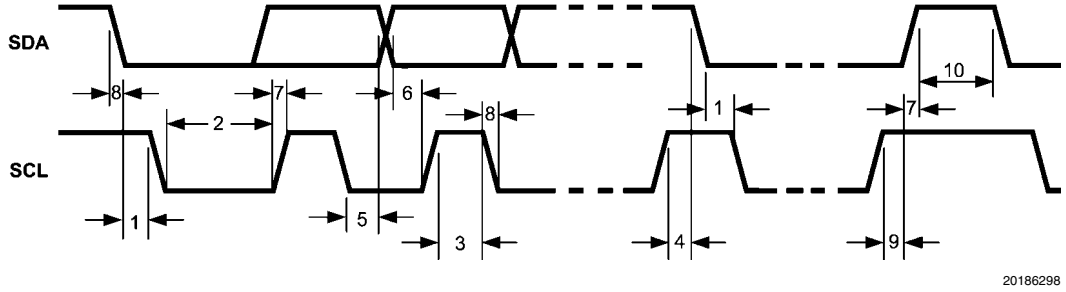
I²C Timing Parameters (SDA, SCL) (Note 13)

Symbol	Parameter	Limit		Units
		Min	Max	
f_{SCL}	Clock Frequency		400	kHz
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time	50		ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF



Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pins.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).

Note 4: For detailed soldering specifications and information, please refer to National Semiconductor Application Note AN1112 : Micro SMD Wafer Level Chip Scale Package or AN1187 : Leadless Leadframe Package (LLP).

Note 5: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Note 6: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 7: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Note 8: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 9: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Note 10: Input, output, and fly capacitors should be of the type X5R or X7R low ESR ceramic capacitor.

Note 11: Matching is the maximum difference from the average of the three output's currents.

Note 12: Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at V_{OUT} - 1V.

Note 13: Guaranteed by design.

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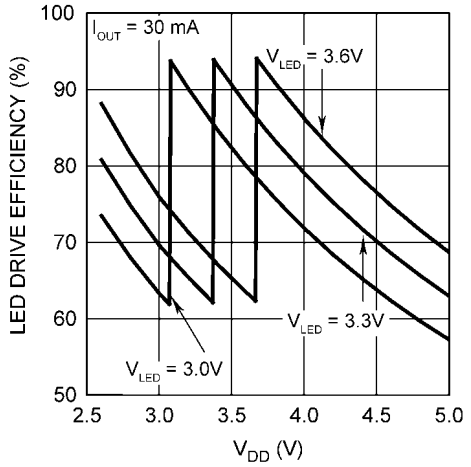
Typical Performance Characteristics

Unless otherwise specified: V_{DD} = 3.6V

LED Drive Efficiency vs. Input Voltage Automatic Gain Change



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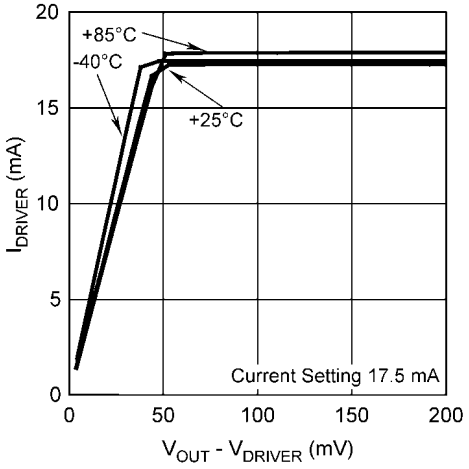
LED Current vs. Output Pin Headroom Voltage



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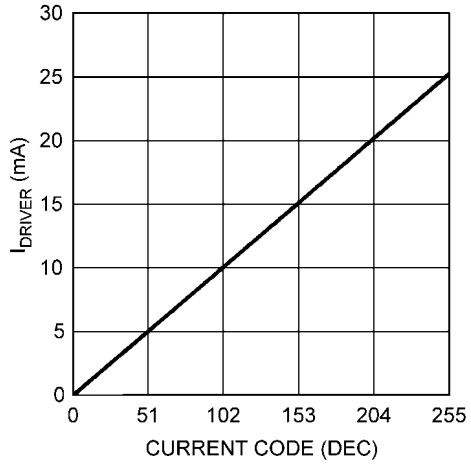
LED Current vs. Current Register Code



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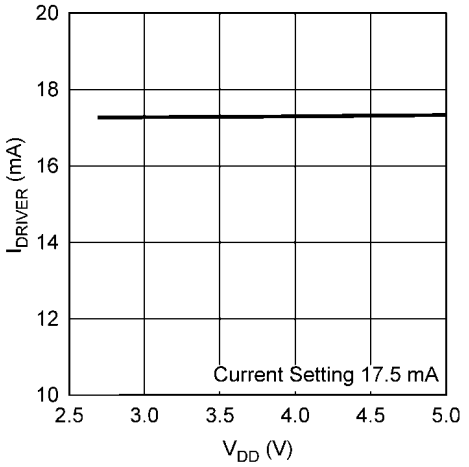
LED Current vs. Supply Voltage



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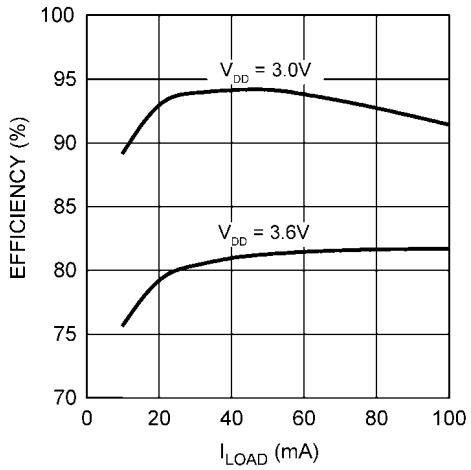
Charge Pump Efficiency vs. Load Current



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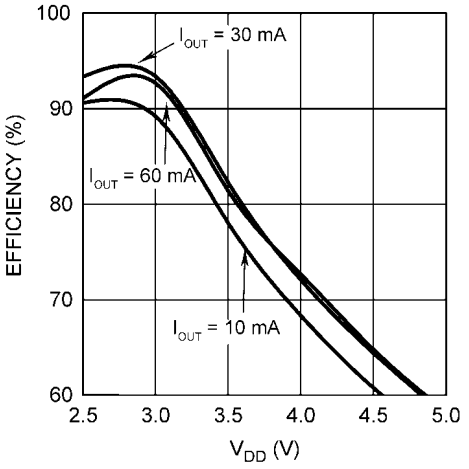
Charge Pump Efficiency vs. Input Voltage 1.5x Mode



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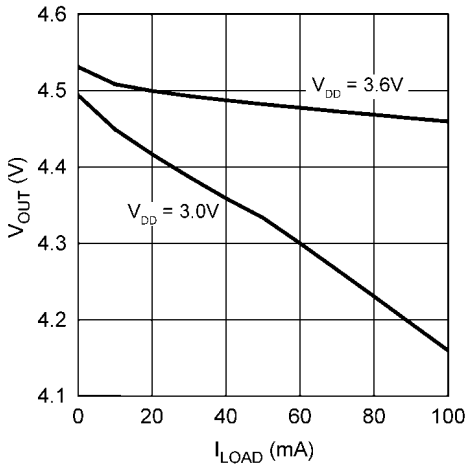
Charge Pump Output Voltage vs. Load Current



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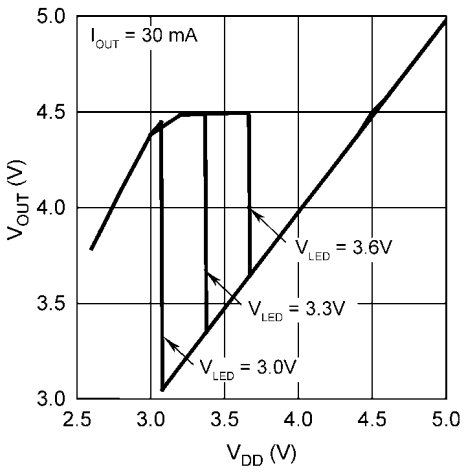
Charge Pump Output Voltage vs. Input Voltage Automatic Gain Change from 1x to 1.5x



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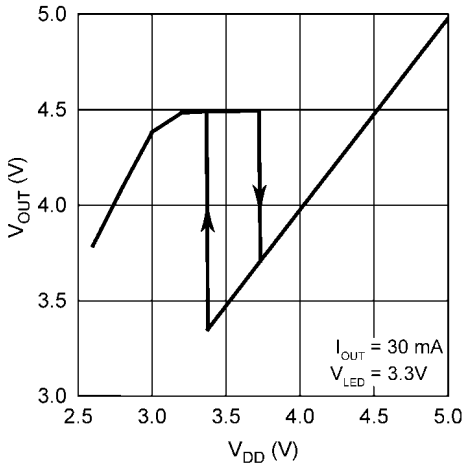
Charge Pump Automatic Gain Change Hysteresis



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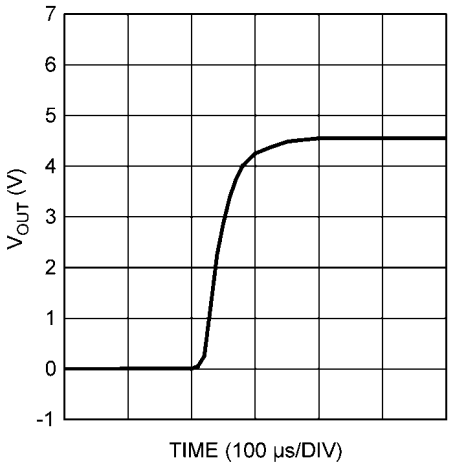
Charge Pump Startup in 1.5x Mode No Load



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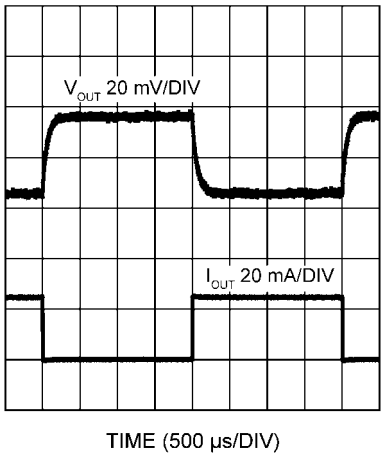
Charge Pump Load Transient Response in 1.5x Mode (0 to 25.5 mA)



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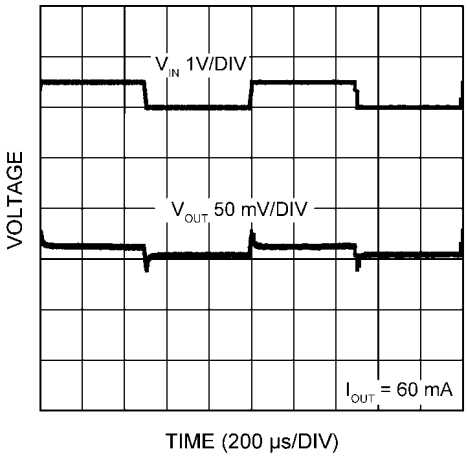
Charge Pump Line Transient Response 1.5x Mode (V_{IN} 3.5V to 4.0V)



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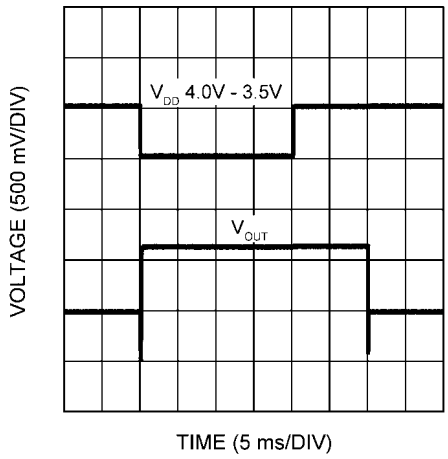
Charge Pump Automatic Gain Change (LED V_F = 3.6V)



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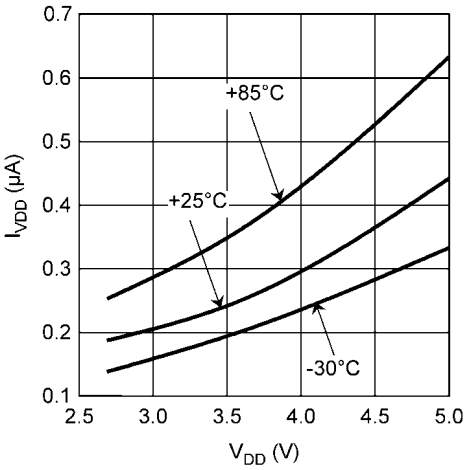
Standby Current vs. Input Voltage



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For full LP5521 datasheet please contact nearest National Semiconductor sales office.

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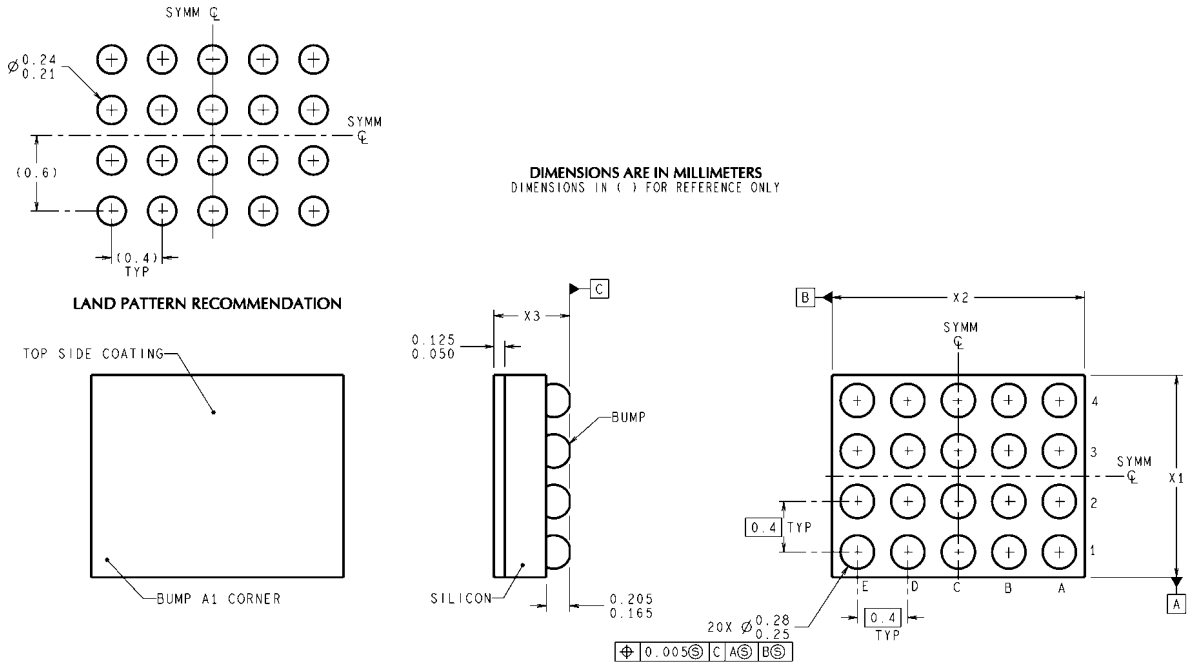
Physical Dimensions inches (millimeters) unless otherwise noted



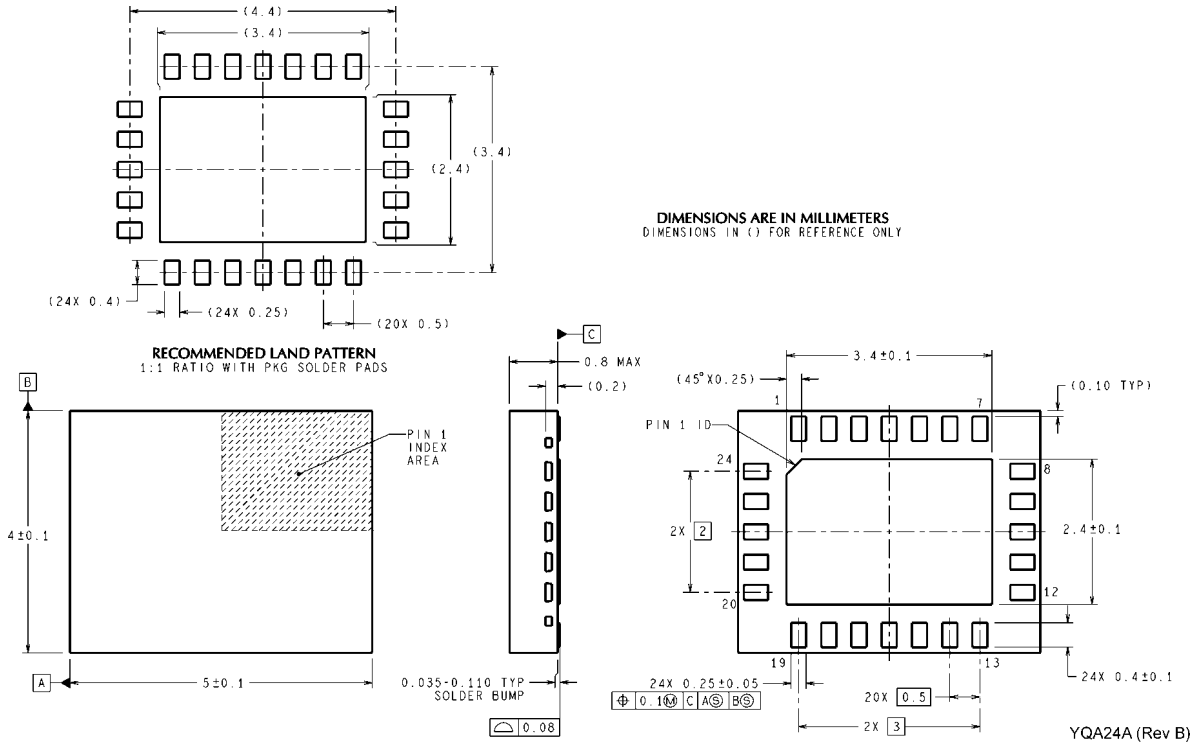
The dimension for X1 ,X2 and X3 are as given:

X1=1.717 mm ± 0.03 mm

X2=2.066 mm ± 0.03 mm

X3=0.600 mm ± 0.075 mm

TMD20ECA: Thin microSMD-20, Small Bump



YQA24A: Bumped LLP-24

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Notes

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