National
Semiconductor

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# LM2702
# TFT Panel Module

## General Description

The LM2702 is a compact bias solution for TFT displays. It has a current mode PWM step-up DC/DC converter with a 2A, 0.2Ω internal switch. Capable of generating 8V at 170mA from a Lithium Ion battery, the LM2702 is ideal for generating bias voltages for large screen LCD panels. The LM2702 operates at a switching frequency of 600kHz allowing for easy filtering and low noise. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. The LM2702 uses a patented internal circuitry to limit startup inrush current of the boost switching regulator without the use of an external softstart capacitor. An external softstart pin enables the user to tailor the softstart to a specific application. The LM2702 has an internal controllable PMOS switch used for controlling the row driver voltages. The switch can be controlled externally with a control pin and delay time. The LM2702 contains a Vcom amplifier and a Gamma buffer capable of supplying 50mA source and sink. The TSSOP-16 package ensures a low profile overall solution.

## Features

- 2A, 0.2Ω, internal power switch
- $V_{IN}$ operating range: 2.2V to 12V
- 600kHz switching frequency step-up DC/DC converter
- Inrush current limiting circuitry
- External softstart override
- Internal 7.3Ω PMOS switch
- PMOS switch control pin
- PMOS switch delay pin
- Vcom amplifier
- Gamma buffer
- 16 pin TSSOP package

## Applications

- LCD Bias Supplies

## Typical Application Circuit



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# Connection Diagram

**Top View**

```
        1 ─── Vcom+          GMA+ ─── 16

        2 ─── Vcom-          GMA  ─── 15

        3 ─── Vcom           AV_IN ─── 14

        4 ─── Delay          SWC  ─── 13

        5 ─── Css            SWO  ─── 12

        6 ─── V_C            SWI  ─── 11

        7 ─── FB             V_IN ─── 10

        8 ─── GND            SW   ─── 9
```

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**TSSOP 16 package**
**$T_{JMAX}$ = 125˚C, $\theta_{JA}$ = 120˚C/W** (Note 1)

# Pin Description

| Pin | Name | Function |
|-----|------|----------|
| 1 | Vcom+ | Vcom Amplifier positive input. |
| 2 | Vcom− | Vcom Amplifier negative input. |
| 3 | Vcom | Vcom Amplifier output. |
| 4 | Delay | Switch delay. |
| 5 | Css | Soft start pin. |
| 6 | $V_C$ | Boost Compensation Network Connection. |
| 7 | FB | Output Voltage Feedback input. |
| 8 | GND | Ground. |
| 9 | SW | NMOS power switch input. |
| 10 | $V_{IN}$ | Main power input, step-up and switch circuitry. |
| 11 | SWI | PMOS switch input. |
| 12 | SWO | PMOS switch output. |
| 13 | SWC | PMOS switch control pin. |
| 14 | $AV_{IN}$ | Analog power input (buffers). |
| 15 | GMA | Gamma buffer output. |
| 16 | GMA+ | Gamma buffer input. |

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## Pin Functions

**Vcom+(Pin 1):** Positive input terminal of Vcom amplifier.

**Vcom–(Pin 2):** Negative input terminal of Vcom amplifier.

**Vcom(Pin 3):** Output terminal of Vcom amplifier.

**Delay(Pin 4):** PMOS switch delay control pin. See *Operation* section for setting the delay time.

The delay time begins when the output voltage of the DC/DC switching regulator reaches 85% of its true output voltage. This corresponds to a FB voltage of about 1.1V. The PMOS switch is controlled with both the delay time and the switch control pin, SWC. If no Cdelay capacitor is used, the PMOS switch is controlled solely with the SWC pin.

**Css(Pin 5):** Softstart pin. Connect capacitor to Css pin and AGND plane to slowly ramp inductor current on startup. See *Operation* section for setting the softstart time.

**$V_C$(Pin 6):** Compensation Network for Boost switching regulator. Connect resistor/capacitor network between $V_C$ pin and AGND for boost switching regulator AC compensation.

**FB(Pin 7):** Feedback pin. Set the output voltage by selecting values of R1 and R2 using:

$$R1 = R2 \left( \frac{V_{OUT}}{1.265V} - 1 \right)$$

Connect the ground of the feedback network to the AGND plane, which should be tied directly to the GND pin.

**GND(Pin 8):** Ground connect for LM2702. Connect all sensitive circuitry, ie. feedback resistors, softstart capacitor, de-lay capacitor, and compensation network to a dedicated AGND plane which connects directly to this pin. Connect all power ground components to a PGND plane which should also connect directly to this pin. Please see Layout Considerations under the Operation section for more details on layout suggestions.

**SW(Pin 9):** This is the drain of the internal NMOS power switch. Minimize the metal trace area connected to this pin to minimize EMI.

**$V_{IN}$(Pin 10):** Input Supply Pin. Bypass this pin with a capacitor as close to the device as possible. The capacitor should connect between $V_{IN}$ and GND.

**SWI(Pin 11):** PMOS switch input. Source connection of PMOS device.

**SWO(Pin 12):** PMOS switch output. Drain connection of PMOS device.

**SWC(Pin13):** PMOS switch control pin. This pin creates an AND function with the delay time after the output of the switching regulator has reached 85% of its nominal value. To ensure the PMOS switch is in the correct state, apply a voltage above 1.5V to this pin to turn on the PMOS switch and apply a voltage below 0.7V to turn off the PMOS switch.

**$AV_{IN}$(Pin 14):** Supply pin for the Vcom opamp and the Gamma buffer. Bypass this pin with a capacitor as close to the device as possible, about 100nF. The capacitor should connect between $AV_{IN}$ and PGND.
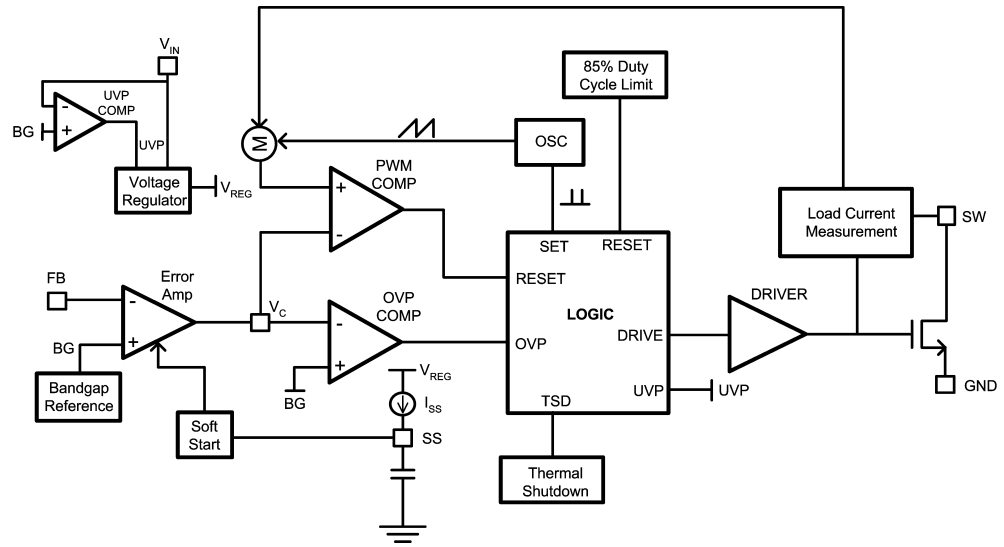
**GMA(Pin 15):** Gamma Buffer output pin.
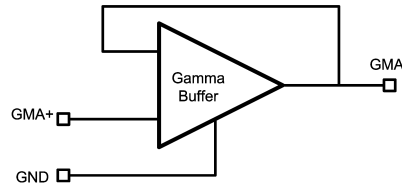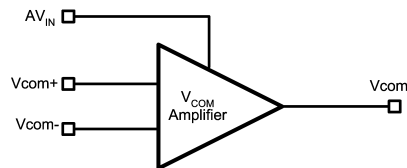
**GMA+(Pin 16):** Gamma Buffer input pin.

## Ordering Information

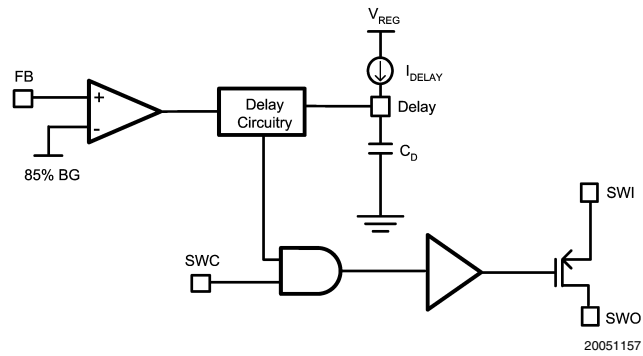| Order Number | Package Type | NSC Package Drawing | Supplied As |
| --- | --- | --- | --- |
| LM2702MT-ADJ | TSSOP-16 | MTC16 | 73 Units, Rail |
| LM2702MTX-ADJ | TSSOP-16 | MTC16 | 2500 Units, Tape and Reel |

# Block Diagrams



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# Absolute Maximum Ratings (Note 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| $V_{IN}$ | -0.3V to 12V |
| SW Voltage | -0.3V to 18V |
| FB Voltage | -0.3V to 7V |
| $V_C$ Voltage | 0.96V to 1.56V |
| Css Voltage | -0.3V to 1.2V |
| SWC Voltage | -0.3V to 12V |
| Supply Voltage, $AV_{IN}$ | -0.3V to 12V |
| Amplifier/Buffer Input/Output Voltage | Rail-to-Rail |
| Delay | GND to 1.3V |
| SWI | -0.3V to 30V |
| SWO | -0.3V to 30V |

ESD Ratings
(Notes 3, 4)

| | |
|---|---|
| Human Body Model | 2kV |
| Machine Model | 200V |

# Operating Conditions

| | |
|---|---|
| Operating Temperature | −40°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Supply Voltage, $V_{IN}$ | 2.2V to 12V |
| SW Voltage | 17.5V |
| Supply $AV_{IN}$ | 4V to 12V |
| SWI | 2.2V to 30V |

# Electrical Characteristics

Specifications in standard type face are for $T_J$ = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J$ = −40°C to +125°C). Unless otherwise specified, $V_{IN}$ =2.2V and $AV_{IN}$ = 8V, $R_{COM}$ = $R_{GAMMA}$ = 50Ω, $C_{COM}$ = $C_{GAMMA}$ = 1nF.

**Switching Regulator**

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 6) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| $I_Q$ | Quiescent Current | Not Switching, FB = 2V | | 1.6 | **2.3** | mA |
| | | Switching, switch open, FB = 0.1V | | 2.6 | **5.2** | |
| $V_{FB}$ | Feedback Voltage | | **1.239** | 1.265 | **1.291** | V |
| %$V_{FB}$/$\Delta V_{IN}$ | Feedback Voltage Line Regulation | | | 0.01 | **0.1** | %/V |
| $I_{CL}$ | Switch Current Limit (Note 7) | $V_{IN}$ = 2.7V | **1.4** | 2 | **2.6** | A |
| $R_{DSON}$ | Switch $R_{DSON}$ (Note 8) | $V_{IN}$ = 2.7V | | 200 | | mΩ |
| $I_B$ | FB Pin Bias Current (Note 9) | | | 60 | **500** | nA |
| $V_{IN}$ | Input Voltage Range | | **2.2** | | **12** | V |
| $I_{SS}$ | Soft Start Current | | **5** | 12 | **15** | µA |
| $T_{SS}$ | Internal Soft Start Ramp Time | | | 7 | **10** | mS |
| $g_m$ | Error Amp Transconductance | $\Delta I$ = 5µA | **40** | 135 | **290** | µmho |
| $A_V$ | Error Amp Voltage Gain | | | 135 | | V/V |
| $D_{MAX}$ | Maximum Duty Cycle | | **78** | 85 | | % |
| $f_S$ | Switching Frequency | | **480** | 600 | **720** | kHz |
| $I_L$ | Switch Leakage Current | $V_{SW}$ = 18V | | 0.1 | **20** | µA |
| UVP | On Threshold | | **1.79** | 1.92 | **2.05** | V |
| | Off Threshold | | **1.69** | 1.82 | **1.95** | V |
| | Hysteresis | | | 100 | | mV |

# Electrical Characteristics

Specifications in standard type face are for $T_J$ = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J$ = −40°C to +125°C). Unless otherwise specified, $V_{IN}$ =2.2V and $AV_{IN}$ = 8V, $R_{COM}$ = $R_{GAMMA}$ = 50Ω, $C_{COM}$ = $C_{GAMMA}$ = 1nF.

**Vcom Amplifier**

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 6) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (Note 10) | $V_{CM}$ = 1V | | 3.5 | 10 | mV |
| | | $V_{CM}$ = 7.5V | | 3 | 10 | |
| $I_B$ | Input Bias Current | $V_{CM}$ = 1V | | 65 | 200 | nA |
| | | $V_{CM}$ = 7.5V | | 190 | 300 | |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = 1V | | 45 | 130 | nA |
| | | $V_{CM}$ = 7.5V | | 5 | 110 | |
| CMVR | Input Common-mode Voltage Range | | **0** | | **8** | V |
| $V_{OUT}$ Swing | | $R_L$=10k, Vo min. | | 0.003 | **.02** | V |
| | | $R_L$=10k, Vo max. | **7.94** | 7.98 | | |
| | | $R_L$=2k, Vo min. | | 0.003 | **.02** | |
| | | $R_L$=2k, Vo max. | **7.9** | 7.95 | | |
| $A_{VOL}$ | Large Signal Voltage Gain | No Load, Vo = 2V to 7V | **74.8** | 87.6 | | dB |
| | | $R_L$=10 kΩ, Vo = 2V to 7V | **66.8** | 75.1 | | |
| | | $R_L$=2 kΩ, Vo = 2V to 7V | | 55.8 | | |
| $AV_{IN}$ | Supply Voltage | | **4** | | **12** | V |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ stepped from 0V to 1.1V | **72** | 91.7 | | dB |
| | | $V_{CM}$ stepped from 3V to 8V | **80** | 105 | | |
| | | $V_{CM}$ stepped from 0V to 8V | **57** | 80.7 | | |
| PSRR | Power Supply Rejection Ratio | $V_{CM}$ = 0.5V, $AV_{IN}$ = 4 to 12V | **70** | 77 | | dB |
| Is+ | Supply Current (Amplifier + Buffer) | Vo = $AV_{IN}$/2, No Load | | 2.2 | **4** | mA |
| $I_{SC}$ | Output Short Circuit Current | Source | **40** | 50 | **70** | mA |
| | | Sink | **40** | 50 | **60** | |

# Electrical Characteristics

Specifications in standard type face are for $T_J$ = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J$ = −40°C to +125°C). Unless otherwise specified, $V_{IN}$ =2.2V and $AV_{IN}$ = 8V, $R_{COM}$ = $R_{GAMMA}$ = 50Ω, $C_{COM}$ = $C_{GAMMA}$ = 1nF.

**Gamma Buffer**

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 6) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage (Note 10) | | | 1 | 10 | mV |
| $I_B$ | Input Bias Current | | | 170 | 300 | nA |
| $V_{GR}$ | Gamma Input Voltage Range | | **0** | | **8** | V |
| $V_{OUT}$ Swing | | $R_L$=10k, Vo min. | | 0.05 | **0.075** | V |
| | | $R_L$=10k, Vo max. | **7.9** | 7.94 | | |
| | | $R_L$=2k, Vo min. | | 0.05 | **0.075** | |
| | | $R_L$=2k, Vo max. | **7.865** | 7.9 | | |
| $A_{VCL}$ | Voltage Gain | No Load, Vo = 2V to 7V | **0.995** | 0.999 | | V/V |
| | | $R_L$=10 kΩ, Vo = 2V to 7V | **0.995** | 0.999 | | |
| | | $R_L$=2 kΩ, Vo = 2V to 7V | **0.993** | 0.998 | | |
| PSRR | Power Supply Rejection Ratio | $AV_{IN}$ = 4 to 12V | **70** | 77 | | dB |

## Electrical Characteristics (Continued)

Specifications in standard type face are for $T_J$ = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J$ = −40°C to +125°C). Unless otherwise specified, $V_{IN}$ =2.2V and $AV_{IN}$ = 8V, $R_{COM}$ = $R_{GAMMA}$ = 50Ω, $C_{COM}$ = $C_{GAMMA}$ = 1nF.

**Gamma Buffer**

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 6) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| $AV_{IN}$ | Supply Voltage | | **4** | | **12** | V |
| Is+ | Supply Current (Amplifier + Buffer) | Vo = $AV_{IN}$/2, No Load | | 2.2 | **4** | mA |
| $I_{SC}$ | Output Short Circuit Current | Source | **50** | 66 | **75** | mA |
| | | Sink | **40** | 56 | **65** | mA |

## Electrical Characteristics

Specifications in standard type face are for $T_J$ = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J$ = −40°C to +125°C). Unless otherwise specified, $V_{IN}$ =2.2V and $AV_{IN}$ = 8V, $R_{COM}$ = $R_{GAMMA}$ = 50Ω, $C_{COM}$ = $C_{GAMMA}$ = 1nF.

**PMOS Switch Logic Control**

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 6) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| $I_{DELAY}$ | Delay Current | | **5.1** | 5.7 | **6.1** | µA |
| $R_{DSON}$ | PMOS Switch ON Resistance | | | 7.3 | **20** | Ω |
| $I_{SWO}$ | PMOS Switch Current | Switch ON | | 20 | | mA |
| $I_{SWI}$ | PMOS Switch Input Current | SWC = 0V, SWO Open, SWI = 30V | | 32 | | µA |
| | | SWC = 1.7V, SWO Open, SWI = 30V | | 118 | | µA |
| $V_{SWC}$ | Switch ON | | **1.5** | 1.1 | | V |
| | Switch OFF | | | 1.1 | **0.7** | V |

**Note 1:** The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$(MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. See the Electrical Characteristics table for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D$ (MAX) = $(T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

**Note 2:** Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

**Note 3:** The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

**Note 4:** Vcom pin is rated for 1.5kV Human Body Model and 150V Machine Model.

**Note 5:** All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested or guaranteed through statistical analysis. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

**Note 6:** Typical numbers are at 25°C and represent the most likely norm.

**Note 7:** Duty cycle affects current limit due to ramp generator. Current limit is at 0% duty cycle and will decrease with higher duty cycles. See *Typical Performance Characteristics* for a graph of Power Switch Current Limit vs. $V_{IN}$ and Power Switch Current Limit vs. Temp.
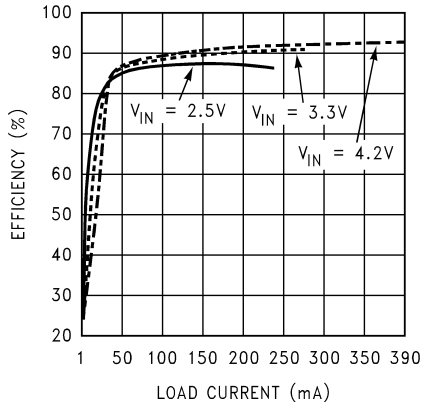
**Note 8:** See the graph titled "$R_{DSON}$ vs. $V_{IN}$" for a more accurate value of the power switch $R_{DSON}$.

**Note 9:** Bias current flows into FB pin.

**Note 10:** Refer to the graphs titled "Input Offset Voltage vs. Common Mode Voltage".
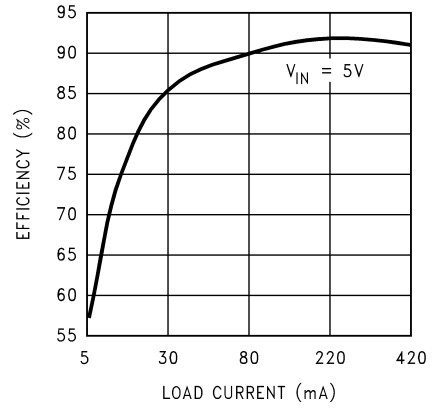
# Typical Performance Characteristics

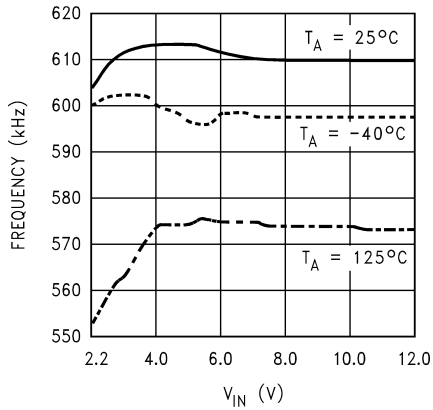**Efficiency vs. Load Current**
**($V_{OUT}$ = 8V)**



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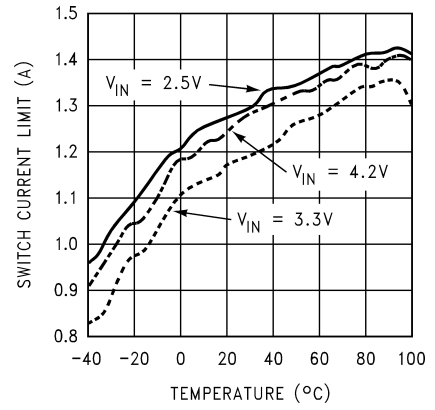**Efficiency vs. Load Current**
**($V_{OUT}$ = 10V)**



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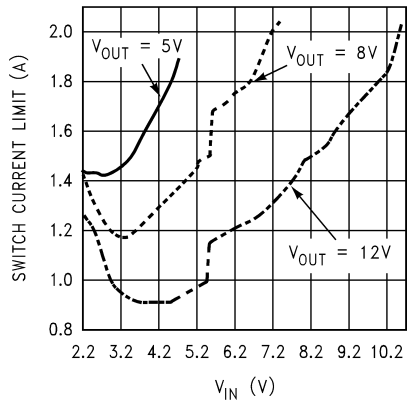
**Frequency vs. $V_{IN}$**
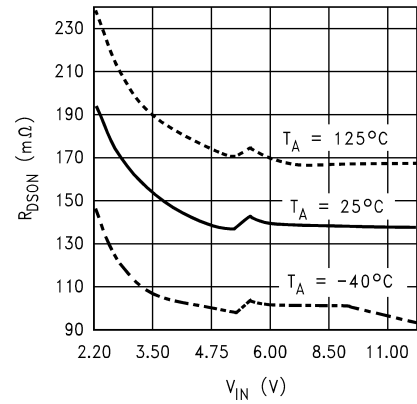


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**Power Switch Current Limit vs. Temperature**
**($V_{OUT}$ = 8V)**



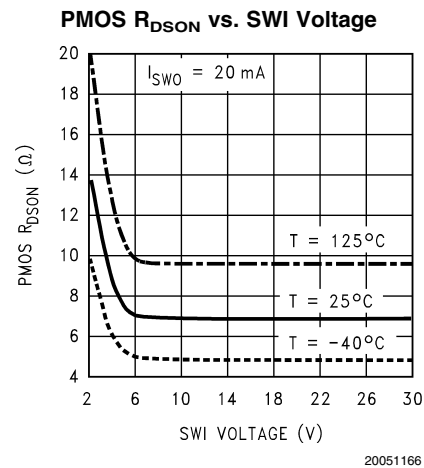20051120

**Power Switch Current Limit vs. $V_{IN}$**



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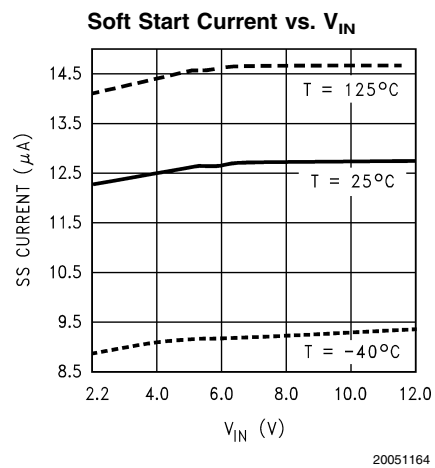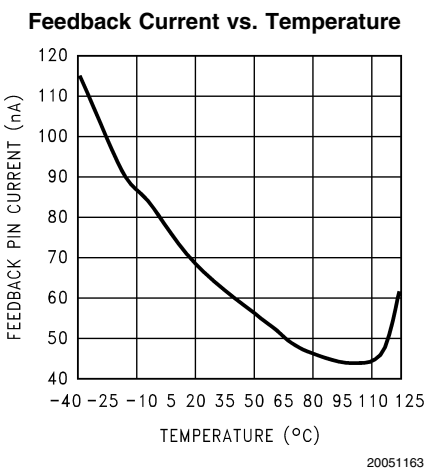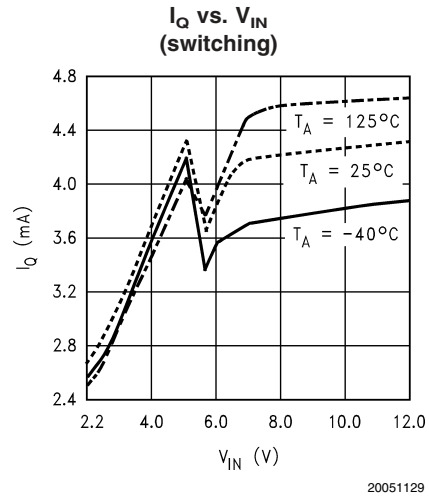
**$R_{DSON}$ vs. $V_{IN}$**
**($I_{SW}$ = 1A)**



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# Typical Performance Characteristics (Continued)

### $I_Q$ vs. $V_{IN}$ (not switching)



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### $I_Q$ vs. $V_{IN}$ (switching)



20051129

### Feedback Current vs. Temperature



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### Soft Start Current vs. $V_{IN}$



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### Delay Current vs. $V_{IN}$



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### PMOS $R_{DSON}$ vs. SWI Voltage
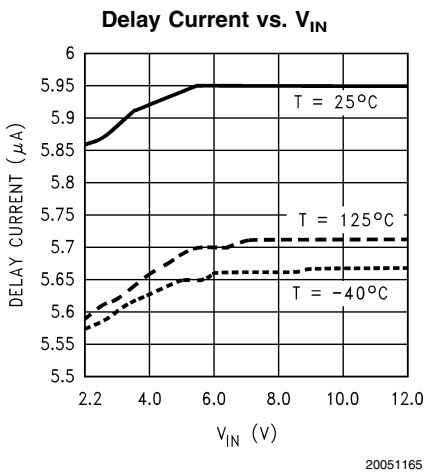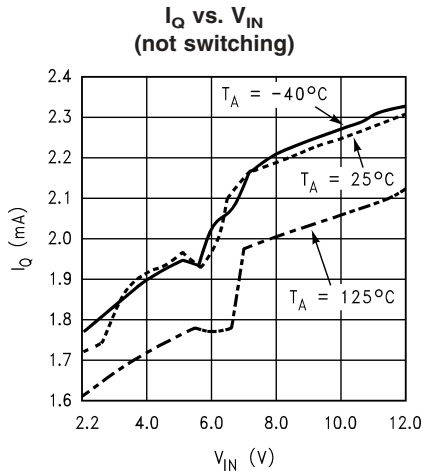


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# Typical Performance Characteristics (Continued)

**SWI Current vs. SWI Voltage
(PMOS ON)**
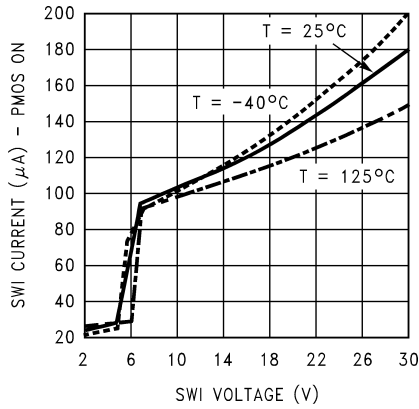


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**SWI Current vs. SWI Voltage
(PMOS OFF)**
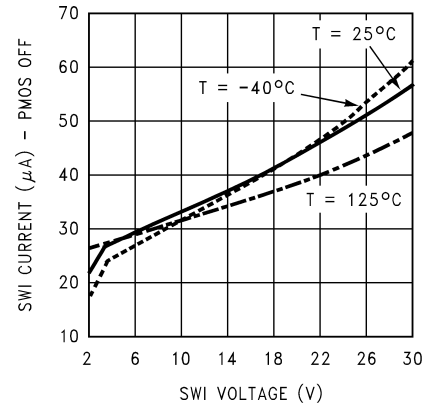


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**Load Transient Response**
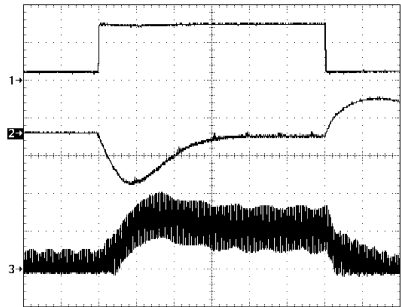


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$V_{OUT}$ = 8V, $V_{IN}$ = 2.5V

1) Load, 20mA to 155mA to 20mA, DC

2) $V_{OUT}$, 200mV/div, AC

3) $I_L$, 500mA/div, DC

T = 50µs/div

**PMOS Switching Waveform**
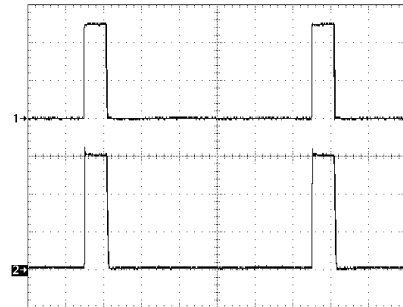


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$V_{OUT}$ = 8V, $V_{IN}$ = 2.5V, $R_{LOAD}$ = 40Ω, $C_{SS}$ = none

$C_D$ = 100nF, $R_{SW}$ = 10k‖1.5k, SWI = 30V, 10% duty cycle

1) SWC, 1V/div, DC

2) SWO, 10V/div, DC

T = 2.5µs/div

**PMOS Rising Edge**



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$V_{OUT}$ = 8V, $V_{IN}$ = 2.5V, $R_{LOAD}$ = 40Ω, $C_{SS}$ = none

$C_D$ = 100nF, $R_{SW}$ = 10k‖1.5k, SWI = 30V

1) SWC, 1V/div, DC

2) SWO, 10V/div, DC

T = 50ns/div

**PMOS Falling Edge**
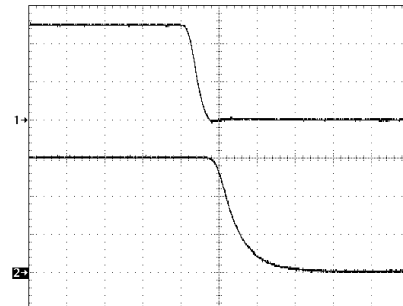


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$V_{OUT}$ = 8V, $V_{IN}$ = 2.5V, $R_{LOAD}$ = 40Ω, $C_{SS}$ = none

$C_D$ = 100nF, $R_{SW}$ = 10k‖1.5k, SWI = 30V

1) SWC, 1V/div, DC

2) SWO, 10V/div, DC

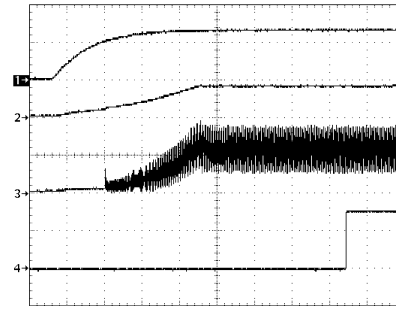T = 50ns/div

# Typical Performance Characteristics (Continued)

### Internal Soft Start and PMOS Delay
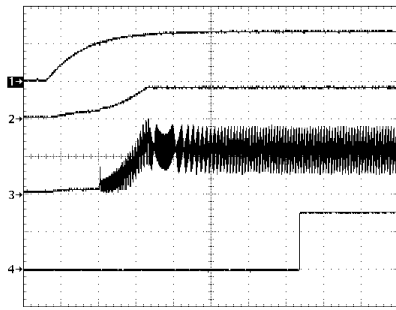


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$V_{OUT}$ = 8V, $V_{IN}$ = 2.5V, $R_{LOAD}$ = 40Ω, $C_{SS}$ = none
$C_D$ = 100nF, $R_{SW}$ = 10k‖1.5k, SWI = 30V, SWC = $V_{IN}$
1) $V_{IN}$, 2V/div, DC
2) $V_{OUT}$, 10V/div, DC
3) $I_L$, 500mA/div, DC
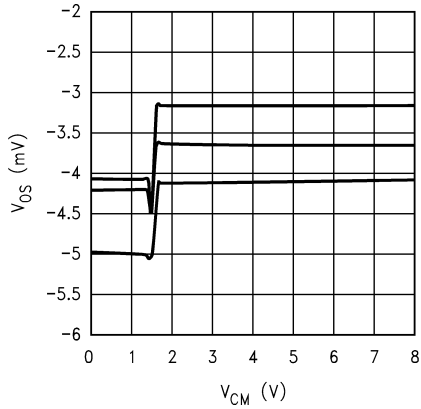4) SWO, 20V/div, DC
T = 5ms/div
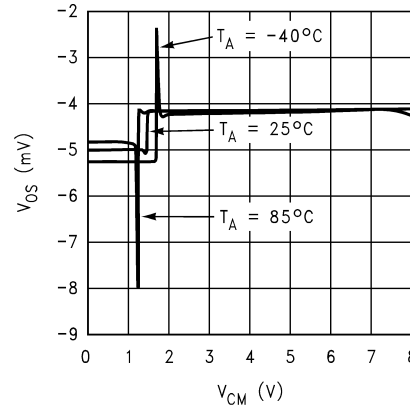
### External Soft Start and PMOS Delay



20051162

$V_{OUT}$ = 8V, $V_{IN}$ = 2.5V, $R_{LOAD}$ = 40Ω, $C_{SS}$ = 330nF
$C_D$ = 100nF, $R_{SW}$ = 10k‖1.5k, SWI = 30V, SWC = $V_{IN}$
1) $V_{IN}$, 2V/div, DC
2) $V_{OUT}$, 10V/div, DC
3) $I_L$, 500mA/div, DC
4) SWO, 20V/div, DC
T = 5ms/div

### Input Offset Voltage vs. Common Mode Voltage (Vcom, 3 units)



20051174

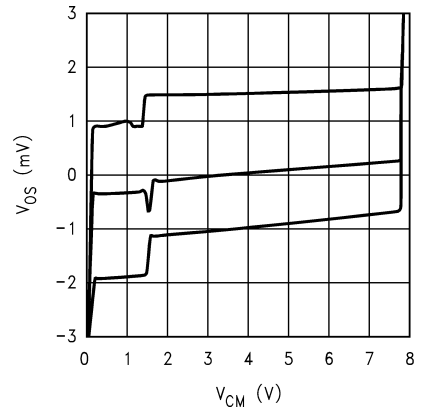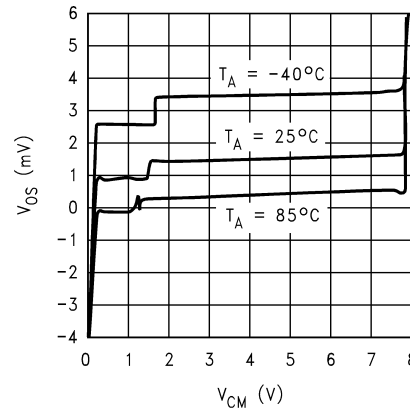### Input Offset Voltage vs. Common Mode Voltage (Vcom Over Temperature)



20051175

### Input Offset Voltage vs. Common Mode Voltage (Gamma, 3 units)
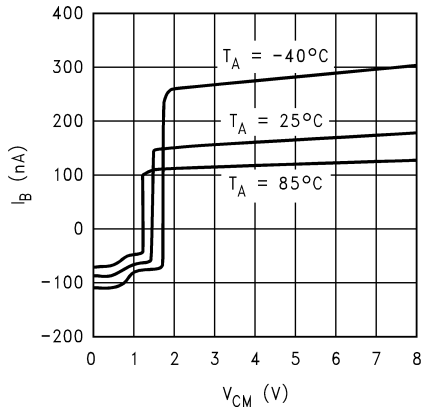


20051176

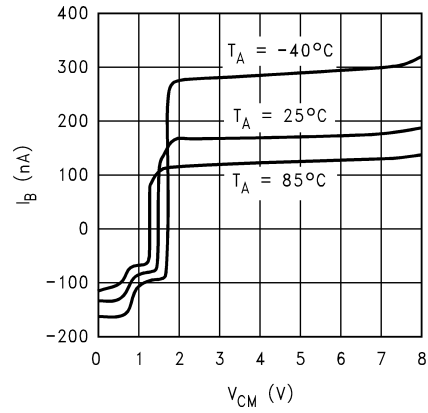### Input Offset Voltage vs. Common Mode Voltage (Gamma Over Temperature)



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# Typical Performance Characteristics (Continued)

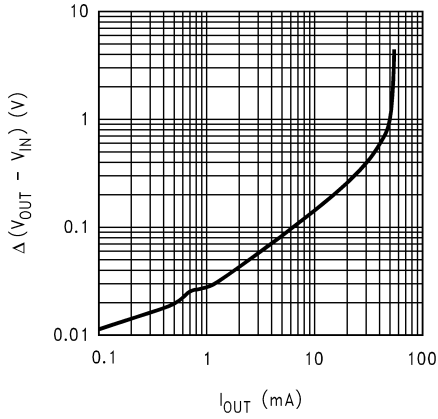**Input Bias Current vs. Common Mode Voltage (Vcom)**



20051178

**Input Bias Current vs. Common Mode Voltage (Gamma)**
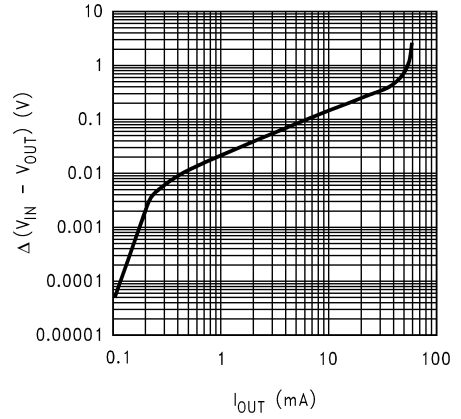


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**Output Voltage vs. Output Current (Vcom or Gamma, sinking)**
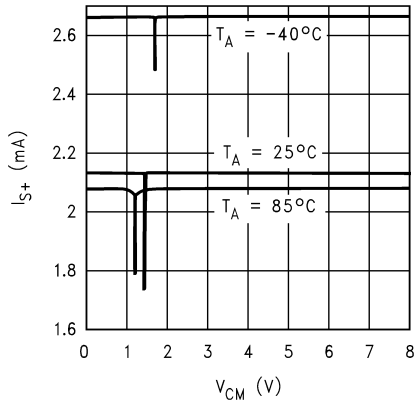


20051180

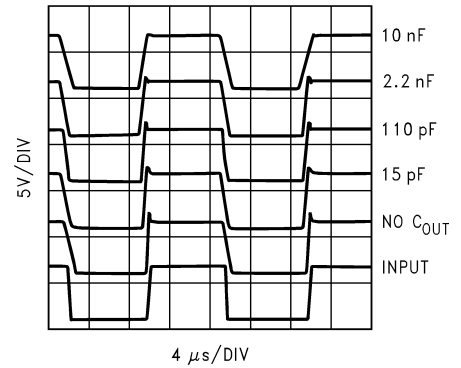**Output Voltage vs. Output Current (Vcom or Gamma, sourcing)**



20051181

**Supply Current vs. Common Mode Voltage (Both Amplifiers)**
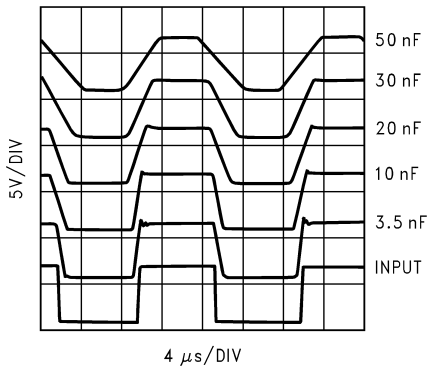


20051182

**Large Signal Step Response (50Ω, 1nF ext. compensation)**



20051183

# Typical Performance Characteristics (Continued)

**Large Signal Step Response
(no ext. compensation)**



5V/DIV

50 nF
30 nF
20 nF
10 nF
3.5 nF
INPUT

4 μs/DIV

20051184

**Positive Slew Rate vs. Capacitive Load
(Vcom or Gamma)**



SR (V/μs)

$T_A = 85°C$
$T_A = 25°C$
$T_A = -40°C$
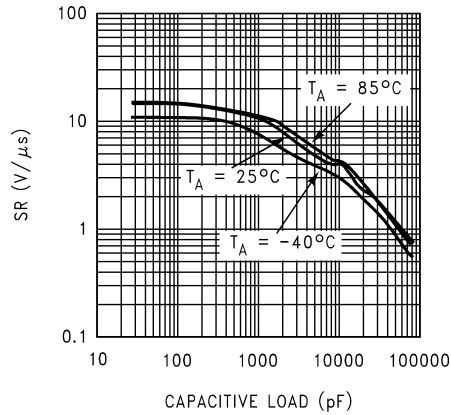
CAPACITIVE LOAD (pF)

20051190

**Negative Slew Rate vs. Capacitive Load
(Vcom or Gamma)**



SR (V/μs)

$T_A = 25°C$
$T_A = 85°C$
$T_A = -40°C$
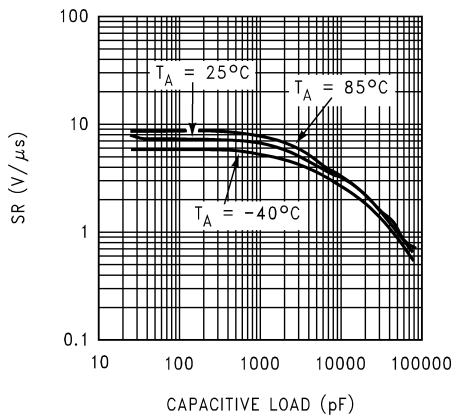
CAPACITIVE LOAD (pF)

20051185

**Phase Margin vs. Capacitive Load
(Vcom)**



PHASE MARGIN (°)

(5 nF)
(No Compensation)
(50 Ω, 1 nF)
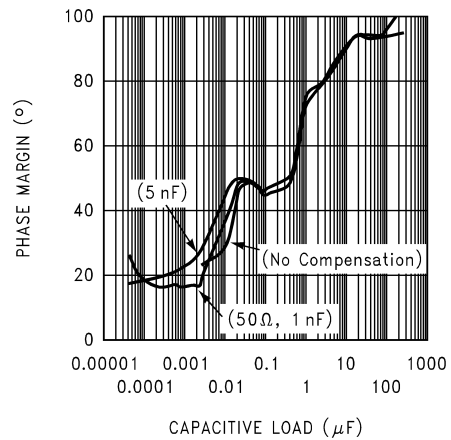
CAPACITIVE LOAD (μF)

20051186

**Unity Gain Frequency vs. Capacitive Load
(Vcom)**



UNITY GAIN FREQUENCY (Hz)

(No Compensation)
(5 nF)
(50 Ω, 1 nF)

CAPACITIVE LOAD (μF)
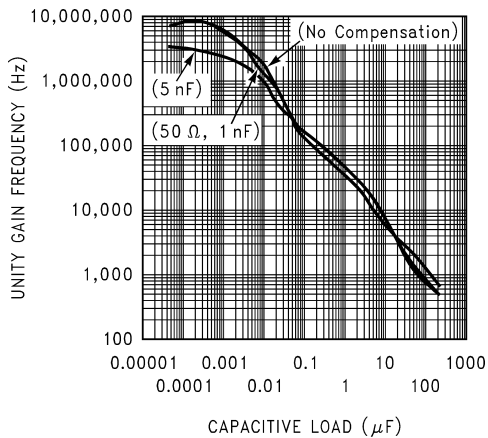
20051187

**CMRR vs. Frequency
(Vcom)**



CMRR (dB)

FREQUENCY (Hz)

20051188

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# Typical Performance Characteristics (Continued)

**PSRR vs. Frequency**
**(Vcom)**
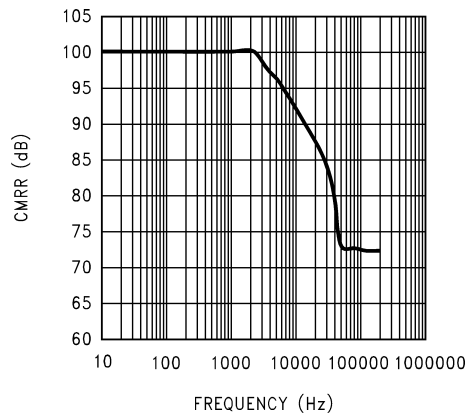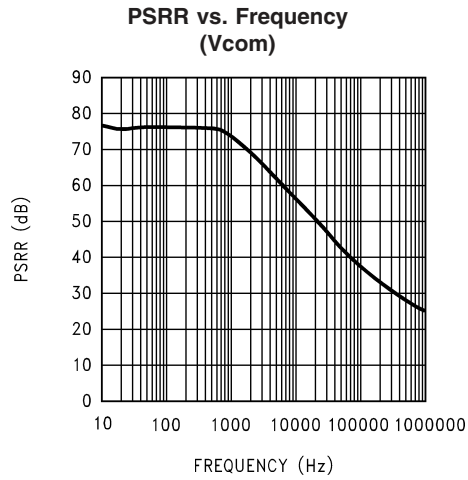


20051189
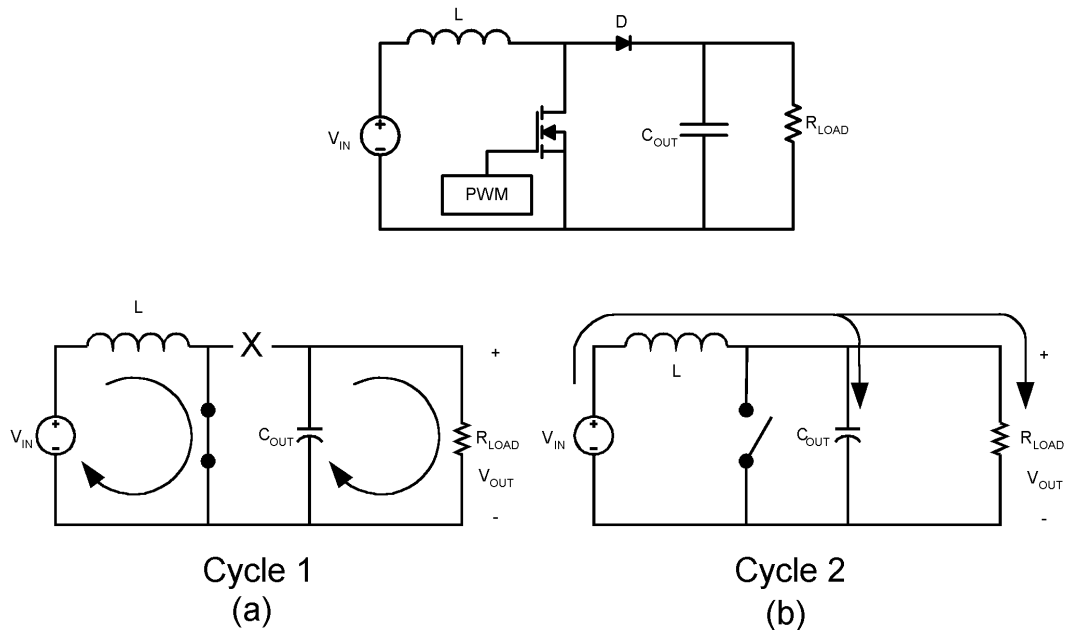
# Operation



**FIGURE 1. Simplified Boost Converter Diagram**
**(a) First Cycle of Operation (b) Second Cycle Of Operation**

## CONTINUOUS CONDUCTION MODE

The LM2702 is a TFT Panel Module containing a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in *Figure 1* (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by $C_{OUT}$.

The second cycle is shown in *Figure 1* (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1-D}, \quad D' = (1-D) = \frac{V_{IN}}{V_{OUT}}$$

where D is the duty cycle of the switch, D and D' will be required for design calculations

## SETTING THE OUTPUT VOLTAGE

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in the typical operating circuit. The feedback pin voltage is 1.265V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$R1 = R2 \left( \frac{V_{OUT}}{1.265V} - 1 \right)$$

## SOFT-START CAPACITOR

The LM2702 has patented internal circuitry that is used to limit the inductor inrush current on start-up of the boost DC/DC switching regulator. This inrush current limiting circuitry serves as a soft-start. However, many applications may require much more soft-start than what is available with the internal circuitry. The external SS pin is used to tailor the soft-start for a specific application. A 12µA current charges the external soft-start capacitor, $C_{SS}$. The soft-start time can be estimated as:

$$T_{SS} = C_{SS}*0.6V/12µA$$

The minimum soft-start time is set by the internal soft-start circuitry, typically 7ms. Only longer soft-start times may be implemented using the SS pin and a capacitor $C_{SS}$. If a shorter time is designed for using the above equation, the internal soft-start circuitry will override it.

Due to the unique nature of the dual internal/external soft-start, care was taken in the design to ensure temperature stable operation. As you can see with the Iss data in the Electrical Characterisitcs table and the graph "Soft-Start Current vs. $V_{IN}$" in the *Typical Performance Characterisitcs*

## Operation (Continued)

section, the soft start curent has a temperature coefficient and would lead one to believe there would be significant variation with temperature. Though the current has a temperature coefficient the actual programmed external soft start time does not show this extreme of a temperature variation. As you can see in the following transient plots:

$V_{OUT}$ = 8V, $V_{IN}$ = 2.5V, $R_L$ = 51Ω, $C_{SS}$ = 330nF, T = 4ms/div. Trace:

1) $V_{IN}$, 5V/div, DC Coupled
2) $V_{OUT}$, 5V/div, DC Coupled
3) $I_L$, 0.5A/div, DC Coupled
4) $V_{SW}$, 5V/div, DC Coupled



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**$T_A$ = −20˚C**



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**$T_A$ = 27˚C**



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**$T_A$ = 85˚C**
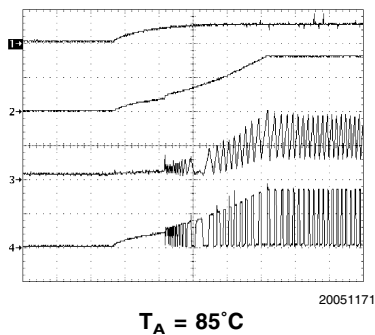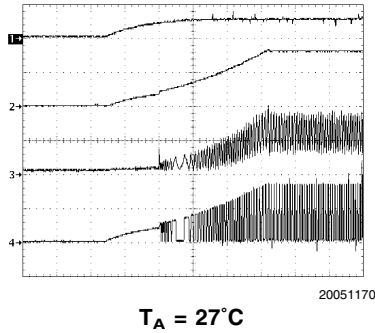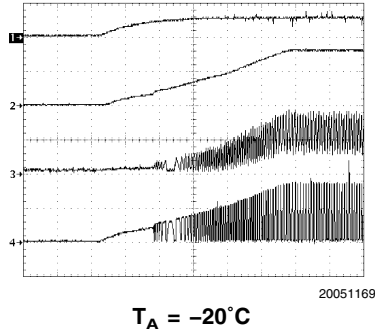
When programming the softstart time externally, simply use the equation given in the *Soft-Start Capacitor* section above. This equation uses the typical room temperature value of the soft start current, 12µA, to set the soft start time.

### DELAY CAPACITOR

The LM2702 has internal circuitry that can be used to set a delay time preventing control of the PMOS switch via SWC until a desired amount of time after the switcher starts up. The PMOS control circuitry remains inactive until $V_{OUT}$

reaches 85% of the nominal output voltage. When this occurs, $C_D$ begins to charge. When the voltage on the Delay pin reaches 1.265V the PMOS switch will become active and can be controlled using the SWC pin. If no $C_D$ is used, the PMOS switch can be controlled immediately after $V_{OUT}$ reaches 85% of the nominal output voltage. The delay time can be calculated using the equation:

$$T_D = C_D * (1.265V/5.7µA)$$

### INTRODUCTION TO COMPENSATION



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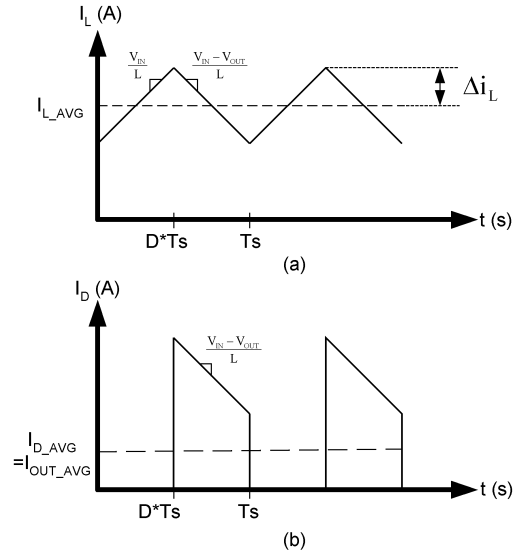
**FIGURE 2. (a) Inductor current. (b) Diode current.**

The LM2702 contains a current mode PWM boost converter. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see *Figure 2* (a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%. A 4.7µH inductor is recommended for most applications. If the duty cycle is approaching the maximum of 85%, it may be necessary to increase the inductance by as much as 2X. See *Inductor and Diode Selection* for more detailed inductor sizing.

The LM2702 provides a compensation pin ($V_C$) to customize the voltage loop feedback. It is recommended that a series combination of $R_C$ and $C_C$ be used for the compensation network, as shown in the typical application circuit. For any given application, there exists a unique combination of $R_C$ and $C_C$ that will optimize the performance of the LM2702 circuit in terms of its transient response. The series combination of $R_C$ and $C_C$ introduces a pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi R_C C_C} \text{ Hz}$$

# Operation (Continued)

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ Hz}$$

where $R_O$ is the output impedance of the error amplifier, approximately 1MΩ. For most applications, performance can be optimized by choosing values within the range 5kΩ ≤ $R_C$ ≤ 40kΩ ($R_C$ can be up to 200kΩ if $C_{C2}$ is used, see *High Output Capacitor ESR Compensation*) and 680pF ≤ $C_C$ ≤ 4.7nF. Refer to the Typical Application Circuit and the *Applications Information* section for recommended values for specific circuits and conditions. Refer to the *Compensation* section for other design requirement.

## COMPENSATION FOR BOOST DC/DC

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation (Inductor current never reaches zero), in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

## INDUCTOR AND DIODE SELECTION

Although the inductor size mentioned earlier is fine for most applications, a more exact value can be calculated. To ensure stability at duty cycles above 50%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

$$L > \frac{V_{IN}R_{DSON}}{0.362 \text{ fs}} \left[ \frac{D}{D'} - 1 \right] \text{ (in H)}$$

where fs is the switching frequency, D is the duty cycle, and $R_{DSON}$ is the ON resistance of the internal switch taken from the graph "$R_{DSON}$ vs. $V_{IN}$" in the *Typical Performance Characteristics* section. This equation is only good for duty cycles greater than 50% (D>0.5), for duty cycles less than 50% the recommended values may be used. The corresponding inductor current ripple as shown in *Figure 2* (a) is given by:

$$\Delta i_L = \frac{V_{IN}D}{2Lfs} \text{ (in Amps)}$$

The inductor ripple current is important for a few reasons. One reason is because the peak switch current will be the average inductor current (input current or $I_{LOAD}$/D') plus $\Delta i_L$. As a side note, discontinuous operation occurs when the inductor current falls to zero during a switching cycle, or $\Delta i_L$ is greater than the average inductor current. Therefore, continuous conduction mode occurs when $\Delta i_L$ is less than the average inductor current. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output and input voltage ripples are also affected by the total ripple current.

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The typical current waveform for the diode in continuous conduction mode is shown in *Figure 2* (b). The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

## DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45˚) is desired for the best stability and transient response. For the purpose of stabilizing the LM2702, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin. A discussion of the right half plane zero and checking the crossover using the DC gain will follow.

## INPUT AND OUTPUT CAPACITOR SELECTION

The switching action of a boost regulator causes a triangular voltage waveform at the input. A capacitor is required to reduce the input ripple and noise for proper operation of the regulator. The size used depends on the application and board layout. If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10μF should be used for the less stressful conditions while a 22μF to 47μF capacitor may be required for higher power and dynamic loads. Larger values and/or lower ESR may be needed if the application requires very low ripple on the input source voltage.

The choice of output capacitors is also somewhat arbitrary and depends on the design requirements for output voltage ripple. It is recommended that low ESR (Equivalent Series Resistance, denoted $R_{ESR}$) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the peak to peak output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \approx 2\Delta i_L R_{ESR} \text{ (in Volts)}$$

A minimum value of 10μF is recommended and may be increased to a larger value. After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi(R_{ESR} + R_L)C_{OUT}} \text{ (in Hz)}$$

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## Operation (Continued)

$$f_{Z1} = \frac{1}{2\pi R_{ESR}C_{OUT}} \text{ (in Hz)}$$

Where $R_L$ is the minimum load resistance corresponding to the maximum load current. The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the *High Output Capacitor ESR Compensation* section.

### RIGHT HALF PLANE ZERO
A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90˚ in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

$$\text{RHPzero} = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD}L} \text{ (in Hz)}$$

where $I_{LOAD}$ is the maximum load current.

### SELECTING THE COMPENSATION COMPONENTS
The first step in selecting the compensation components $R_C$ and $C_C$ is to set a dominant low frequency pole in the control loop. Simply choose values for $R_C$ and $C_C$ within the ranges given in the *Introduction to Compensation* section to set this pole in the area of 10Hz to 500Hz. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ (in Hz)}$$

where $R_O$ is the output impedance of the error amplifier, approximately 1MΩ. Since $R_C$ is generally much less than $R_O$, it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero $f_{ZC}$. $f_{ZC}$ is created to cancel out the pole created by the output capacitor, $f_{P1}$. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of $f_{P1}$ over the expected loads and then set the zero $f_{ZC}$ to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi C_C R_C} \text{ (in Hz)}$$

Now $R_C$ can be chosen with the selected value for $C_C$. Check to make sure that the pole $f_{PC}$ is still in the 10Hz to 500Hz range, change each value slightly if needed to ensure both component values are in the recommended range. After checking the design at the end of this section, these values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance

circuit. For improved transient response, higher values of $R_C$ should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimal performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

### HIGH OUTPUT CAPACITOR ESR COMPENSATION
When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, $C_{C2}$, directly from the compensation pin $V_C$ to ground, in parallel with the series combination of $R_C$ and $C_C$. The pole should be placed at the same frequency as $f_{Z1}$, the ESR zero. The equation for this pole follows:

$$f_{PC2} = \frac{1}{2\pi C_{C2}(R_C //R_O)} \text{ (in Hz)}$$

To ensure this equation is valid, and that $C_{C2}$ can be used without negatively impacting the effects of $R_C$ and $C_C$, $f_{PC2}$ must be greater than $10f_{ZC}$.

### CHECKING THE DESIGN
The final step is to check the design. This is to ensure a bandwidth of ½ or less of the frequency of the RHP zero. This is done by calculating the open-loop DC gain, $A_{DC}$. After this value is known, you can calculate the crossover visually by placing a –20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than ½ the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved by adding $C_{C2}$ as discussed earlier in the section. The equation for $A_{DC}$ is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left\langle\left(\frac{R_{FB2}}{R_{FB1}+R_{FB2}}\right)\frac{g_m R_O D'}{R_{DSON}}\{[(\omega cLeff)// R_L]//R_L\}\right\rangle \text{(in dB)}$$

$$\omega c \cong \frac{2fs}{nD'} \text{ (in rad/s)}$$

$$Leff = \frac{L}{(D')^2}$$

$$n = 1+\frac{2mc}{m1} \text{ (no unit)}$$

$$mc \cong 0.181fs \text{ (in V/s)}$$

$$m1 \cong \frac{V_{IN}R_{DSON}}{L} \text{ (in V/s)}$$

where $R_L$ is the minimum load resistance, $V_{IN}$ is the minimum input voltage, $g_m$ is the error amplifier transconductance found in the *Electrical Characteristics* table, and $R_{DSON}$ is the value chosen from the graph "$R_{DSON}$ vs. $V_{IN}$" in the *Typical Performance Characteristics* section.

## Operation (Continued)

### Vcom AND Gamma COMPENSATION

The architecture used for the amplifiers in the LM2702 requires external compensation on the output. Depending on the equivalent capacitive load of the TFT-LCD panel, external components at the amplifier outputs may or may not be necessary. If the capacitance presented by the load is equal to or greater than 5nF no external components are needed as the TFT-LCD panel will act as compensation itself. Distributed resistive and capacitive loads enhance stability and increase performance of the amplifiers. If the capacitance presented by the load is less than 5nF external components will be required as the load itself will not ensure stability. No external compensation in this case will lead to oscillation of the amplifier and an increase in power consumption. A single 5nF or greater capacitor on the output will ensure a stable amplifier with no oscillations. For applications requiring a higher slew rate, a good choice for compensation is to add a $50\Omega$ ($R_{COM}$ or $R_{GAMMA}$) in series with a 1nF ($C_{COM}$ or $C_{GAMMA}$) capacitor from the output of the amplifier to ground. This allows for driving zero to infinite capacitance loads with no oscillations, minimal overshoot, and a higher slew rate than using a large capacitor. The high phase margin created by the external compensation will guarantee stability and good performance for all conditions.

For noise sensitive applications greater output capacitance may be desired. When the power supply for the amplifiers ($AV_{IN}$) is connected to the output of the switching regulator, the output ripple of the regulator will produce ripple at the output of the amplifiers.

### LAYOUT CONSIDERATIONS

The LM2702 uses a single ground connection, GND. The feedback, softstart, delay, and compensation networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the GND pin, as shown in *Figure 3*. If no analog ground plane is available then the ground connections of the feedback, softstart, delay, and compensation networks must tie directly to the GND pin, as show in *Figure 4*. Connecting these networks to the PGND plane can inject noise into the system and effect performance.

The input bypass capacitor $C_{IN}$ must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with $C_{IN}$, close to the $V_{IN}$ pin, to shunt any high frequency noise to ground. The output capacitor, $C_{OUT}$, should also be placed close to the IC. Any copper trace connections for the $C_{OUT}$ capacitor can increase the series resistance, which directly effects output voltage ripple and efficiency. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency.
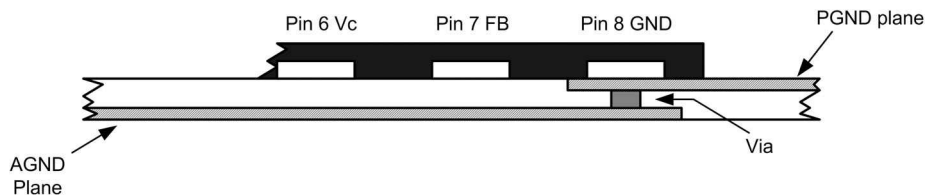


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**FIGURE 3. Multi-Layer Layout**

# Operation  (Continued)



AGND Trace

Power GND Trace

6

7

9

8

Bottom View
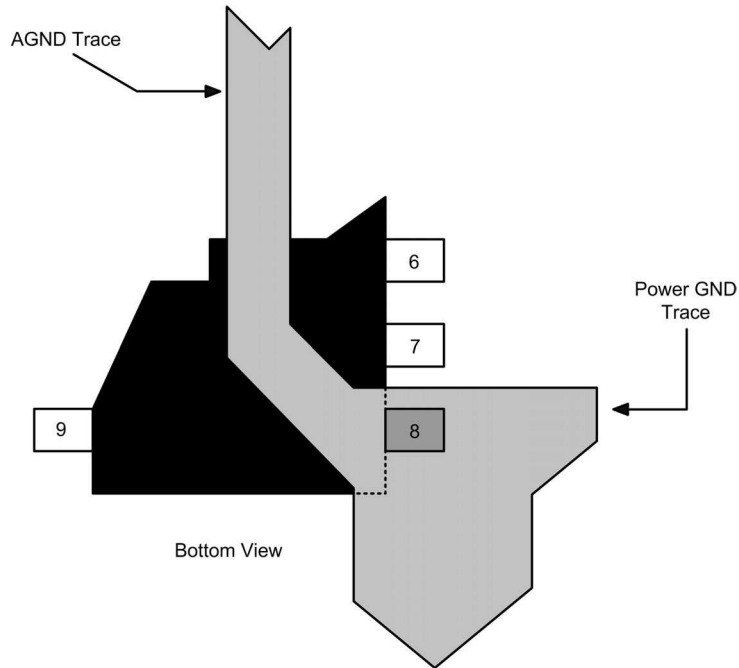
20051153

**FIGURE 4. Single Layer Layout**

# Application Information



$D_2$    $D_3$

0.1 μF

0.1μF    $D_4$    -10 V

$D_5$    4.7 μF

$V_{IN} = + 5V$    L = 10 μH    $D_1$    $V_{OUT} = + 10V$ 250mA

AVIN

AVIN

Gamma Reference    $V_G$

$V_G^+$

$V_{COM+}$    **LM2702**

$C_{IN}$ 4.7μF ceramic

$V_{COM-}$

$V_{COM}$

Common Backplane

$V_{IN}$    SW

$AV_{IN}$

FB    $R_1$ 470k

$C_{OUT}$ 4.7μF ceramic    $C_{OUT}$ 4.7μF ceramic

$R_2$ 68k

Css

Delay

SWI    +20V

$V_C$  GND  SWC  SWO

$R_C$ 10k    $V_{IN}$    +20 $V_{OUT}$    $C_D$    $C_{SS}$    4.7 μF

$C_C$ 2.2nF
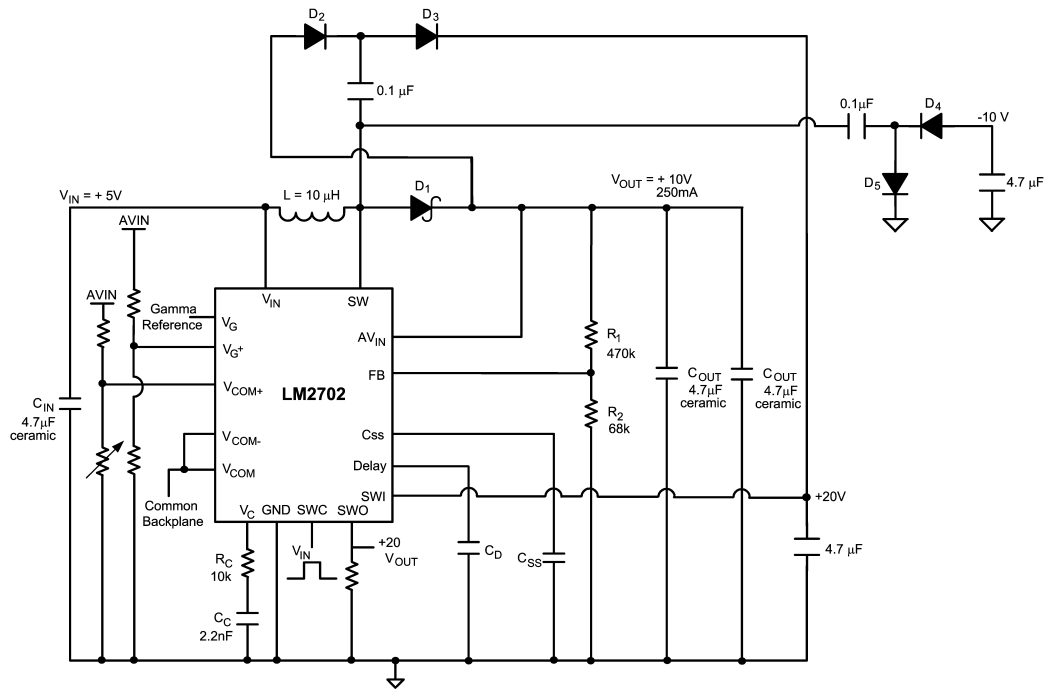
20051172

**FIGURE 5. 5V to 10V TFT Application**

LM2702 TFT Panel Module

## Physical Dimensions  inches (millimeters)
unless otherwise noted



DIMENSIONS METRIC ONLY

LAND PATTERN RECOMMENDATION

DETAIL A
TYPICAL, SCALE: 40X
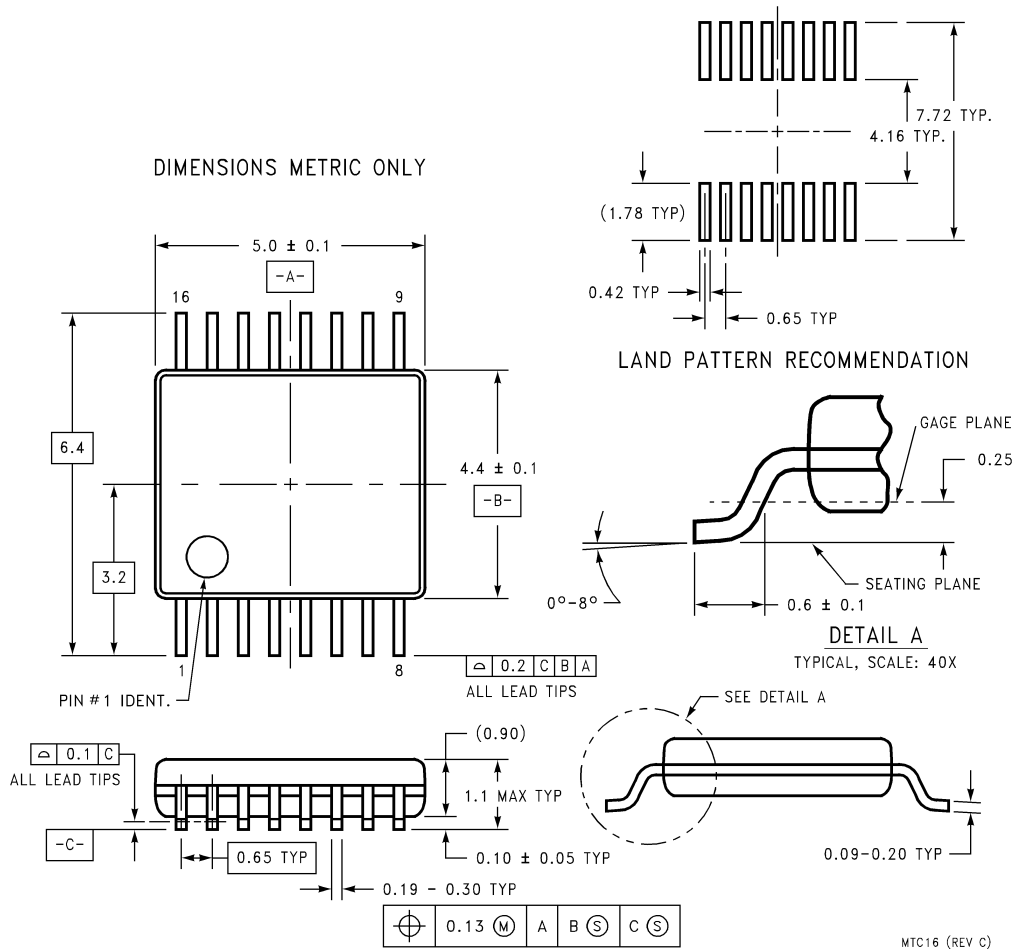
MTC16 (REV C)

**TSSOP-16 Pin Package (MTC)**
**For Ordering, Refer to Ordering Information Table**
**NS Package Number MTC16**

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