

LM2757

Switched Capacitor Boost Regulator with High Impedance Output in Shutdown

General Description

The LM2757 is a constant frequency pre-regulated switched-capacitor charge pump that operates at 1.25 MHz to produce a low-noise regulated output voltage. The device can be configured to provide up to 100 mA at 4.1V, 110 mA at 4.5V, or 180 mA at 5V. Excellent efficiency is achieved without the use of an inductor by operating the charge pump in a gain of either 3/2 or 2 according to the input voltage and output voltage option selection.

The LM2757 presents a high impedance at the V_{OUT} pin when shut down. This allows for use in applications that require the regulated output bus to be driven by another supply while the LM2757 is shut down.

A perfect fit for space-constrained, battery-operated applications, the LM2757 requires only 4 small, inexpensive ceramic capacitors. LM2757 is a tiny 1.2 mm X 1.6 mm 12-bump micro SMD device. Built in soft-start, over-current protection, and thermal shutdown features are also included in this device.

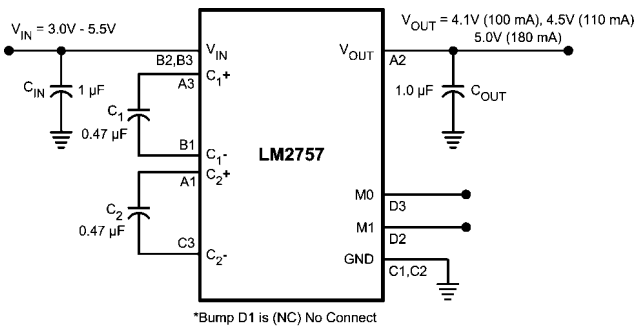
Features

- Dual gain converter (2x, 3/2x) with up to 93% Efficiency.
- Inductorless solution uses only 4 small ceramic capacitors.
- Total solution area < 12mm².
- True input-output and output-input disconnect.
- Up to 180 mA output current capability (5V).
- Selectable 4.1V, 4.5V or 5.0V output.
- Pre-regulation minimizes input current ripple.
- 1.24 MHz switching frequency for a low-noise, low-ripple output voltage.
- Integrated Over Current and Thermal Shutdown Protection.
- Tiny 1.2 mm X 1.6 mm X 0.4 mm pitch, 12-bump micro SMD package.

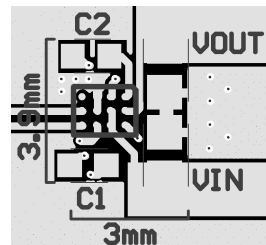
Applications

- USB/USB-OTG Power
- Supercapacitor Charger
- Keypad LED Drive
- Audio amplifier power supply
- Low-current Camera Flash
- General Purpose Li-Ion-to-5V Conversion
- Cellular Phone SIM cards

Typical Application Circuit



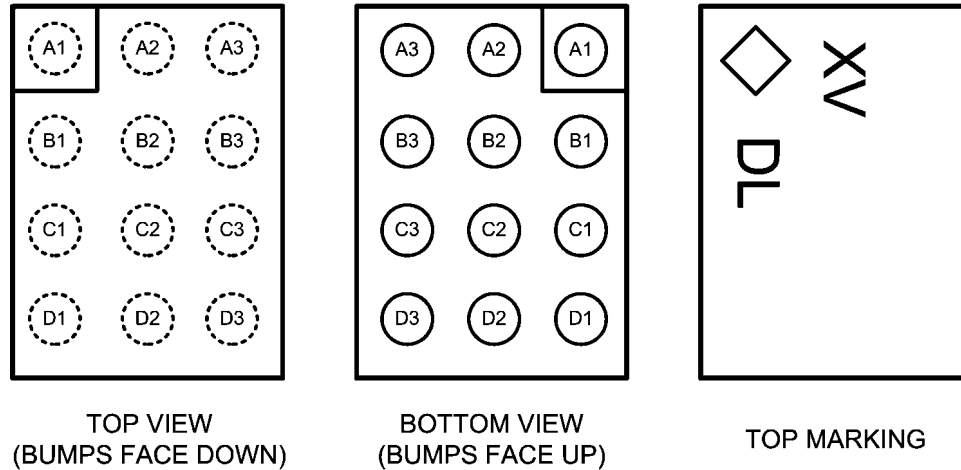
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Connection Diagram and Package Mark Information

12-Bump Micro SMD Package, 0.4mm Pitch
National Semiconductor Package Number TMD12



30033702

Note 1: The actual physical placement of the package marking will vary from part to part. The package marking "X" designates the single digit date code. "V" is a NSC internal code for die traceability. Both will vary considerably. "DL" identifies the device (part number, option, etc.).

Pin Descriptions

Pin #	Name	Description
A1	C2+	Flying Capacitor C2 Connection
A2	V _{OUT}	Regulated Output Voltage
A3	C1+	Flying Capacitor C1 Connection
B1	C1-	Flying Capacitor C1 Connection
B2	V _{IN}	Input Voltage Connection
B3	V _{IN}	Input Voltage Connection
C1	GND	Ground Connection
C2	GND	Ground Connection
C3	C2-	Flying Capacitor C2 Connection
D1	NC	No Connect — Do not connect this pin to any node, voltage or GND. Must be left floating.
D2	M1	Mode select pin 1
D3	M0	Mode select pin 0

Mode Selection Definition

M0	M1	OUTPUT VOLTAGE MODE
0	0	Device Shutdown, Output High Impedance
0	1	5.0V
1	0	4.5V
1	1	4.1V

Order Information

Order Number	Package Mark ID	Package	Supplied as:
LM2757TM	XV	12-Bump μ SMD	1000 Units, Tape & Reel
LM2757TMX	(A1 Bump Marking) DL	0.4mm pitch	4000 Units, Tape & Reel

Absolute Maximum Ratings (Notes 2, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{IN} Pin: Voltage to GND	-0.3V to 6.0V
M0, M1 pins: Voltage to GND	-0.3V to 6.0V
Continuous Power Dissipation (Note 4)	Internally Limited
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec.)	265°C
ESD Rating (Note 5)	
Human Body Model:	2.5 kV

Operating Ratings

(Notes 2, 3)

Input Voltage Range	2.7V to 5.5V
Junction Temperature (T_J) Range	-30°C to +110°C
Ambient Temperature (T_A) Range (Note 6)	-30°C to +85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), micro SMD Package (Note 7)	75°C/W
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Electrical Characteristics (Notes 3, 8)

Limits in standard typeface are for $T_A = 25^\circ\text{C}$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$). Unless otherwise noted, specifications apply to the Typical Application Circuit (pg. 1) with: $V_{IN} = 3.6\text{V}$, $V(M0) = 0\text{V}$, $V(M1) = V_{IN}$, $C_{IN} = C_2 = 0.47\ \mu\text{F}$, $C_{IN} = C_{OUT} = 1.0\ \mu\text{F}$ (Note 9).

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage	$3.2\text{V} \leq V_{IN} \leq 5.5\text{V}$ $-30^\circ\text{C} \leq T_A \leq +60^\circ\text{C}$ $I_{OUT} = 0$ to 180 mA $V(M0) = 0\text{V}$, $V(M1) = V_{IN}$	4.870 (-2.6%)	5.0	5.130 (+2.6%)	V
		$3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$ $-30^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $I_{OUT} = 0$ to 150 mA $V(M0) = 0\text{V}$, $V(M1) = V_{IN}$	4.865 (-2.7%)	5.0	5.130 (+2.6%)	
		$3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$ $I_{OUT} = 0$ to 110 mA $V(M0) = V_{IN}$, $V(M1) = 0\text{V}$	4.406 (-2.1%)	4.5	4.613 (+2.5%)	
		$3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$ $I_{OUT} = 0$ to 100 mA $V(M0) = V_{IN}$, $V(M1) = V_{IN}$	3.985 (-2.8%)	4.1	4.223 (+3.0%)	
I_Q	Quiescent Supply Current	$V(M0) = 0\text{V}$, $V(M1) = V_{IN}$ (5.0V) $I_{OUT} = 0$ mA $V_{IN} = 3.6\text{V}$		2.4	2.79	mA
		$V(M0) = V_{IN}$, $V(M1) = 0\text{V}$ (4.5V) $I_{OUT} = 0$ mA $V_{IN} = 3.6\text{V}$		1.5	1.80	
		$V(M0) = V_{IN}$, $V(M1) = V_{IN}$ (4.1V) $I_{OUT} = 0$ mA $V_{IN} = 3.6\text{V}$		1.3	1.65	
I_{SD}	Shutdown Supply Current	$V(M0) = 0\text{V}$, $V(M1) = 0\text{V}$ $V_{IN} = 3.6\text{V}$		1.1	2.0	μA
V_R	Output Voltage Ripple	$I_{OUT} = 150$ mA $V(M0) = 0\text{V}$, $V(M1) = V_{IN}$ (5.0V) $3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$		20		mVp-p
f_{SW}	Switching Frequency	$3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$	0.932 (-25%)	1.242	1.552 (+25%)	MHz
V_{IN}	Logic Input High	Input pins: M1, M0 $3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$	1.0		V_{IN}	V

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Logic Input Low	Input pins: M1, M0 $3.0V \leq V_{IN} \leq 5.5V$	0		0.40	V
$R_{PULLDOWN}$	Logic Input Pulldown Resistance (M0, M1)	$V(M1, M0) = 5.5V$	324	457		$k\Omega$
I_{IH}	Logic Input High Current	Input Pins: M1, M0 $V(M1, M0) = 1.8V$ (Note 11)		5		μA
I_{IL}	Logic Input Low Current	Input Pins: M1, M0 $V(M1, M0) = 0V$		10		μA
V_G	Gain Transition Voltage	1.5X to 2X, $V(M0) = V_{IN}$, $V(M1)=0V$		3.333		V
		2X to 1.5X, $V(M0) = V_{IN}$, $V(M1)=0V$		3.413		V
		Hysteresis, $V(M0) = V_{IN}$, $V(M1)=0V$		80		mV
		1.5X to 2X, $V(M0) = 0V$, $V(M1)=V_{IN}$		3.87		V
		2X to 1.5X, $V(M0) = 0V$, $V(M1)=V_{IN}$		3.93		V
		Hysteresis, $V(M0) = 0V$, $V(M1)=V_{IN}$		60		mV
I_{SC}	Short Circuit Output Current	$V_{OUT} = 0V$		250		mA
t_{ON}	V_{OUT} Turn-On Time from Shutdown (Note 10)			300		μs

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 3: All voltages are with respect to the potential at the GND pins.

Note 4: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J=145^\circ C$ (typ.) and disengages at $T_J=135^\circ C$ (typ.).

Note 5: The Human body model is a 100 pF capacitor discharged through a 1.5 k Ω resistor into each pin.

Note 6: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}=125^\circ C$), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 7: Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2x1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 36 μm /18 μm /18 μm /36 μm (1.5 oz./1 oz./1 oz./1.5 oz.). Ambient temperature in simulation is 22 $^\circ C$, still air. Power dissipation is 1W.

The value of θ_{JA} in LM2757 in micro SMD-12 could fall in a range as wide as 50 $^\circ C/W$ to 150 $^\circ C/W$ (if not wider), depending on PWB material, layout and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN} , high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to **Application Note 1112: Micro SMD Wafer Level Chip Scale Package (μSMD)**.

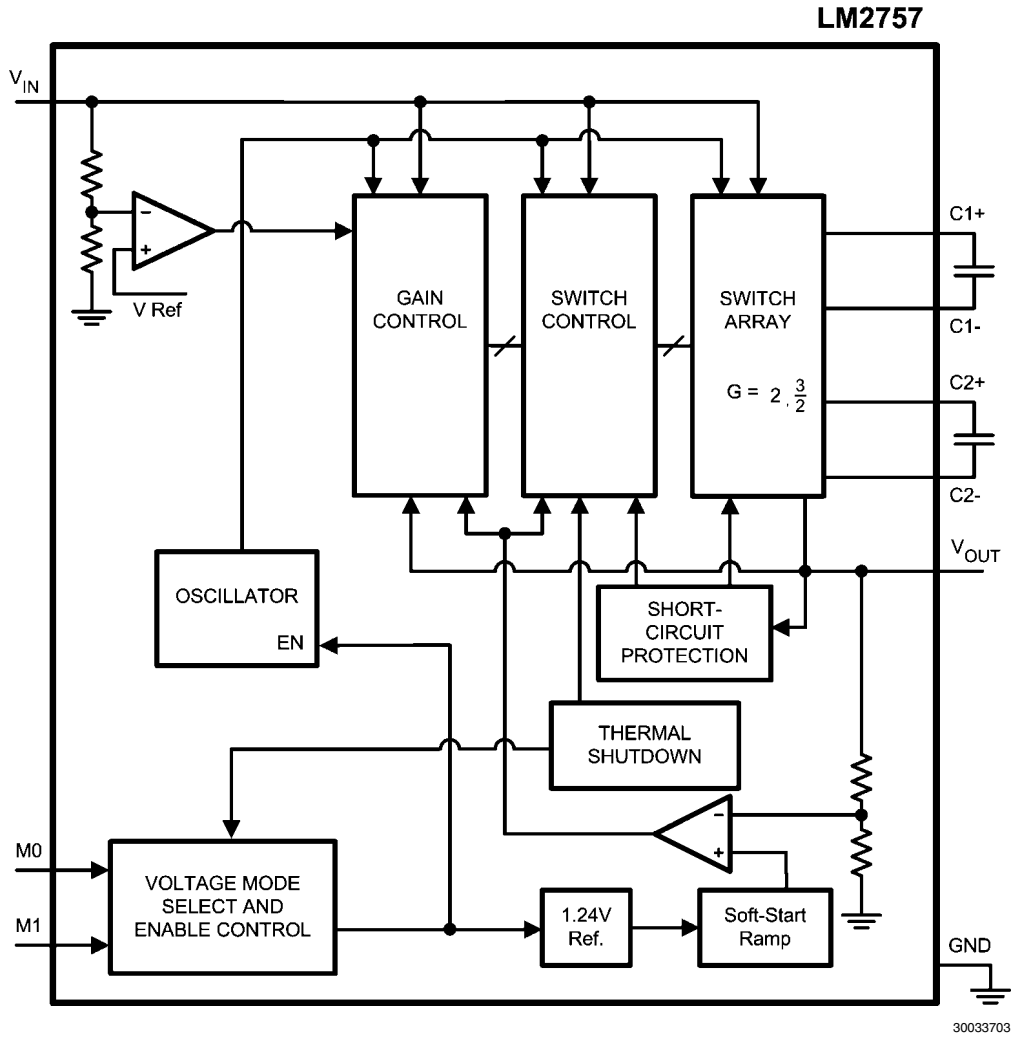
Note 8: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 9: C_{IN} , C_{OUT} , C_1 , C_2 : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Note 10: Turn-on time is measured from when the M0 or M1 signal is pulled high until the output voltage crosses 90% of its final value.

Note 11: There is a 450 k Ω (typ.) pull-down resistor connected internally to each logic input.

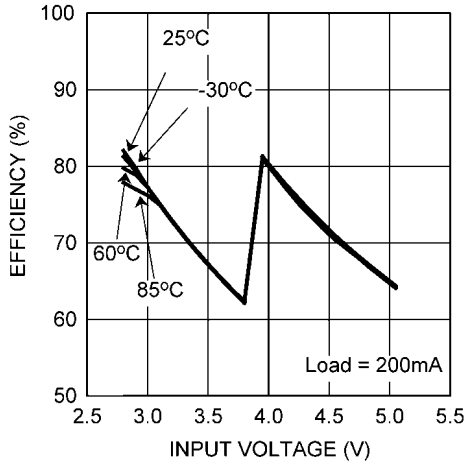
Block Diagram



Typical Performance Characteristics

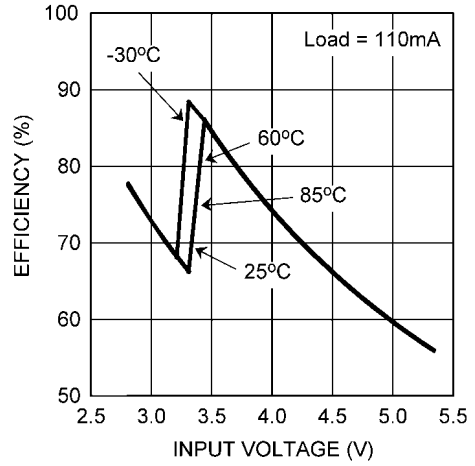
Unless otherwise specified: $V_{IN} = 3.6V$, $V(M0) = 0V$, $V(M1) = V_{IN}$, $C_1 = C_2 = 0.47\mu F$, $C_{IN} = C_{OUT} = 1.0\mu F$, $T_A = 25^\circ C$. Capacitors are low-ESR multi-layer ceramic capacitors (MLCC's).

Efficiency vs. Input Voltage, 5V Mode



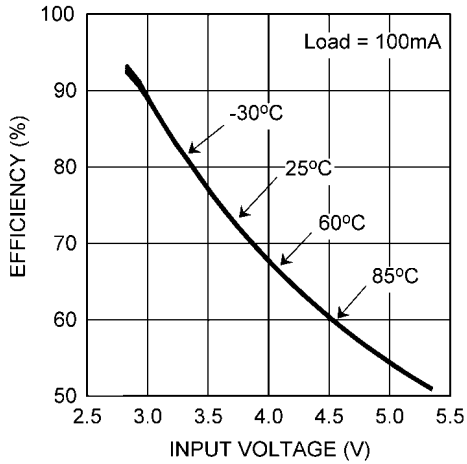
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Efficiency vs. Input Voltage, 4.5V Mode



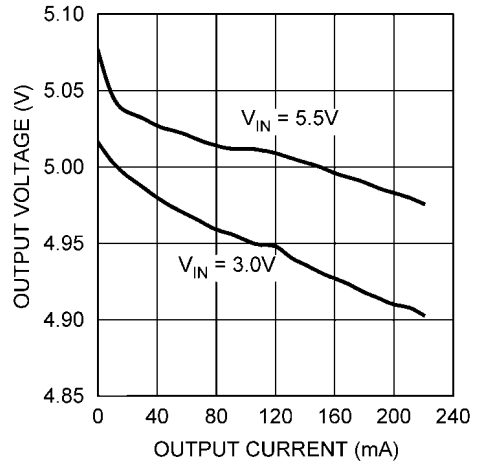
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Efficiency vs. Input Voltage, 4.1V Mode



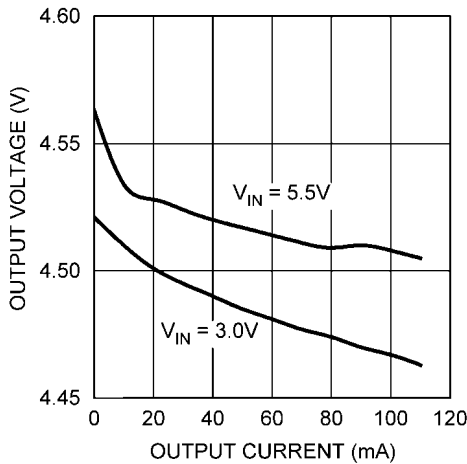
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Output Voltage vs. Output Current, 5V Mode



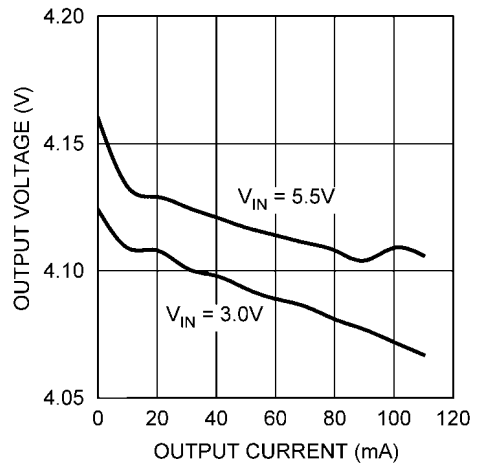
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Output Voltage vs. Output Current, 4.5V Mode



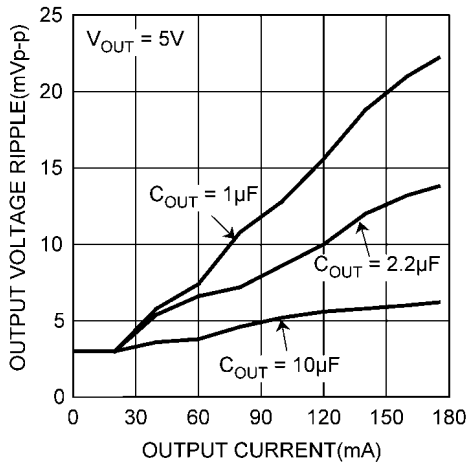
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Output Voltage vs. Output Current, 4.1V Mode



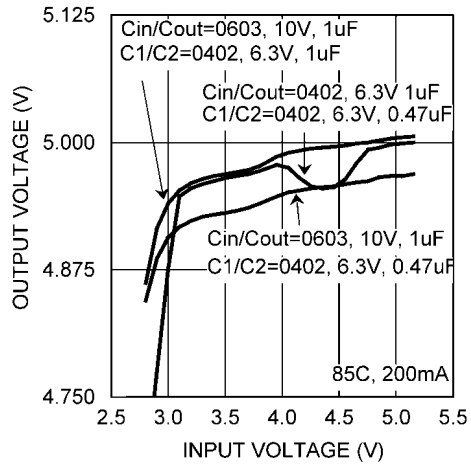
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Output Voltage Ripple vs. Output Current, 5V Mode



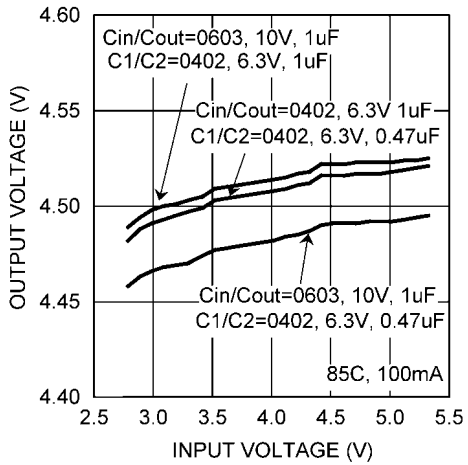
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Output Voltage vs. Input Voltage, 5V Mode



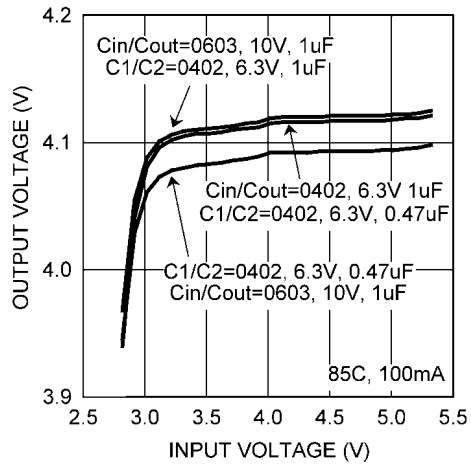
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Output Voltage vs. Input Voltage, 4.5V Mode



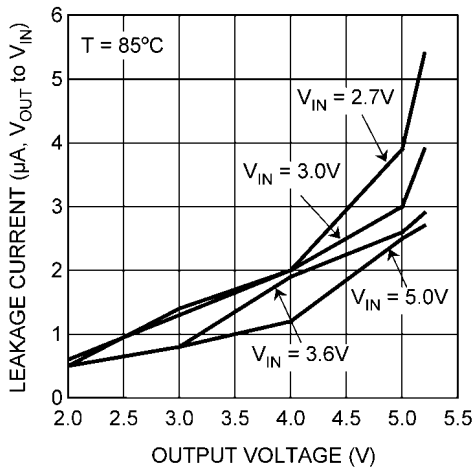
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Output Voltage vs. Input Voltage, 4.1V Mode



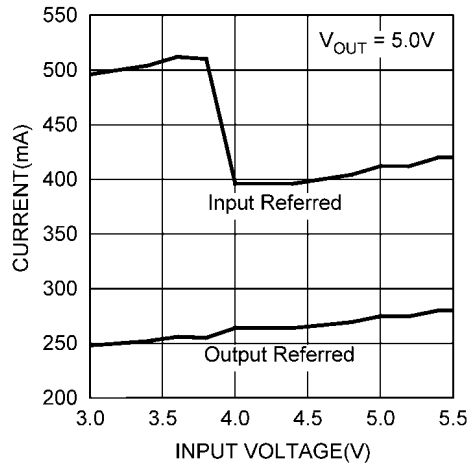
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Output Leakage Current, Device Shutdown



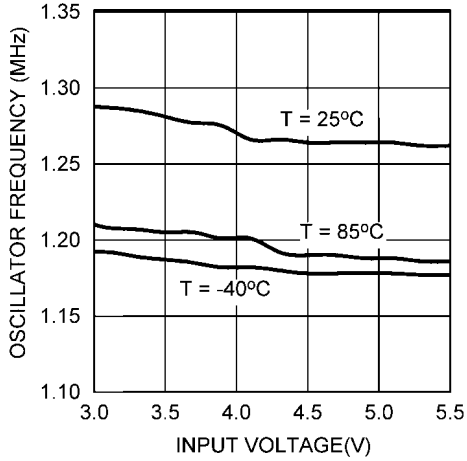
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Current Limit vs. Input Voltage



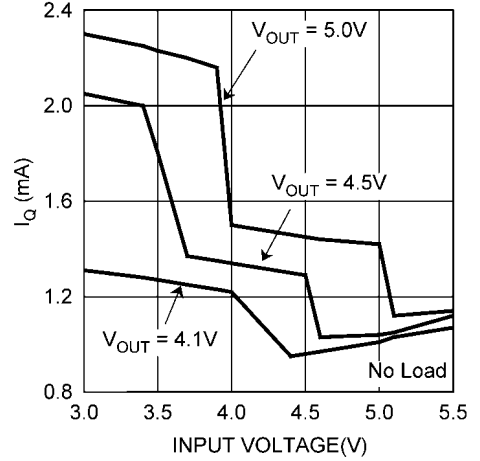
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Oscillator Frequency vs. Input Voltage



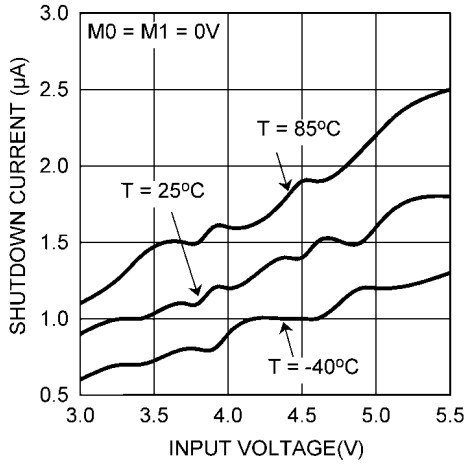
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Operating Current vs. Input Voltage



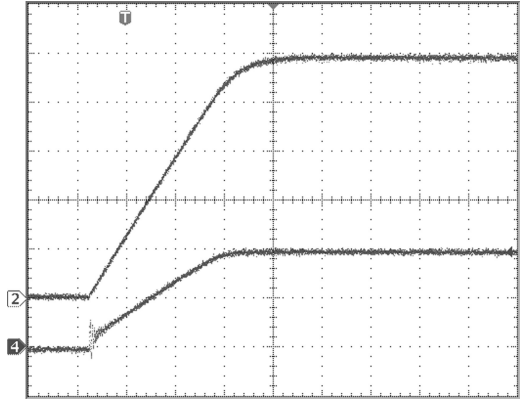
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Shutdown Supply Current vs. Input Voltage



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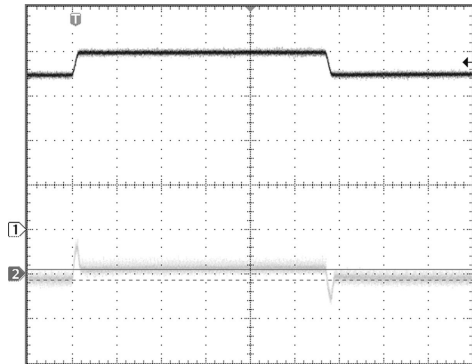
Startup Behavior, 5V Mode



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$V_{IN} = 3.6V$, Load = 200mA
 CH2: V_{OUT} ; Scale: 1V/Div, DC Coupled
 CH4: I_{IN} ; Scale: 200mA/Div, DC Coupled
 Time scale: 100µs/Div

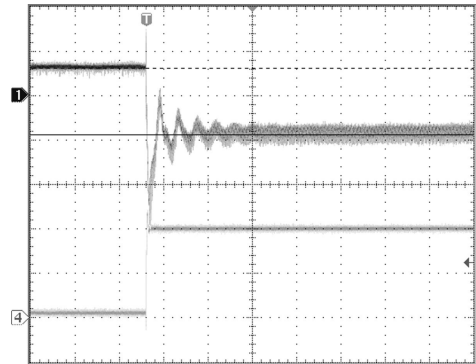
Line Step (3.5V to 4V)



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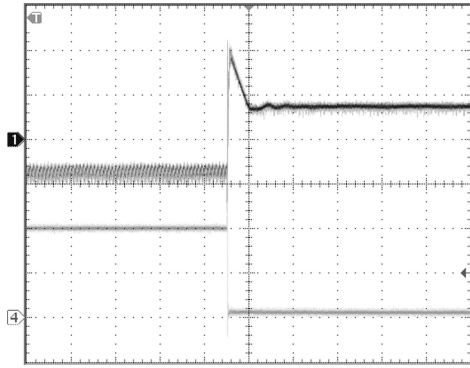
Load = 200mA, $V_{OUT} = 5V$ Mode
 CH1: V_{IN} ; Scale: 1V/Div, DC Coupled
 CH2: V_{OUT} ; Scale: 100mV/Div, AC Coupled
 Time scale: 100µs/Div

Load Step with a Li-Ion Battery, 10mA to 200mA



30033721

$V_{BATT} = 4V$, $V_{OUT} = 5V$ Mode
 CH1: V_{OUT} ; Scale: 50mV/Div, AC Coupled
 CH4: I_{OUT} ; Scale: 100mA/Div, DC Coupled
 Time scale: 10µs/Div

Load Step with a Li-Ion Battery 200mA to 10mA

30033722

 $V_{\text{BATT}} = 4\text{V}$, $V_{\text{OUT}} = 5\text{V}$ ModeCH1: V_{OUT} ; Scale: 50mV/Div, AC CoupledCH4: I_{OUT} ; Scale: 100mA/Div, DC Coupled

Time scale: 10µs/Div

Operation Description

OVERVIEW

The LM2757 is a switched capacitor converter that produces a regulated output voltage of either 5V, 4.5V or 4.1V depending on the mode selected. The core of the part is a highly efficient charge pump that utilizes fixed frequency pre-regulation to minimize ripple and power losses over wide input voltage and output current ranges. A description of the principal operational characteristics of the LM2757 is detailed in the **Circuit Description**, and **Efficiency Performance** sections. These sections refer to details in the **Block Diagram**.

CIRCUIT DESCRIPTION

The core of the LM2757 is a two-phase charge pump controlled by an internally generated non-overlapping clock. The charge pump operates by using external flying capacitors C_1 , C_2 to transfer charge from the input to the output. At input voltages below 3.9V (typ.) for the 5V mode, the LM2757 operates in a 2x gain, with the input current being equal to 2x the load current. At input voltages above 3.9V (typ.) for the 5V mode, the part utilizes a gain of 3/2x, resulting in an input current equal to 3/2 times the load current. For the 4.5V mode, the LM2757 operates in a 2x gain when the input voltage is below 3.35V (typ.) and transitions to a 3/2x gain when the input voltage is above 3.35V (typ.). For the 4.1V mode, the device utilizes the 3/2x gain for the entire input voltage range.

The two phases of the switched capacitor switching cycle will be referred to as the "phase one" and the "phase two". During phase one, one flying capacitor is charged by the input supply while the other flying capacitor is connected to the output and delivers charge to the load. After half of the switching cycle [$t = 1/(2 \times F_{SW})$], the LM2757 switches to phase two. In this configuration, the capacitor that supplied charge to the load in phase one is connected to the input to be recharged while the capacitor that had been charged in the previous phase is connected to the output to deliver charge. With this topology, output ripple is reduced by delivering charge to the output in every phase.

The LM2757 uses fixed frequency pre-regulation to regulate the output voltage. The input and output connections of the flying capacitors are made with internal MOS switches. Pre-regulation limits the gate drive of the MOS switch connected between the voltage input and the flying capacitors. Controlling the on resistance of this switch limits the amount of charge transferred into and out of each flying capacitor during the charge and discharge phases, and in turn helps to keep the output ripple very low.

EFFICIENCY PERFORMANCE

Charge-pump efficiency is derived in the following two ideal equations (supply current and other losses are neglected for simplicity):

$$E = (V_{OUT} \times I_{OUT}) \div (V_{IN} \times I_{IN}) = V_{OUT} \div (G \times V_{IN})$$

In the equations, G represents the charge pump gain. Efficiency is at its highest as $G \times V_{IN}$ approaches V_{OUT} . Refer to the efficiency graph in the **Typical Performance Characteristics** section for detailed efficiency data. The transition between gains of 3/2, and 2 are clearly distinguished by the sharp discontinuity in the efficiency curve.

ENABLE AND VOLTAGE MODE SELECTION

The LM2757 is enabled when either one of the mode select pins (M0, M1) has a logic High voltage applied to it. There are 450k Ω pulldown resistors connected internally to each of the

mode select pins. The voltage mode is selected according to the following table.

M0	M1	Output Voltage Mode
0	0	Device Shutdown, Output High Impedance
0	1	5V
1	0	4.5V
1	1	4.1V

SHUTDOWN WITH OUTPUT HIGH IMPEDANCE

The LM2757 is in shutdown mode when there is a logic Low voltage on both mode select pins (M0, M1). When in shutdown, the output of the LM2757 is high impedance, allowing an external supply to drive the output line such as in USB OTG applications. Refer to the output leakage current graph in the **Typical Performance Characteristics** section for typical leakage currents into the V_{OUT} pin, when driven by a separate supply during shutdown. Output leakage increases with temperature, with the lowest leakage occurring at -30°C and the highest leakage at 85°C (on which the graph is based).

SOFT START

The LM2757 employs soft start circuitry to prevent excessive input inrush currents during startup. At startup, the output voltage gradually rises from 0V to the nominal output voltage. This occurs in 300 μ s (typ.). Soft-start is engaged when the part is enabled.

THERMAL SHUTDOWN

Protection from damage related to overheating is achieved with a thermal shutdown feature. When the junction temperature rises to 145°C (typ.), the part switches into shutdown mode. The LM2757 disengages thermal shutdown when the junction temperature of the part is reduced to 135°C (typ.). Due to the high efficiency of the LM2757, thermal shutdown and/or thermal cycling should not be encountered when the part is operated within specified input voltage, output current, and ambient temperature operating ratings. If thermal cycling is seen under these conditions, the most likely cause is an inadequate PCB layout that does not allow heat to be sufficiently dissipated out of the device.

CURRENT LIMIT PROTECTION

The LM2757 charge pump contains current limit protection circuitry that protects the device during V_{OUT} fault conditions where excessive current is drawn. Output current is limited to 250mA (typ.).

Application Information

RECOMMENDED CAPACITOR TYPES

The LM2757 requires 4 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR, $\leq 15\text{m}\Omega$ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are not recommended for use with the LM2757 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with an X7R or X5R temperature characteristic are preferred for use with the LM2757. These capacitors have tight capacitance tolerance (as good as $\pm 10\%$) and hold their value over temperature (X7R: $\pm 15\%$ over -55°C to 125°C; X5R: $\pm 15\%$ over -55°C to 85°C).

Capacitors with a Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2757. These types of capacitors typically have wide capacitance tolerance (+80%, -20%) and vary significantly over temperature (Y5V: +22%, -82% over -30°C to +85°C range; Z5U: +22%, -56% over +10°C to +85°C range). Under some conditions, a 1 μ F-rated Y5V or Z5U capacitor could have a capacitance as low as 0.1 μ F. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2757.

Net capacitance of a ceramic capacitor decreases with increased DC bias. This degradation can result in lower capacitance than expected on the input and/or output, resulting in higher ripple voltages and currents. Using capacitors at DC bias voltages significantly below the capacitor voltage rating will usually minimize DC bias effects. Consult capacitor manufacturers for information on capacitor DC bias characteristics.

Capacitance characteristics can vary quite dramatically with different application conditions, capacitor types, and capacitor manufacturers. It is strongly recommended that the LM2757 circuit be thoroughly evaluated early in the design-in process with the mass-production capacitors of choice. This will help ensure that any such variability in capacitance does not negatively impact circuit performance.

The voltage rating of the output capacitor should be 10V or more. For example, a 10V 0603 1.0 μ F is acceptable for use with the LM2757, as long as the capacitance does not fall below a minimum of 0.5 μ F in the intended application. All other capacitors should have a voltage rating at or above the maximum input voltage of the application. The capacitors should be selected such that the capacitance on the input does not fall below 0.7 μ F, and the capacitance of the flying capacitors does not fall below 0.2 μ F.

The table below lists some leading ceramic capacitor manufacturers.

Manufacturer	Contact Information
AVX	www.avx.com
Murata	www.murata.com
Taiyo-Yuden	www.t-yuden.com
TDK	www.component.tdk.com
Vishay-Vitramon	www.vishay.com

OUTPUT CAPACITOR AND OUTPUT VOLTAGE RIPPLE

The output capacitor in the LM2757 circuit (C_{OUT}) directly impacts the magnitude of output voltage ripple. Other prominent factors also affecting output voltage ripple include input voltage, output current and flying capacitance. Due to the complexity of the regulation topology, providing equations or models to approximate the magnitude of the ripple can not be easily accomplished. But one important generalization can be made: increasing (decreasing) the output capacitance will result in a proportional decrease (increase) in output voltage ripple.

In typical high-current applications, a 1.0 μ F low-ESR ceramic output capacitor is recommended. Different output capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution. But changing the output capacitor may also require changing the flying capacitor and/or input capacitor to maintain good overall circuit performance. Performance of the LM2757 with different capacitor setups is discussed in the section **Recommended Capacitor Configurations**.

High ESR in the output capacitor increases output voltage ripple. If a ceramic capacitor is used at the output, this is usually not a concern because the ESR of a ceramic capacitor is typically very low and has only a minimal impact on ripple magnitudes. If a different capacitor type with higher ESR is used (tantalum, for example), the ESR could result in high ripple. To eliminate this effect, the net output ESR can be significantly reduced by placing a low-ESR ceramic capacitor in parallel with the primary output capacitor. The low ESR of the ceramic capacitor will be in parallel with the higher ESR, resulting in a low net ESR based on the principles of parallel resistance reduction.

INPUT CAPACITOR AND INPUT VOLTAGE RIPPLE

The input capacitor (C_{IN}) is a reservoir of charge that aids a quick transfer of charge from the supply to the flying capacitors during the charge phase of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase when the flying capacitors are connected to the input. It also filters noise on the input pin, keeping this noise out of sensitive internal analog circuitry that is biased off the input line.

Much like the relationship between the output capacitance and output voltage ripple, input capacitance has a dominant and first-order effect on input ripple magnitude. Increasing (decreasing) the input capacitance will result in a proportional decrease (increase) in input voltage ripple. Input voltage, output current, and flying capacitance also will affect input ripple levels to some degree.

In typical high-current applications, a 1.0 μ F low-ESR ceramic capacitor is recommended on the input. Different input capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution. But changing the input capacitor may also require changing the flying capacitor and/or output capacitor to maintain good overall circuit performance. Performance of the LM2757 with different capacitor setups is discussed below in **Recommended Capacitor Configurations**.

FLYING CAPACITORS

The flying capacitors (C_1 , C_2) transfer charge from the input to the output. Flying capacitance can impact both output current capability and ripple magnitudes. If flying capacitance is too small, the LM2757 may not be able to regulate the output voltage when load currents are high. On the other hand, if the flying capacitance is too large, the flying capacitor might overwhelm the input and output capacitors, resulting in increased input and output ripple.

In typical high-current applications, 0.47 μ F low-ESR ceramic capacitors are recommended for the flying capacitors. Polarized capacitors (tantalum, aluminum electrolytic, etc.) must not be used for the flying capacitor, as they could become reverse-biased during LM2757 operation.

RECOMMENDED CAPACITANCE

The data in *Table 1* can be used to assist in the selection of capacitance for each node that best balances solution size and cost with the electrical requirements of the application.

As previously discussed, input and output ripple voltages will vary with output current and input voltage. The numbers provided show expected ripple voltage with $V_{IN} = 3.6V$ and a load current of 200mA at 5V output, 100mA at 4.5V output, and 100mA at 4.1V output. The table offers a first look at approximate ripple levels and provides a comparison of different capacitance configurations, but is not intended to be a guarantee of performance. With any capacitance configuration

chosen, always verify that the performance of the ripple waveforms are suitable for the intended application. The same capacitance value must be used for all the flying capacitors.

TABLE 1. LM2757 Performance with Different Capacitor Configurations (Note 12)

Capacitor Configuration ($V_{IN} = 3.6V$)	Typical 5.0V, 200mA Output Ripple	Typical 4.5V, 100mA Output Ripple	Typical 4.1V, 100mA Output Ripple
$C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, $C_1, C_2 = 0.47\mu F$	32mV	12mV	11mV
$C_{IN} = 0.68\mu F$, $C_{OUT} = 1\mu F$, $C_1, C_2 = 0.47\mu F$	32mV	11mV	11mV
$C_{IN} = 0.68\mu F$, $C_{OUT} = 0.47\mu F$, $C_1, C_2 = 0.47\mu F$	51mV	15mV	15mV
$C_{IN} = 0.68\mu F$, $C_{OUT} = 0.47\mu F$, $C_1, C_2 = 0.22\mu F$	53mV	18mV	18mV

Note 12: Refer to the text in the Recommended Capacitor Configurations section for detailed information on the data in this table

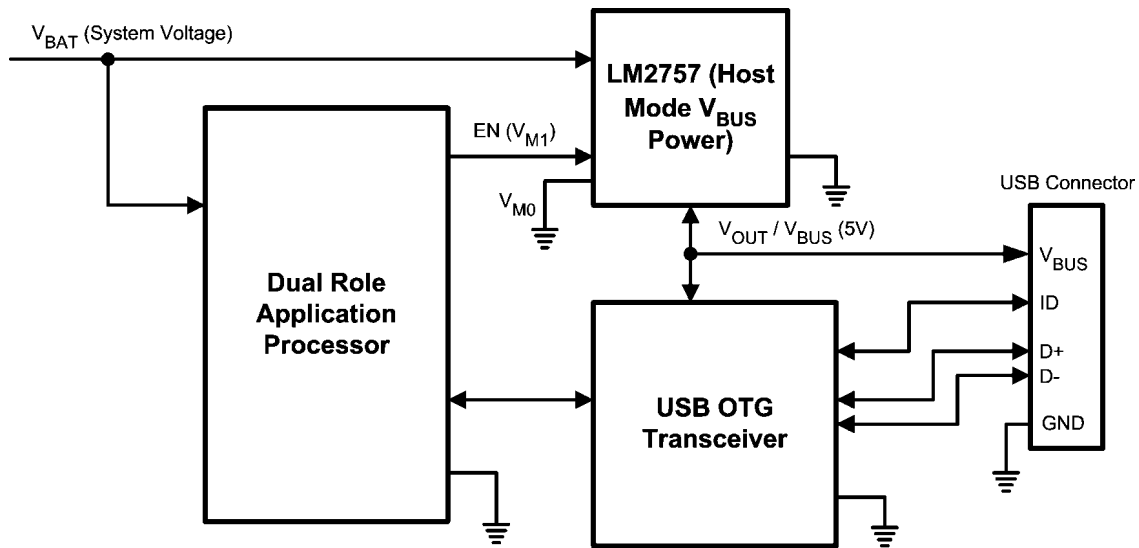
Layout Guidelines

Proper board layout will help to ensure optimal performance of the LM2757 circuit. The following guidelines are recommended:

- Place capacitors as close to the LM2757 as possible, and preferably on the same side of the board as the IC.
- Use short, wide traces to connect the external capacitors to the LM2757 to minimize trace resistance and inductance.
- Use a low resistance connection between ground and the GND pin of the LM2757. Using wide traces and/or multiple vias to connect GND to a ground plane on the board is most advantageous.

Application Circuits

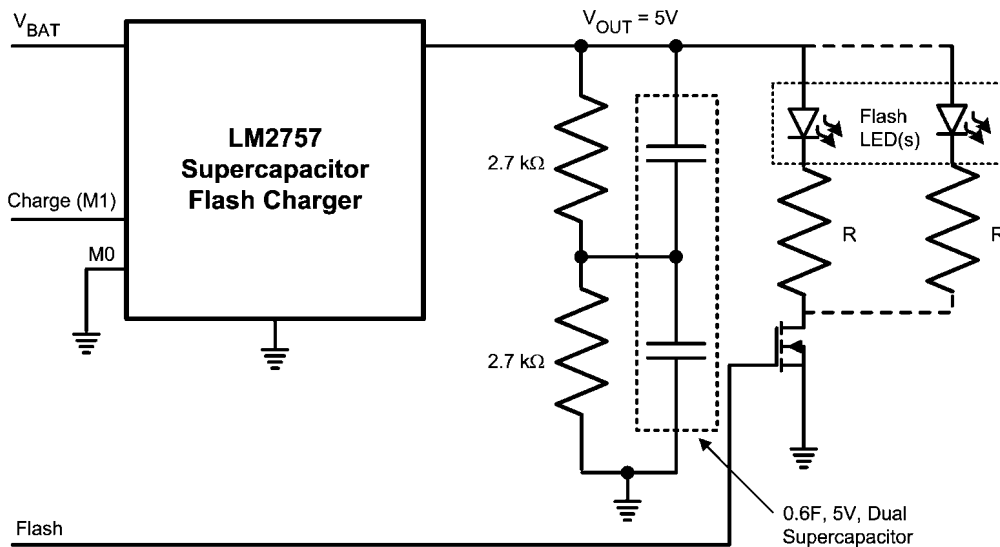
USB OTG POWER SUPPLY



30033724

The 5V output mode will normally be used for the USB OTG application. Therefore the LM2757 can be enabled/disabled by applying a logic signal on only the M1 pin while grounding the M0 pin. Depending on the USB mode of the application, the LM2757 can be enabled to drive the USB power bus line **SUPERCAPACITOR FLASH DRIVER**

(Host), or disabled to put its output in high impedance allowing an external supply to drive the bus line (Slave).



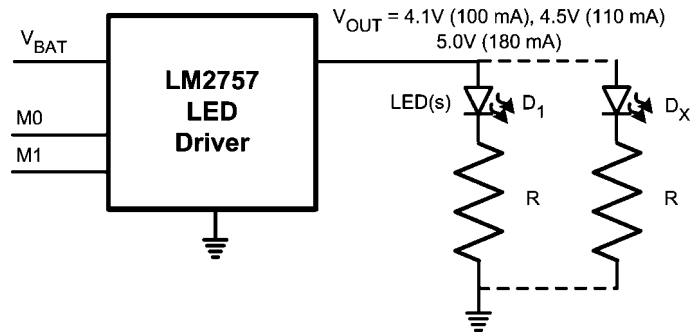
30033725

Using the 5V output voltage mode, the LM2757 can be used to charge a Supercapacitor for LED Flash applications while limiting the peak current drawn off the battery during the charge cycle. The LM2757 can be disabled for the Flash event, placing its output in high impedance with the input. In this way, all charge for the Flash LED(s) will come directly off the Supercapacitor and not load the main battery line. The LM2757 can be enabled/disabled by applying a logic signal on only the M1 pin while grounding the M0 pin.

Special consideration must be taken when using Supercapacitors for LED flash applications where the voltage on the

capacitor is charged to a fixed value. This is due to the possible power management issues that could arise as a result of the high flash current and wide tolerance ranges (V-I characteristics) of typical Flash LEDs. If the voltage across the Flash LED(s) is not managed, damage could occur where a relatively low V_f LED is overdriven or places excessive voltage across the bottom control FET. To help reduce this issue, the use of a high power current sink is advised in applications where the forward voltage specification of the Flash LED has a wide range.

LED DRIVER

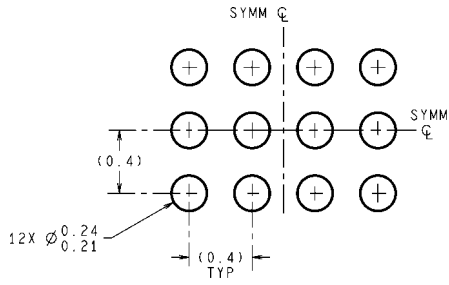


30033726

The 5.0V, 4.5V, or the 4.1V mode can be used depending on the forward voltage and load requirements of the LED application. The LM2757 can be enabled/disabled by applying the appropriate combination of logic signals on the M1 and M0

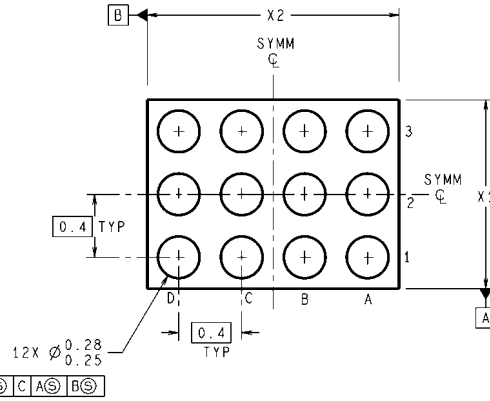
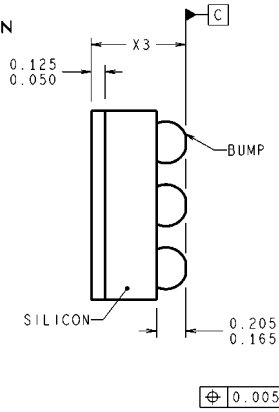
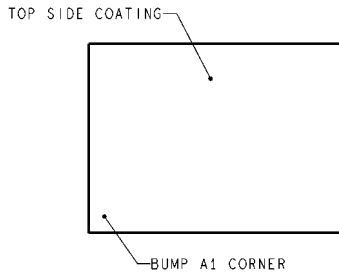
pins. LED current for each string in this application is limited by the voltage across the string's ballast resistor, which is dependent on the output voltage mode selected and the V-I profile of each LED used.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TMD12XXX (Rev B)

NSC Package TMD12AAA
Micro SMD Wafer Level Package
X1: 1215 μm +/- 30 μm
X2: 1615 μm +/- 30 μm
X3: 600 μm +/- 75 μm
Bump pitch: 0.4 mm

Notes

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