

TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

# TB62747AFG, TB62747AFNG, TB62747AFNAG, TB62747BFNAG

## 16-Output Constant Current LED Driver

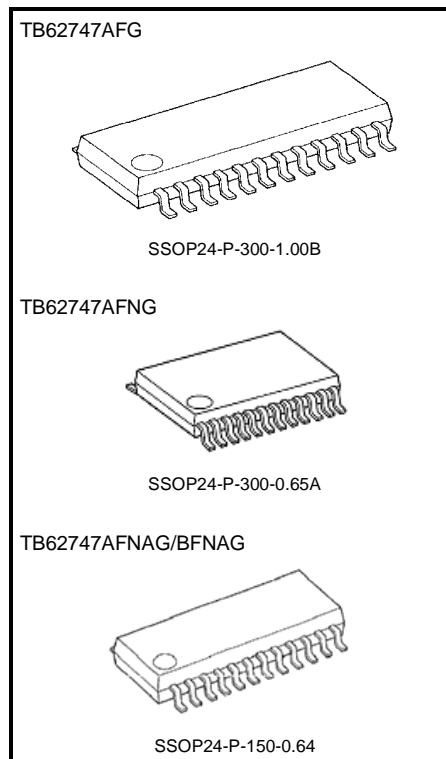
The TB62747 series is comprised of constant-current drivers designed for LEDs and LED panel displays.

The regulated current sources are designed to provide a constant current, which is adjustable through one external resistor.

The TB62747 series incorporates 16 channels of shift registers, latches, AND gates and constant-current outputs.

Fabricated using the Bi-CMOS process, the TB62747 series satisfies the system requirement of high-speed data transmission.

The TB62747 series is RoHS compatible



## Features

- Power supply voltages:  $V_{DD} = 3.3\text{ V to }5.0\text{ V}$
- 16-output built-in
- Output current setting range
  - :  $1.5\text{ to }35\text{ mA @ }V_{DD} = 3.3\text{ V, }V_O = 0.4\text{ to }1.0\text{ V}$
  - :  $1.5\text{ to }45\text{ mA @ }V_{DD} = 5.0\text{ V, }V_O = 0.4\text{ to }1.2\text{ V}$
- Constant current output voltage:  $V_O = 26\text{ V (max)}$
- Current accuracy (@  $R_{EXT} = 1.2\text{ k}\Omega, V_O = 0.4\text{ V, }V_{DD} = 3.3\text{ V, }5.0\text{ V}$ )
  - : Between outputs:  $\pm 1.5\% \text{ (max)}$
  - : Between devices:  $\pm 1.5\% \text{ (max)}$
- Fast response of output current :  $t_{wOE(L)} = 100\text{ ns (min)}$
- Control data format: serial-in, parallel-out
- Input signal voltage level: 3.3 V and 5 V CMOS interfaces (Schmitt trigger input)
- Serial data transfer rate: 25 MHz (max) @cascade connection
- Operation temperature range:  $T_{opr} = -40\text{ to }85\text{ }^\circ\text{C}$
- Power on reset (POR)
- Package
 

|              |                      |
|--------------|----------------------|
| : AFG type   | : SSOP24-P-300-1.00B |
| : AFNG type  | : SSOP24-P-300-0.65A |
| : AFNAG type | : SSOP24-P-150-0.64  |
| : BFNAG type | : SSOP24-P-150-0.64  |

### Weight

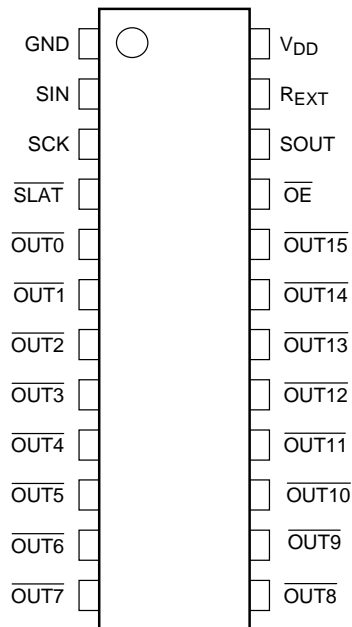
SSOP24-P-300-1.00B : 0.29 g (typ.)

SSOP24-P-300-0.65A : 0.14 g (typ.)

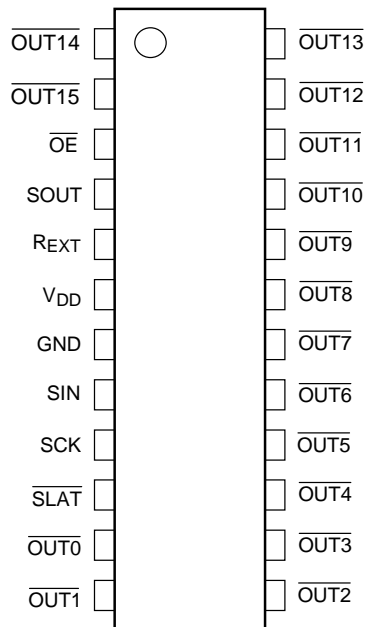
SSOP24-P-150-0.64 : 0.14 g (typ.)

**Pin Assignment (top view)**

TB62747AFG/AFNG/AFNAG

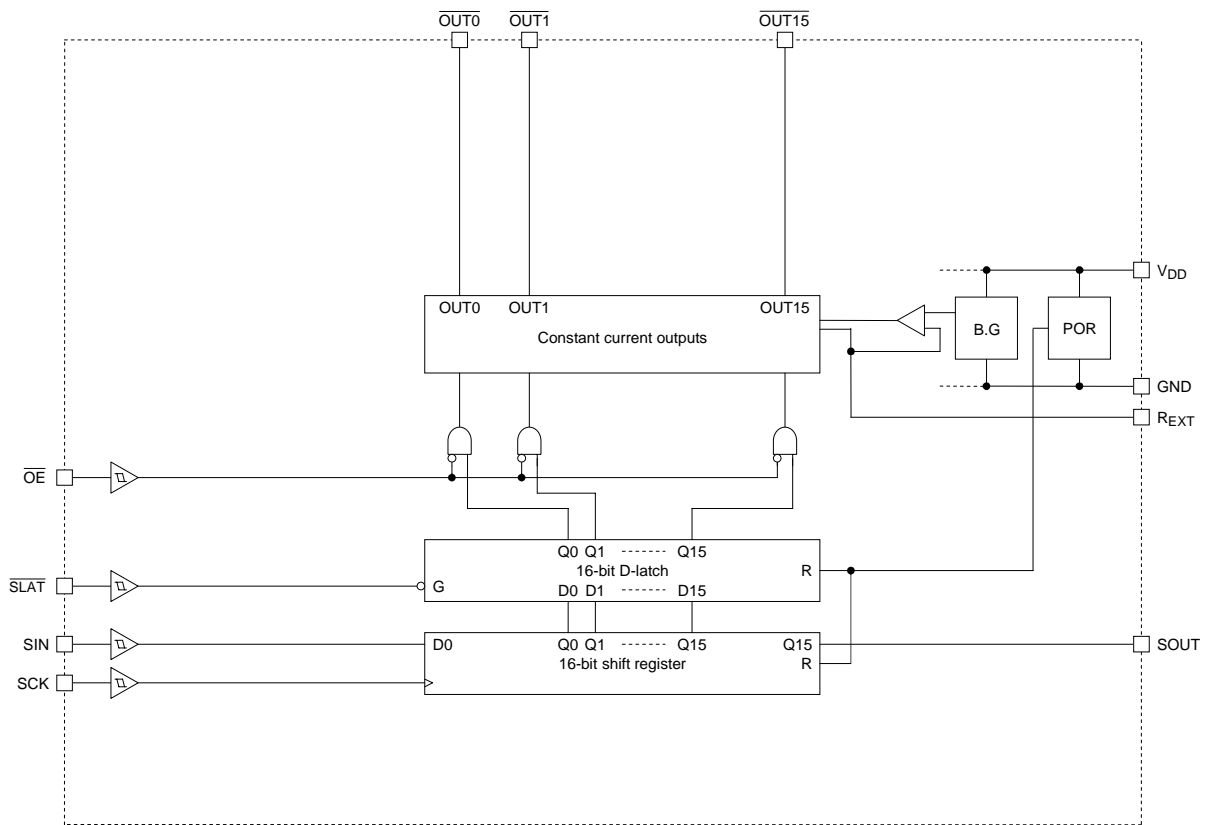


TB62747BFNAG



Note1: Short circuiting an output pin to a power supply pin (V<sub>DD</sub> or V<sub>LED</sub>\*), or short-circuiting the R<sub>EXT</sub> pin to the GND pin will likely exceed the rating, which in turn may result in smoldering and/or permanent damage. Please keep this in mind when determining the wiring layout for the power supply and GND pins.  
 \*V<sub>LED</sub>: LED power supply

**Block Diagram**



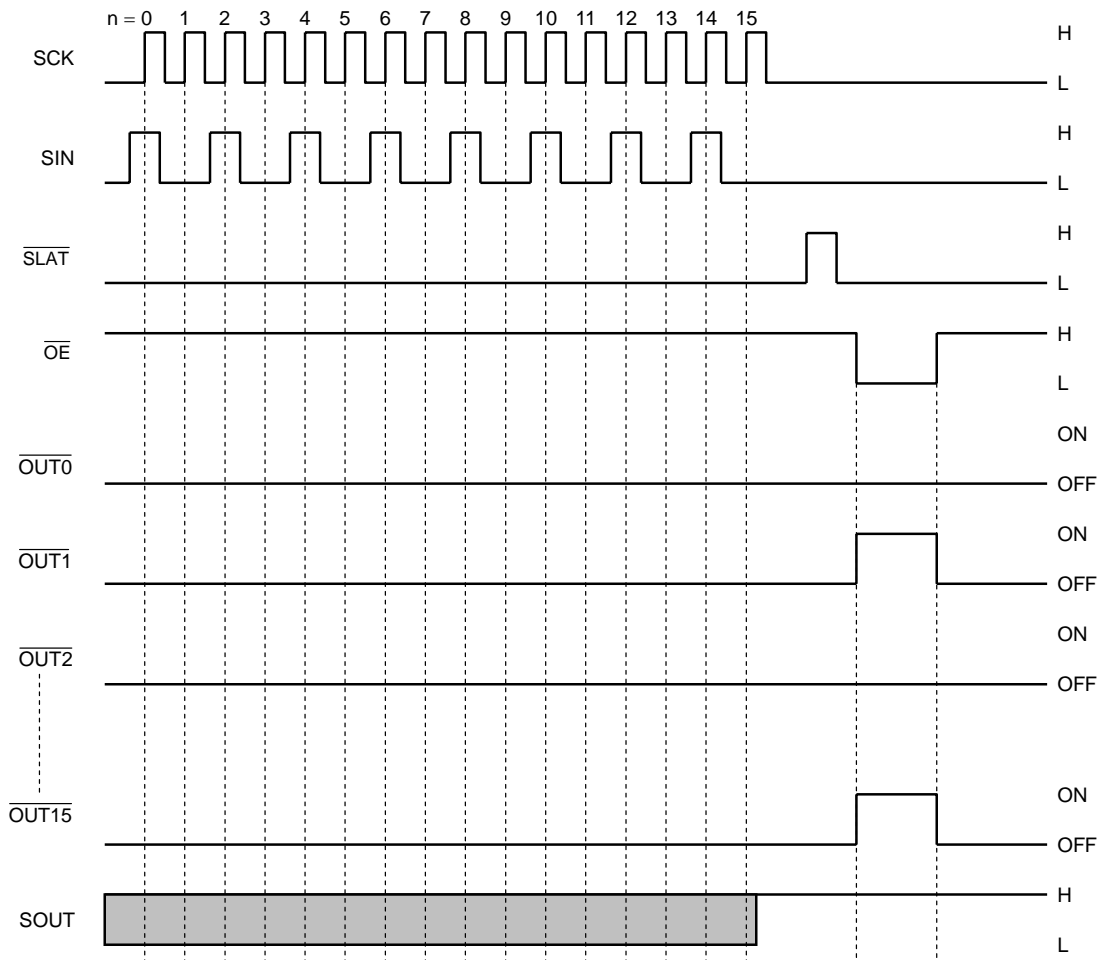
**Truth Table**

| SCK | $\overline{\text{SLAT}}$ | $\overline{\text{OE}}$ | SIN    | $\overline{\text{OUT0}} \dots \overline{\text{OUT7}} \dots \overline{\text{OUT15}}^*1$ | SOUT    |
|-----|--------------------------|------------------------|--------|--|---------|
|     | H                        | L                      | Dn     | Dn ... Dn - 7 ... Dn - 15  | Dn - 15 |
|     | L                        | L                      | Dn + 1 | No Change  | Dn - 14 |
|     | H                        | L                      | Dn + 2 | Dn + 2 ... Dn - 5 ... Dn - 13  | Dn - 13 |
|     | -*2                      | L                      | Dn + 3 | Dn + 2 ... Dn - 5 ... Dn - 13  | Dn - 13 |
|     | -*2                      | H                      | Dn + 3 | OFF  | Dn - 13 |

Note1: When  $\overline{\text{OUT0}}$  to  $\overline{\text{OUT15}}$  output pins are set to "H" the respective output will be ON and when set to "L" the respective output will be OFF.

Note2: "-\*" is irrelevant to the truth table.

**Timing Diagram**



Note 1: The latch circuit is a leveled-latch circuit. Please exercise precaution as it is not triggered-latch circuit.

Note 2: Keep the  $\overline{\text{SLAT}}$  pin is set to "L" to enable the latch circuit to hold data. In addition, when the  $\overline{\text{SLAT}}$  pin is set to "H" the latch circuit does not hold data. The data will instead pass onto output.

When the  $\overline{\text{OE}}$  pin is set to "L" the  $\overline{\text{OUT0}}$  to  $\overline{\text{OUT15}}$  output pins will go ON and OFF in response to the data. In addition, when the  $\overline{\text{OE}}$  pin is set to "H" all the output pins will be forced OFF regardless of the data.

**Pin Functions**

| Pin No               |       | Pin Name                  | I/O | Function   |
|----------------------|-------|---------------------------|-----|--|
| AFG<br>AFNG<br>AFNAG | BFNAG |                           |     |  |
| 1                    | 7     | GND                       | —   | The ground pin.  |
| 2                    | 8     | SIN                       | I   | The serial data input pin.   |
| 3                    | 9     | SCK                       | I   | The serial data transfer clock input pin.  |
| 4                    | 10    | $\overline{\text{SLAT}}$  | I   | The latch signal input pin.<br>Data is saved at L level.   |
| 5                    | 11    | $\overline{\text{OUT0}}$  | O   | A sink type constant current output pin.   |
| 6                    | 12    | $\overline{\text{OUT1}}$  | O   | A sink type constant current output pin.   |
| 7                    | 13    | $\overline{\text{OUT2}}$  | O   | A sink type constant current output pin.   |
| 8                    | 14    | $\overline{\text{OUT3}}$  | O   | A sink type constant current output pin.   |
| 9                    | 15    | $\overline{\text{OUT4}}$  | O   | A sink type constant current output pin.   |
| 10                   | 16    | $\overline{\text{OUT5}}$  | O   | A sink type constant current output pin.   |
| 11                   | 17    | $\overline{\text{OUT6}}$  | O   | A sink type constant current output pin.   |
| 12                   | 18    | $\overline{\text{OUT7}}$  | O   | A sink type constant current output pin.   |
| 13                   | 19    | $\overline{\text{OUT8}}$  | O   | A sink type constant current output pin.   |
| 14                   | 20    | $\overline{\text{OUT9}}$  | O   | A sink type constant current output pin.   |
| 15                   | 21    | $\overline{\text{OUT10}}$ | O   | A sink type constant current output pin.   |
| 16                   | 22    | $\overline{\text{OUT11}}$ | O   | A sink type constant current output pin.   |
| 17                   | 23    | $\overline{\text{OUT12}}$ | O   | A sink type constant current output pin.   |
| 18                   | 24    | $\overline{\text{OUT13}}$ | O   | A sink type constant current output pin.   |
| 19                   | 1     | $\overline{\text{OUT14}}$ | O   | A sink type constant current output pin.   |
| 20                   | 2     | $\overline{\text{OUT15}}$ | O   | A sink type constant current output pin.   |
| 21                   | 3     | $\overline{\text{OE}}$    | I   | The constant current output enable signal input pin.<br>During the "H" level, the output will be forced off. |
| 22                   | 4     | SOUT                      | O   | The serial data output pin.  |
| 23                   | 5     | R <sub>EXT</sub>          | —   | The constant current value setting resistor connection pin.  |
| 24                   | 6     | V <sub>DD</sub>           | —   | The power supply input pin.  |

**Absolute Maximum Ratings (T<sub>a</sub> = 25°C)**

| Characteristics       | Symbol            | Rating *1  | Unit |
|-----------------------|-------------------|--|------|
| Power supply voltage  | V <sub>DD</sub>   | -0.4 to 6.0  | V    |
| Output current        | I <sub>O</sub>    | 55   | mA   |
| Logic input voltage   | V <sub>IN</sub>   | -0.3 to V <sub>DD</sub> + 0.3 *2                                     | V    |
| Output voltage        | V <sub>O</sub>    | -0.3 to 26   | V    |
| Operating temperature | T <sub>opr</sub>  | -40 to 85  | °C   |
| Storage temperature   | T <sub>stg</sub>  | -55 to 150   | °C   |
| Thermal resistance    | Rth(j-a)          | 94 (AFG) *3, 120 (AFNG) *3, 80.07(AFNAG/BFNAG)<br>When mounted PCB   | °C/W |
| Power dissipation     | P <sub>D</sub> *4 | 1.32 (AFG) *3, 1.04 (AFNG) *3, 1.56(AFNAG/BFNAG)<br>When mounted PCB | W    |

Note1: Voltage is ground referenced.

Note2: However, do not exceed 6V.

Note3: PCB condition 76.2 x 114.3 x 1.6 mm, Cu 30% (SEMI conforming)

Note4: The power dissipation decreases the reciprocal of the saturated thermal resistance (1/ Rth(j-a)) for each degree (1°C) that the ambient temperature is exceeded (T<sub>a</sub> = 25°C).

**Operating Conditions**

**DC Items (Unless otherwise specified, V<sub>DD</sub> = 3.0 to 5.5 V, T<sub>a</sub> = -40°C to 85°C)**

| Characteristics                | Symbol              | Test Conditions  | Min                   | Typ. | Max                   | Unit |
|--------------------------------|---------------------|--|-----------------------|------|-----------------------|------|
| Power supply voltage           | V <sub>DD</sub>     | —  | 3.0                   | —    | 5.5                   | V    |
| Output voltage when OFF        | V <sub>O (ON)</sub> | $\overline{OUTn}$  | 0.4                   | —    | 4.0                   | V    |
| High level logic input voltage | V <sub>IH</sub>     | SIN,SCK, $\overline{SLAT}$ , $\overline{OE}$                               | 0.7 × V <sub>DD</sub> | —    | V <sub>DD</sub>       | V    |
| Low level logic input voltage  | V <sub>IL</sub>     | SIN,SCK, $\overline{SLAT}$ , $\overline{OE}$                               | GND                   | —    | 0.3 × V <sub>DD</sub> | V    |
| High level SOUT output current | I <sub>OH</sub>     | —  | —                     | —    | -1                    | mA   |
| Low level SOUT output current  | I <sub>OL</sub>     | —  | —                     | —    | 1                     | mA   |
| Constant current output        | I <sub>O1</sub>     | $\overline{OUTn}$ , V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 0.4 to 1.0 V | 1.5                   | —    | 35                    | mA   |
|                                | I <sub>O2</sub>     | $\overline{OUTn}$ , V <sub>DD</sub> = 5.0 V, V <sub>O</sub> = 0.4 to 1.2 V | 1.5                   | —    | 45                    |      |

**AC Items (Unless otherwise specified, V<sub>DD</sub> = 3.0 to 5.5 V, T<sub>a</sub> = -40°C to 85°C)**

| Characteristics                | Symbol              | Test Circuits | Test Conditions | Min | Typ. | Max | Unit |
|--------------------------------|---------------------|---------------|-----------------|-----|------|-----|------|
| Serial data transfer frequency | f <sub>SCK</sub>    | 6             | —               | —   | —    | 25  | MHz  |
| Hold time                      | t <sub>HOLD1</sub>  | 6             | —               | 5   | —    | —   | ns   |
|                                | t <sub>HOLD2</sub>  | 6             | —               | 5   | —    | —   | ns   |
| Setup time                     | t <sub>SETUP1</sub> | 6             | —               | 5   | —    | —   | ns   |
|                                | t <sub>SETUP2</sub> | 6             | —               | 5   | —    | —   | ns   |
| Maximum clock rise time        | t <sub>r</sub>      | 6             | *1              | —   | —    | 500 | ns   |
| Maximum clock fall time        | t <sub>f</sub>      | 6             | *1              | —   | —    | 500 | ns   |

Note1: If the device is connected in a cascade and the tr/tf of the clock waveform increases due to deceleration of the clock waveform, it may not be possible to achieve the timing required for data transfer. Please keep these timing conditions in mind when designing your application.

**Electrical Characteristics (Unless otherwise specified,  $V_{DD} = 3.3V$ ,  $T_a = 25^\circ C$ )**

| Characteristics                                  | Symbol                  | Test Circuits | Test Conditions  | Min            | Typ.    | Max       | Unit          |
|--|-------------------------|---------------|--|----------------|---------|-----------|---------------|
| High level logic output voltage                  | $V_{OH}$                | 1             | $I_{OH} = -1 \text{ mA}$   | $V_{DD} - 0.4$ | —       | —         | V             |
| Low level logic output voltage                   | $V_{OL}$                | 1             | $I_{OL} = +1 \text{ mA}$   | —              | —       | 0.4       | V             |
| High level logic input current                   | $I_{IH}$                | 2             | $V_{IN} = V_{DD}, \overline{OE}, \text{SIN}, \text{SCK}$   | —              | —       | 1         | $\mu\text{A}$ |
| Low level logic input current                    | $I_{IL}$                | 3             | $V_{IN} = \text{GND}, \overline{\text{SLAT}}, \text{SIN}, \text{SCK}$  | —              | —       | -1        | $\mu\text{A}$ |
| Power supply current                             | $I_{DD1}$               | 4             | $V_O = 25 \text{ V}, R_{EXT} = \text{OPEN}, \text{SCK} = \text{"L"}, \overline{OE} = \text{"H"}$                   | —              | —       | 1.0       | mA            |
|  | $I_{DD2}$               | 4             | $R_{EXT} = 1.2 \text{ k}\Omega, \text{All output off}$   | —              | —       | 4.0       | mA            |
|  | $I_{DD3}$               | 4             | $R_{EXT} = 1.2 \text{ k}\Omega, \text{All output on}$  | —              | —       | 8.0       | mA            |
| Output current                                   | $I_O$                   | 5             | $V_{DD} = 3.3 \text{ V}, V_O = 0.4 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$                 | —              | 14      | —         | mA            |
| Constant current error(Ch to Ch)                 | $\Delta I_O$            | 5             | $V_{DD} = 3.3 \text{ V}, V_O = 0.4 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$                 | —              | $\pm 1$ | $\pm 1.5$ | %             |
| Constant current error(IC to IC)                 | $\Delta I_O(\text{IC})$ | 5             | $V_{DD} = 3.3 \text{ V}, V_O = 0.4 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$                 | —              | $\pm 1$ | $\pm 1.5$ | %             |
| Output OFF leak current                          | $I_{OK}$                | 5             | $V_{DD} = 3.3 \text{ V}, V_O = 25 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$                  | —              | —       | 0.5       | $\mu\text{A}$ |
| Constant current power supply voltage regulation | $\%V_{DD}$              | 5             | $V_{DD} = 3.0 \text{ to } 3.6 \text{ V}, V_O = 0.4 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$ | —              | $\pm 1$ | $\pm 2$   | %             |
| Constant current output voltage regulation       | $\%V_O$                 | 5             | $V_{DD} = 3.3 \text{ V}, V_O = 0.4 \text{ to } 3.0 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$ | —              | $\pm 1$ | —         | %/V           |
| Pull-up resistor                                 | $R_{UP}$                | 3             | $\overline{OE}$  | 250            | 500     | 800       | k $\Omega$    |
| Pull-down resistor                               | $R_{DOWN}$              | 2             | $\overline{\text{SLAT}}$   | 250            | 500     | 800       | k $\Omega$    |

**Electrical Characteristics (Unless otherwise specified,  $V_{DD} = 5.0V$ ,  $T_a = 25^\circ C$ )**

| Characteristics                                  | Symbol                  | Test Circuits | Test Conditions  | Min            | Typ.    | Max       | Unit          |
|--|-------------------------|---------------|--|----------------|---------|-----------|---------------|
| High level logic output voltage                  | $V_{OH}$                | 1             | $I_{OH} = -1 \text{ mA}$   | $V_{DD} - 0.4$ | —       | —         | V             |
| Low level logic output voltage                   | $V_{OL}$                | 1             | $I_{OL} = +1 \text{ mA}$   | —              | —       | 0.4       | V             |
| High level logic input current                   | $I_{IH}$                | 2             | $V_{IN} = V_{DD}, \overline{OE}, \text{SIN}, \text{SCK}$   | —              | —       | 1         | $\mu\text{A}$ |
| Low level logic input current                    | $I_{IL}$                | 3             | $V_{IN} = \text{GND}, \overline{\text{SLAT}}, \text{SIN}, \text{SCK}$  | —              | —       | -1        | $\mu\text{A}$ |
| Power supply current                             | $I_{DD1}$               | 4             | $V_O = 25 \text{ V}, R_{EXT} = \text{OPEN}, \text{SCK} = \text{"L"}, \overline{OE} = \text{"H"}$                   | —              | —       | 1.0       | mA            |
|  | $I_{DD2}$               | 4             | $R_{EXT} = 1.2 \text{ k}\Omega, \text{All output off}$   | —              | —       | 4.5       | mA            |
|  | $I_{DD3}$               | 4             | $R_{EXT} = 1.2 \text{ k}\Omega, \text{All output on}$  | —              | —       | 8.0       | mA            |
| Output current                                   | $I_O$                   | 5             | $V_{DD} = 5.0 \text{ V}, V_O = 0.4 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$                 | —              | 14      | —         | mA            |
| Constant current error(Ch to Ch)                 | $\Delta I_O$            | 5             | $V_{DD} = 5.0 \text{ V}, V_O = 0.4 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$                 | —              | $\pm 1$ | $\pm 1.5$ | %             |
| Constant current error(IC to IC)                 | $\Delta I_O(\text{IC})$ | 5             | $V_{DD} = 5.0 \text{ V}, V_O = 0.4 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$                 | —              | $\pm 1$ | $\pm 1.5$ | %             |
| Output OFF leak current                          | $I_{OK}$                | 5             | $V_{DD} = 5.0 \text{ V}, V_O = 25 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$                  | —              | —       | 0.5       | $\mu\text{A}$ |
| Constant current power supply voltage regulation | $\%V_{DD}$              | 5             | $V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, V_O = 0.4 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$ | —              | $\pm 1$ | $\pm 2$   | %             |
| Constant current output voltage regulation       | $\%V_O$                 | 5             | $V_{DD} = 5.0 \text{ V}, V_O = 0.4 \text{ to } 3.0 \text{ V}, R_{EXT} = 1.2 \text{ k}\Omega, \text{OUT0 to OUT15}$ | —              | $\pm 1$ | —         | %/V           |
| Pull-up resistor                                 | $R_{UP}$                | 3             | $\overline{OE}$  | 250            | 500     | 800       | k $\Omega$    |
| Pull-down resistor                               | $R_{DOWN}$              | 2             | $\overline{\text{SLAT}}$   | 250            | 500     | 800       | k $\Omega$    |

**Switching Characteristics (Unless otherwise specified, V<sub>DD</sub> = 3.3V, T<sub>a</sub> = 25°C)**

| Characteristics        |   | Symbol            | Test Circuits                           | Test Conditions  | Min | Typ. | Max | Unit |
|------------------------|---|-------------------|---|--|-----|------|-----|------|
| Propagation delay time | SCK- $\overline{\text{OUT0}}$                     | t <sub>pLH1</sub> | 6                                       | $\overline{\text{SLAT}} = \text{"H"}, \overline{\text{OE}} = \text{"L"}$ | —   | 20   | 300 | ns   |
|                        | $\overline{\text{SLAT}} - \overline{\text{OUT0}}$ | t <sub>pLH2</sub> | 6                                       | $\overline{\text{OE}} = \text{"L"}$                                      | —   | 20   | 300 | ns   |
|                        | $\overline{\text{OE}} - \overline{\text{OUT0}}$   | t <sub>pLH3</sub> | 6                                       | $\overline{\text{SLAT}} = \text{"H"}$                                    | —   | 20   | 300 | ns   |
|                        | SCK-SOUT  | t <sub>pLH</sub>  | 6                                       | CL=10.5 pF   | 10  | 20   | 35  | ns   |
|                        | SCK- $\overline{\text{OUT0}}$                     | t <sub>pHL1</sub> | 6                                       | $\overline{\text{SLAT}} = \text{"H"}, \overline{\text{OE}} = \text{"L"}$ | —   | 30   | 340 | ns   |
|                        | $\overline{\text{SLAT}} - \overline{\text{OUT0}}$ | t <sub>pHL2</sub> | 6                                       | $\overline{\text{OE}} = \text{"L"}$                                      | —   | 70   | 340 | ns   |
|                        | $\overline{\text{OE}} - \overline{\text{OUT0}}$   | t <sub>pHL3</sub> | 6                                       | $\overline{\text{SLAT}} = \text{"H"}$                                    | —   | 70   | 340 | ns   |
|                        | SCK-SOUT  | t <sub>pHL</sub>  | 6                                       | CL=10.5 pF   | 10  | 20   | 35  | ns   |
| Output rise time       | t <sub>or</sub>                                   | 6                 | 10 to 90% of voltage waveform           | —  | 20  | 90   | ns  |      |
| Output fall time       | t <sub>of</sub>                                   | 6                 | 90 to 10% of voltage waveform           | —  | 25  | 180  | ns  |      |
| Enable pulse width     | t <sub>wOE(L)</sub>                               | 6                 | $\overline{\text{OE}} = \text{"L"} * 1$ | 100  | —   | —    | ns  |      |
| Clock pulse width      | t <sub>wSCK</sub>                                 | 6                 | SCK = "H" or "L"                        | 20   | —   | —    | ns  |      |
| Latch pulse width      | t <sub>wSLAT</sub>                                | 6                 | $\overline{\text{SLAT}} = \text{"H"}$   | 20   | —   | —    | ns  |      |

Note1: At the condition of t<sub>wOE(H)</sub> = 250ns or more

**Switching Characteristics (Unless otherwise specified, V<sub>DD</sub> = 5.0V, T<sub>a</sub> = 25°C)**

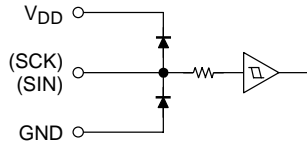
| Characteristics        |   | Symbol            | Test Circuits                           | Test Conditions  | Min | Typ. | Max | Unit |
|------------------------|---|-------------------|---|--|-----|------|-----|------|
| Propagation delay time | SCK- $\overline{\text{OUT0}}$                     | t <sub>pLH1</sub> | 6                                       | $\overline{\text{SLAT}} = \text{"H"}, \overline{\text{OE}} = \text{"L"}$ | —   | 20   | 300 | ns   |
|                        | $\overline{\text{SLAT}} - \overline{\text{OUT0}}$ | t <sub>pLH2</sub> | 6                                       | $\overline{\text{OE}} = \text{"L"}$                                      | —   | 20   | 300 | ns   |
|                        | $\overline{\text{OE}} - \overline{\text{OUT0}}$   | t <sub>pLH3</sub> | 6                                       | $\overline{\text{SLAT}} = \text{"H"}$                                    | —   | 20   | 30  | ns   |
|                        | SCK-SOUT  | t <sub>pLH</sub>  | 6                                       | CL=10.5 pF   | 10  | 20   | 35  | ns   |
|                        | SCK- $\overline{\text{OUT0}}$                     | t <sub>pHL1</sub> | 6                                       | $\overline{\text{SLAT}} = \text{"H"}, \overline{\text{OE}} = \text{"L"}$ | —   | 30   | 340 | ns   |
|                        | $\overline{\text{SLAT}} - \overline{\text{OUT0}}$ | t <sub>pHL2</sub> | 6                                       | $\overline{\text{OE}} = \text{"L"}$                                      | —   | 70   | 340 | ns   |
|                        | $\overline{\text{OE}} - \overline{\text{OUT0}}$   | t <sub>pHL3</sub> | 6                                       | $\overline{\text{SLAT}} = \text{"H"}$                                    | —   | 70   | 340 | ns   |
|                        | SCK-SOUT  | t <sub>pHL</sub>  | 6                                       | CL=10.5 pF   | 10  | 20   | 35  | ns   |
| Output rise time       | t <sub>or</sub>                                   | 6                 | 10 to 90% of voltage waveform           | —  | 20  | 90   | ns  |      |
| Output fall time       | t <sub>of</sub>                                   | 6                 | 90 to 10% of voltage waveform           | —  | 25  | 180  | ns  |      |
| Enable pulse width     | t <sub>wOE(L)</sub>                               | 6                 | $\overline{\text{OE}} = \text{"L"} * 1$ | 100  | —   | —    | ns  |      |
| Clock pulse width      | t <sub>wSCK</sub>                                 | 6                 | SCK = "H" or "L"                        | 20   | —   | —    | ns  |      |
| Latch pulse width      | t <sub>wSLAT</sub>                                | 6                 | $\overline{\text{SLAT}} = \text{"H"}$   | 20   | —   | —    | ns  |      |

Note1: At the condition of t<sub>wOE(H)</sub> = 250ns or more

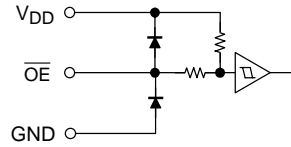


## I/O Equivalent Circuits

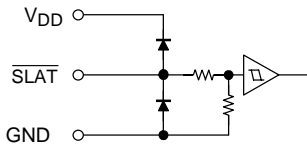
### 1. SCK, SIN



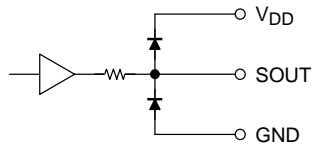
### 2. $\overline{OE}$



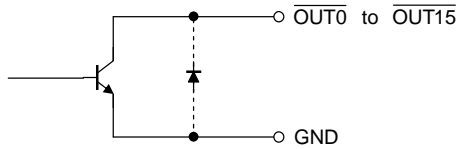
### 3. $\overline{SLAT}$



### 4. SOUT

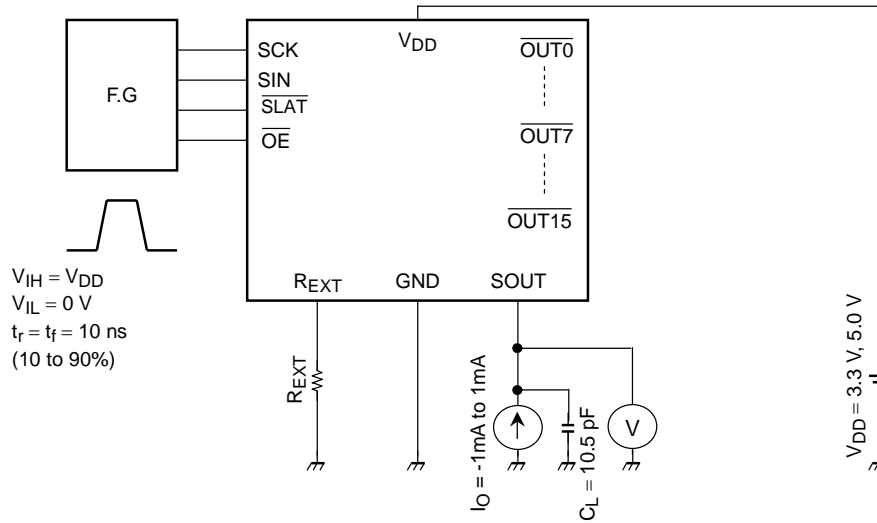


### 5. $\overline{OUT0}$ to $\overline{OUT15}$

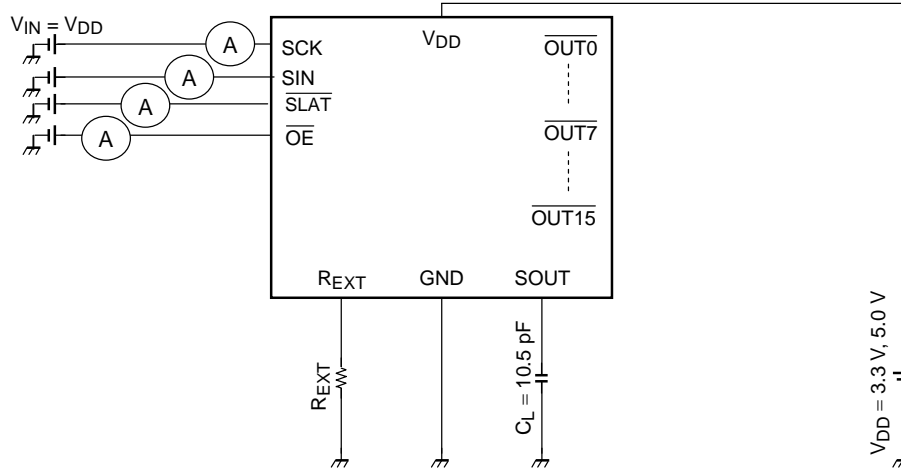


## Test Circuits

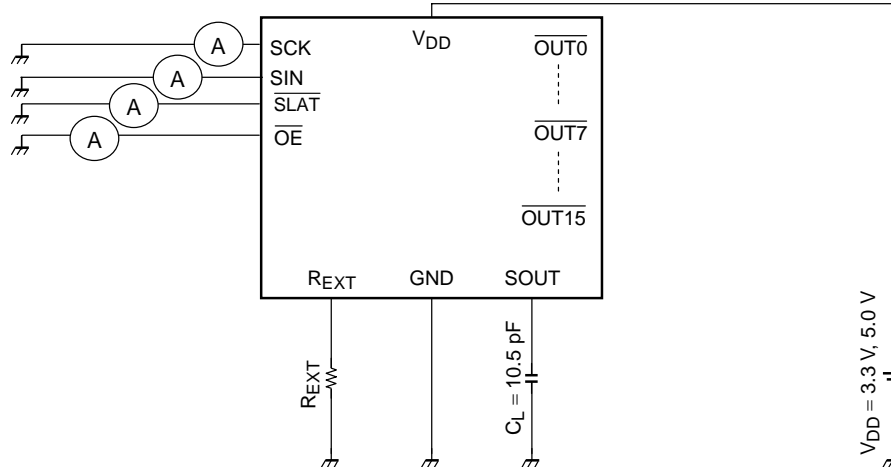
Test Circuit1: High level logic input voltage / Low level logic input voltage



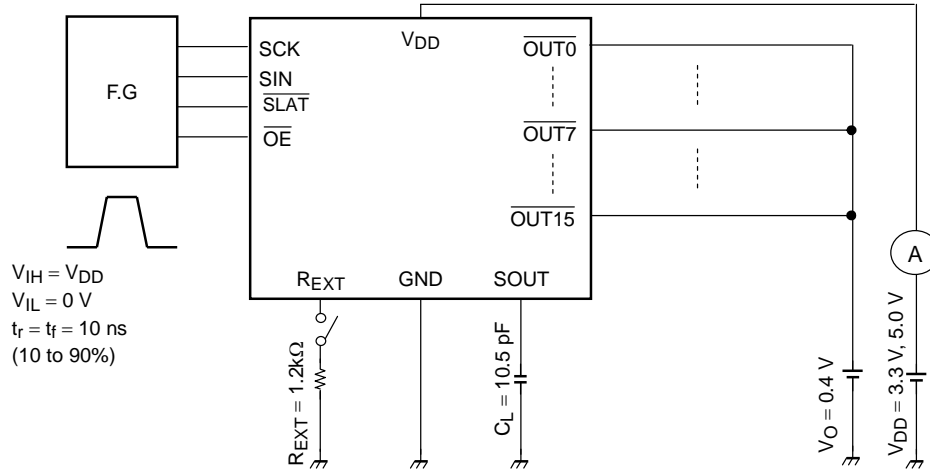
Test Circuit2: High level logic input current / Pull-down resistor



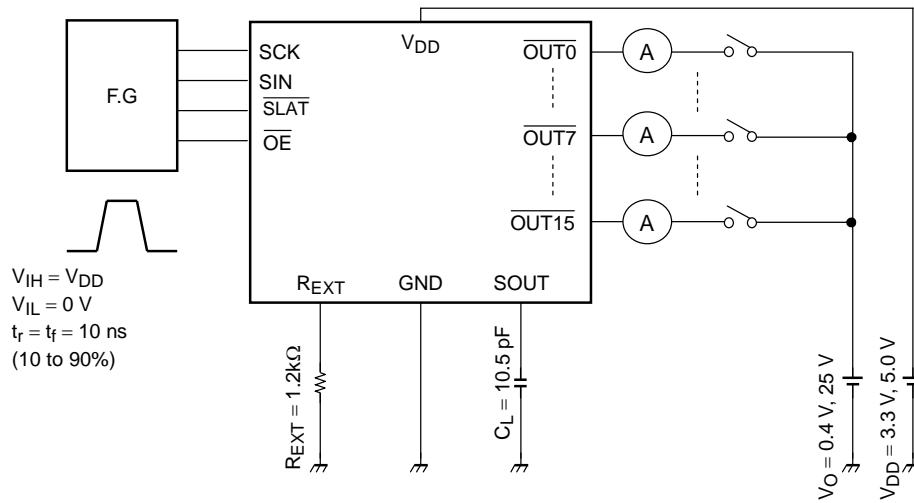
Test Circuit3: Low level logic input current / Pull-up resistor



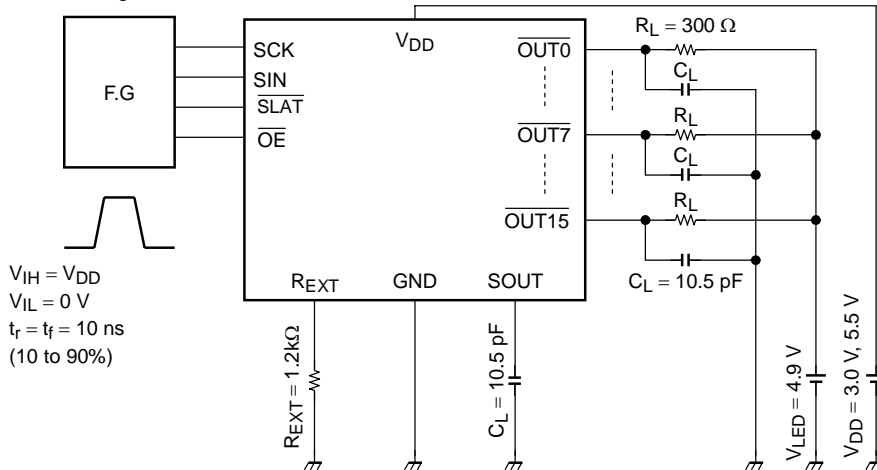
Test Circuit4: Power supply current



Test Circuit5: Constant current output / Output OFF leak current / Constant current error  
Constant current power supply voltage regulation / Constant current output voltage regulation

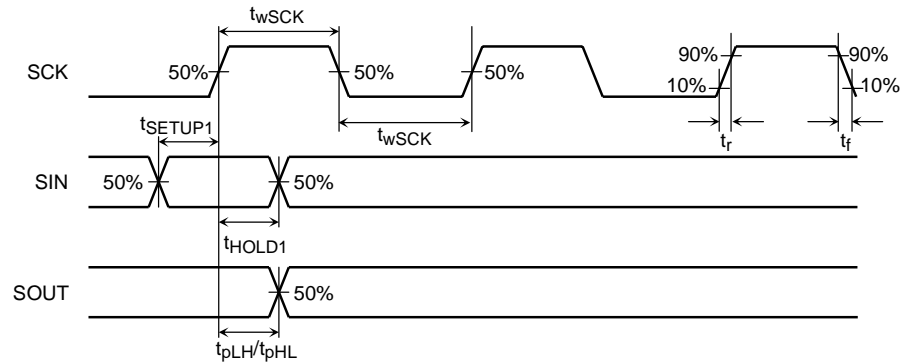


Test Circuit6: Switching Characteristics

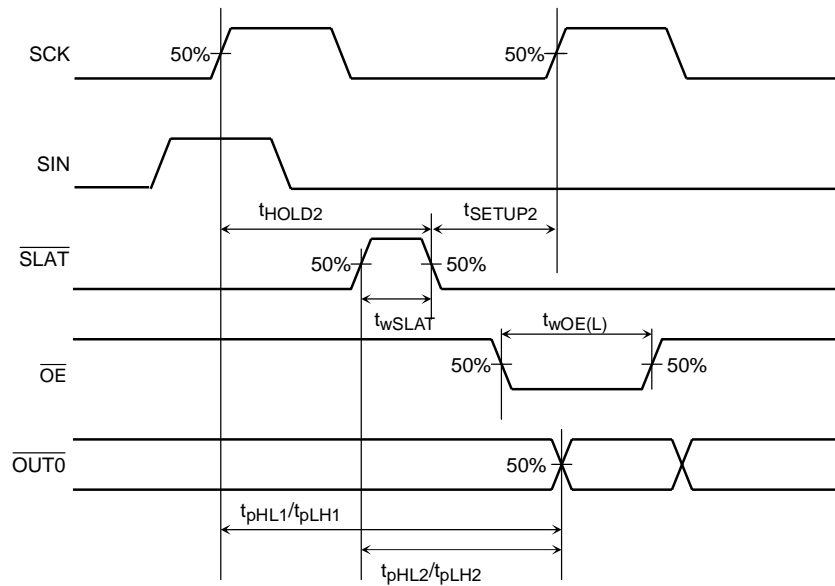


## Timing Waveforms

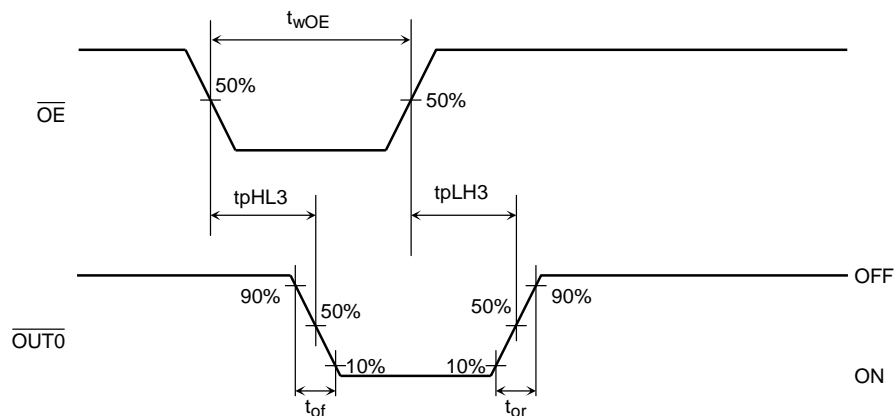
### 1. SCK, SIN, SOUT



### 2. SCK, SIN, $\overline{SLAT}$ , $\overline{OE}$ , $\overline{OUT0}$



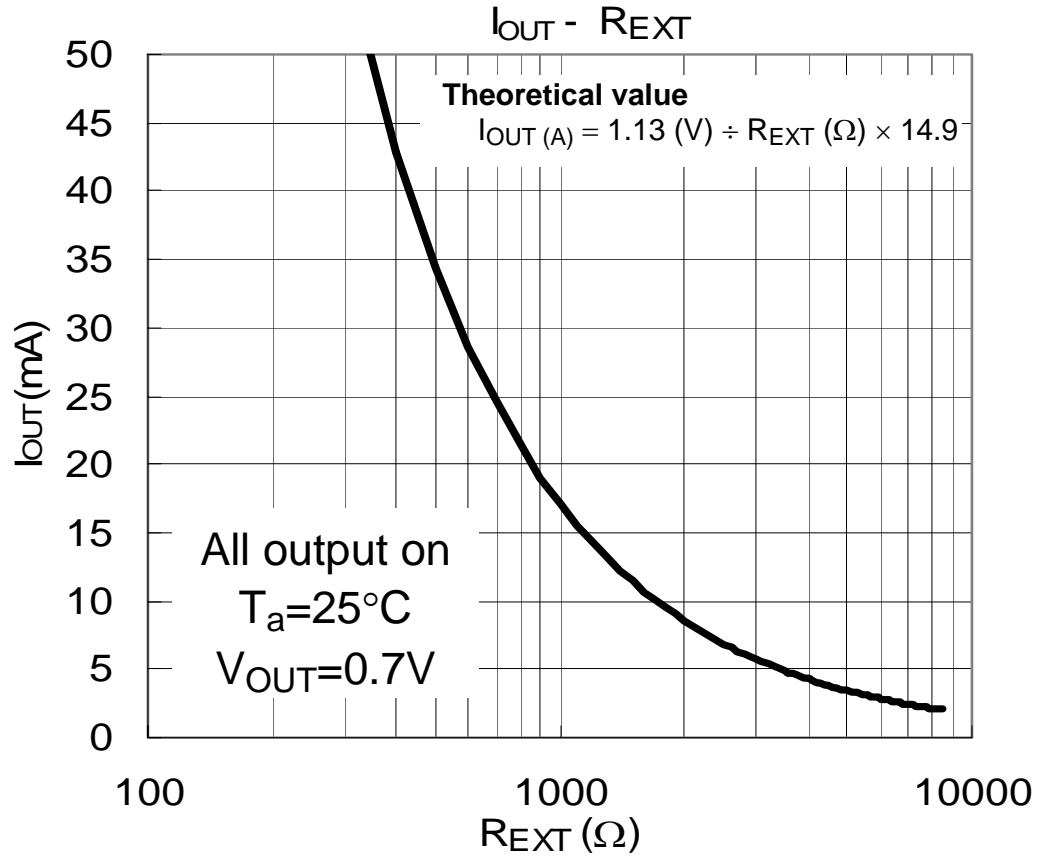
### 3. $\overline{OE}$ , $\overline{OUT0}$



**Reference data**

\*This data is provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design.

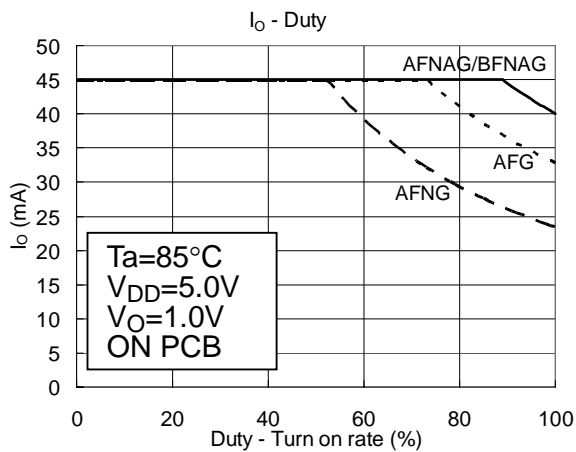
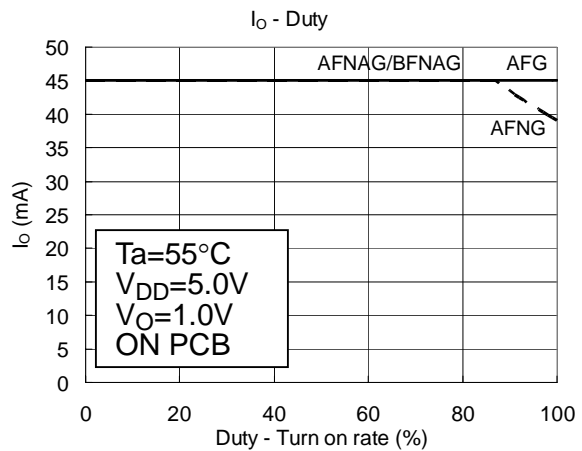
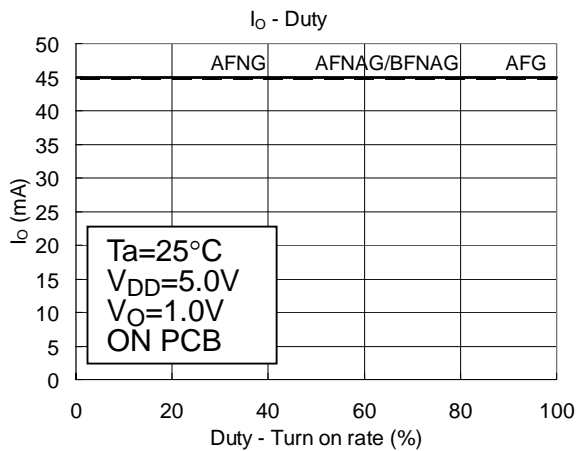
**Output Current – R<sub>EXT</sub> Resistor**



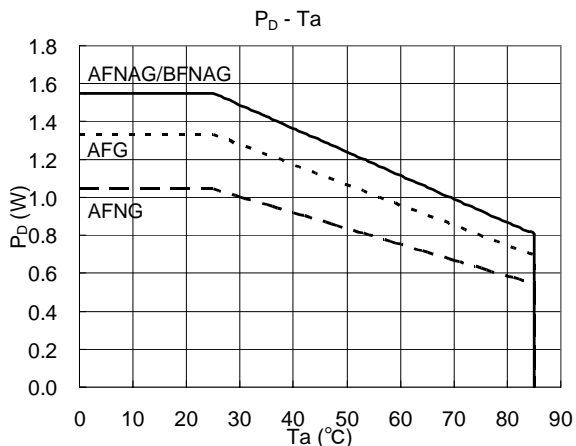
**Reference data**

\*This data is provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design.

**Output Current – Duty (LED turn-on rate)**



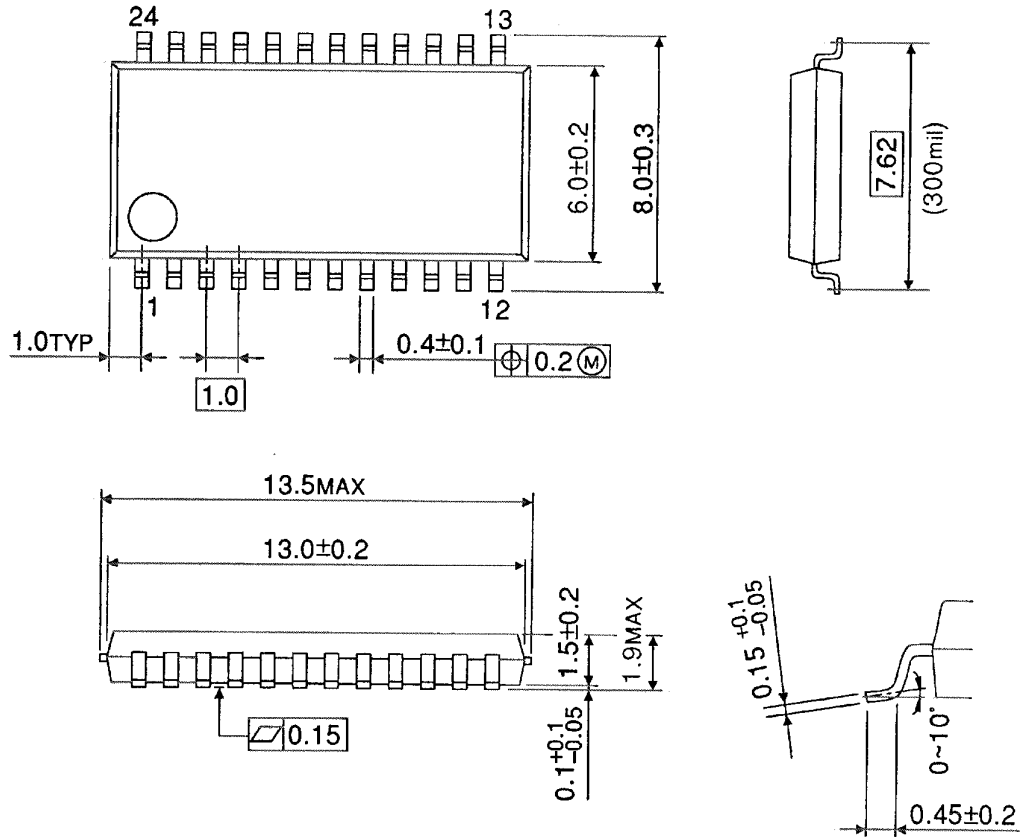
**Power dissipation – Ta**



## Package Dimensions

SSOP24-P-300-1.00B

Unit : mm

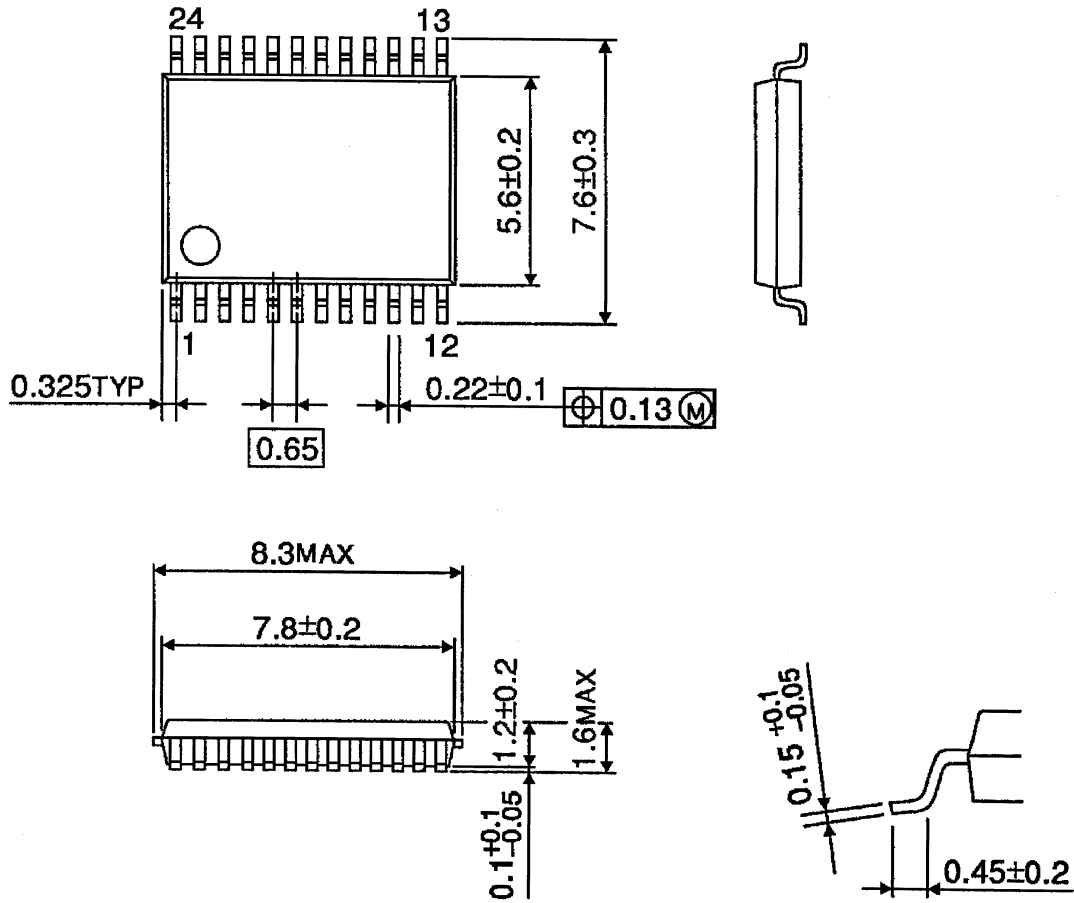


Weight: 0.29 g (typ.)

Package Dimensions

SSOP24-P-300-0.65A

単位 : mm



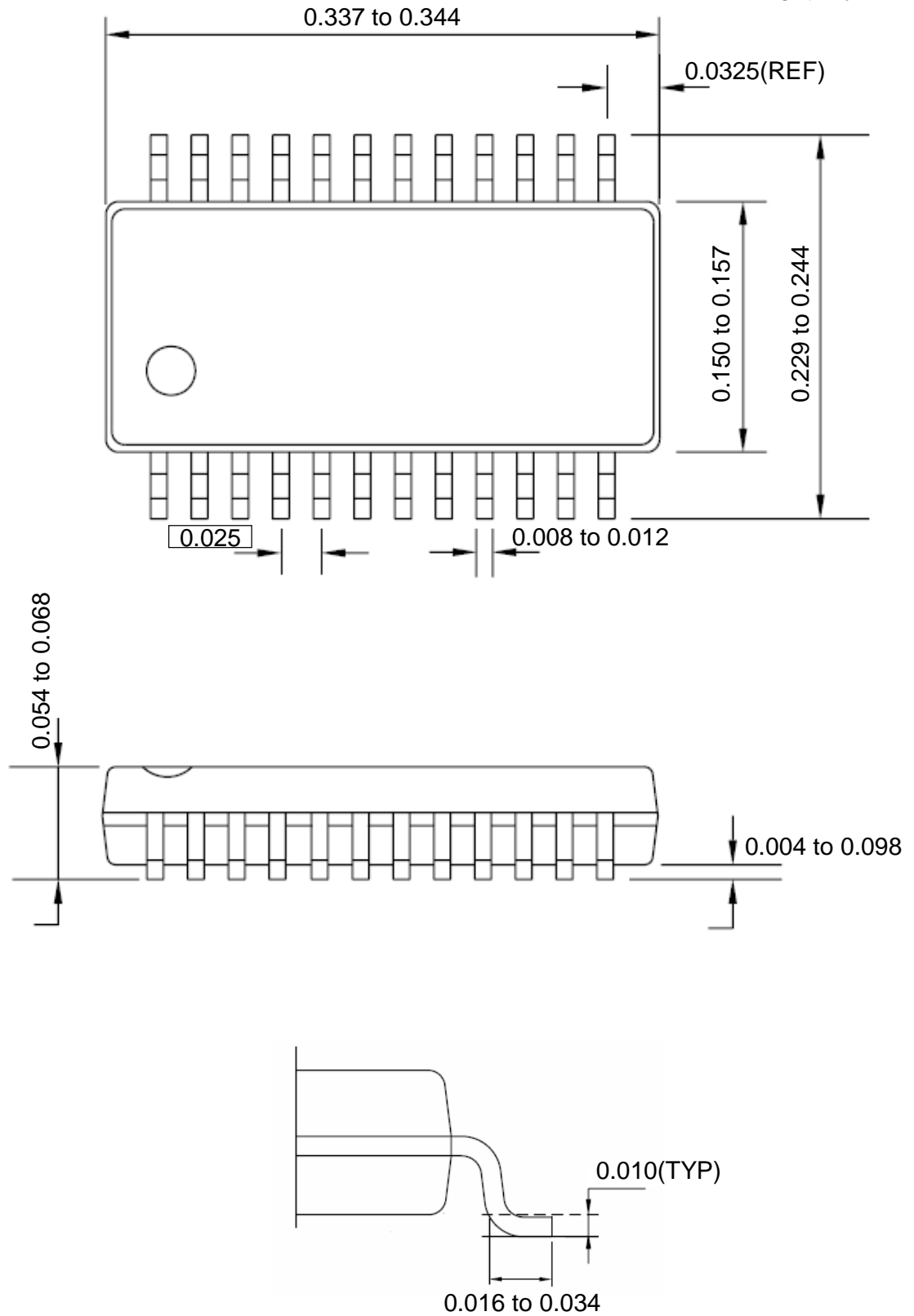
Weight: 0.14 g (typ.)



## Package Dimensions

SSOP24-P-150-0.64

Unit : Inch



Weight: 0.14 g (typ.)

**Notes on Contents****1. Block Diagrams**

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

**2. Equivalent Circuits**

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

**3. Timing Charts**

Timing charts may be simplified for explanatory purposes.

**4. Application Circuits**

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

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**5. Test Circuits**

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

**IC Usage Considerations****Notes on handling of ICs**

- [1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.  
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- [2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- [3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.  
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- [4] Do not insert devices in the wrong orientation or incorrectly.  
Make sure that the positive and negative terminals of power supplies are connected properly.  
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.  
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.
- [5] Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.  
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

**Points to remember on handling of ICs****(1) Heat Radiation Design**

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature ( $T_j$ ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

**(2) Back-EMF**

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

About solderability, following conditions were confirmed

- Solderability
  - (1) Use of Sn-37Pb solder Bath
    - solder bath temperature = 230°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux
  - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
    - solder bath temperature = 245°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux

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20070701-EN

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