TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62719AF

16ch constant current drivers and controller for full-color LED modules and panels

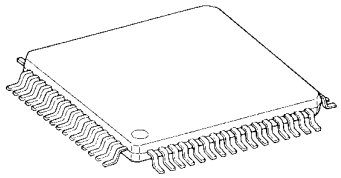
The TB62719AF is an LED driver which is suitable for driving full-color LED modules.

This device has built-in 8-bit PWM grayscale and each output current adjustment functions. It can turn on to 16 LEDs.

This device has a heat sink fitting side on the surface of the package.

Then, a heat sink will dissipate heat generated in the device.

In addition, this device built-in TSD (Thermal Shut Down) and output-open detection functions to protect the device.



HQFP64-P-1010-0.50

Weight: 0.26 g (typ.)

Features

- Output current capability and number of outputs: 90 mA × 16 outputs
- Recommended constant current range: 2.5 to 75 mA
- Application output voltage: 0.7 V (I_{OUT} = 2.5 to 90 mA)
  0.4 V (I_{OUT} = 2.5 to 40 mA)
- Adjustment function
  1. Standard current adjustment (8-bit serial data input)
     This function supports standard current adjustment using an external resistance connected to the REXT pin.
     2 high-order bits: Output current can be adjusted to any one of 4 levels in the range 25 to 100%.
     6 low-order bits: Output current can be adjusted to any one of 64 levels in the range 40 to 100%.
  2. Each dot adjustment (128-bit serial data input)
     This function allows adjustment of the current value for each output (dot).
     : Output current can be adjusted to any one of 64 levels in the range 20 to 100%.
  3. All dot adjustment 1 (8-bit parallel data input)
     This function allows adjustment of brightness for each LED module.
     5 low-order bits: Output current can be adjusted to any one of 32 levels in the range 50 to 100%.
  4. All dot adjustment 2 (8-bit parallel data input)
     This function allows changes to the frequency of the PWM clock and allows major brightness adjustment for the display.
     3 high-order bits: PWM clock frequency can be adjusted to any one of 8 levels in the range 1/1 to 1/8.
  5. 256-grayscale PWM function (8-bit parallel data input)
     This function controls the pulse width for each output, yielding 256 grayscales.
     Maximum PWM clock frequency 10 MHz (for all temperature range), Minimum pulse width 2 μs.
- Accuracy of bits in constant-current output levels prior to adjustment
  ±6.0% max (for output current of 5 mA to 75 mA)
- Protection functions
  1. Thermal shutdown function (TSD)
     This function monitors the rise in junction temperature.
     Connect a pull-up resistor to the ALARM1 pin in order to monitor the temperature.
     Step 1 When junction temperature is 120° or more: Error signal is driven out from the ALARM1 pin.
     Step 2 When junction temperature is 140° or more: Error signal is driven out from the ALARM1 pin and all outputs are turned off.
  2. Output Open Detection (OOD)
     This function operates when an output pin is open.
     Connect a pull-up resistor to the ALARM2 pin in order to monitor this.
- For anode-common LEDs
- Input signal voltage level: CMOS level (schmitt trigger input)

- Power supply voltage range: V_{DD} = 4.5 V to 5.5 V
- Maximum output pin voltage: 26 V
- Serial and parallel data transfer rate: 20 MHz (max, cascade connection)
- Operating temperature range: T_{opr} = −40 to 85°C
- Package: HQFP64-P-1010-0.50. A Heat sink can be fitted
- Existing product: The same pin assignment and function as TB62718AF

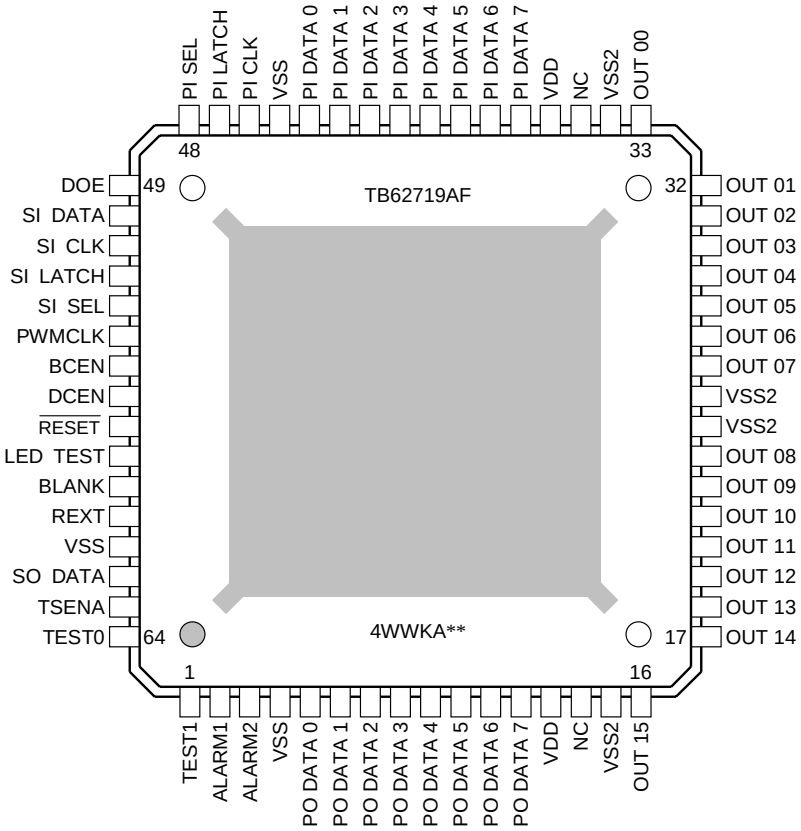
Warnings

Short-circuiting an output pin to GND or to the power supply pin may destroy the device. Take care when wiring the output pins, the power supply pin and the GND pins (V_{SS}, V_{SS2}).

Do not apply either positive or negative voltages to the heat sink on the surface of the IC.

In addition, do not solder anything to the heat sink.

Pin Assignment (top view) and Markings



Note: Indicates device name on the upper surface of the package.
Indicates weekly code on the lower surface of the package.

Details of weekly code on lower surface:

From left,

1st character = rightmost digit of year 3 for 2003, 4 for 2004

2nd and 3rd characters = week of manufacture during year: maximum value = 52.

4th characters = manufacturing factory ('K' means the Kita Kyushu factory.)

5th to 7th characters = lot number within week

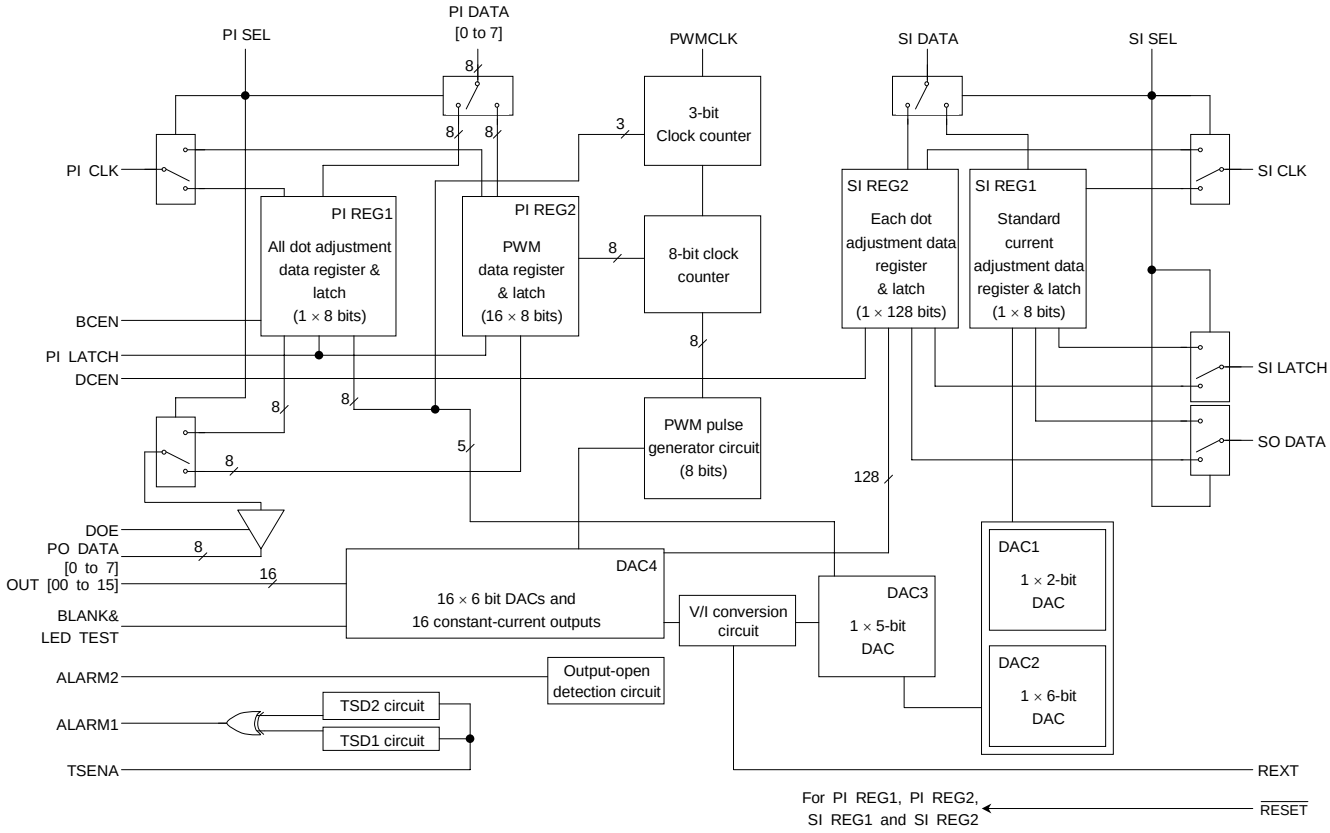
1st lot is A11, 2nd lot is A1 and 3rd lot is A.

4th lot is B11, 5th lot is B1 and 6th lot is B.

64th lot is Z11, 65th lot is Z1 and 66th lot is Z.

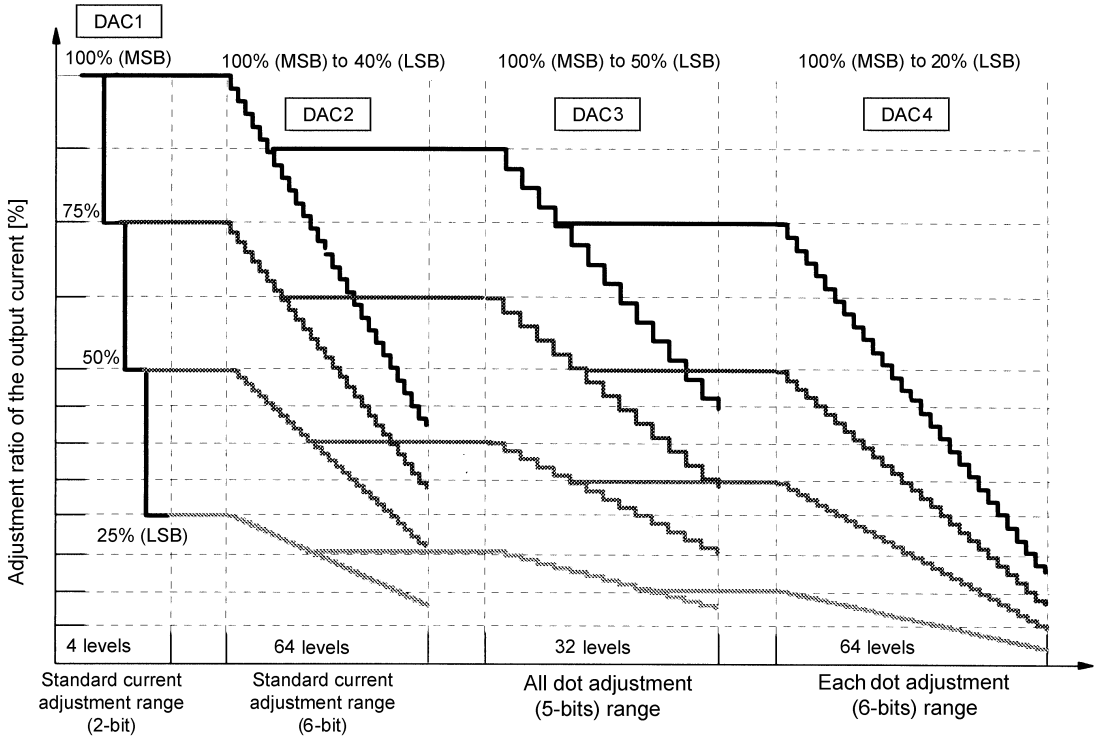
The four characters of 'I', 'M', 'O' and 'W' are not used.

Block Diagram (entire device)



Constant Current Adjustment Range (graph)

This Graph Shows How Current May Be Adjusted to a Fraction of Its Full-Scale Value.



Note: In each case, the value input to each DAC is the value output from the previous DAC.

Reference: Current adjustment functions

DAC1 to DAC3 are the current adjustment functions for all outputs.

The adjustment width of DAC1 is large and approximate (1LSB ≃ 25%).
The adjustment width of DAC2 is the smallest and has a large error (1LSB ≃ 0.95%).
The adjustment width of DAC3 is small. DAC3 is a high-performance DAC with a small error (1LSB ≃ 1.61%).

Therefore,
It is recommended that DAC1 and DAC2 be used for adjusting the REXT resistance.
It is recommended that DAC3 be used for adjusting brightness between module.
(after it was set and it had DAC4 adjusted to the dot.)
The beginning is set in about 75% of the middle value, after that it is effective to use ±25% of set width.

DAC4 is the current adjustment function for each outputs.

The adjustment width of DAC4 is small. But it is a high-performance DAC with a small error (1LSB ≃ 1.27%).

And also, DAC4 has a very wide setting range.

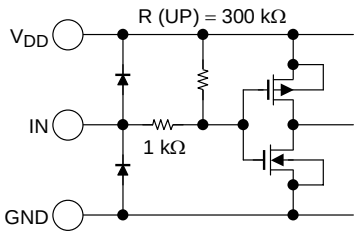
Therefore, DAC4 can be used to adjust the brightness of LEDs without a rank classification.
This method allows brightness to be adjusted with a degree of accuracy of 1.27% of full scale.

Note: Assuming precise linear correlation between output current and LED brightness

Equivalent Input and Output Circuit (resistance values are typical values.)

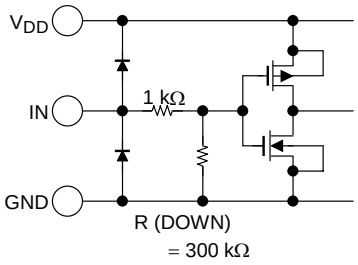
1. Input pins with pull-up resistor

TSENA, BLANK



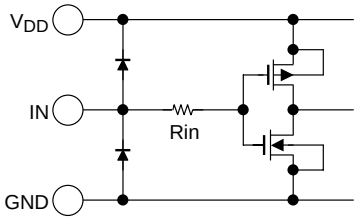
2. Input pins with pull-down resistor.

SI/PI LATCH, PI DATA0 to DATA7, BC/DCEN, LED TEST



3. Input terminals

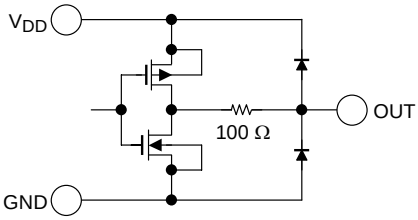
(A) SI DATA, SI/PI CLK, PWMCLK
(B) $\overline{\text{RESET}}$, DOE, PI/SI SEL



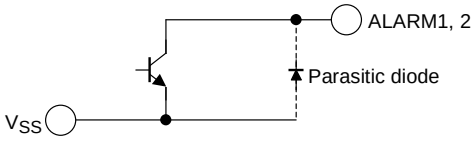
(A) Rin = 250 Ω
(B) Rin = 1 kΩ

4. Output terminals

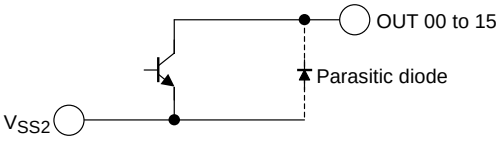
PO DATA0 to DATA7, SO DATA



5. Protection circuit for monitor terminals



6. Constant-current output terminals



Explanation of Pin Functions Table

No.	Name	I/O	Function Explanation	
4, 45	VSS	P	—	Logic ground pins. Be sure to use all.
35, 14	NC	—	Pull up	Unused
63	TSENA	I	Pull up	This pin is used to reset the IC's built-in temperature monitoring circuit (TSD). Rising edge of input signal re-enables outputs which had been forced to OFF. The latched data as the setting is not reset. Either in case of H- or L-level of this terminal can be operated TSD circuit.
15, 24, 25, 34	VSS2	P	—	Ground pin for output. Be sure to use all.
13, 36	VDD	P	—	Logic power supply input pins. Be sure to use all.
16 to 23, 26 to 33	OUT 00 to 15	O	—	LED drive output pins. Connect to cathode of LED.
50	SI DATA	I	—	Serial data input pin. Used for input of standard current adjustment data and dot adjustment data
51	SI CLK	I	—	Serial data transfer clock input pin. Data is transferred at positive edge.
52	SI LATCH	I	Pull down	Serial data latch signal input pin. Data is held on positive edge.
53	SI SEL	I	—	Serial data selection pin. Either standard current adjustment data or dot adjustment data may be selected.
62	SO DATA	O	—	Serial data output pin. The output data type is selected using SI SEL.
37 to 44	PI DATA [0 to 7]	I	Pull down	Input pins for parallel data. Inputs for all output adjustment data and PWM data
46	PI CLK	I	—	Input pin for parallel data transfer clock. Data is transferred on positive edge.
47	PI LATCH	I	Pull down	Input pin for parallel data latch signal. Data is held on positive edge.
48	PI SEL	I	—	Parallel data selection pin. Either total dot adjustment data or PWM data may be selected.
5 to 12	PO DATA [0 to 7]	O	—	Output pin for parallel data. The output data type is selected using PI SEL.
49	DOE	I	—	Control pin for parallel data output PO DATA. PI DATA is out on input of an H-level signal. PI DATA is set to High-impedance by input of an L-level signal.
59	BLANK	I	Pull up	PWM circuit control signal input pin. Output is turn OFF by input of an H-level signal. PWM output is initiated by input of an L-level signal accordingly to the input data.
54	PWMCLK	I	—	Standard clock input pin for PWM circuit. One clock cycle is equivalent to the minimum pulse width of the PWM output.
55	BCEN	I	Pull up	Selection signal input pin for all output adjustment functions. All output adjustment is fixed to 100% when this signal is Low. All bit adjustments become effective when it is High. It is not influent anything to all output adjustment by PWM clock.
56	DCEN	I	Pull up	Selection signal input pin for dot adjustment function. Dot adjustment value is fixed to 100% when this signal is Low. Dot adjustment becomes effective when it is High.
57	$\overline{\text{RESET}}$	I	—	Reset signal input pin. Setting and registered data are reset when it is Low. A reset also releases TSD.
58	LED TEST	I	Pull down	Connection confirmation signal input pin for an LED. When this signal is High, all outputs are ON. This signal should normally be kept Low.
60	REXT	P	—	Connection pin of resistor for setting for the current.
2	ALARM1	O	—	Open-collector monitor pin for TSD circuit. When the TSD circuit detects an abnormal temperature, this signal is turned ON. IO monitor the TSD circuit connect this pin to a pull-up resistor. ALARM1 is independent of the $\overline{\text{RESET}}$ signal.
3	ALARM2	O	—	Open-collector monitor pin for output-open detection circuit. When an open output is detected, this signal is turned ON.
1, 64	TEST [0:1]	I	—	Pins for the device testing. Connect all these pins to ground.

Pin attributes P: power supply/ground/other, I: input pin, O: output pin

Note: It is recommended that pins with pull-up or pull-down resistors not be left open.
Ambient noise may cause malfunction of the device.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{DD}	−0.3 to +7	V
Constant-current output voltage		V_O	−0.3 to +26	V
Output current		I_{OUT}	+90	mA/bit
Logic output voltage		V_{OUT}	−0.3 to +7	V
Logic input voltage		V_{IN}	−0.3 to V_{DD} + 0.3	V
Total V_{SS2} current (Note 1)		IV_{SS2}	1.44	A
Power dissipation	When device mounted on PCB	P_d (Note 2)	1.19 (Note 3)	W
	When device mounted on PCB of any size		5.0 (Note 4)	
Saturation heat resistance of package	When device mounted on PCB	$\theta_{(j\text{-}a)}$	105 (Note 3)	°C/W
	When device mounted on PCB of any size	$\theta_{(j\text{-}c)}$	25 (Note 4)	
Operating temperature		T_{opr}	−40 to 85	°C
Storage temperature		T_{stg}	−55 to 150	°C

Note 1: All four V_{SS2} pins must be connected. If not, device characteristics cannot be guaranteed.

Note 2: If the operating temperature exceeds 25°C, derate the power dissipation rating by 0.95 mW/°C.

Note 3: When device mounted on PCB with dimensions 100 × 100 × 1.6 mm

Note 4: When using heat sink fin which allows the device for more heat dispersion

Recommended Operating Conditions

DC Characteristics (unless otherwise specified, V_{DD} = 4.5 to 5.5 V, T_{opr} = –40 to 85°C)

Characteristics	Symbol	Conditions & Terminals	Min	Typ.	Max	Unit
Supply voltage	V_{DD}	—	4.5	5.0	5.5	V
High-level input voltage	V_{IH}	PI DATA, PI CLK, PI SEL, PI LATCH, SI DATA, SI CLK, SI SEL, SI LATCH, PWM CLK	0.7 × V_{DD}	—	V_{DD}	V
Low-level input voltage	V_{IL}	BLANK, LED TEST, TSENA, DOE, DCEN, BCEN	V_{SS}	—	0.3 × V_{DD}	V
High-level output current	I_{OH}	DATA PO0 to 7, SO DATA	—	—	−1	mA
Low-level output current	I_{OL}	V_{DD} = 4.5 V, ALARM1/2	—	—	1	mA
Constant-current output	I_{OUT}	OUT00 to 15	5	—	80	mA/bit
Output voltage	V_{OUT}	OUT00 to 15 OFF	—	—	26	V
	V_{OH}	ALARM1/2 OFF	—	—	5	V
Operating temperature	T_{opr}	—	−40	—	85	°C

Timing Recommended Operating Conditions
(unless otherwise specified, V_{DD} = 4.5 V to 5.5 V, T_{opr} = –40 to 85°C)

Characteristics	Symbol	Condition & Terminals	Min	Typ.	Max	Unit
Clock frequency	f_{PWM}	PWM CLK, Ratio of High-level: Low level = 50%,	—	—	10	MHz
	f_{PI1}	PI CLK	—	—	15	
	f_{PI2}	PI CLK, connected in cascade	—	—	10	
	f_{SI1}	SI CLK	—	—	15	
	f_{SI2}	SI CLK, connected in cascade	—	—	10	
Minimum pulse width	t_{wH}/t_{wL}	PWM CLK	30	—	—	ns
		PI CLK, SI CLK	30	—	—	
	t_{wltH}/t_{pltL}	PI LATCH, SI LATCH	50	—	—	
	t_{wrstH}/t_{wrstL}	$\overline{\text{RESET}}$	50	—	—	
	t_{wblkH}/t_{wblkL}	BLANK	400	—	—	
	t_{wledH}/t_{wledL}	LED TEST	400	—	—	
Set-up time	t_{setup}	PI DATA → PI CLK	10	—	—	ns
		PI LATCH → PI CLK	10	—	—	
		SI DATA → SI CLK	10	—	—	
		SI LATCH → SI CLK	10	—	—	
		SI LATCH → SI CEL	50	—	—	
Hold time	t_{hold}	PI DATA → PI CLK	5	—	—	ns
		PI LATCH → PI CLK	5	—	—	
		SI DATA → SI CLK	5	—	—	
		SI LATCH → SI CLK	5	—	—	
		SI LATCH → SI CEL	50	—	—	

Electrical Characteristics 1

(unless otherwise specified, typ.: V_{DD} = 5.0 V, T_{opr} = 25°C, load capacitance = 50 pF, min/max: V_{DD} = 4.5 to 5.5 V, T_{opr} = –40 to 85°C, load capacitance = 50 pF)

Characteristics	Symbol	Test Terminals	Test Conditions	Min	Typ.	Max	Unit
High-level output voltage	V_{OH}	PO DATA 0 to 7 SO DATA	I_{OH} = –1.0 mA	V_{DD} –0.5	—	—	V
Low-level output voltage	V_{OL}	PO DATA 0 to 7 SO DATA	I_{OL} = +1.0 mA PO DATE 0 to 7, SD DATE	—	—	0.5	V
		ALARM1, 2	I_{OL} = +2.5 mA	—	—	0.5	
Tri-state output leakage current	I_{OZ}	PO DATA 0 to 7	V_{OUT} = V_{DD} or V_{SS}	—	±0.5	±5	μA
Input current	I_I		All pins without pull-up/pull-down resistors	—	—	±1	μA
Supply current	I_{DD1}	V_{DD}	PI DATA = 1/2 PI CLK SI DATA = 1/2 SI CLK PI CLK = SI CLK = 20 MHz PWMCLK = "L", BLANK = "H" T_{opr} = 25°C Settings *1	4	13	23	mA
	I_{DD2}		PI DATA = SI DATA = "L" PI CLK = SI CLK = "L" PWMCLK = 20 MHz T_{opr} = 25°C Settings *5a	12	21	35	
	I_{DD3}		PI DATA = 1/2 PI CLK SI DATA = 1/2 SI CLK PI CLK = SI CLK = PWMCLK = 20 MHz Settings *5a	20	32	47	
			T_{opr} = –40°C, Other conditions are the same as above.	—	—	55	
	I_{DD4}		PI DATA = SI DATA = "L" PI CLK = SI CLK = "L" PWMCLK = 20 MHz T_{opr} = 25°C Settings *6a	14	27	44	
	I_{DD5}		PI DATA = 1/2 PI CLK SI DATA = 1/2 SI CLK PI CLK = SI CLK = PWMCLK = 20 MHz T_{opr} = 25°C Settings *6a	22	38	56	
			T_{opr} = –40°C, Other conditions are the same as above.	—	—	70	

Electrical Characteristic Settings
(unless otherwise specified, OUT00 to 15 ON, V_{OUT} = 0.7 V and R_{EXT} = 910 kΩ)

NO.	DAC Settings	All Dot Adjustment (DAC3)	Constant Output Current (typ.)
*1	OUT00 to 15 OFF, V_{OUT} = 26 V, DAC1, 2, 4 = initial setting, BLANK = "H"	DAC3 = 31	I_{OUT} = 0 mA
*2a	DAC1 = 0, DAC2 = 0, DAC4 = 39, BLANK = "L"		I_{OUT} = 5 mA
*3a	DAC1 = 0, DAC2 = 18, DAC4 = 63, BLANK = "L"		I_{OUT} = 10 mA
*4a	DAC1 = 1, DAC2 = 18, DAC4 = 63, BLANK = "L"		I_{OUT} = 20 mA
*5a	DAC1 = 2, DAC2 = 38, DAC4 = 63, BLANK = "L"		I_{OUT} = 40 mA
*6a	DAC1 = 3, DAC2 = 46, DAC4 = 63, BLANK = "L"		I_{OUT} = 60 mA
*7	DAC1 = 3, DAC2 = 63, DAC4 = 63, BLANK = "L"		I_{OUT} = 70 mA
*2b	DAC1 = 0, DAC2 = 0, DAC4 = 39, BLANK = "L"	DAC3 = 00	I_{OUT} = 2.5 mA
*3b	DAC1 = 0, DAC2 = 18, DAC4 = 63, BLANK = "L"		I_{OUT} = 5 mA
*4b	DAC1 = 1, DAC2 = 18, DAC4 = 63, BLANK = "L"		I_{OUT} = 10 mA
*5b	DAC1 = 2, DAC2 = 38, DAC4 = 63, BLANK = "L"		I_{OUT} = 20 mA
*6b	DAC1 = 3, DAC2 = 46, DAC4 = 63, BLANK = "L"		I_{OUT} = 30 mA

Electrical Characteristics 2
(unless otherwise specified, typ.: V_{DD} = 5.0 V, T_{opr} = 25°C, load capacitance = 50 pF, min/max: V_{DD} = 4.5 to 5.5 V, T_{opr} = –40 to 85°C, load capacitance = 50 pF)

Characteristics	Symbol	Test Terminals	Test Condition	Min	Typ.	Max	Unit
Constant-current output	I_{OUT1}	OUT 00 to 15	Settings *7	60.4	71.0	81.6	V
	I_{OUT2}		Settings *6a	51.0	60.0	69.0	
	I_{OUT3}		Settings *5a	34.0	40.0	46.0	
	I_{OUT4}		Settings *4a	16.6	20.0	23.4	
	I_{OUT5}		Settings *3a	7.8	10.0	12.2	
	I_{OUT6}		Settings *2a	3.2	5.0	6.8	
Constant-current output Depends on temperature	$\%T_{OPR1}$		I_{OUT} = 2.5 to 75 mA, V_{OUT} = 1.0 V, T_{opr} is varied in the range –40°C to 85°C	—	±25	±50	μA/°C
Leakage current for constant-current output	I_{OLK}		Settings *1, V_{OUT} = 26 V	—	—	0.1	μA
Constant current accuracy between bits	ΔI_{OUT}		I_{OUT} = 2.5 to 75 mA	—	±1.5	±6	%
Dot adjustment deviation between bits (Note)	$\%I_{OUT}$		I_{OUT} = 2.5 to 75 mA	—	±1	±2.5	%
Constant-current output depends on output voltage	$\%V_{OUT}$		I_{OUT} = 2.5 to 75 mA, V_{OUT} is varied in the range 0.7 V to 3 V.	—	±3	±5	%
Constant-current output depends on supply voltage	$\%V_{DD}$		Settings *4a, 5a, 6a V_{DD} = 4.5 → 5.5 V	–2.0	—	2.0	%
			Settings *3a, 2a V_{DD} = 4.5 → 5.5 V	–5.0	—	5.0	
TSD detection temperature	T_{sd1}		—	120	—	—	°C
	T_{sd2}		—	140	—	—	
Output-open detection voltage	V_{ARL}		ALARM2	—	0.04 × V_{DD}	—	V
Pull-up/down resistor	R_{up}/R_{dw}	—	—	150	300	600	kΩ

Note: When DAC3 data were changed from MSB to LSB.

Electrical Characteristic Settings

(unless otherwise specified, OUT00 to 15 ON, V_{OUT} = 0.7 V and R_{EXT} = 910 Ω)

NO.	DAC Settings	All Dot Adjustment (DAC3)	Constant Output Current (typ.)
*1	OUT00 to 15 OFF, V_{OUT} = 26 V, DAC1, 2, 4 = initial setting, BLANK = "H"	DAC3 = 31	I_{OUT} = 0 mA
*2a	DAC1 = 0, DAC2 = 0, DAC4 = 39, BLANK = "L"		I_{OUT} = 5 mA
*3a	DAC1 = 0, DAC2 = 18, DAC4 = 63, BLANK = "L"		I_{OUT} = 10 mA
*4a	DAC1 = 1, DAC2 = 18, DAC4 = 63, BLANK = "L"		I_{OUT} = 20 mA
*5a	DAC1 = 2, DAC2 = 38, DAC4 = 63, BLANK = "L"		I_{OUT} = 40 mA
*6a	DAC1 = 3, DAC2 = 46, DAC4 = 63, BLANK = "L"		I_{OUT} = 60 mA
*7	DAC1 = 3, DAC2 = 63, DAC4 = 63, BLANK = "L"		I_{OUT} = 70 mA
*2b	DAC1 = 0, DAC2 = 0, DAC4 = 39, BLANK = "L"	DAC3 = 00	I_{OUT} = 2.5 mA
*3b	DAC1 = 0, DAC2 = 18, DAC4 = 63, BLANK = "L"		I_{OUT} = 5 mA
*4b	DAC1 = 1, DAC2 = 18, DAC4 = 63, BLANK = "L"		I_{OUT} = 10 mA
*5b	DAC1 = 2, DAC2 = 38, DAC4 = 63, BLANK = "L"		I_{OUT} = 20 mA
*6b	DAC1 = 3, DAC2 = 46, DAC4 = 63, BLANK = "L"		I_{OUT} = 30 mA

Switching Characteristics

(unless otherwise specified, typ.: V_{DD} = 5.0 V, T_{opr} = 25°C, load capacitance = 50 pF, min/max: V_{DD} = 4.5 to 5.5 V, T_{opr} = –40 to 85°C, load capacitance = 50 pF)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Maximum SI CLK/PI CLK frequency	f_{MAX1}	When connected in cascade	15	—	—	MHz
	f_{MAX2}	Without a board	20	—	—	
Maximum PWMCLK frequency	f_{MAX3}	Without a board	15	—	—	
Tri-state output enable propagation delay time	$t_{pZH/ZL}$	DOE → PO DATA0 to PO DATA7	8	16	30	ns
Tri-state output disable propagation delay time	$t_{pHZ/LZ}$	DOE → PO DATA0 to PO DATA7	8	16	30	ns
Rise time	t_r	OUT00 to OUT15	25	120	220	μs
		ALARM1, 2	65	120	170	ns
Fall time	t_f	OUT00 to OUT15	15	60	105	ns
		ALARM1, 2	5	15	25	
Propagation delay time (Note)	t_{pHL}	BLANK → OUT00 to OUT15	40	230	410	ns
	t_{pLH}	PWM CLK → OUT00 to OUT15	35	85	130	
	t_{pHL}	PWM CLK → OUT00 to OUT15	40	230	410	
	t_{pLH}	LED TEST → OUT00 to OUT15	30	75	120	
	t_{pHL}		40	230	410	
	t_{pHL}	$\overline{\text{RESET}}$ → OUT00 to OUT15	30	100	170	
	t_{pd} (voltage waveform)	PI CLK → PO DATA0 to PO DATA7	20	30	70	
		PI SEL → PO DATA0 to PO DATA7	20	30	70	
		SI SEL → SO DATA	10	18	40	
		SI SEL → SO DATA	10	20	40	

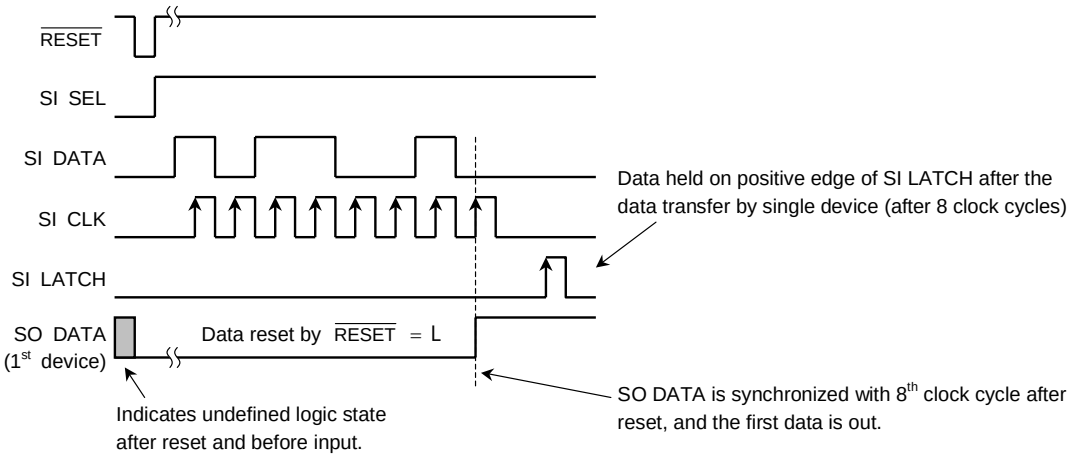
Note: For the switching test condition, refer to No. *5a in the table "Electrical Characteristic Settings".

Explanation of Operation and Truth Tables

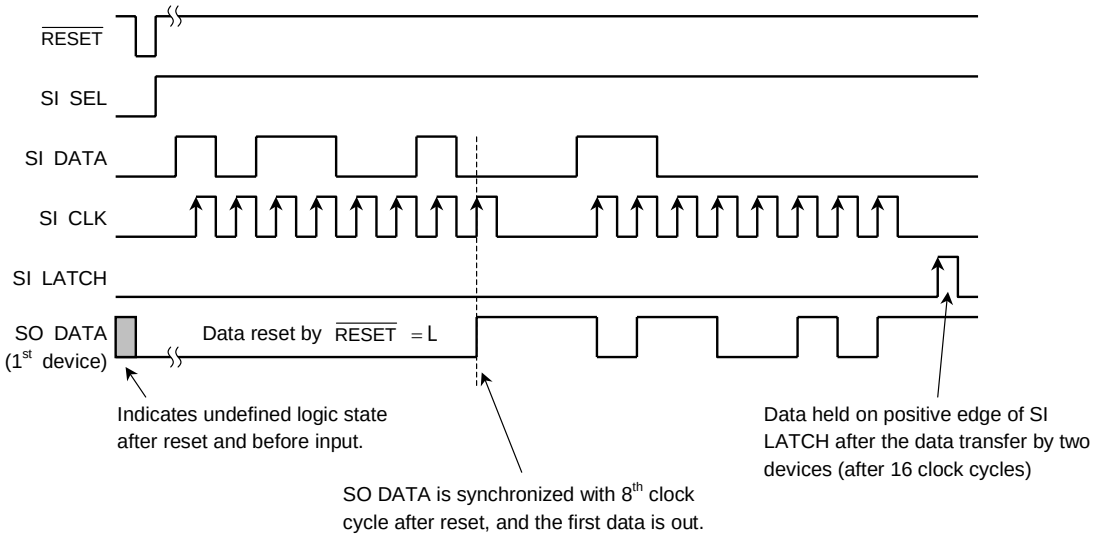
Serial Data Transfer: Standard Current Adjustment Using DAC1 and DAC2 (data register SI REG1 [7:0])

Process	SI DATA	SI CLK	SI LATCH	SI SEL	SO DATA	Operation and Function
1	H or L	(×8)	L	H	H or L	Selects standard current adjustment (8 bits, 2 bits and 6 bits) for input data. When SI REL is high, data is transferred to SI REG [1] on 8th positive edge of SI CLK input.
2		L	(×1)	H	No change	Holds the data transferred to SI REG [1] on positive edge of SI Latch. Set is reflected on standard current adjustment from the moment when it is held.

Serial Data Transfer Timing (standard current adjustment, SI SEL = H, single device)



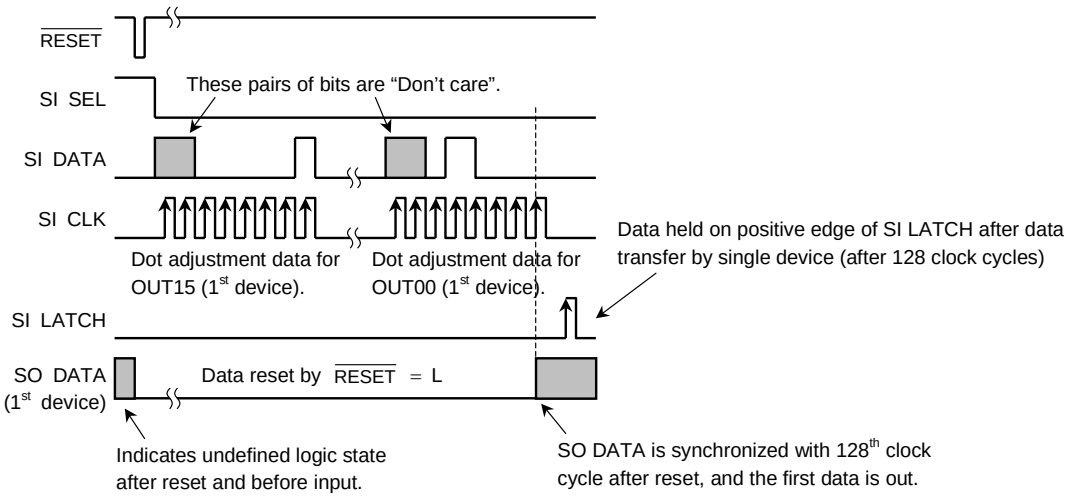
Serial Data Transfer Timing (standard current adjustment, SI SEL = H, two devices connected in cascade)



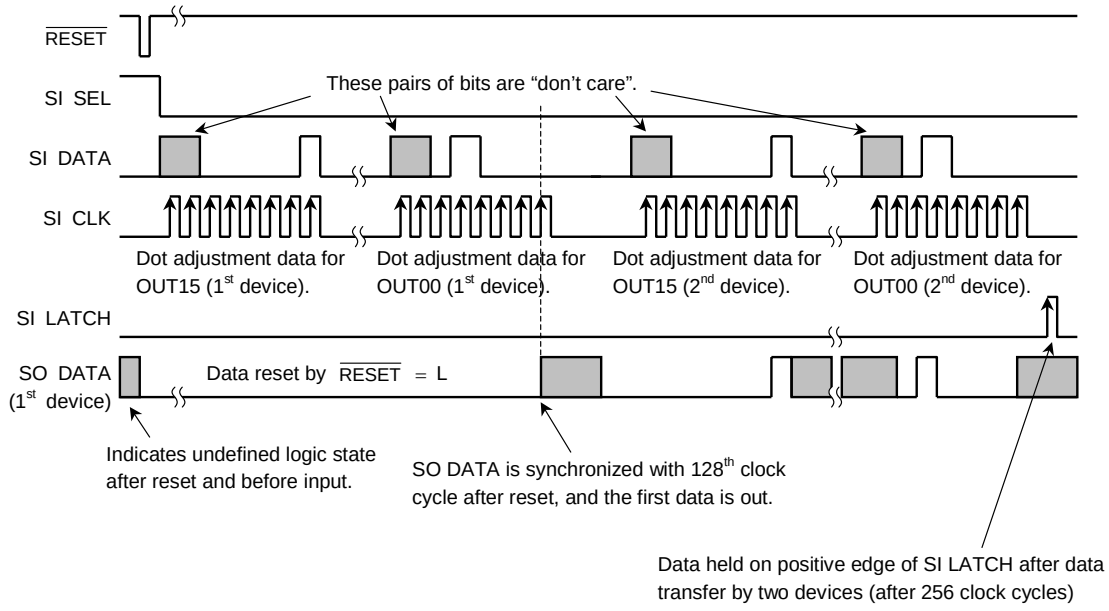
Serial Data Transfer: Dot Adjustment DAC4. (data register SI REG1 [127:0])

Process	SI DATA	SI CLK	SI LATCH	SI SEL	SO DATA	Operation and Function
1	H or L	(×128)	L	L	H or L	Selects dot adjustment (128 bits) for input data. Data is transferred to SI REG2 on 128th positive edge of SI CLK.
2		L	(×1)	L	No change	Holds the data transferred to SI REG2 on positive edge of SI Latch. Set is reflected on dot adjustment from the moment when it is held.

Serial Data Transfer Timing
(dot adjustment, SI SEL = L, single device)



Serial Data Transfer Timing
(dot adjustment, SI SEL = L, two devices connected in cascade)



DAC1: Standard Current Adjustment Settings for DAC1 (SI REG1 [7:6])

$\overline{\text{RESET}}$	SI SEL	SI REG (7:6)	SI REG (5:0)	Current Rate	Operation and Function	Notes
H	H	HH	XXXXXX	100% (1.0)	100% of base current setting as determined by R_{EXT} (Ω)	When SI SEL = H, 2 bits on MSB sides are corresponding to set of standard current adjustment DAC1. The output current can be set to one of 4 levels.
H	H	HL	XXXXXX	75% (0.75)	75% of base current setting as determined by R_{EXT} (Ω)	
H	H	LH	XXXXXX	50% (0.5)	50% of base current setting as determined by R_{EXT} (Ω)	
H	H	LL	XXXXXX	25% (0.25)	25% of base current setting as determined by R_{EXT} (Ω)	
⌐¬	X	LL	LLLLLL	25% (0.25)	Initial state after input of reset signal: 25% of base current setting as determined by R_{EXT} (Ω) (as described above)	

DAC2: Standard Current Adjustment Settings for DAC2 (SI REG1 [5:0])

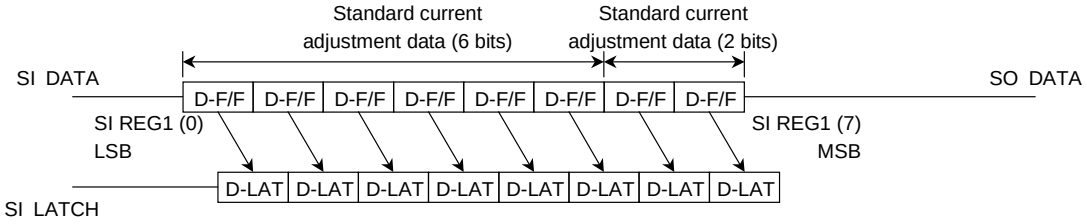
$\overline{\text{RESET}}$	SI SEL	SI REG (7:6)	SI REG (5:0)	Current Rate	Operation and Function	Notes
H	H	XX	HHHHHH	100% (1.0)	100% of base current value as set using DAC1 current adjustment	When SI SEL = H, 6 bits on MSB sides are corresponding to set of standard current adjustment DAC2. The output current can be set to one of 64 levels.
H	H	XX	HHHHHL ↑ ↓ LLLLLH	(0.9905) ↑ 1LSB = ±0.95% (±0.0095) ↓ (0.4095)	Any one or 64 levels in the range 100 to 40% of the current can be set. (1LSB = 0.95%) 6-bit DAC performance	
H	H	XX	LLLLLL	40% (0.4)	40% of base current value as set using DAC1 current adjustment	
⌐¬	X	LL	LLLLLL	40% (0.4)	Initial state after input of reset signal: 40% of base current value set as described above	

DAC4: Set Details of Dot Adjustment DAC4 (SI REG2 [127:0])

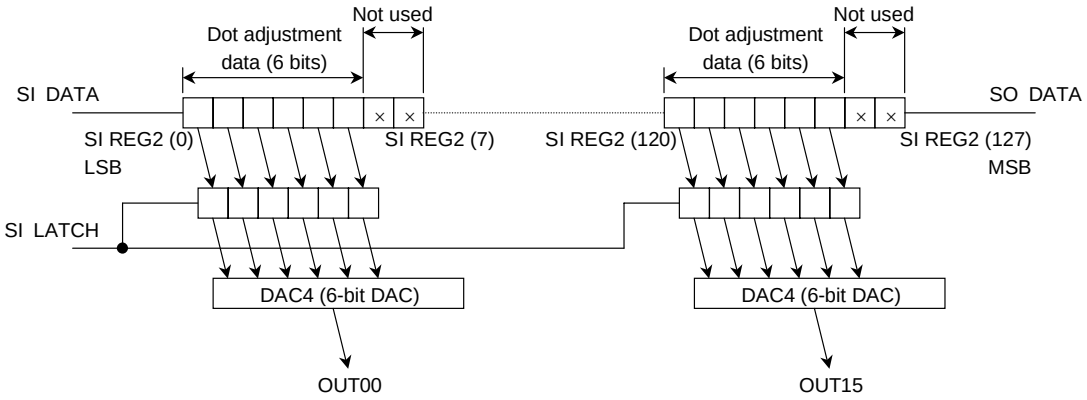
$\overline{\text{RESET}}$	SI SEL	DCEN	About 8 bits Unit of SI REG [127:0]	Current Rate	Operation and Function	Notes
H	L	H	XXHHHHHH	100% (1.0)	Output current is 100% of base current value as set using DAC1 and DAC2 base current adjustment and DAC3 surface brightness adjustment	When SI SEL = L 8 bits out of 128 bits are corresponding to set of each output, and the 6 bits on MSB sides of 8 bits are data on dot adjustment The output current can be set to one of 64 levels. SI REG2 [7:0] → adjustment data for OUT0. SI REG2 [15:8] → adjustment data for OUT1. SI REG2 [127:120] → adjustment data for OUT15.
H	L	H	XXHHHHHL ↑ ↓ XXLLLLLH	(0.9874) ↑ 1LSB = ±1.269% (±0.0126) ↓ (20.0126)	Any one of 64 levels in the range 100 to 20% of the current can be set. (1LSB ≃ 1.27%) (6-bit DAC performance) 1LSB variation: ±1.269% (typ.) Non linearity error: ±1/2LSB Differential non linearity error: ±1/2LSB	
H	L	H	XXLLLLLL	20% (0.2)	20% of base current value as set using DAC3 current adjustment.	
⌐¬	X	H	XXLLLLLL	20% (0.2)	Initial state after input of reset signal: 20% of base current value set as described above	
H	X	L	XXHHHHHH	100% (1.0)	Output current is 100% of base current value set as described above.	Data input is still enabled if DCEN = L. If DCEN = H, adjustment is performed at the same time.

Polarity of Serial Input Data for Standard Current Adjustment (SI REG1 [7:0]) and Dot Adjustment (SI REG2 [127:0])

Serial Data Transfer Timing
SI SEL = H, Input of Standard Current Adjustment Data for DAC1 and DAC2



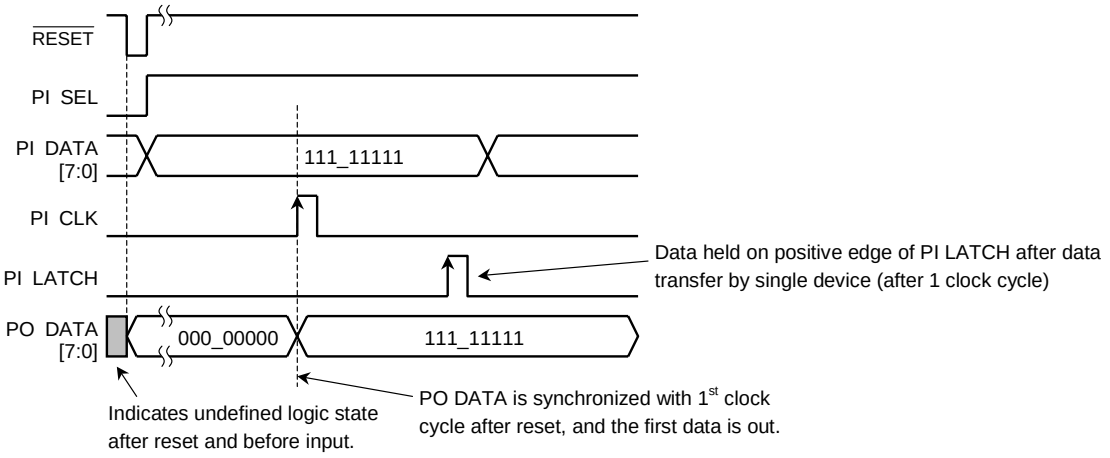
SI SEL = L, Input of Dot Adjustment Data for DAC4



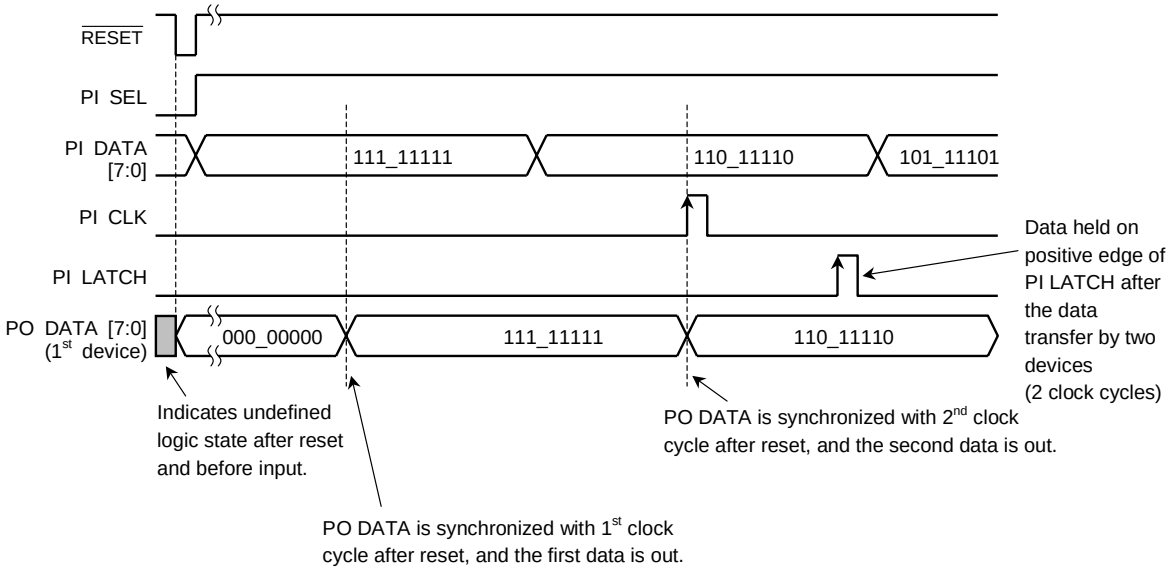
Parallel Data Transfer: All Dot Adjustment DAC3. (data register: PI REG1 [7:0])

Process	PI DATA [7:0]	PI CLK	PI LATCH	PI SEL	PO DATA [7:0]	Operation and Function
1	H or L	(×1)	L	H	H or L	Selects total dot adjustment (8-bit, 3-bit and 5-bit) for input data. Data is transferred to PI REG1 on 128th positive edge of PI CLK.
2		L	(×1)	H	No change	Holds the data transferred to PI REG1. Set is reflected on all dot adjustment from the moment when it is held.

Parallel Data Transfer Timing
(all dot adjustment, PI SEL = H, single device)



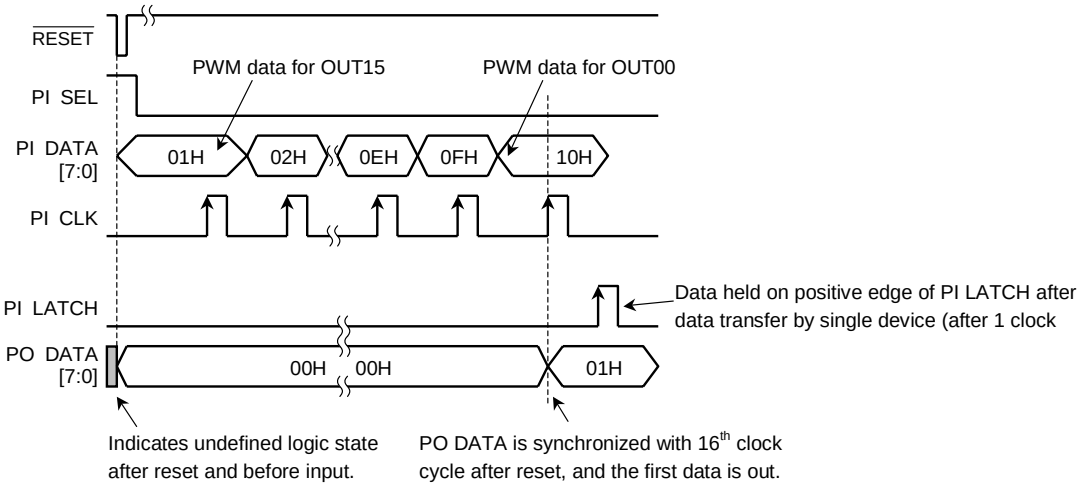
Parallel Data Transfer Timing
(all dot adjustment, PI SEL = H, two devices connected in cascade)



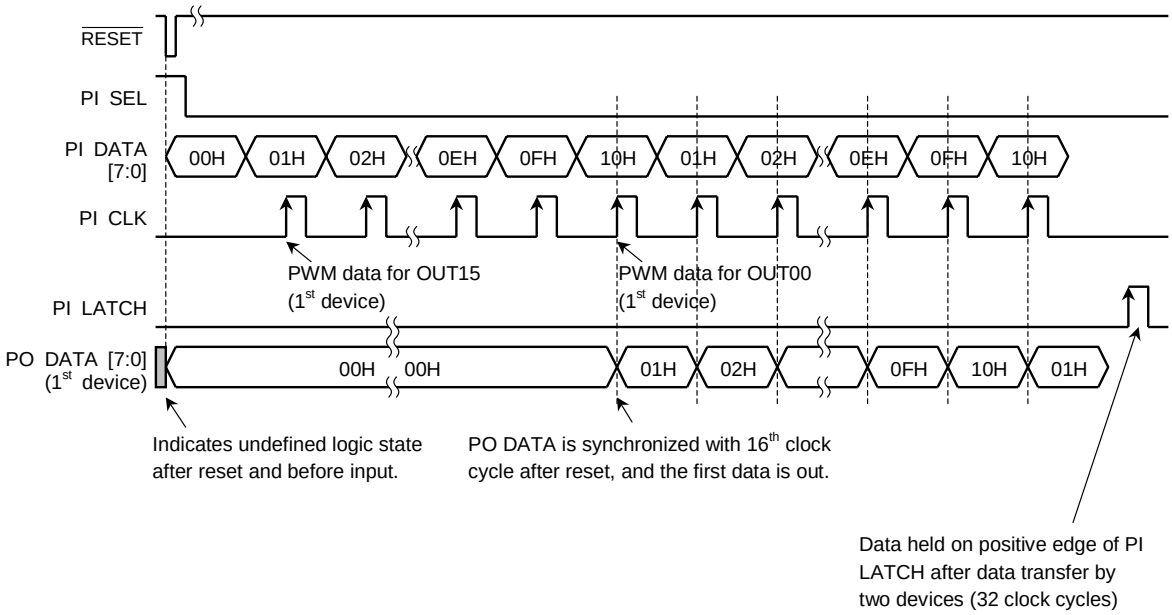
Parallel Data Transfer PMW Display Data (data register: PI REG2 [127:0])

Process	PI DATA	PI CLK	PI LATCH	PI SEL	PO DATA	Operation and Function
1	H or L	(×16)	L	L	H or L	Selects for input data of PWM display data (8 bit × 16). Data is transferred to PI REG2 on 16th positive edge of PI CLK.
2		L	(×1)	L	No change	Holds the data transferred to PI REG2. Set is reflected on PWM 256 grayscales from the next BLANK = L when it is held.

Parallel Data Transfer Timing
(PWM data SI SEL = L, single device)



Parallel Data Transfer Timing
(PWM data SI SEL = L, two devices connected in cascade)



Parallel Data Transfer: Optional Function to Change PO DATA [7:0] Delay Time

8 Bits of SI REG [127:120]	PO DATA [7:0]	Operation and Function	Notes
LLXXXXXXXX	t_{pd}, constant	Normal operating mode. Same as in the specification.	Delay time in PO DATA [7:0] can be varied using 2 bits of dot adjustment register SI REG [127:126].
LHXXXXXXXX		Small delay mode.	
HLXXXXXXXX		Switching Characteristics are minimized for 2 ns to 3 ns compare to the values in the specification.	
HHXXXXXXXX	t_{pd}, 2 ns to 3 ns minimized		

Details All Dot Adjustment Setting Using PWMCLK Division (PI REG1 [7:5])

$\overline{\text{RESET}}$	PI SEL	BCEN	PI REG1 [7:5]	PWMCLK Divisor	Operation and Function	Notes
H	H	H	LLL	PWMCLK = 8/8 PWMCLK (Hz)	The period of PWMCLK is set to equal the change in the PWM pulse width data. 1LSB.	When PI SEL = H is selected, 3 bits on MSB sides are corresponding to set of total dot adjustment by PWM frequency dividing. PI REG [7:5] varies the pulse width of PWM data corresponding to 1LSB for eight levels and adjusts brightness. This setting values affects pulse widths on all outputs.
H	H	H	LLH ↑ ⋮ ↓ HHL	1LSB = 1/8 divides PWMCLK	Variable does the frequency of PWMCLK to 1/8 of the minimal. It is set in 8 levels.	
H	H	H	HHH	PWMCLK = 1/8 PWMCLK (Hz)	The period of PWMCLK is set to one-eighth the change in the PWM pulse width data. 1LSB.	
⊓	X	H	LLL	PWMCLK = 8/8 PWMCLK (Hz)	The period of PWMCLK is set to equal the change in the PWM pulse width data. 1LSB.	
H	H	L	Refer to notes	Refer to notes	BCEN signal does not affect PWMCLK frequency dividing.	Data input is still enabled if BCEN = L. Output current level reflects input settings.

DAC3: Details of All Dot Adjustment Setting for DAC3 (PI REG2 [4:0])

$\overline{\text{RESET}}$	PI SEL	PI REG1 [4:0]	BCEN	Current Rate	Operation and Function	Notes
H	H	HHHHH	H	100% (1.0)	100% of base current value as set using DAC1 and DAC2 current adjustment and DAC4 dot adjustment	When PI SEL = H is selected, 5 bits on LSB side are corresponding to set of surface brightness adjustment. The output current can be set to one of 32 levels.
H	H	HHHHL ↑ ⋮ ↓ LLLLH	H	(0.9839) ↑ 1LSB = ±1.61% (±0.0161) ↓ (0.5161)	Any one of 32 levels in the range 100 to 50% of the current can be set. (1LSB = 1.61%) (5-bit DAC performance) 1LSB variation: ±1.61% Non linearity error: ±1/2LSB Differential non linearity error: ±1/2LSB (no guarantee for monotonicity)	
H	H	LLLLL	H	50% (0.5)	50% of base current value as set using DAC1 and DAC2 current adjustment and DAC4 dot adjustment	
⊓	X	HHHHH	H	100% (1.0)	Initial state after input of reset signal: 100% of base current value set as described above	
H	X	HHHHH	L	100% (1.0)	Initial state after input of DCEN signal: 100% of base current value set as described above	Data input is still enabled if BCEN = L. If BCEN = H, adjustment is performed at the same time.

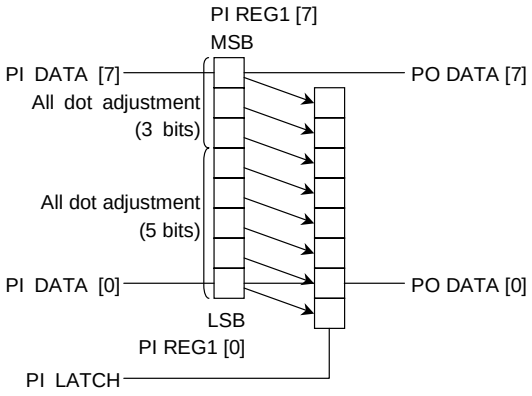
Detailed PWM 256 Grayscales Setting (PI REG2 [127:0], 16 × 1 word (8 bits))

$\overline{\text{RESET}}$	PI SEL	1 word (8 bits) of PI REG2	Output Pulse Rate	Operation and Function	Notes
H	L	HHHHHHHH	255/255 100%	Output pulse width is at its maximum value when input data is FF.	When PI SEL = L, The PWM grayscale controls the output pulse width. 1 word (8 bits) × 16 are transferred in parallel. 1 word is the PWM data of each output pulse width is set in 256 step. PI REG2 [7:0] → PWM data for OUT0. PI REG2 [15:8] → PWM data for OUT1. PI REG2 [127:120] → PWM data for OUT15. Minimum output pulse width is 1/PWMCLK.
H	L	HHHHHHHL ↑ ↓ LLLLLLLH	—	Outputs are OFF when the input data is 00. The input data can be used to control the PWM pulse width and hence generate 256 grayscales.	
H	L	LLLLLLLL	0/255 0%	Outputs are OFF when the input data is 00.	
	X	LLLLLLLL	0/255 0%	Early condition after the reset signal input is set in 0/256 (output off).	

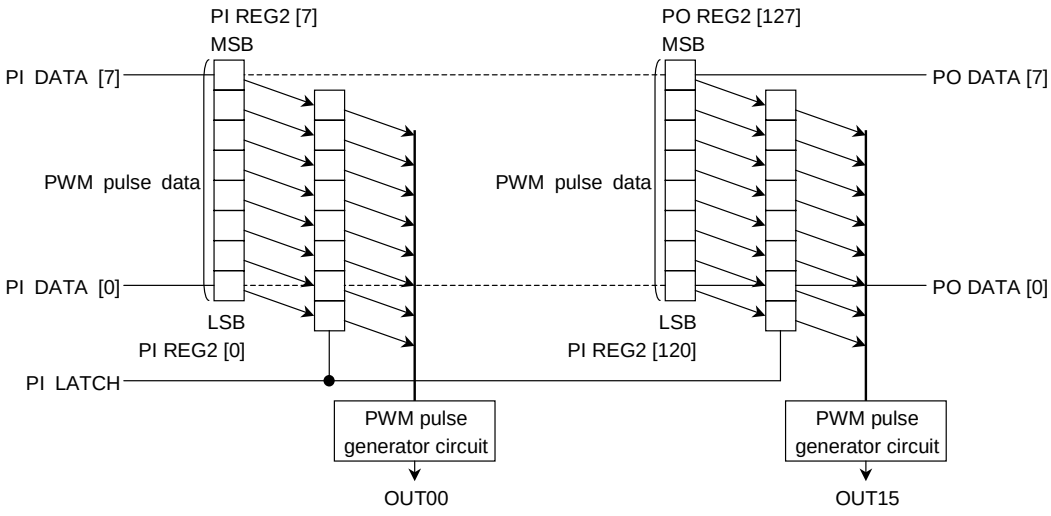
Polarity of Serial Input Data for All Dot Adjustment (PI REG [7:0]) and PWM 256 grayscales (PI REG2 [127:0])

Parallel Data Transfer Timing

PI SEL = H, Selects Data Input for All Dot Adjustment for DAC3.



PI SEL = L, Selects Data Input for PWM 256 Grayscales.



Reference Table: Output Current Setting Vales (1)

DAC1 (2 bit)			DAC2 (6 bit)			DAC3 (5 bit)			DAC4 (6 bit)		
No.	Input Data	Current Rate1	No.	Input Data	Current Rate2	No.	Input Data	Current Rate3	No.	Input Data	Current Rate4
3	11	1.00	63	111111	1.000	31	**11111	**1.000	63	111111	1.000
2	10	0.75	62	111110	0.990	30	11110	0.984	62	111110	0.987
1	01	0.50	61	111101	0.981	29	11101	0.968	61	111101	0.975
0	**00	**0.25	60	111100	0.971	28	11100	0.952	60	111100	0.962
—	—	—	59	111011	0.962	27	11011	0.936	59	111011	0.949
—	—	—	58	111010	0.952	26	11010	0.919	58	111010	0.937
—	—	—	57	111001	0.943	25	11001	0.903	57	111001	0.924
—	—	—	56	111000	0.933	24	11000	0.887	56	111000	0.911
—	—	—	55	110111	0.924	23	10111	0.871	55	110111	0.898
—	—	—	54	110110	0.914	22	10110	0.855	54	110110	0.886
—	—	—	53	110101	0.905	21	10101	0.839	53	110101	0.873
—	—	—	52	110100	0.895	20	10100	0.823	52	110100	0.860
—	—	—	51	110011	0.886	19	10011	0.807	51	110011	0.848
—	—	—	50	110010	0.876	18	10010	0.790	50	110010	0.835
—	—	—	49	110001	0.867	17	10001	0.774	49	110001	0.822
—	—	—	48	110000	0.857	16	10000	0.758	48	110000	0.810
—	—	—	47	101111	0.848	15	01111	0.742	47	101111	0.797
—	—	—	46	101110	0.838	14	01110	0.726	46	101110	0.784
—	—	—	45	101101	0.829	13	01101	0.710	45	101101	0.771
—	—	—	44	101100	0.819	12	01100	0.694	44	101100	0.759
—	—	—	43	101011	0.820	11	01011	0.677	43	101011	0.746
—	—	—	42	101010	0.800	10	01010	0.661	42	101010	0.733
—	—	—	41	101001	0.791	9	01001	0.645	41	101001	0.721
—	—	—	40	101000	0.781	8	01000	0.629	40	101000	0.708
—	—	—	39	100111	0.771	7	00111	0.613	39	100111	0.695
—	—	—	38	100110	0.762	6	00110	0.597	38	100110	0.683
—	—	—	37	100101	0.752	5	00101	0.581	37	100101	0.670
—	—	—	36	100100	0.743	4	00100	0.565	36	100100	0.657
—	—	—	35	100011	0.733	3	00011	0.549	35	100011	0.644
—	—	—	34	100010	0.724	2	00010	0.532	34	100010	0.632
—	—	—	33	100001	0.714	1	00001	0.516	33	100001	0.619
—	—	—	32	100000	0.705	0	00000	0.500	32	100000	0.606
—	—	—	31	011111	0.695	—	—	—	31	011111	0.594
—	—	—	30	011110	0.686	—	—	—	30	011110	0.581
—	—	—	29	011101	0.676	—	—	—	29	011101	0.568
—	—	—	28	011100	0.667	—	—	—	28	011100	0.556
—	—	—	27	011011	0.657	—	—	—	27	011011	0.543
—	—	—	26	011010	0.648	—	—	—	26	011010	0.530
—	—	—	25	011001	0.638	—	—	—	25	011001	0.517
—	—	—	24	011000	0.629	—	—	—	24	011000	0.505
—	—	—	23	010111	0.619	—	—	—	23	010111	0.492
—	—	—	22	010110	0.610	—	—	—	22	010110	0.479
—	—	—	21	010101	0.600	—	—	—	21	010101	0.467
—	—	—	20	010100	0.591	—	—	—	20	010100	0.454
—	—	—	19	010011	0.581	—	—	—	19	010011	0.441
—	—	—	18	010010	0.571	—	—	—	18	010010	0.429
—	—	—	17	010001	0.562	—	—	—	17	010001	0.416
—	—	—	16	010000	0.552	—	—	—	16	010000	0.403
—	—	—	15	001111	0.543	—	—	—	15	001111	0.390
—	—	—	14	001110	0.533	—	—	—	14	001110	0.378
—	—	—	13	001101	0.524	—	—	—	13	001101	0.365
—	—	—	12	001100	0.514	—	—	—	12	001100	0.352
—	—	—	11	001011	0.505	—	—	—	11	001011	0.340
—	—	—	10	001010	0.495	—	—	—	10	001010	0.327
—	—	—	9	001001	0.486	—	—	—	9	001001	0.314
—	—	—	8	001000	0.476	—	—	—	8	001000	0.302
—	—	—	7	000111	0.467	—	—	—	7	000111	0.289
—	—	—	6	000110	0.457	—	—	—	6	000110	0.276
—	—	—	5	000101	0.448	—	—	—	5	000101	0.263
—	—	—	4	000100	0.438	—	—	—	4	000100	0.251
—	—	—	3	000011	0.429	—	—	—	3	000011	0.238
—	—	—	2	000010	0.419	—	—	—	2	000010	0.225
—	—	—	1	000001	0.410	—	—	—	1	000001	0.213
—	—	—	0	**000000	**0.4	—	—	—	0	**000000	0.200

Note 1: **: Indicates post-reset initialization value ($\overline{\text{RESET}}$= L).

Note 2: The formula for calculating resistance settings is as follows: This value is theory value. Actual current value contains error and so on in this value.
REXT [kΩ] = { (1.8 × current rate 1 × current rate 2 × current rate 3) × (current rate 4 × 34.5) } ÷ output current [mA]

Reference Table: Output Current Setting Value (2)
Reference Value for Standard Current Adjustment Under Conditions:
R_{EXT} = 910 kΩ (fixed), All Dot Adjustment = MSB and Dot Adjustment = MSB

Unit [mA]

		DAC 2															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DAC 1	0	5.8	5.9	6.0	6.2	6.3	6.4	6.6	6.7	6.8	7.0	7.1	7.2	7.4	7.5	7.6	7.8
	1	11.6	11.8	12.1	12.3	12.6	12.9	13.1	13.4	13.7	13.9	14.2	14.5	14.7	15.0	15.3	15.5
	2	17.3	17.7	18.1	18.5	18.9	19.3	19.7	20.1	20.5	20.9	21.3	21.7	22.1	22.5	22.9	23.3
	3	23.1	23.6	24.2	24.7	25.2	25.8	26.3	26.8	27.3	27.9	28.4	28.9	29.5	30.0	30.5	31.1

		DAC 2															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DAC 1	0	7.9	8.0	8.2	8.3	8.4	8.6	8.7	8.8	9.0	9.1	9.2	9.4	9.5	9.6	9.7	9.9
	1	15.8	16.1	16.3	16.6	16.8	17.1	17.4	17.6	17.9	18.2	18.4	18.7	19.0	19.2	19.5	19.8
	2	23.7	24.1	24.5	24.9	25.3	25.7	26.1	26.5	26.9	27.3	27.7	28.1	28.4	28.8	29.2	29.6
	3	31.6	32.1	32.6	33.2	33.7	34.2	34.8	35.3	35.8	36.3	36.9	37.4	37.9	38.5	39.0	39.5

		DAC 2															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
DAC 1	0	10.0	10.1	10.3	10.4	10.5	10.7	10.8	10.9	11.1	11.2	11.3	11.5	11.6	11.7	11.9	12.0
	1	20.0	20.3	20.6	20.8	21.1	21.3	21.6	21.9	22.1	22.4	22.7	22.9	23.2	23.5	23.7	24.0
	2	30.0	30.4	30.8	31.2	31.6	32.0	32.4	32.8	33.2	33.6	34.0	34.4	34.8	35.2	35.6	36.0
	3	40.0	40.6	41.1	41.6	42.2	42.7	43.2	43.8	44.3	44.8	45.3	45.9	46.4	46.9	47.5	48.0

		DAC 2															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
DAC 1	0	12.1	12.3	12.4	12.5	12.7	12.8	12.9	13.1	13.2	13.3	13.5	13.6	13.7	13.8	14.0	14.1
	1	24.3	24.5	24.8	25.1	25.3	25.6	25.8	26.1	26.4	26.6	26.9	27.2	27.4	27.7	28.0	28.2
	2	36.4	36.8	37.2	37.6	38.0	38.4	38.8	39.2	39.6	40.0	40.4	40.8	41.2	41.5	41.9	42.3
	3	48.5	49.0	49.6	50.1	50.6	51.2	51.7	52.2	52.7	53.3	53.8	54.3	54.9	55.4	55.9	56.5

Note: If the second decimal is less than five, round off to the first decimal place. If the second decimal is more than five, round up to the first decimal place.

Temperature detection function (can be monitored via the ALARM1 pin.)

Perform two-stage temperature detection as described in the table below (TSD1/TSD2).

Junction Temperature °C	ALARM1	Output Terminals OUT (15:0)	Function
−40 to 120	OFF (high impedance)	Normal operation	—
120 to	ON (low level)	Normal operation	When the chip temperature reaches the specified range the ALARM1 signal goes Low (TSD1), Other functions are not affected.
140 to	ON (low level)	Forced OFF (high impedance)	When the chip temperature reaches the specified range the ALARM1 signal goes Low and all output pins are turned OFF (TSD2). Outputs are re-enabled on the TSENA signal goes Low or when the $\overline{\text{RESET}}$ signal goes Low. Neither of these causes the internal data to be reset. If $\overline{\text{RESET}}$ pin = L, all internal data is reset.

Output-Open Detection Function (can be monitored via the ALARM2 pin.)

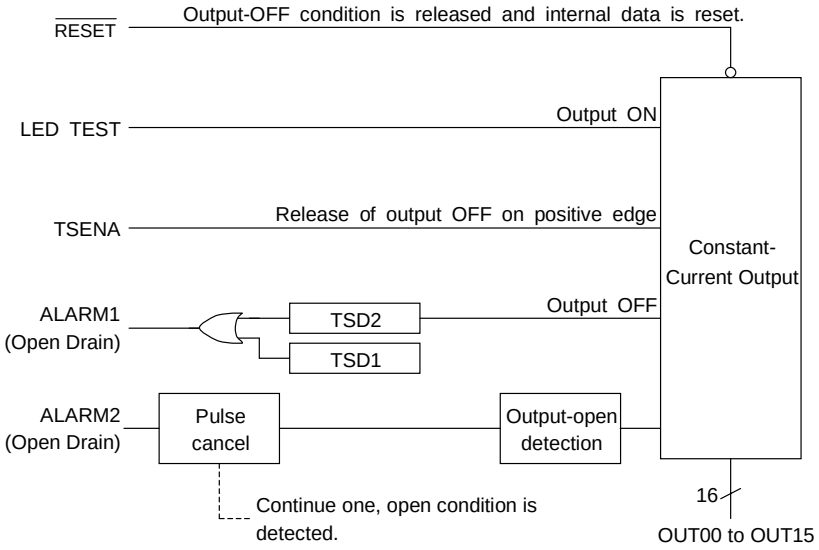
Reform output-open detection as described in the table below.

Output Voltage V (typ.)	ALARM2	Function
$\geqq V_{DD} \times 0.04$	OFF (high impedance)	—
$\leqq V_{DD} \times 0.04$	ON (low level)	The output-open condition is detected when the ARARM2 pin signal is ON and the specified voltage level is detected. (it is also detected when the output voltage falls to near GND for some reason)

Pulse Cancellation Circuit
(when monitored using output-open detection pin ARARM2.)

PWMCLK	ALARM2	Function
Input signal	Operating	Output open detection operates when the LED string is disconnected for the specified period.
No input	Always high impedance	The device incorporates pulse cancel circuit to avoid detecting instantaneous errors, for example, output switching noise. However, if there is no input on PWMCLK, ALARM2 output will not be turned ON (low level).

Block Diagram of Protection Circuit

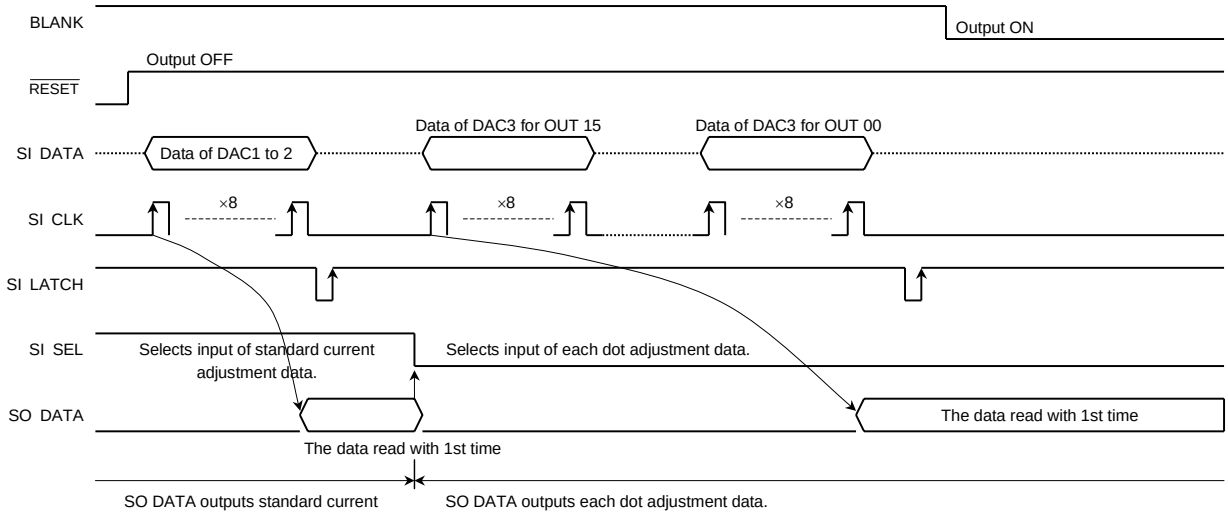


Protection Circuit Function
Operating Chart (terminals for TESNA, ALARM1 and outputs OUT00 to OUT15)

TSENA	$\overline{\text{RESET}}$	Junction Temperature			ALARM1	OUT00 to OUT15	Function
		$T_j \leqq 120°C$	TSD1 $120 \leqq T_j$	TSD2 $140 \leqq T_j$			
X	L	O	—	—	high impedance	OFF	Device reset
X	H	O	—	—	high impedance	OFF	Outputs operate normally.
X	L	—	O	—	ON (low level)	OFF	Device reset
X	H	—	O	—	ON (low level)	Normal operation	ALARM1 goes Low, indicating a rise in temperature. Outputs operate normally.
X	L	—	—	O	ON (low level)	Forced OFF	Even after a reset, if the junction temperature is high, outputs are forced OFF.
X	H	—	—	O	ON (low level)	Forced OFF	ALARM1 goes Low, indicating a rise in temperature. Outputs are forced OFF.

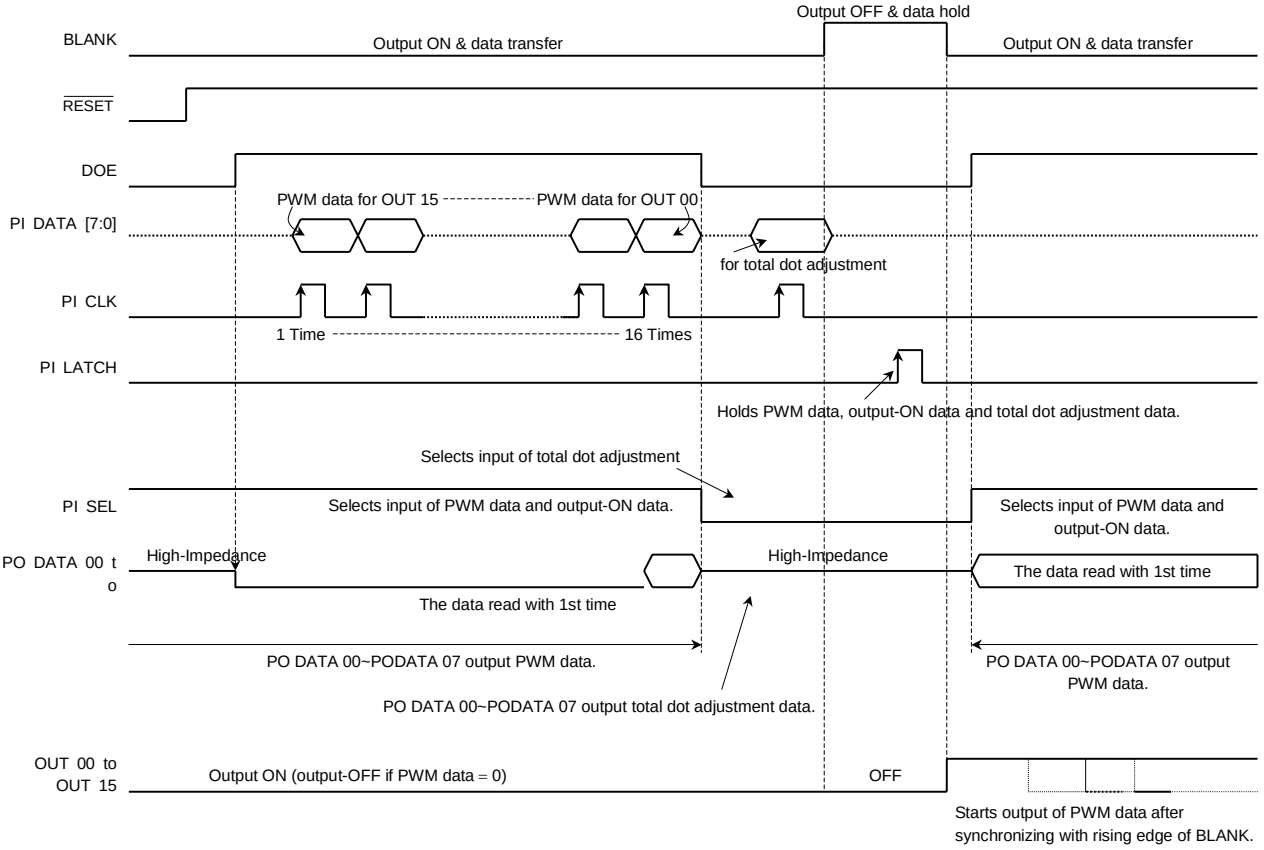
Note: The internal operation of the TSD circuit is independent of the TSENA and $\overline{\text{RESET}}$ pin voltage levels. When pins TSENA and RESET are High, the forced OFF mode by the TSD circuit can not be canceled.

Serial Data Input Timing Chart



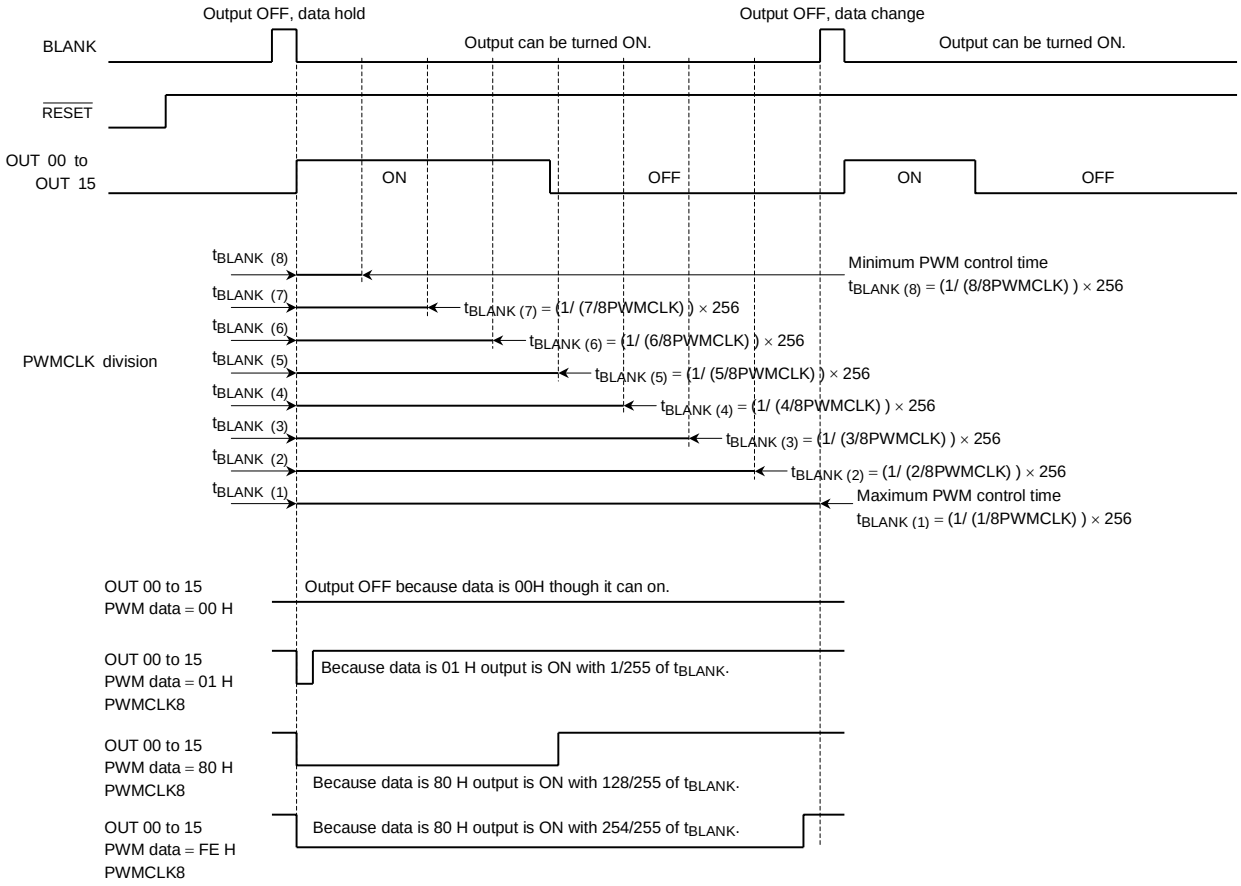
Note 10: Serial data input has no effect on the ON/OFF state of the outputs.
When the SI LATCH signal holds the serial data, the output current values and output pulse width are affected.

Parallel Data Input Timing Chart



Note 11: The BLANK signal has not effect on parallel data input. The PWM pulse can be controlled using the BLANK signal.
It is recommended that, on completion of data transfer, BLANK be set to High and outputs be turned OFF.

PWM Operating Timing Chart and All Bit Adjustment Using Division by PWMCLK



Note 12: PWM operation timing:

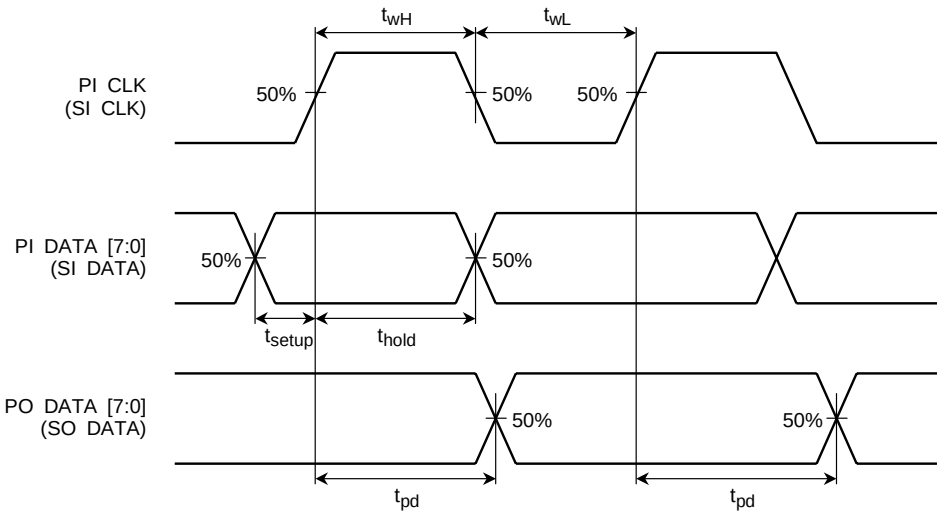
PWM pulse output on the output pins is initiated when BLANK goes Low. (there is simultaneous output on all 16 pins)
Output pulse only once toward BLANK signal's changing once in L from H.
Hence, if PWM data is to be re-used, BLANK must be pulled Low again.

PWMCLK division:

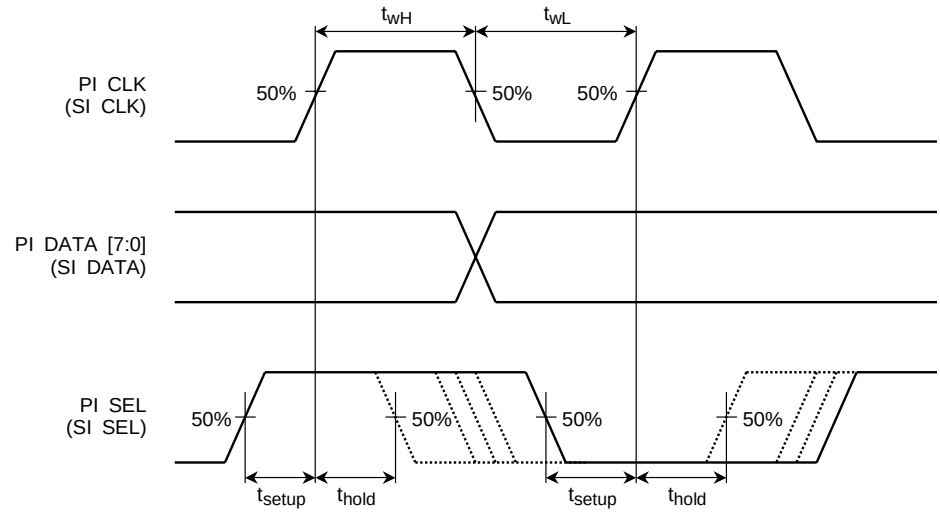
As shown in the central part of the upper figure, the brightness of the LED module can be set to any one of eight levels without adjusting the current value, simply by dividing by PWMCLK.
For large-scale brightness adjustment, division by PWMCLK is recommended.

Logic Input and Output Timing Waveforms

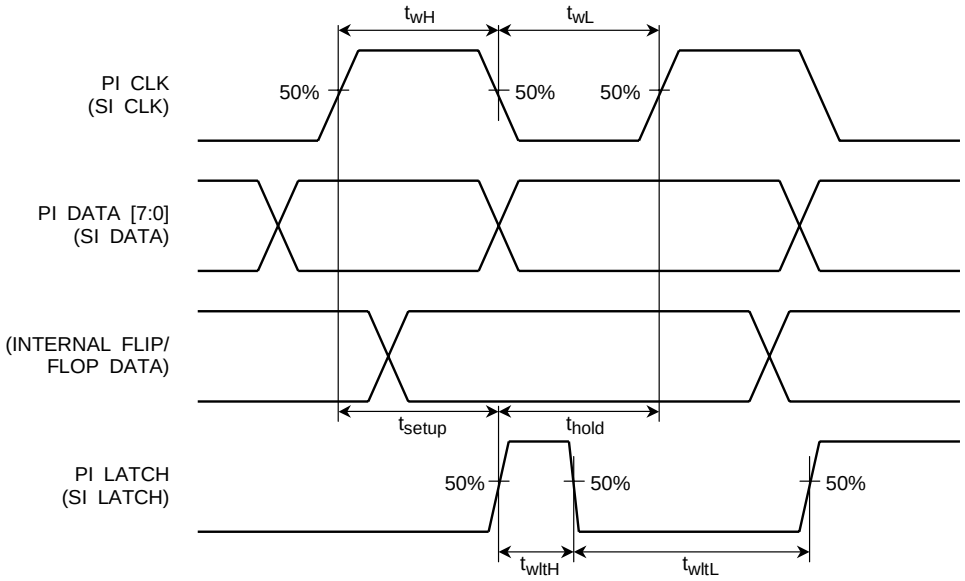
1. PI CLK (SI CLK) vs PI DATA [7:0] (SI DATA)
PI CLK (SI CLK) vs PO DATA [7:0] (SO DATA)



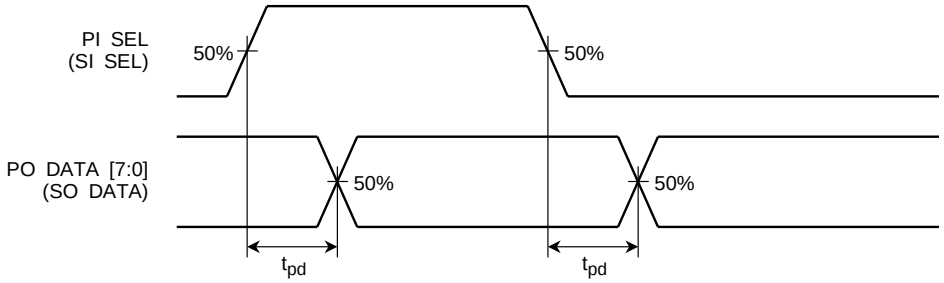
2. PI SEL (SI SEL) vs PI CLK (SI CLK)



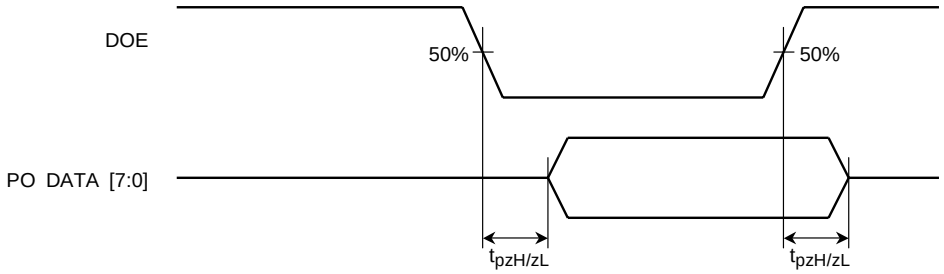
3. PI LATCH (SI LATCH) vs PI CLK (SI CLK)



4. PI SEL (SI SEL) vs PO DATA [7:0] (SO DATA)

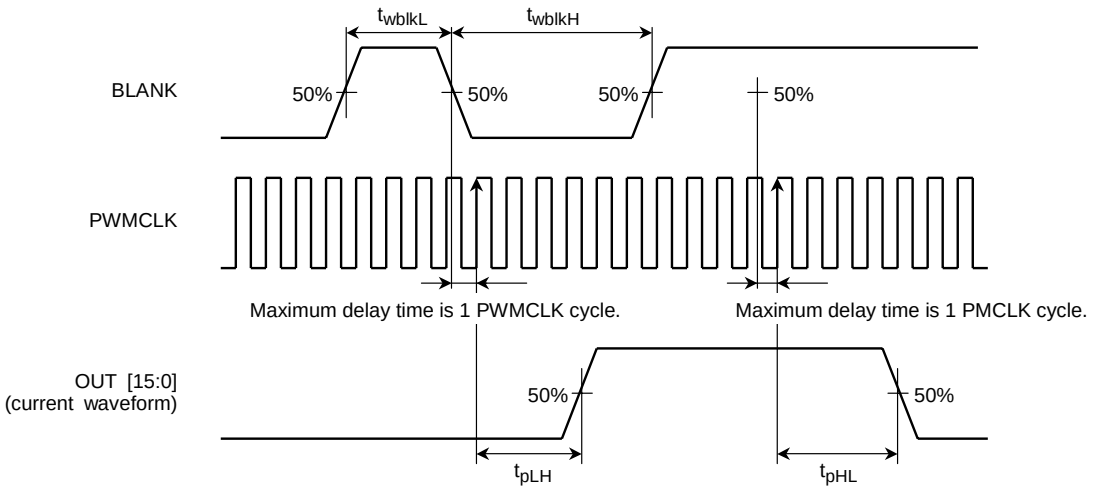


5. DOE vs PO DATA [7:0]

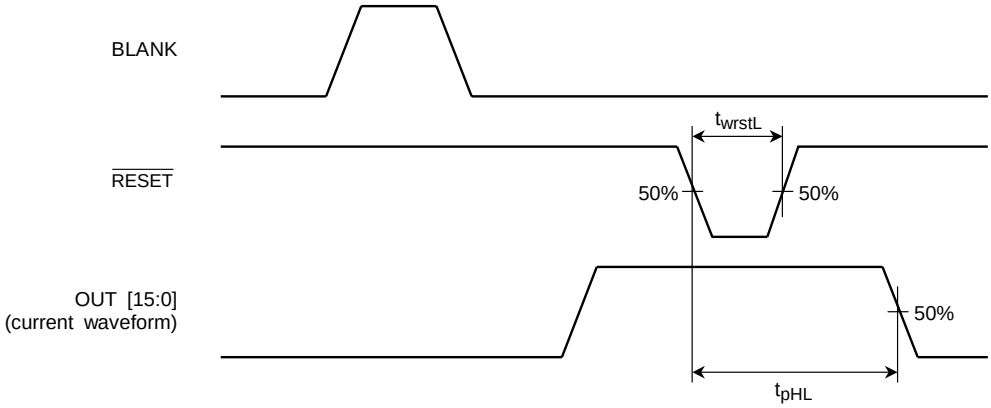


Logic Input and Constant-current Output Timing Waveforms

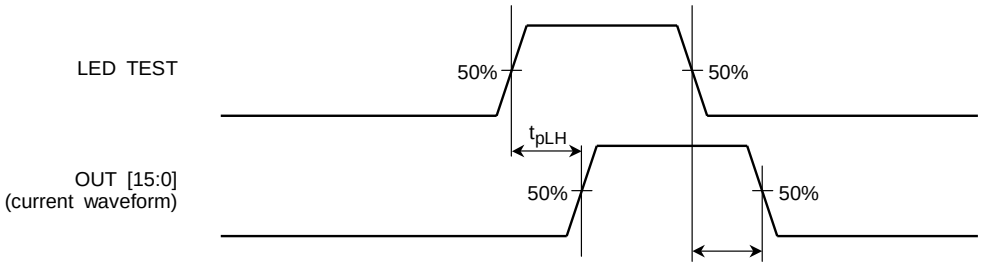
1. BLANK vs OUT [15:0] with PWMCLK



2. $\overline{\text{RESET}}$ vs OUT [15:0]

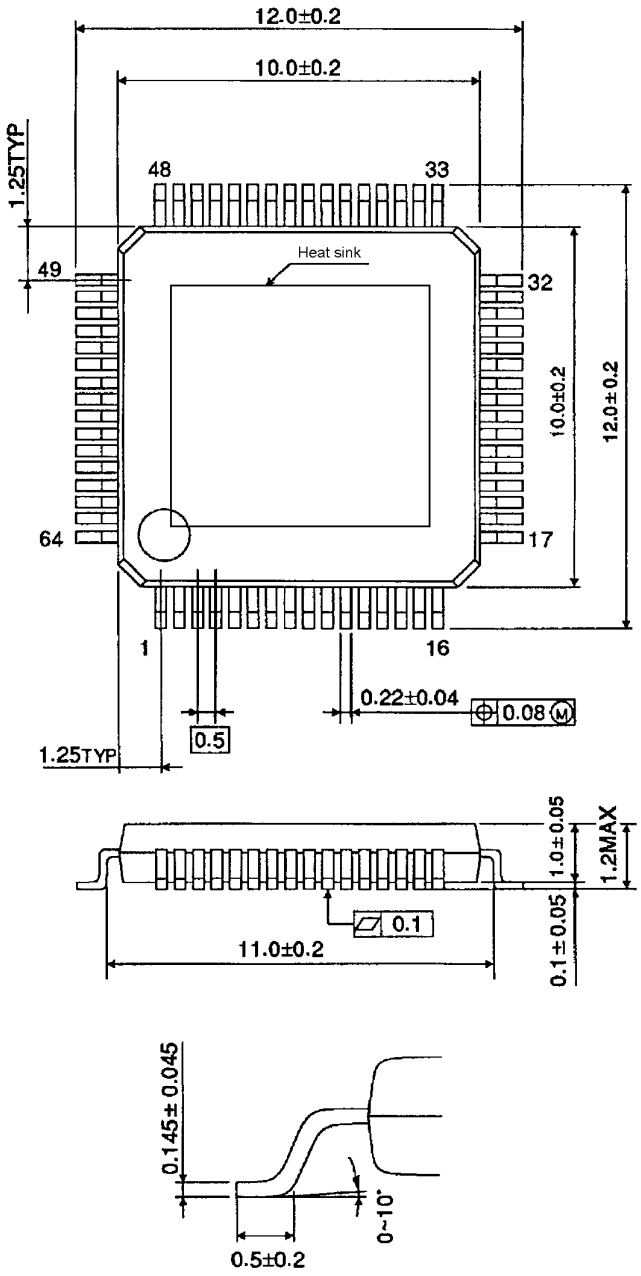


3. LED TEST vs OUT [15:0]



Package Dimensions

HQFP64-P-1010-0.50 Unit : mm



Weight: 0.26 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.
Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs

(1) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(2) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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