TOSHIBA Bi-CMOS INTEGRATED CIRCIUTS SILICON MONOLITHIC

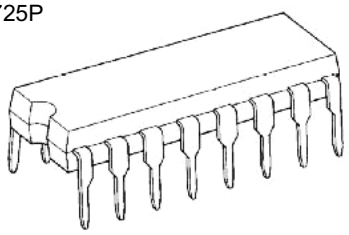
T B 6 2 7 2 5 P / F / F N

8BIT CONSTANT CURRENT LED DRIVER OF OPERATING VOLTAGE 3.3V

TB62725 series is the constant current driver designed for LED and the LED display. Output current value is set with one resistor with the outside.
Then, all the output becomes the about same current.
This driver builds in the constant current output of eight bits, the shift register of eight bits, the latch of eight bits and gate circuit.
This driver is designed by using the BI-CMOS process.

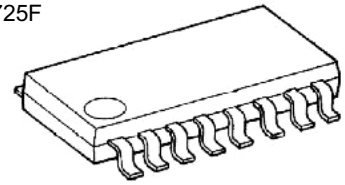
FEATURE
*Output Current Capability and the number of the output :
90mA X 8 outputs
*Constant Current Range : 5 to 90mA
*Application Output Voltage :
0.7V (output current 40 to 80 mA)
0.4V (output current 5 to 40 mA)
*For Annode Common LED
*Input Signal Voltage Level :
3.3V CMOS Level (Shmitt Triggered Input)
*Power Supply Voltage Range VDD=3.0 to 3.6V
*Muximum output terminal voltage 17V
*Serial and Pararell Data Transfer Rate :
20MHz (max, Cascade Connection)
*Operation Temperature Range :
Topr= -40 to 85 degrees
*Package :
Type P : DIP16-P-300-2.56A
Type F : SSOP16-P-225-1.00
Type FN : SSOP16-P-225-0.65
*Package and Pin Layout : Same as the TB62705 series.

TB62725P



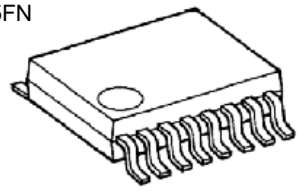
DIP16-P-300-2.56A

TB62725F



SSOP16-P-225-1.00

TB62725FN



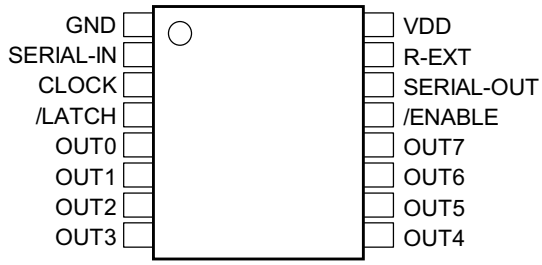
SSOP16-P-225-0.65

Weight : 1.11 g(Typ.) - - - Type P
0.14 g(Typ.) - - - Type F
0.07 g(Typ.) - - - Type FN

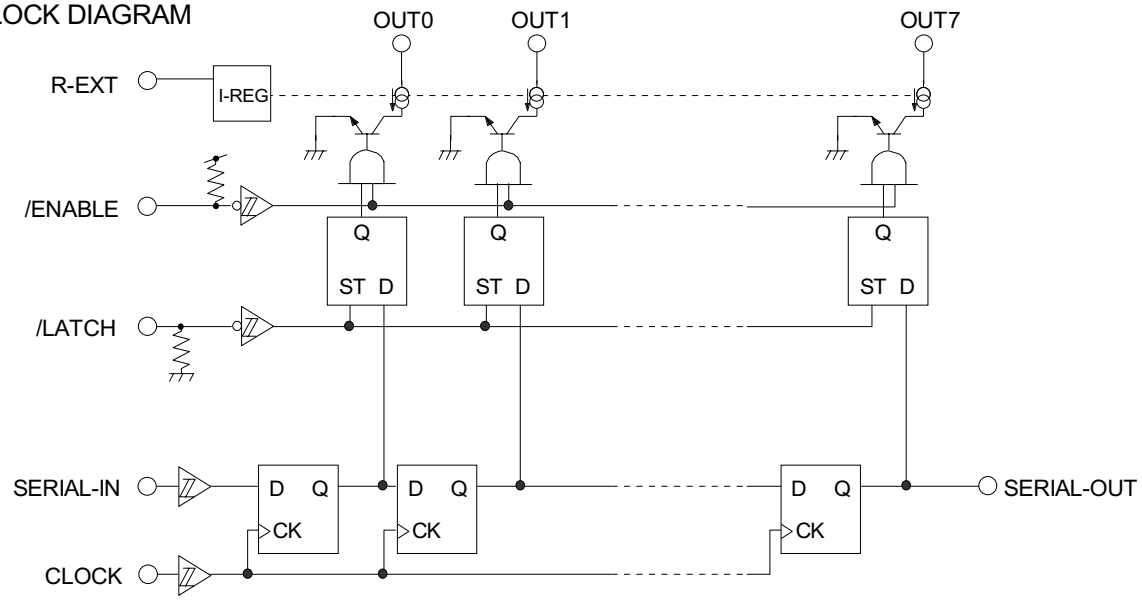
*Constant Current Error bitween bits (All Output On)

Output Voltage	Current Error between bits	Current Error between ICs	Output Current
>= 0.4V	+/- 6%	+/- 15%	2 to 40 mA
>= 0.7V			2 to 90 mA

Pin layout (TOP VIEW)



BLOCK DIAGRAM

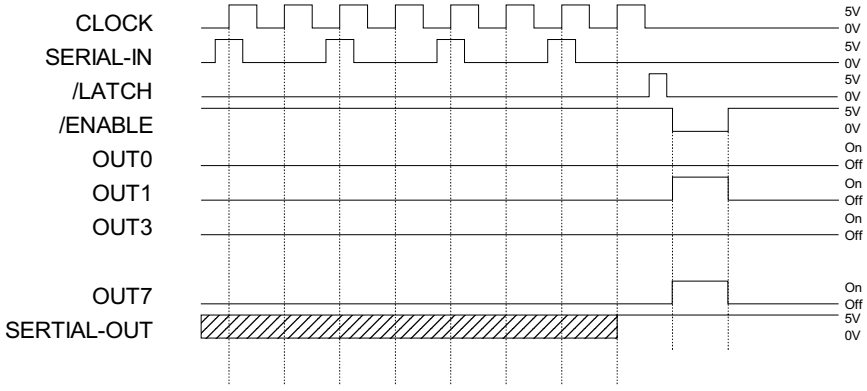


TRUTH TABLE

CLOCK	/LATCH	/ENABLE	SERIAL-IN	OUT0 --- OUT5 --- OUT7	SERIAL-OUT
UP	H	L	Dn	Dn --- Dn-5 --- Dn-7	Dn-7
UP	L	L	Dn+1	No Change	Dn-6
UP	H	L	Dn+2	Dn+2 --- Dn-3 --- Dn-5	Dn-5
DOWN	X	L	Dn+3	Dn+2 --- Dn-3 --- Dn-5	Dn-5
DOWN	X	H	Dn+3	Off	Dn-5

Note) "OUT0 to 7 = On" in case of Dn= "H" Level and "OUT0 to 7 = Off" in case of Dn= "L" Level.
A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

TIMING DIAGRAM



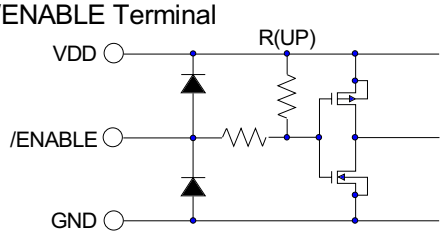
Note) Latches are level sensitive, not rising edge sensitive and not syncronus CLOCK.
Input of LATCH-terminal to "H" level, data passes latches and input to "L" level, data hold latches.
Input of ENABLE-terminal to "H" level, all output (OUT0 to 7) off.

TERMINAL DISCRIPTION

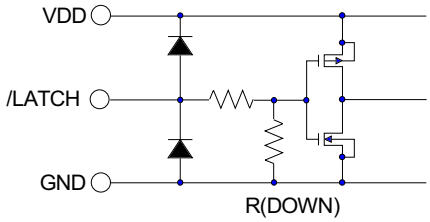
PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal of a serial-data for shift-register
3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	/LATCH	Input terminal of a data strobe. Latches passes data with "H" level input of LATCH-terminal, and hold data with "L" level input.
5~12	OUT0 to 7	Output terminals.
13	/ENABLE	Input terminal of output enable. All outputs (OUT0 to 7) do off with "H" level input of ENABLE-terminal, and do on with "L" level input.
14	SERIAL-OUT	Output terminal of a serial-data for next SERIAL-IN terminal.
15	R-EXT	Input terminal of connects with a resister for to set up all output current.
16	VDD	5V Supply voltage terminal

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

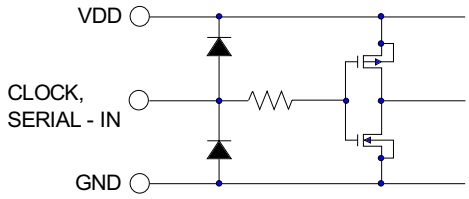
1. /ENABLE Terminal



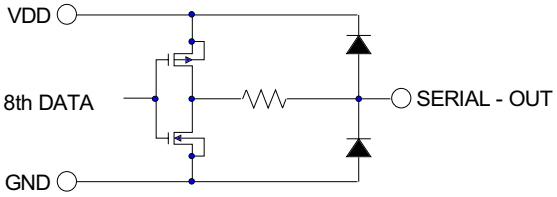
2. /LATCH Terminal



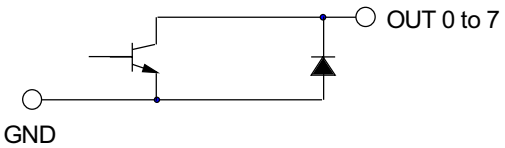
3. CLOCK,SERIAL-IN Terminal



4. SERIAL-OUT Terminal



5. OUT0 to 7 Terminal



MAXIMUM RATINGS (Ta = 25degC)

CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	VDD	0 to 7	V
Input Voltage	VIN	-0.2 to VDD+0.2	
Output Current	IOUT	+90	mA/ch
Output Voltage	VOUT	-0.5 to 17	V
Power Dissipation	Pd1	Type P : 1.47(Free Air)	W
	Pd2	Type F and FN : 0.37 (Free Air), 0.78 (On PCB)	
Thrmal Resistance	Rth(j-a)1	Type P : 85(Free Air)	degC/W
	Rth(j-a)2	Type F and FN : 330 (Free Air),160 (On PCB)	
Oparating Temperature	Topr	-40 to 85	degC
Storage Temperature	Tstg	-55 to 150	

Note) Type P : Ambient temperature delated above 25degC in the proportion of 11.76 mW/degC.
Type F and FN : Ambient temperature delated above 25degC in the proportion of 7.69 mW/degC.
Condition) On PCB at 50 X 50 X 1.6mm Cu <= 40% (Glass Epoxy PCB)

RECOMMENDED OPERATING CONDITION (Ta=-40 to 85degC unless otherwise noted)

CHARACTERISTICS	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD		3	3.3	3.6	V
Output Voltage	VOUT			0.7	4	V
Output Current	IOUT	Each DC 1 Circuit	2		70	mA/ch
	IOH	SERIAL-OUT			-1	mA
	IOL				1	
Input Voltage	VIH		0.7VDD		VDD +0.15	V
	VIL		-0.15		0.3VDD	
Clock Frequency	fCLK	Cascade Connected			20	MHz
/LATCH Pulse Width	tw /LATCH		50			ns
CLOCK Pulse Width	tw CLOCK				25	
/ENABLE Pulse Width	tw /ENABLE	Upper IOUT = 20 mA	2000			
		Lower IOUT = 20 mA	4500			
Setup Time for CLOCK Terminal	tsetup1		10			
Hold Time for CLOCK Terminal	thold		5			
Setup Time for /LATCH Terminal	tsetup2		50			

ELECTRICAL CHARACTERISTICS (VDD=3.3V, Ta=25degC unless otherwise noted)

CHARACTERISTICS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	VDD	Normal Operation	3.0	3.3	3.6	V
Output Current	IOUT1	VOUT=0.4V,REXT=490ohms	31.9	37.5	43.1	mA
	IOUT2	VOUT=0.7V,REXT=250ohms	62.6	73.6	84.6	
Output Current	dIOUT1	VOUT>=0.4V,REXT=490ohms All outout on.		+/-1.5	+/-6	%
Error bitween bits	dIOUT2	VOUT>=0.7V,REXT=250ohms All outout on.		+/-1.5	+/-6	
Output Leakage Current	IOZ	VOUT=15.0V		1.0	5.0	uA
Input Voltage	VIH		0.7 VDD		VDD	V
	VIL		GND		0.3 VDD	
SOUT Terminal	VOL	IOH=+1mA			0.4	
Output Voltage	VOH	IOL=-1mA	2.8			
Output Currnet Supply Voltage Reguration	%/VDD	VDD = 3V to 3.6V		+/-1.5	+/-5.0	%
Pull up Resistor	R(up)	/ENABLE Terminal	100	200	400	kohms
Pull down Resistor	R(down)	/LATCH Terminal	125	250	500	
Supply Current	IDD(OFF)1	REXT=OPEN,VOUT=15.0V		1	2	mA
	IDD(OFF)2	REXT=490Ohms, VOUT=15V,OUT0 to 7 are Off.	1	3	5	
	IDD(OFF)3	REXT=250Ohms, VOUT=15V,OUT0 to 7 are Off.	3	6	8	
	IDD(ON)1	REXT=490Ohms, VOUT=0.7V,OUT0 to 7 are On.		7		
		Same as the avobe , Ta=-40degC			14	
	IDD(ON)2	REXT=250Ohms, VOUT=0.7V,OUT0 to 7 are On.		13		
		Same as the avobe , Ta=-40degC			25	

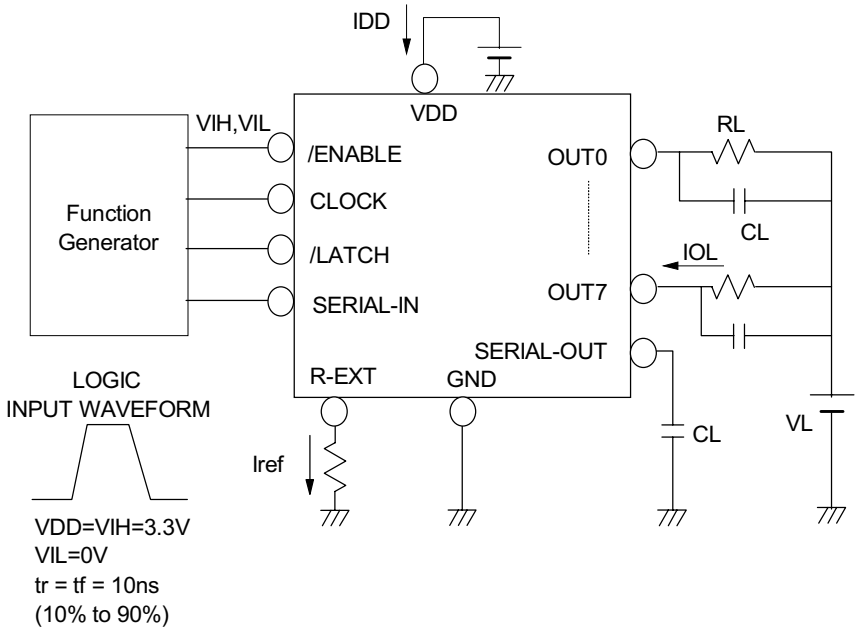
SWITCHING CHARACTERISTICS (Ta=25degC unless otherwise noted)

CHARACTERISTICS	SYBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Propagation Delay Time	tpLH1	CLK - OUTn, /LATCH="H",/ENABLE="L"		140		ns
	tpLH2	/LATCH - OUTn, /ENABLE="L"		140		
	tpLH3	/ENABLE - OUTn, /LATCH="H"		140		
	tpLH	CLK - SERIAL OUT		5		
	tpHL1	CLK - OUTn, /LATCH="H",/ENABLE="L"		170		
	tpHL2	/LATCH - OUTn, /ENABLE="L"		170		
	tpHL3	/ENABLE - OUTn, /LATCH="H"		170		
	tpHL	CLK - SERIAL OUT		6		
Output Rise Time	t or	Voltage Waveform 10% to 90%		70		
Output Fall Time	t of	Voltage Waveform 90% to 10%		90		
Muximum CLOCK Rise Time	tr	Cascade connection isn't guarantee. (Note1)			5	us
Muximum CLOCK Fall Time	tf				5	

Condition : (Refer to test circuit.)
Ta= 25 degC, VDD=VIH=3.3V, VOUT=0.7V, VIL=0V, REXT=490ohms, VL=3.0V, RL=60ohms, CL=10.5pF

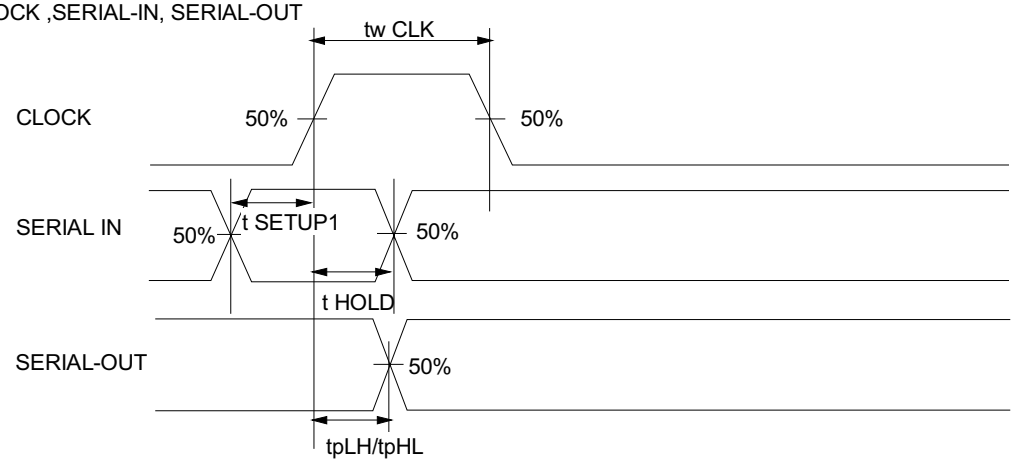
Note 1 : When tf / tf of clock wave form is enlarged at the time as the cascade connection, the timing condition which is necessary for the data transfer may not be able to be secured. Give careful consideration to the timing condition.

TEST CIRCUIT

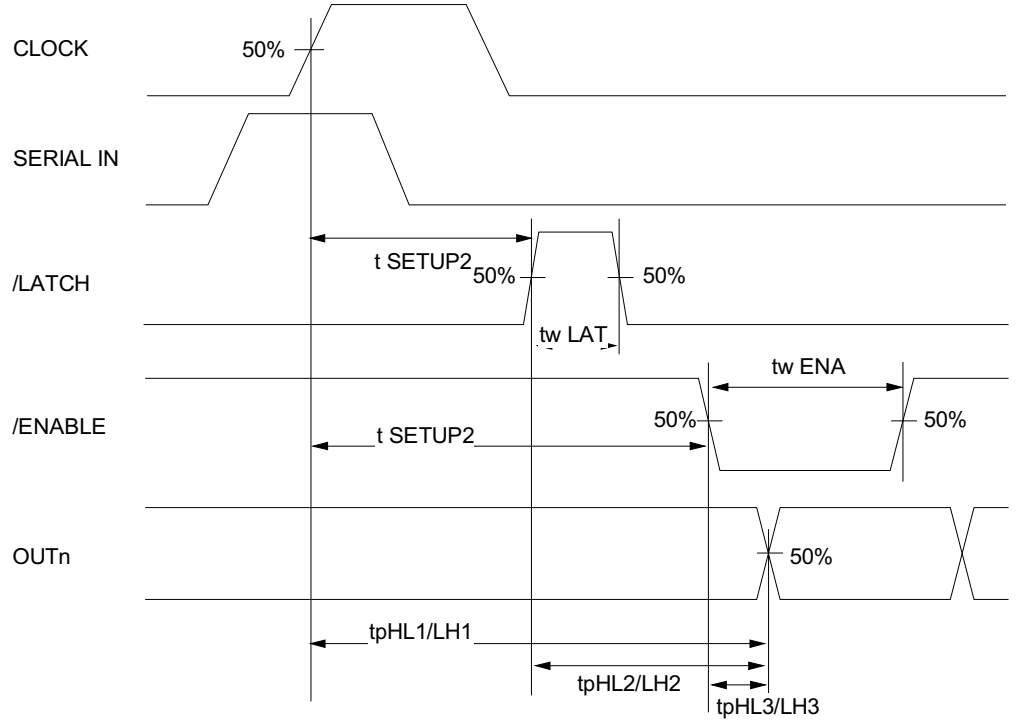


TIMING WAVEFORM

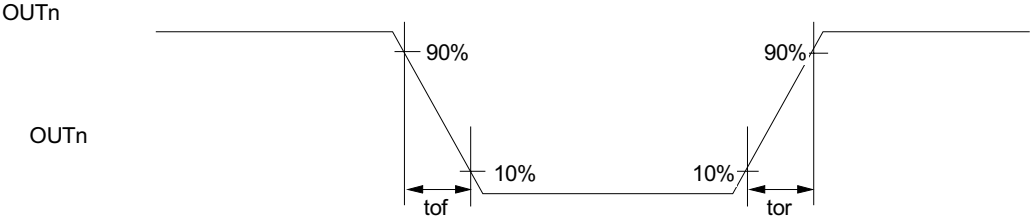
1. CLOCK ,SERIAL-IN, SERIAL-OUT



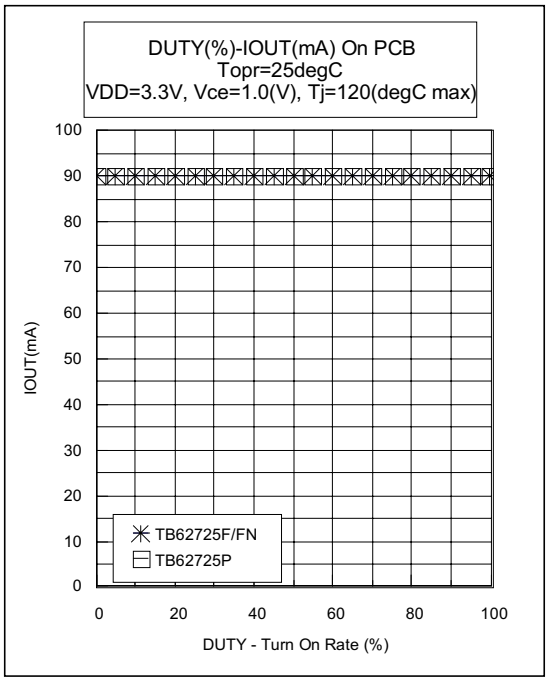
2. CLOCK, SERIAL-IN , /LATCH, /ENABLE, OUTn

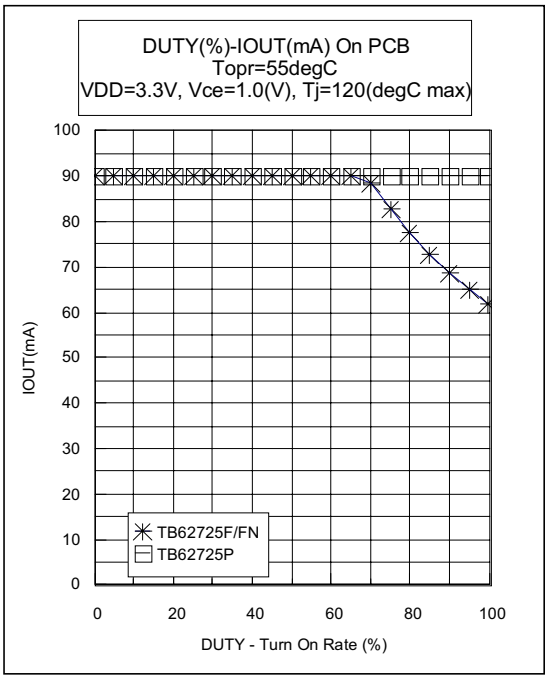


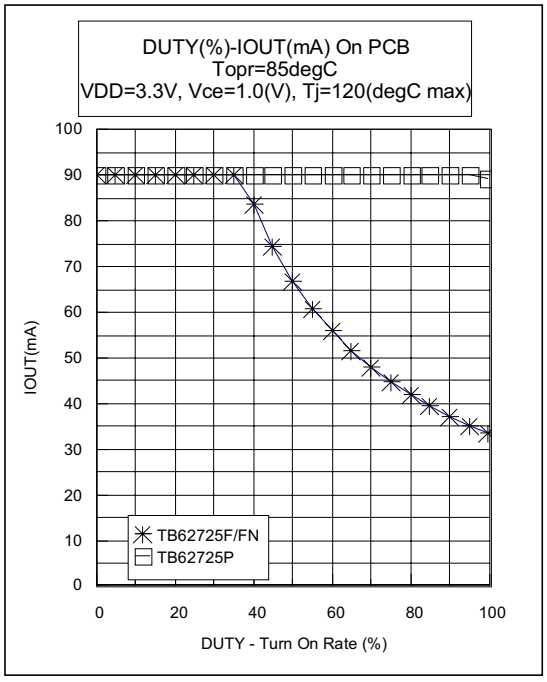
3. OUTn



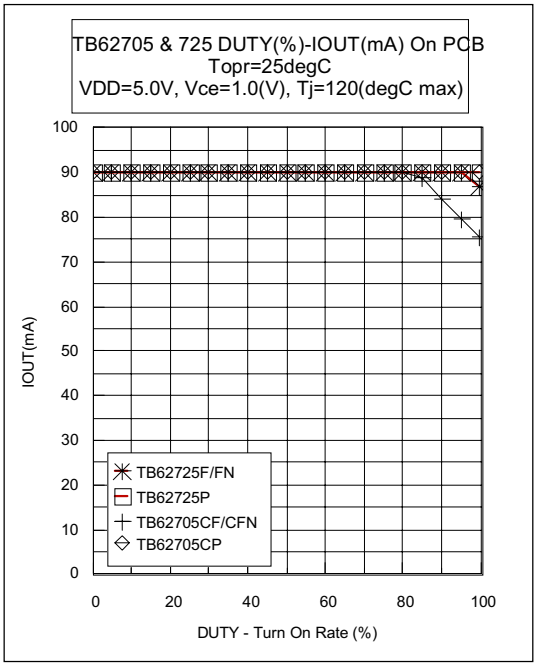
OUTPUT CURRNET vs Duty (LED Turn On Rate)

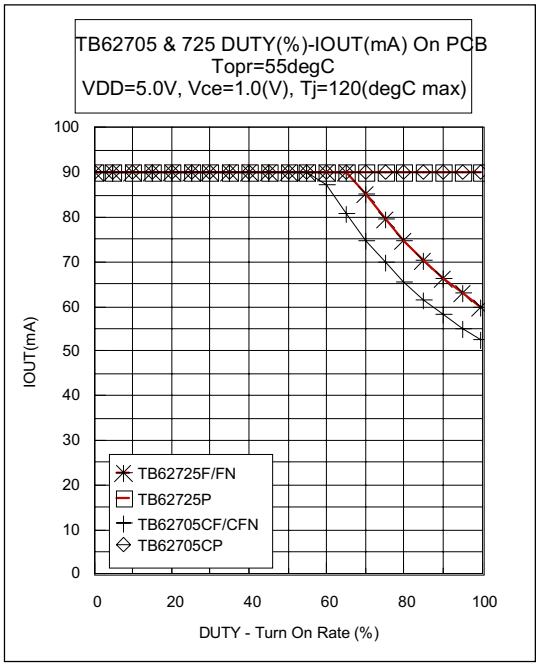


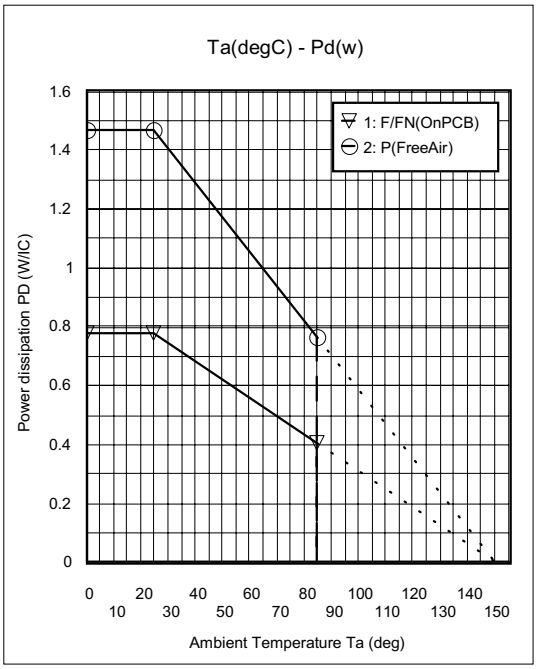


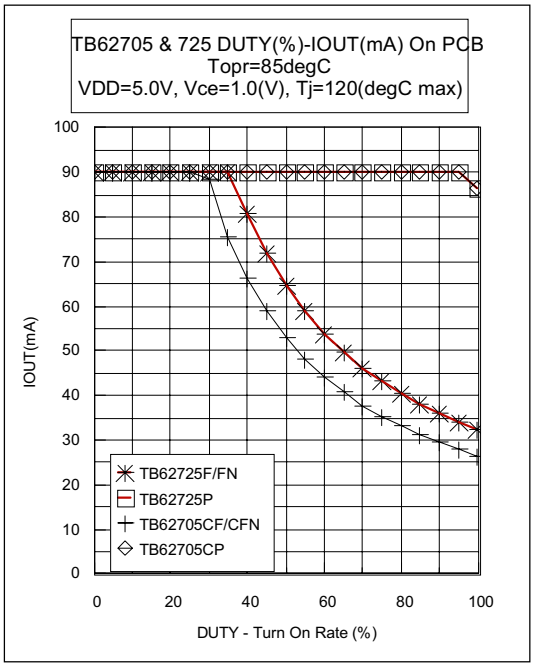


OUTPUT CURRNET vs Duty (LED Turn On Rate)
** Comparison in VDD=5V of TB62705 and TB6272

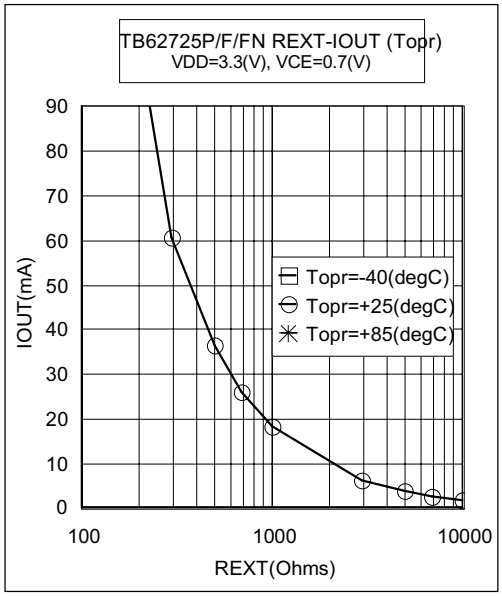








OUTPUT CURRNET vs REXT RESISTOR



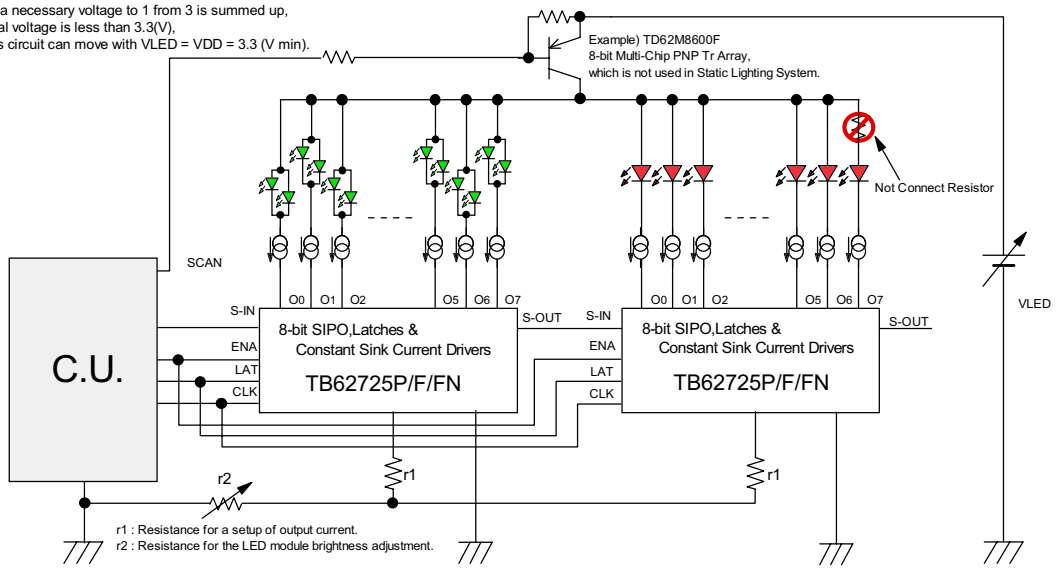
IOUT[mA]=(1.14/REXT[ohms])*16 -- Theory formula

APPLICATION NOTES(1 of 2)

TB62725P/F/FN application circuit (a general example)

TB62725 Series recommend VLED=VDD= 3.3(V min) and data transfer of fclk=20(MHz) is possible at cascade connection.

1 : Vf of LED is Vf=2.5 (V max).
2 : Output saturation Vce1 = 0.4(V min) at Iout <= 40(mA) of TB62725.
3 : Output saturation Vce2 = -0.25(V max) at Ic = -1(A) of TD62M8600F.
4 : TB62725 can move with VDDopr = 3 to 3.6(V).
5 : When a necessary voltage to 1 from 3 is summed up, the total voltage is less than 3.3(V), and this circuit can move with VLED = VDD = 3.3 (V min).

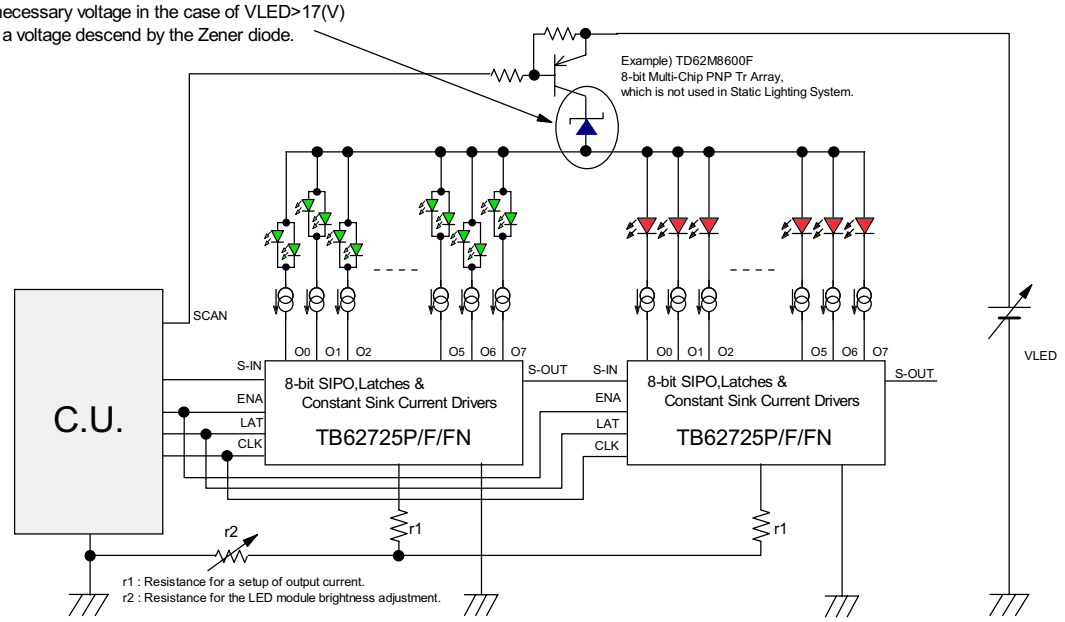


This device owns only one ground pin that means signal ground pin and power ground pin are common.
If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 0.5*Vdd by switching noise in operation, this device may miss-operate.
So we would lile you to pay attention to pattern layout to minimize inductance.

APPLICATION NOTES(2 of 2)

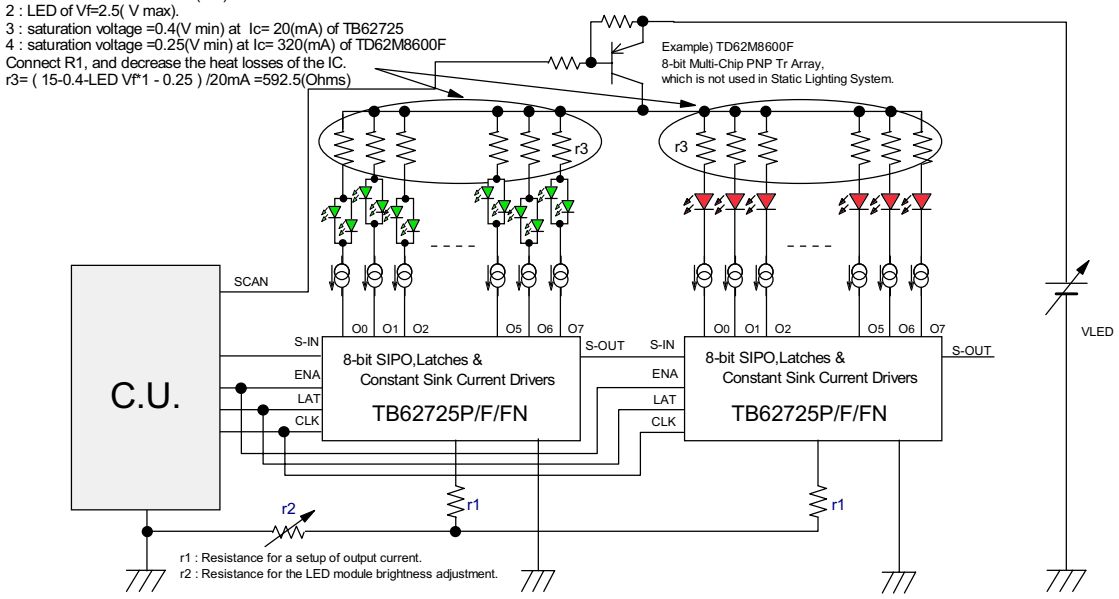
TB62725P/F/FN application circuit (the case of VLED>17(V))

Example :
An unnecessary voltage in the case of VLED>17(V)
makes a voltage descend by the Zener diode.



TB62725P/F/FN application circuit (with VLED<=17(V), the case of the over-saturation)

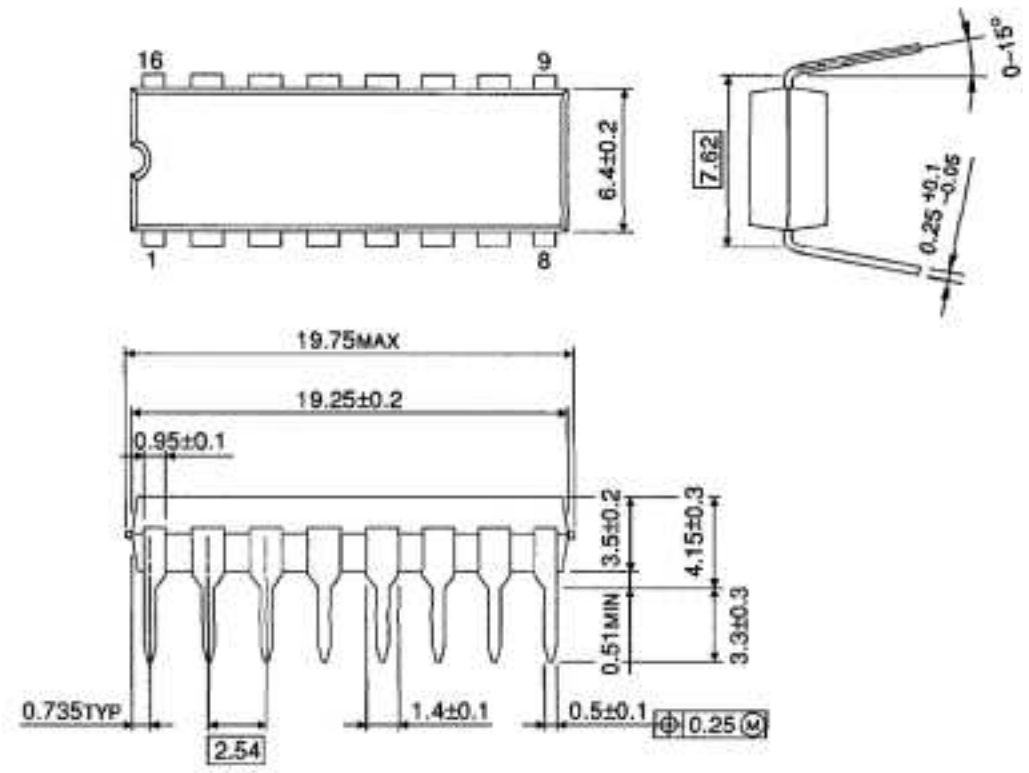
Example :
An over-saturation voltage makes a voltage descend by the resistance with the outside.
Condition :
1 : Turn on LED with Iout=20(mA).
2 : LED of Vf=2.5(V max).
3 : saturation voltage =0.4(V min) at Ic= 20(mA) of TB62725
4 : saturation voltage =0.25(V min) at Ic= 320(mA) of TD62M8600F
Connect R1, and decrease the heat losses of the IC.
r3= (15-0.4-LED Vf*1 - 0.25) /20mA =592.5(Ohms)



OUTLINE DRAWING

DIP16-P-300-2.54A

Unit : mm

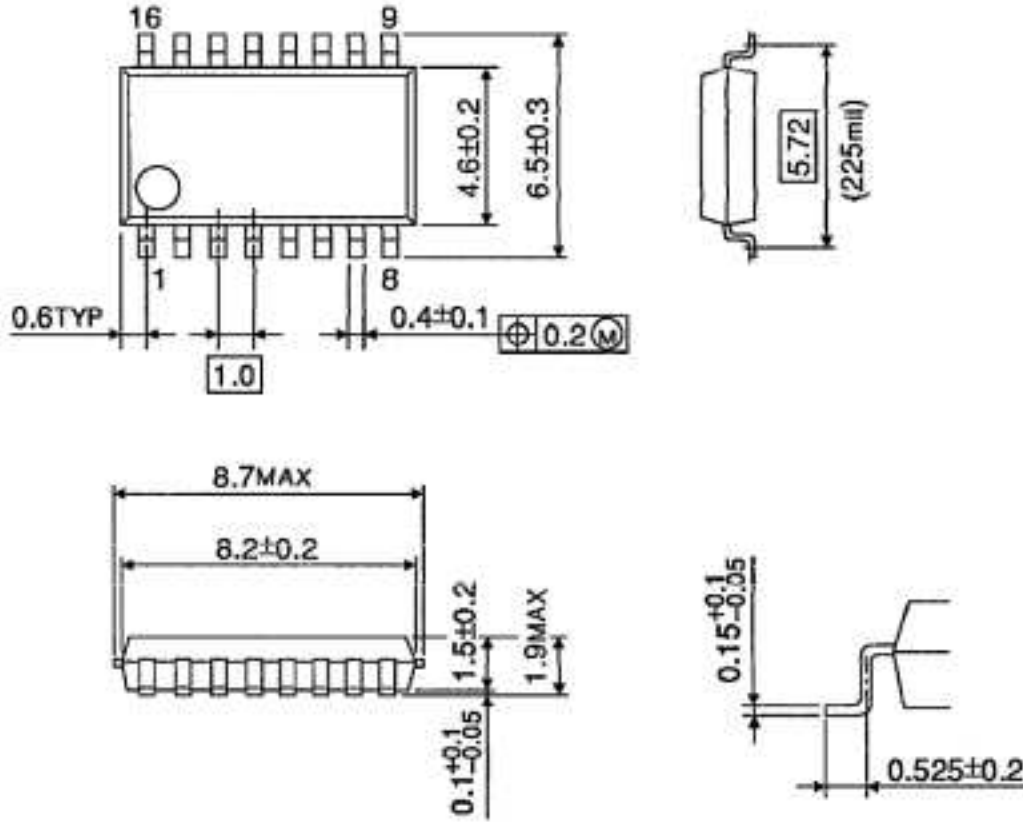


Weight : 1.11g (Typ.)

OUTLINE DRAWING

SSOP16-P-225-1.00A

Unit : mm

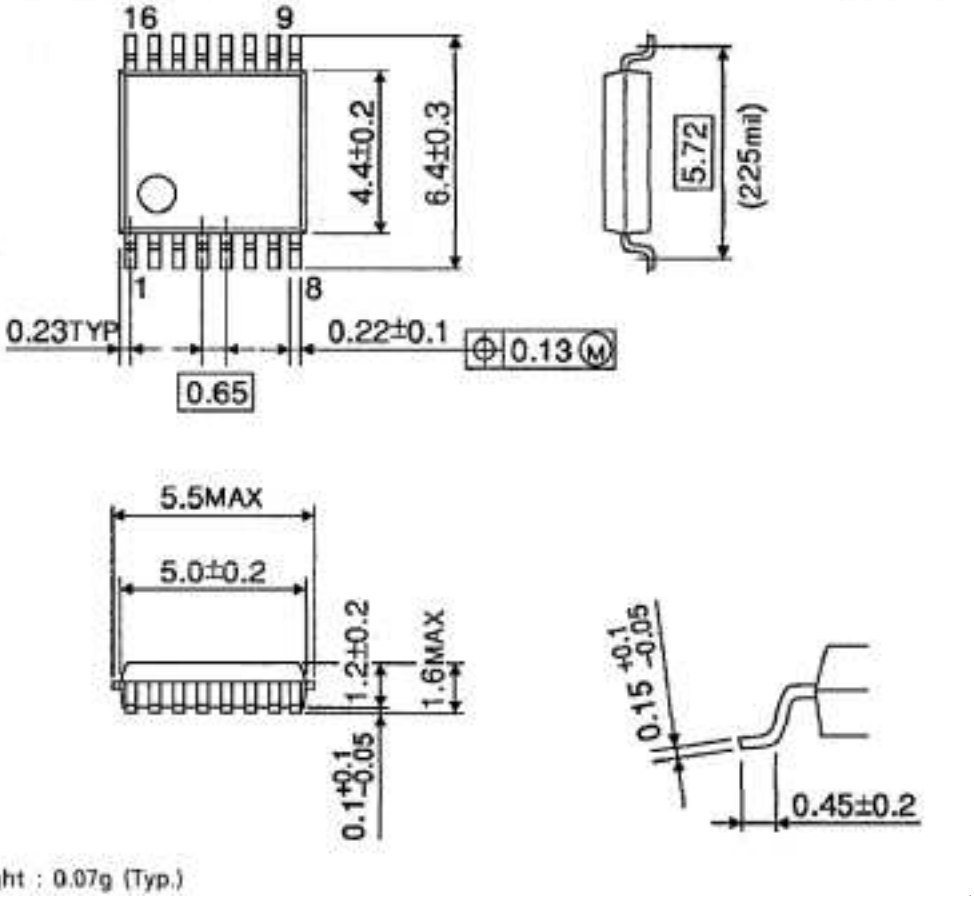


Weight : 0.14g (Typ.)

OUTLINE DRAWING

SSOP16-P-225-0.65B

Unit : mm



Weight : 0.07g (Typ.)

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