

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

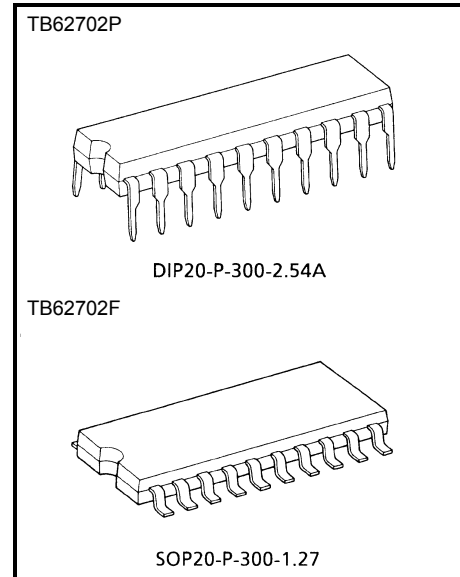
TB62702P, TB62702F

10BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER / LATCH / 10SEGMENT LED DRIVERS

The TB62702P, TB62702F are specifically designed for 10-Segment LED Drivers and LED display. And these are monolithic integrated circuits designed to be used together with Bi-CMOS (DMOS) integrated circuit. The devices consist of a 10bit shift Register and 10bit Latches, and 10bit DMOS structures.

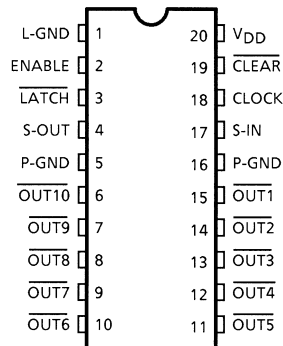
FEATURES

- 10bit serial-in parallel-out shift register / latch / 10segment LED driver (Bi-CMOS process)
- CMOS compatible inputs
- Open-drain DMOS outputs
- Low steady-state power consumption
- Serial data output for cascade operation
- Package ; P-type DIP-20-P-300A
F-type SOP-20-P-300

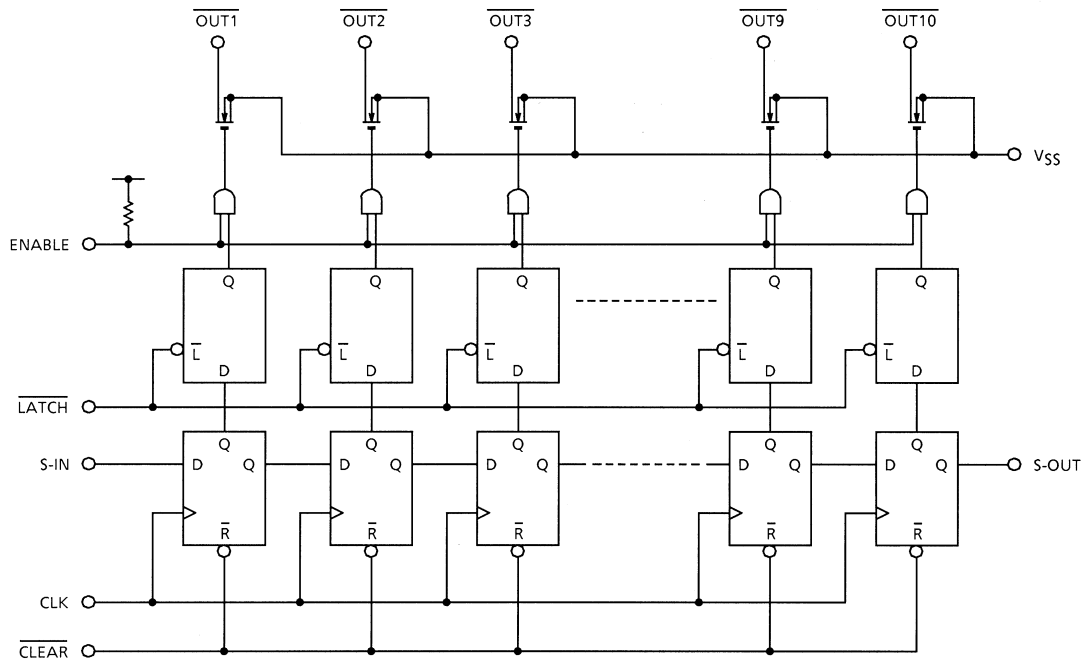


Weight
 DIP20-P-300-2.54A: 2.25 g (typ.)
 SOP20-P-300-1.27: 0.48 g (typ.)

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, VSS = 0 V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~7.0	V
Input Voltage	V _{IN}	-0.3~V _{DD} +0.3	V
Output Drain-Source Voltage	V _{OUT}	-0.4~30	V
Output Current	I _{OUT}	30	mA / bit
Power Dissipation	P	P _D (Note 1)	1.47
	F		0.96 (Note 2)
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

Note 1: Delated above 25°C in the proportion of 11.7 mW / °C(P-type),
7.7 mW / °C(F-type).

Note 2: On Glass Epoxy (50 × 50 × 1.6mm Cu 40%)

RECOMMENDED OPERATING CONDITIONS (Ta = -40~85°C, VSS = 0 V)

CHARACTERISTIC		SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage		V _{DD}	—	4.5	5	5.5	V
Input Voltage	"H" Level	V _{IH}	—	0.7 V _{DD}	—	V _{DD}	V
	"L" Level	V _{IL}	—	0	—	0.3 V _{DD}	
Output Drain-Source Voltage		V _{OUT}	—	—	—	30	V
Output Current		I _{OUT}	Duty = 100%, All output on	—	—	24	mA / ch
Power Dissipation	P	P _D	—	—	—	760	mW
	F		(Note 1)	—	—	470	

Note 1: On Glass Epoxy (50 × 50 × 1.6 mm Cu 40%)

ELECTRICAL CHARACTERISTICS (Ta = -40~85°C, V_{DD} = 4.5~5.5 V, V_{SS} = 0 V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Voltage	"L" Level	V _{DS1}	—	I _{OUT} = 15 mA, Ta = 25°C	—	—	0.18	V
	"L" Level	V _{DS1}	—	I _{OUT} = 15 mA	—	—	0.27	
	"L" Level	V _{DS2}	—	I _{OUT} = 26 mA, Ta = 25°C	—	—	0.31	
	"L" Level	V _{DS2}	—	I _{OUT} = 26 mA	—	—	0.47	
Output Resistor		R _{ON}	—	Ta = 25°C, I _{OUT} = 26 mA	—	—	12	Ω
Output Leakage Current		I _{OZ1}	—	V _{OUT} = 30 V, EN = "L" 1 bit	—	—	10	μA
		I _{OZ2}	—	V _{OUT} = 30 V, EN = "L" 10 bit	—	—	±1	
Input Current		I _{IN}	—	V _{IN} = V _{DD} or V _{SS}	—	—	±1	μA
		I _{IL}	—	ENABLE, V _{IN} = V _{SS}	-27.5	-55.0	-110.0	
Output Current	"H" Level	I _{OH}	—	S-OUT V _{DS} = 4.6 V, V _{DD} = 5.0 V	-400	-600	—	μA
	"L" Level	I _{OL}	—	S-OUT V _{DS} = 0.4 V, V _{DD} = 5.0 V	400	600	—	
Input Voltage	"H" Level	V _{IH}	—	—	0.7 V _{DD}	—	V _{DD}	V
	"L" Level	V _{IL}	—	—	0	—	0.3 V _{DD}	
Operating Supply Current		I _{DD1}	—	f _{CLK} = 5 MHz NO loads, 1 bit	—	—	1500	μA
Standby Supply Current		I _{DD2}	—	—	—	—	500	

SWITCHING CHARACTERISTICS

($T_a = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $V_{OUT} = 30\text{ V}$, $R_L = 1150\ \Omega$, $C_L = 15\text{ pF}$, "H" = V_{IH} , "L" = V_{IL})

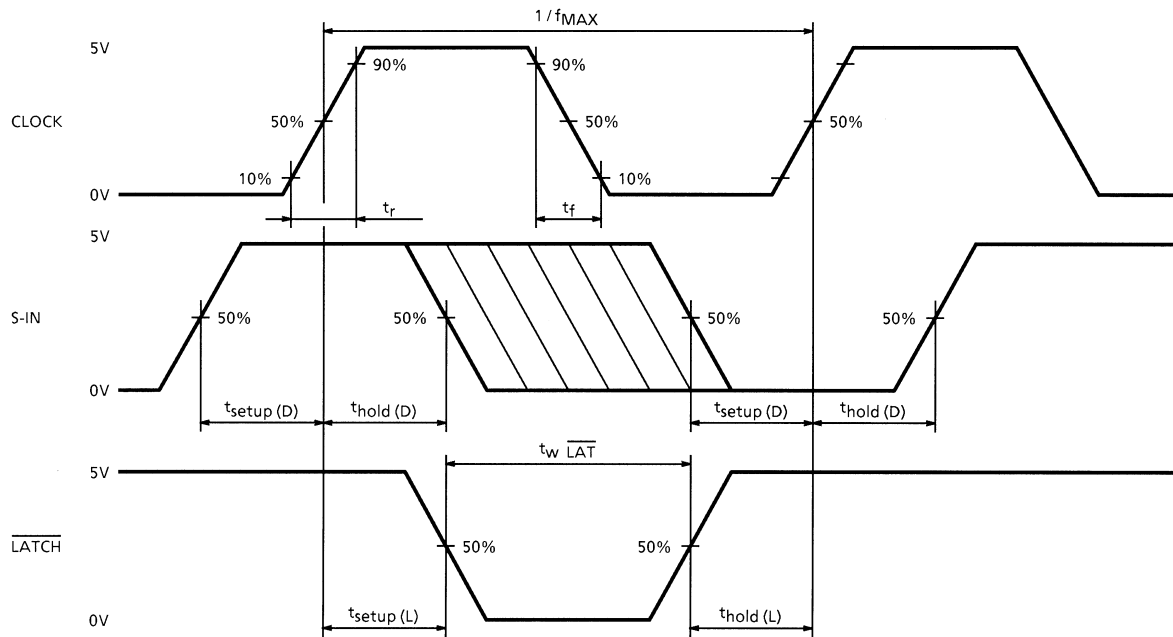
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT	
Propagation Delay Time (Low-to-High)	CLK- $\overline{\text{OUTn}}$	t_{pLH}	$\overline{\text{LAT}} = \text{"H"} , \overline{\text{CLR}} = \text{"H"} , \text{EN} = \text{"H"}$	—	—	250	ns	
	CLK- $\overline{\text{OUTn}}$		$\overline{\text{LAT}} = \text{"H"} , \text{EN} = \text{"H"}$	—	—	250		
	$\overline{\text{LAT}} - \overline{\text{OUTn}}$		$\overline{\text{CLR}} = \text{"H"} , \text{EN} = \text{"H"}$	—	—	200		
	EN- $\overline{\text{OUTn}}$		$\overline{\text{LAT}} = \text{"H"} , \overline{\text{CLR}} = \text{"H"}$	—	—	150		
Propagation Delay Time (High-to-Low)	CLK- $\overline{\text{OUTn}}$	t_{pHL}	$\overline{\text{LAT}} = \text{"H"} , \overline{\text{CLR}} = \text{"H"} , \text{EN} = \text{"H"}$	—	—	250	ns	
	$\overline{\text{LAT}} - \overline{\text{OUTn}}$		$\overline{\text{CLR}} = \text{"H"} , \text{EN} = \text{"H"}$	—	—	200		
	EN- $\overline{\text{OUTn}}$		$\overline{\text{LAT}} = \text{"H"} , \overline{\text{CLR}} = \text{"H"}$	—	—	150		
Set Up Time	CLK- $\overline{\text{LAT}}$	$t_{\text{setup}}(\text{L})$	—	—	50	ns		
	CLK-S-IN	$t_{\text{setup}}(\text{D})$	—	—	35			
Hold Time	CLK- $\overline{\text{LAT}}$	$t_{\text{hold}}(\text{L})$	—	—	105		ns	
	CLK-S-IN	$t_{\text{hold}}(\text{D})$	—	—	50			
Clock Pulse Width		$t_w \text{ CLK}$	—	—	100	ns		
Latch Pulse Width		$t_w \overline{\text{LAT}}$	—	—	50			
Clear Pulse Width		$t_w \overline{\text{CLR}}$	—	—	50			
Enable Pulse Width		$t_w \text{ EN}$	—	—	400			
Output Rise Time		t_{or}	$\overline{\text{OUTn}}$	—	—	1000	ns	
		t_r	S-OUT, $V_{SS} = 0\text{ V}$	—	—	50		
Output Fall Time		t_{of}	$\overline{\text{OUTn}}$	—	—	150		ns
		t_f	S-OUT, $V_{SS} = 0\text{ V}$	—	—	50		
Maximum Clock Frequency		f_{MAX1}	Duty = 50% Cascade connected	5	8	—	MHz	
		f_{MAX2}	Duty = 50%	6	12	—		

RECOMMENDED TIMING CONDITIONS ($T_a = -40\sim 85^\circ\text{C}$, $V_{DD} = 4.5\sim 5.5\text{ V}$, $V_{SS} = 0$)

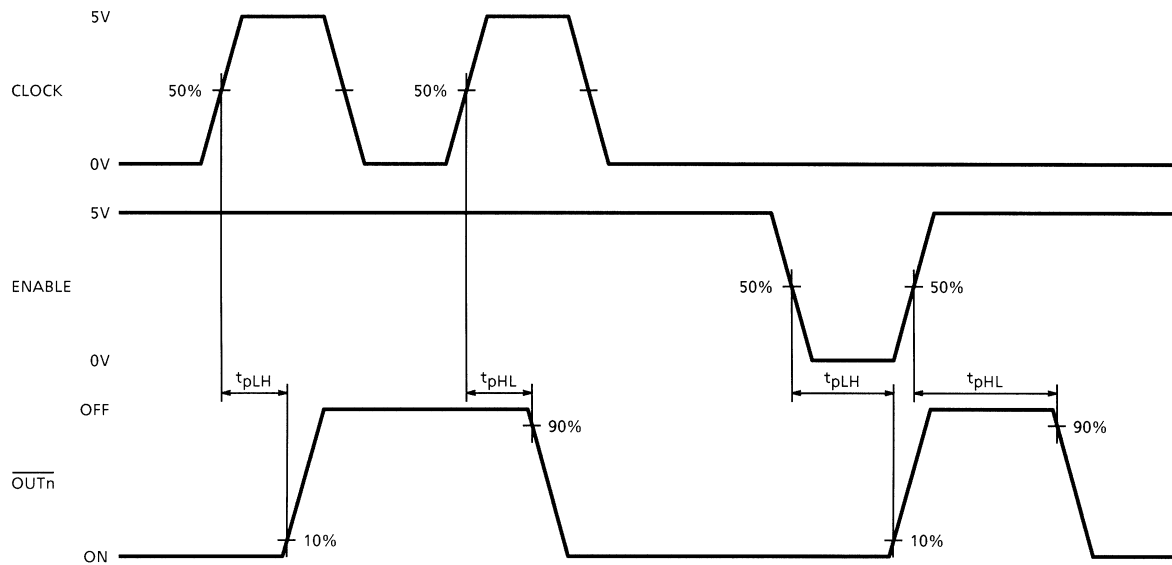
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Pulse Width	$t_w \text{ CLK}$	—	100	—	—	ns
Enable Pulse Width	$t_w \text{ EN}$	—	400	—	—	μs
Latch Pulse Width	$t_w \overline{\text{LAT}}$	—	100	—	—	ns
Clear Pulse Width	$t_w \overline{\text{CLR}}$	—	100	—	—	ns
Data Set Up Time	t_{setup}	—	100	—	—	ns
Data Hold Time	t_{hold}	—	150	—	—	ns

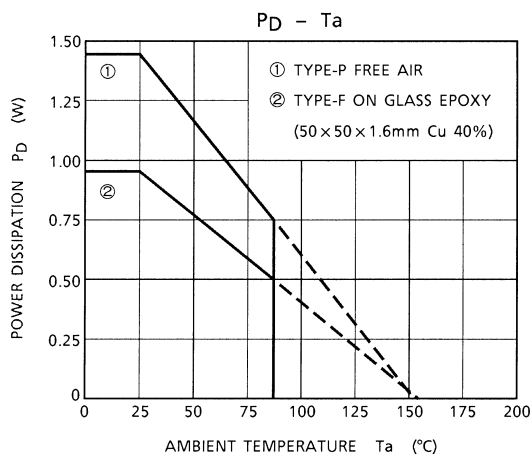
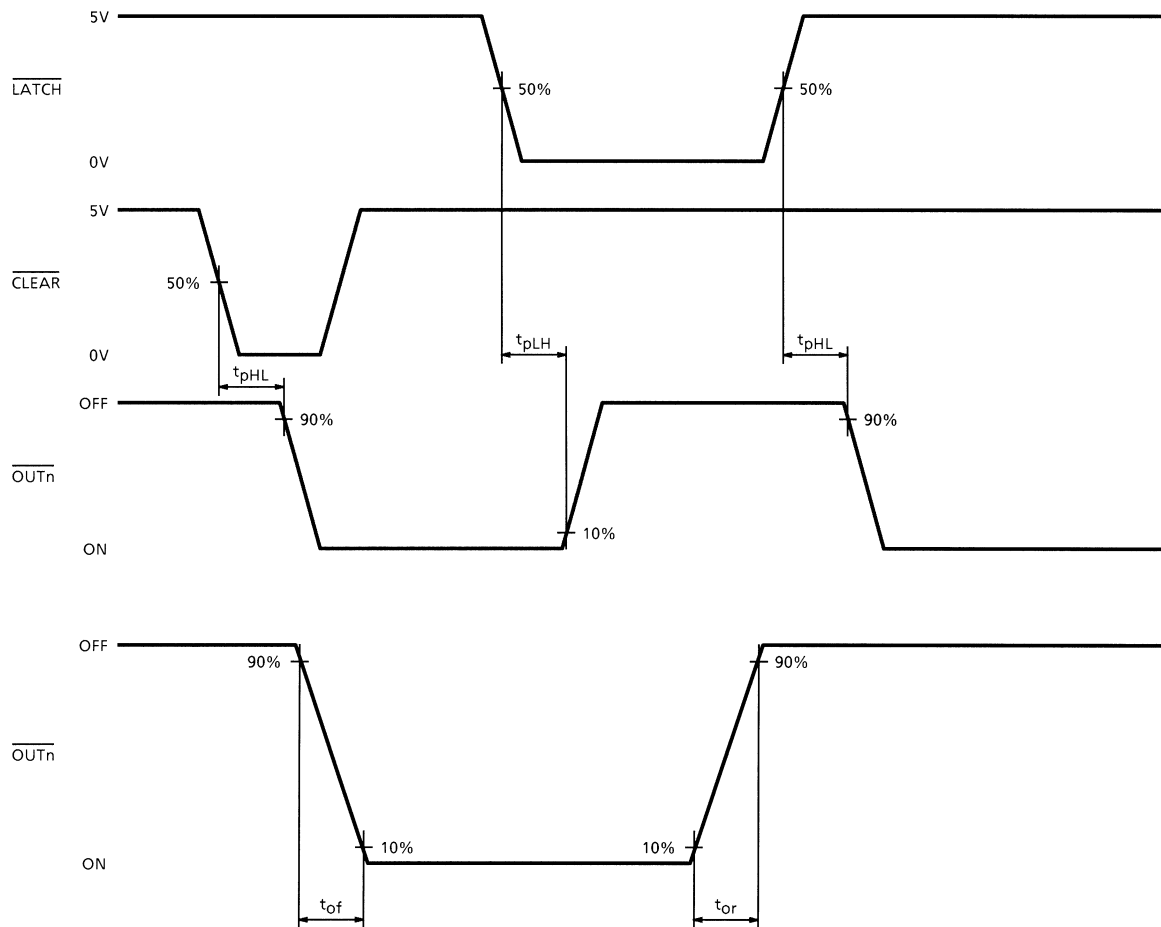
TIMING DIAGRAM

1. Input timing diagram



2. Propagation delay time





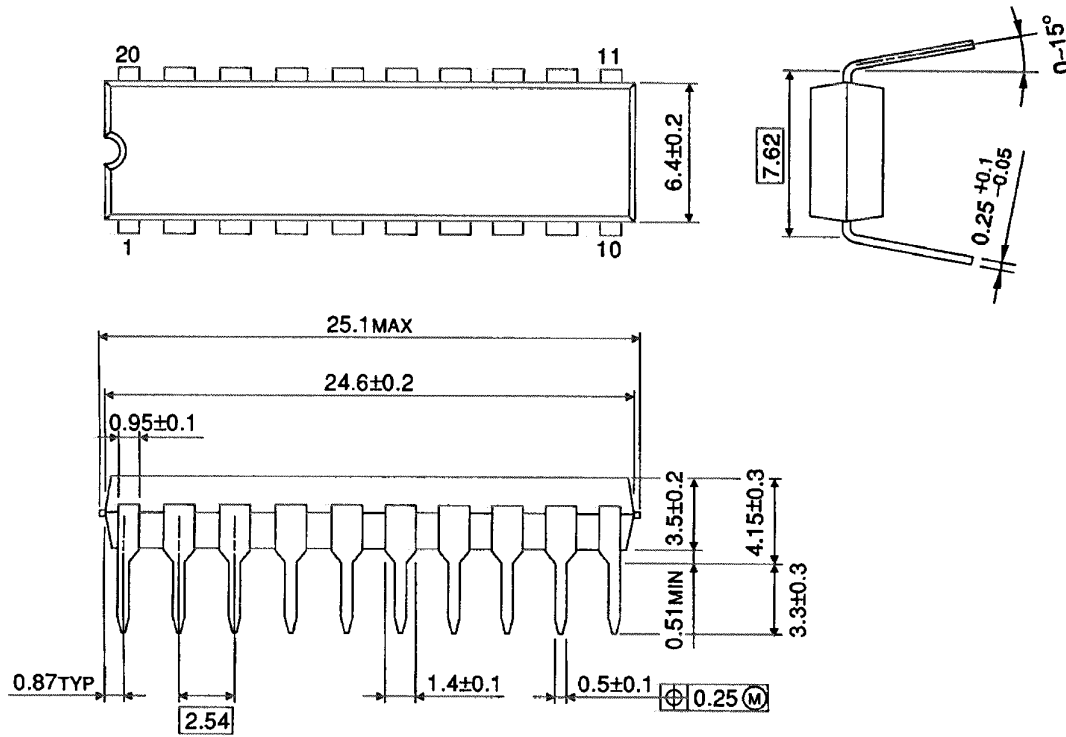
PRECUATIONS for USING

Utmost care is necessary in the design of the output line, VCC (V_{DD}) and GND (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

Package Dimensions

DIP20-P-300-2.54A

Unit : mm

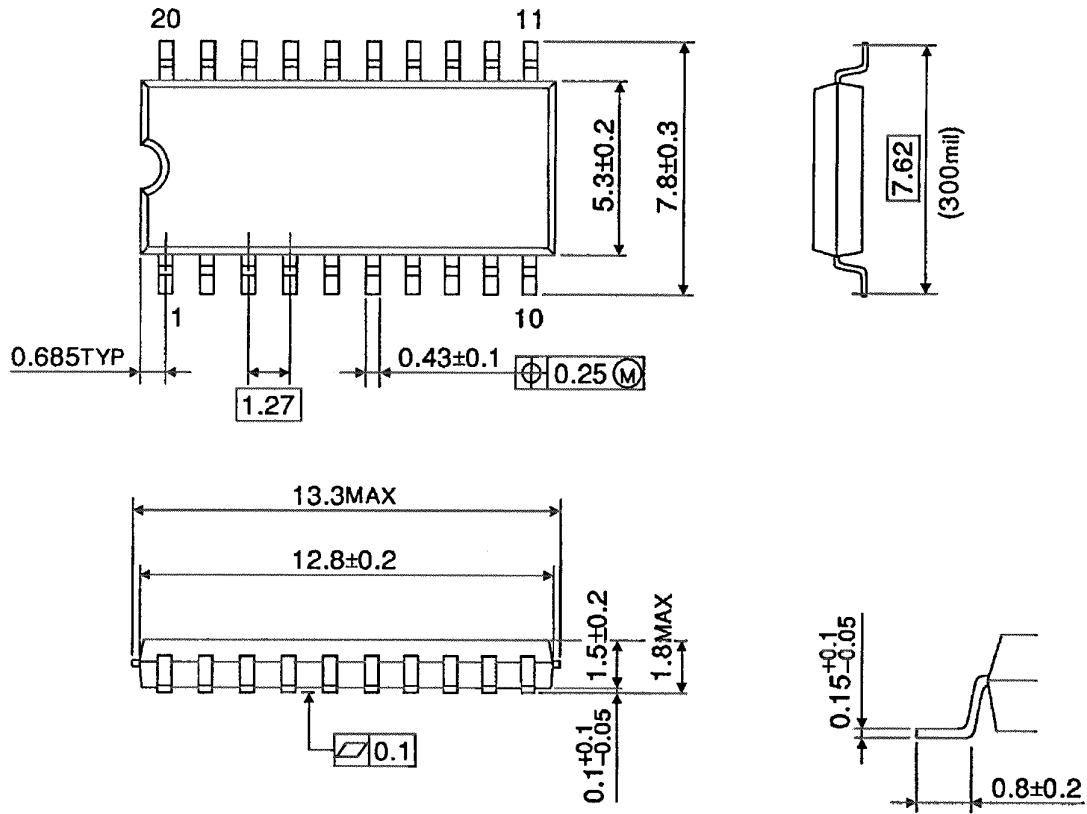


Weight: 2.25 g (typ.)

Package Dimensions

SOP20-P-300-1.27

Unit : mm



Weight: 0.48 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.
- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs

(1) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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