LX1977

SMBus Ambient Light Sensor

PRODUCTION DATASHEET

DESCRIPTION

The LX1977 is a CMOS based Ambient Light Sensor (ALS) with an I²C compatible SMBus interface.

This device is ideal for controlling display back lighting systems of low cost consumer products such as TV, portable computers, handheld devices, or medical devices. The LX1977 is optimized for a linear, accurate, and very repeatable input and output transfer function. The device also features adjustable input range and gain.

The LX1977 has a spectral response that emulates the human eye. Specially designed circuitry produces peak spectral response at 555 nm, with IR response less than 10% above 810 nm.

Input dynamic range of this device is adjustable via SMBus command. It can be set to either 0 ~ 500 lux, 0 ~ 1000 lux, 0 ~ 2500 lux or 0 ~ 5000 lux.

ALS internal compensation ensures photodiode dark current are at very low levels, providing high output accuracy at low ambient light levels.

The LX1977 integrates a 12-bit Sigma-Delta A/D converter that converts the ALS photodiode output into a digital word. This value is read via the I²C compatible SMBus interface.

The LX1977 ALS is internally optimized to an accuracy of approximately 5% over temperature. The high accuracy and repeatability of this device eliminates the need of calibration during product production, which results in reduced assembly time and lower production cost.

The LX1977 is available in an 8-pin MSOP package, and is operational over the ambient temperature range -40˚C to 85˚C.

KEY FEATURES

- Human Eye Spectral Response
- Very Low IR Sensitivity
- 12-bit Resolution
- 5% Typical Accuracy
- Rejection to 50/60Hz Interference
- Programmable Integration Time
- Programmable Interrupt Pin
- I²C compatible SMBus Interface
- Easy Processor Interface
- No Optical Filter Needed

APPLICATIONS

- Backlight Control for Notebook
- Backlight Control for TV
- Handheld Devices
- Medical Devices

Note: I²C is a trade mark of Philips

PACKAGE ORDER INFO

T_A (°C)	DU	3 x 5 Glass Top MSOP 8-pin
		RoHS Compliant / Pb-free
-40 to 85	LX1977IDU	

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1977IDU -TR)

THERMAL DATA

θ_{JA} = 152 °C/W

THERMAL RESISTANCE-JUNCTION TO AMBIENT

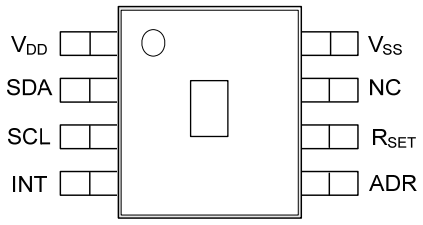
Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$. The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3 to 6V DC
Input Voltage to All Input Pins	-0.3V to V_{DD} + 0.3V
SMBus Pin Voltage (SCL, SDA)	-0.3V to 5.5V
SMBus Pin Current (SCL, SDA)	< 10 mA
Operating Temperature Range	-40 to +85°C
Storage Temperature Range	-40 to 100°C
RoHS / Pb-free Peak Package Solder Reflow Temperature (40 seconds maximum exposure)	260° (+0, -5)

Notes: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



GLASS TOP MSOP 8 PIN
(Top View)
RoHS / Pb-free 100% Matte Tin

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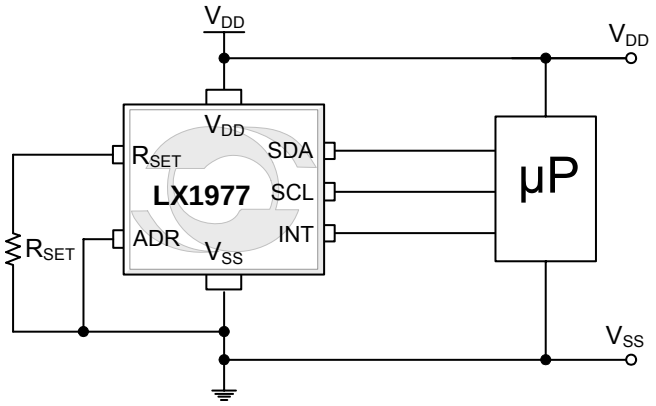
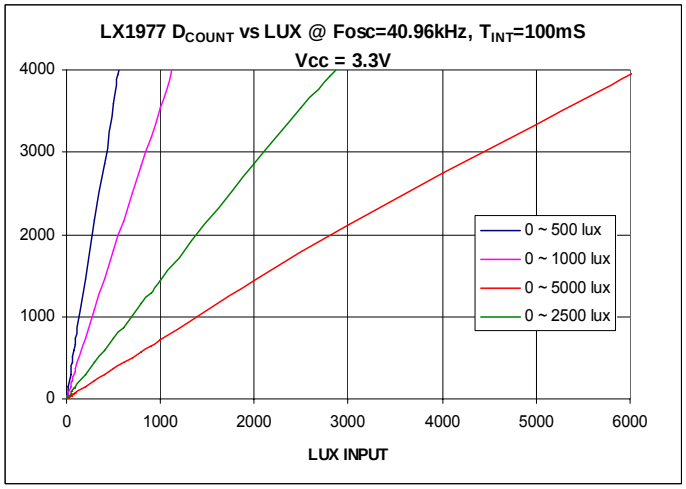
SMBus Ambient Light Sensor

PRODUCTION DATASHEET

PRODUCT HIGHLIGHT





SIMPLIFIED BLOCK DIAGRAM

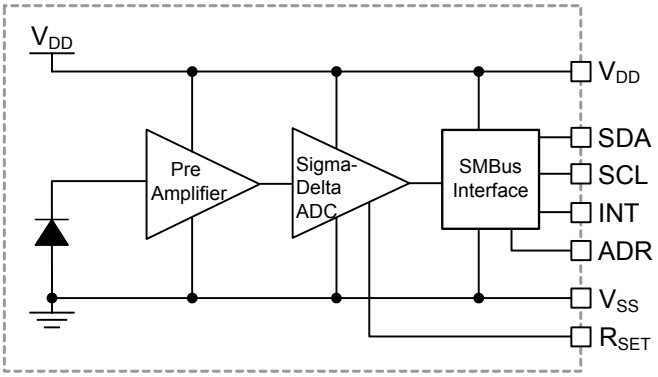


Figure 1 – Simplified Block Diagram

PACKAGE PHOTO

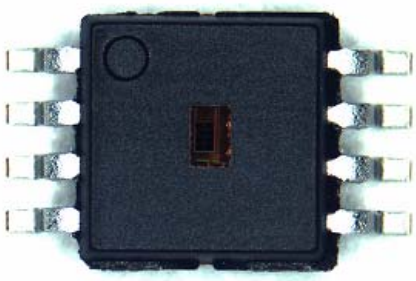


Figure 2 – Product Photo

FUNCTIONAL PIN DESCRIPTION

Name	Pin #	Dir	Description
V_{DD}	1	PWR	Power Supply Voltage
SDA	2	I / O	SMBus Data – Connect To SMBus Data Line
SCL	3	I	SMBus Clock – Connect To SMBus Clock Line
INT	4	O	Interrupt Output Pin, Active Low, Open Drain
ADR	5	I	SMBus Address – The Address For This Device Is Determined By The State Of This Pin. ADR = GND sets address 20H, ADR = OPEN sets address 22H, ADR=V_{DD} sets address 70H.
R_{SET}	6	I	Gain Setting. For Gain Fine Adjustment. Typically, connect this pin to ground through a 1% 267k resistor.
NC	7		No Connection Pin
V_{SS}	8	PWR	Ground Reference For Power And Signal Output

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 70°C and the following test conditions: 3.0V ≤V_{DD} ≤ 4.5V

Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
POWER SUPPLY						
Operational Voltage	V_{DD}	Note 5	3.0		4.5	V
Supply Current	I_{DD}				0.2	mA
Supply Current	I_{DD}	Shut Down ALS			15	µA
INTERNAL						
Internal Oscillator Frequency	F_{OSC}	3.0V ≤V_{DD}.≤ 3.6V	38.91	40.96	43.00	kHz
		3.0V ≤V_{DD}.≤ 4.5V	36.86	40.96	45.06	
ALS RESPONSE						
Peak Spectral Response	$\lambda_{PR(ALS)}$			555		nm
Infrared Response	Δ_{IR}	$E_{V(white)}$ = 100 lux, $E_{V(810nm)}$ = 14.6µW/cm^2, Note 3	-8		8	%
Full Scale ADC Output Value @ F_{OSC}= 40.96kHz, RANGE_SEL = 00b (0 ~ 500 lux)	D_{COUNT}	T_{INT} = 100 ms, Note 4			4095	Counts
RANGE_SEL = 01b (0 ~ 1000 lux)	D_{COUNT}	T_{INT} = 50 ms, Note 4			2047	
RANGE_SEL = 10b (0 ~ 5000 lux)	D_{COUNT}	T_{INT} = 25 ms, Note 4			1023	
RANGE_SEL = 11b (0 ~ 2500 lux)	D_{COUNT}	T_{INT} = 6.25 ms, Note 4			255	
Enable Time	t_{ON}	Software Enable		100		µs
Disable Time	t_{OFF}	Software Disable		100		µs
Dynamic Response Time	$T_{F(90\%\sim10\%)}$	Light Input Change From 200 lux to 20 lux		1		ms
	$T_{R(10\%\sim90\%)}$	Light Input Change From 20 lux to 200 lux		1		
ADC						
Non-Linearity	DNL	T_{INT} = 100ms, RANGE_SEL=00b Note 6	-5		5	%
ALS						
ADC Output Count @ F_{OSC} = 40.96kHz, T_{INT} = 50ms RANGE_SEL = 01b (0 ~ 1000 lux)	D_{COUNT}	E_V = 200 lux, Note 1,2	346	372	398	Counts
		E_V = 500 lux, Note 1,2	880	931	982	
		E_V = 1000 lux, Note 1,2	1768	1861	1955	
ADC Output Count @ F_{OSC} = 40.96kHz, T_{INT} = 100ms RANGE_SEL = 00b (0 ~ 500 lux)	D_{COUNT}	E_V = 100 lux, Note 1,2	692	745	797	Counts
		E_V = 200 lux, Note 1,2	1403	1489	1575	
		E_V = 500 lux, Note 1,2	3537	3723	3909	
ADC Output Count @ F_{OSC} = 40.96kHz, T_{INT} = 100ms RANGE_SEL = 01b (0 ~ 1000 lux)	D_{COUNT}	E_V = 200 lux		733		Counts
		E_V = 500 lux		1808		
		E_V = 1000 lux		3535		
ADC Output Count @ F_{OSC} = 40.96kHz, T_{INT} = 100ms RANGE_SEL = 10b (0 ~ 5000 lux)	D_{COUNT}	E_V = 500 lux		364		Counts
		E_V = 1000 lux		713		
		E_V = 2000 lux		1437		
ADC Output Count @ F_{OSC} = 40.96kHz, T_{INT} = 100ms RANGE_SEL = 11b (0 ~ 2500 lux)	D_{COUNT}	E_V = 500 lux		734		Counts
		E_V = 1000 lux		1433		
		E_V = 2000 lux		2851		
Dark ADC Count Value	D_{COUNT}	E_V = 0 lux, T_A = 25°C, RANGE_SEL=00b, T_{INT}=100mS		0	4	Counts

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 70°C and the following test conditions: 3.0V ≤V_{DD} ≤ 4.5V

Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
		E_V = 0 lux, T_A = 70°C, RANGE_SEL=00b, T_{INT}=100mS, Note 7			18	
SMBUS INTERFACE						
Clock Frequency	F_{CLK}		10		400	kHz
High Level Input Voltage	V_{SDA} V_{SCL}		0.8			V
Low Level Input Voltage					2.1	V
Input Leakage Current	I_{SDA}/I_{SCL}		-5		5	µA
SDA Low Output Voltage	V_{SDA}	I_{SDA} = 3mA			0.4	V
SDA Current Sinking Capacity	I_{SDA}		3			mA
INT Low Output Voltage	V_{INT}	I_{INT} = 3mA			0.4	V
INT Leakage Current	I_{LEAK}		-10		10	µA
ADR High Level Input Voltage	V_{ADR}		80%			V_{DD}
ADR Open			40%		60%	V_{DD}
ADR Low Level Input Voltage					20%	V_{DD}
ADR Input Leakage Current	I_{ADR}		-10		10	µA

Notes:

1. In production, the input irradiance is supplied from a point source which is a white LED.
2. See Figure 3
3. $\Delta_{IR} = \frac{D_{COUNT}(E_{V(WHITE)} + E_{V(IR)}) - D_{COUNT}(E_{V(WHITE)})}{D_{COUNT}(E_{V(WHITE)})}$
4. Guarantee by scan tests.
5. Specifications in the EC table are for 3.0V ~ 4.5V. Device is operational down to 2.5V and up to 5.0V with relaxed specifications.
6. Gain1 = (D_{COUNT}2-D_{COUNT}1) / (Lux2-Lux1), Gain2 = (D_{COUNT}3-D_{COUNT}2) / (Lux3-Lux2), DNL1 = (Gain1 * 2 / (Gain1+Gain2) -1) %, DNL2 = (Gain2 * 2 / (Gain1+Gain2) – 1) %. Lux1 = 100 lux, Lux2 = 200 lux, Lux3 = 500 lux.
7. For the setting RANGE_SEL=00b and T_{INT}=100mS, the full scale output is typical 3723 decimal. A dark ADC output count of maximum 18 at T_A = 70°C is only 0.5% of 3723.

TEST CIRCUITS

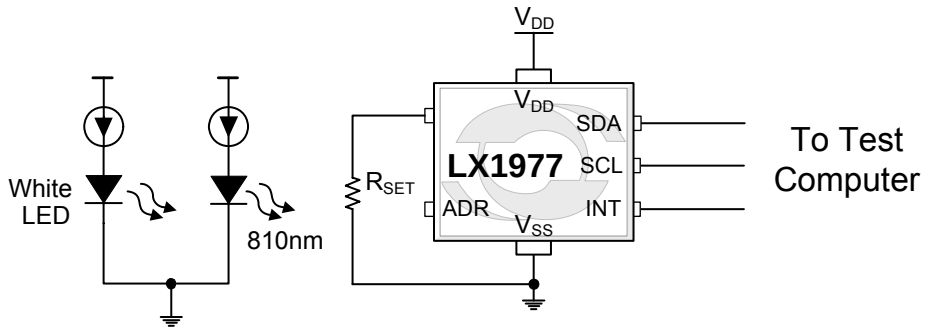

Figure 3 – ALS Output Measurement

APPLICATION NOTE

BASIC FUNCTIONALITY

The LX1977 is an ALS with an I²C compatible SMBus interface. It contains a high sensitivity close to human eye response photodiode, a 12-bit Sigma-Delta ADC and a SMBus interface. The Sigma-Delta ADC converts photodiode current to digital values that correspond to the light incident on the photodiode. The integrating nature of the ADC allows the device to reject 50Hz and 60Hz flicker noise from environmental lighting.

The Sigma-Delta ADC provides the flexibility to set different conversion times, or integration time. It has four conversion time selections to meet different application requirements. The clock source for the ADC is also selectable from either an internal clock or a SMBus clock. For internal clock selection, the device features full speed (40.96kHz) and quarter speed (10.24kHz) selection. The ADC conversion result is stored in a 12-bit register for read back even when another conversion is in process.

SMBus INTERFACE

LX1977 is a nine-register device which uses SMBus or I²C protocols to communicate with the host system. All registers are defined as full byte wide. Some registers contain reserved (undefined) bits with a default value of "0", or are read only bits that are status indicators. Six of the nine registers are capable of both read and write, and three registers are read only. See the LX1977 Register Definitions section for details.

The LX1977 communicates over the SMBus and operates in a "slave" mode receiving commands and sending / receiving data to / from the host or "master". Only standard two-wire SMBus and I²C compatible serial bus and protocols may be used for this device. The LX1977 can be configured for one of the three addresses by connecting the ADR input pin to ground, V_{DD}, or simply leaving it OPEN.

Table 1: Address strapping codes

Option #	ADR	Hex Address
1	GND	20h
2	OPEN	22h
3	V_{DD}	70h

In this document, the device address is always expressed as full 8 bit address. The high nibble of the address is from bit 7 to bit 4. In the low nibble, bit 0 is always the R/W bit and in 8 bit address format it is considered 0.

The address could be changed dynamically. The requirement is that after the change, the LX1977 ALS should be disabled and then enabled either via bit 6 of register 00h or a V_{DD} power cycle.

Table 2: Address = 20h

1	7	1	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Data Byte**	**A**	**P**
	0 0 1 0 0 0 0	**0**				

Table 3: Address = 22h

1	7	1	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Data Byte**	**A**	**P**
	0 0 1 0 0 0 1	**0**				

Table 4: Address = 70h

1	7	1	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Data Byte**	**A**	**P**
	0 1 1 1 0 0 0	**0**				

SMBus PROTOCOL

The only required command protocols are SMBus Send Byte, Receive Byte, Read Byte / Word, and the Write Byte / Word protocols. See Table 7 ~ Table 12 for details.

Writes to registers can be performed by either the SMBus Write Byte / Word protocols and / or by internal IC logic, depending on the register type (see Table 13). Send Byte protocol can only be used on the Command / Status register (register 00h).

Read can be performed on all registers by issuing the Read Byte / Word protocol. Note that Receive Byte protocol can only be used on the Command / Status register (register 00h) for a quick test of the status bits. Read Only registers can be written only by internal logics. Their contents will not be affected by SMBus write commands.

When LX1977 is initially powered, it will first test the address selection pin input to determine its own address and then look for its unique address each time it detects a "Start Condition". If the address does not match, the LX1977 ignores all bus activity until it encounters another "Start Condition". If the address is a match, the LX1977 acknowledges that it has detected its address and a W/R bit to either read or write. If the

APPLICATION NOTE

W/R bit is a "0", signifying a "Write" command, the next byte of data sent from the host will be a Data Byte or a Command Code (also called index), depending on whether there is a Stop Condition afterwards. If there is a Stop Condition, then the received byte is a data byte (not a Command Code or register index) to the LX1977 and this command will be sent to register 00h and executed. Note that this is considered a Send Byte Protocol, which can only be used on register 00h as stated before. If there is no Stop Condition detected, then the received byte is a Command Code (or register index). In this case, either one or two bytes of data will follow. The index points to an internal register in the LX1977 that will be the object of the subsequent data transfer.

In a Write protocol, the LX1977 will acknowledge the receipt of a valid index. After the index, there will be another byte / word of data; this byte of data will be loaded into the indexed register. In LX1977 Read / Write word protocols, the Command Code (or register index) will always be the lower byte data register address. The higher byte of the data will be loaded into the register corresponding to the lower byte register index / command code incremented by 1.

The LX1977 will ignore all additional bus activity once it has acknowledged the receipt of the data byte(s) followed by a "Stop Condition", and until the next "Start Condition" is detected. Note that receipt of a "Stop Condition" or "Start Condition" will reset the address detection state machine. The LX1977 does not support "Packet Error Code".

The host can read the contents of register 00h which contains the device status bits by issuing a simple Receive Byte protocol. In this command line, the W/R bit is set to a "1". Upon the receipt of a Receive Byte protocol, the LX1977 will acknowledge that it has detected its address and a valid W/R bit; the device will then put a copy of the register 00h data onto the bus.

The host can read the contents of the indexed register(s) within the LX1977 using a Read Byte / Word protocol. In this protocol, the host first will send a Write command indicating the device address and Command Code. After the write command is issued, the host initiates a repeat "Start Condition" followed by issuing a Read from device's address.

In Read protocol, the Command Code is the index of the register(s) to be read. The repeat "Start Condition" will be followed by the Slave address (refer to Table 11 and Table 12) and a read command bit. Upon receipt of a Read command, the LX1977 will acknowledge that it has detected its address and a valid Read bit. Subsequently, one byte of data starting from the indexed register address will be put onto the bus. A NACK from the host signifies the end of the Read command. If instead, an ACK is received, then the LX1977 will put another byte of data from the next incremented register address onto the bus. A NACK will signify the end of the Read command. Once the LX1977 has placed the byte(s) of data on the serial bus, it will ignore all additional bus activity until the next "Start Condition" is detected.

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SMBUS COMMON AC SPECIFICATIONS

The diagram below illustrates the various SMBus timings and sets the context for the specifications to follow. Note that the following are not production tested specifications, but are common SMBus protocol specifications practiced.

Table 5: SMBus (I^2C compatible) Timing

Symbol	Parameter	FAST_MODE		Units
		MIN	MAX	
F_{SMB}	SMBus Operating Frequency	10	400	kHz
T_{BUF}	Bus free time between Stop and Start Condition	1.3	-	µs
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	0.6	-	µs
$T_{SU:STA}$	Repeated Start Condition setup time	0.6	-	µs
$T_{SU:STO}$	Stop Condition setup time	0.6	-	µs
$T_{HD:DAT}$	Data hold time	0	0.9	µs
$T_{SU:DAT}$	Data setup time	100	-	ns
T_{LOW}	Clock low period	1.3	-	µs
T_{HIGH}	Clock high period	0.6	-	µs
T_F	Clock / Data Fall Time	-	300	ns
T_R	Clock / Data Rise Time	-	300	ns
T_{POR}	Time in which a device must be operational after power-on reset		500	ms
C_{IN}	Capacitance for SCL or SDA pin		10	pF

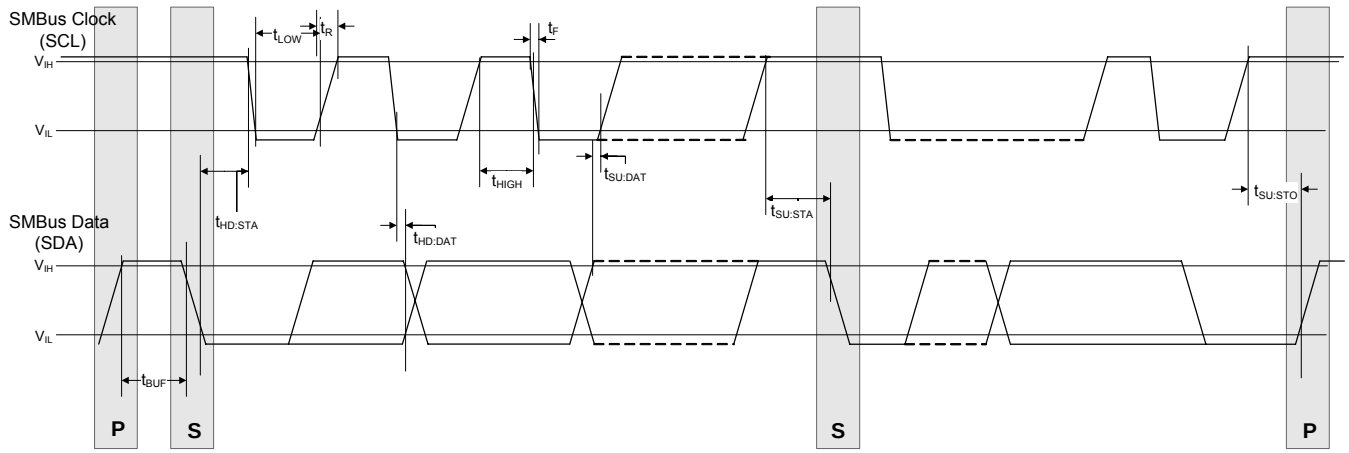

Figure 4 – SMBus Timing Measurement

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SMBUS COMMUNICATION PROTOCOL

LX1977 employs the following SMBus 2.0 protocols that are also compatible to I^2C protocols. Protocols used to communicate with LX1977 must be per standard SMBus specification version 2.0 or higher.

- Send Byte
- Receive Byte
- Write Byte
- Write Word
- Read Byte
- Read Word

The individual protocol format is shown in tables below. For a complete description of SMBus protocols, please review the SMBus Specification at www.smbus.org/specs.

Table 6: SMBus Packet Protocol Diagram Element Key

S	Slave Address	Wr	A	Data Byte	A	P
			X		X	

S	Start Condition	**Rd**	Read (bit value of 1)
Wr	Write (bit value of 0)	**A**	Acknowledge (‘0’ for an ACK, or ‘1’ for a NACK)
P	Stop Condition	**Command Code**	Register Address
☐	Master-to-Slave	▒	Slave-to-Master

Grey shading represents cycles during which the LX1977 “owns” or “drives” the Data line. All other cycles are driven by the host.

Table 7: Send Byte Protocol:

1	7	1	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Data Byte**	**A**	**P**
		0				

Table 8: Receive Byte Protocol:

1	7	1	1	8	1	1
S	**Slave Address**	**Rd**	**A**	**Data Byte**	**A**	**P**
		1			**1**	

Table 9: Write Byte Protocol:

1	7	1	1	8	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Command Code**	**A**	**Data Byte**	**A**	**P**
		0						

Table 10: Write Word Protocol:

1	7	1	1	8	1	8	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Command Code**	**A**	**Data Byte Low**	**A**	**Data Byte High**	**A**	**P**
		0								

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Table 11: Read Byte Protocol:

1	7	1	1	8	1	1	7	1	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Command Code**	**A**	**S**	**Slave Address**	**Rd**	**A**	**Data Byte**	**A**	**P**
		0						**1**			**1**	

Table 12: Read Word Protocol:

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	**Slave Address**	**Wr**	**A**	**Command Code**	**A**	**S**	**Slave Address**	**Rd**	**A**	**Data Byte Low**	**A**	**Data Byte High**	**A**	**P**
		0						**1**					**1**	

SMBUS REQUIREMENTS

- When the ALS SMBus interface is not powered, it will not affect other SMBus traffic that may occur. The SMBus interface pins should be in high impedance mode when the interface is not powered.
- SMBus pull-up resistors should be provided on the system, and is not provided by the LX1977 device.
- The ALS shall NACK any SMBus operation directed to it that addresses a register that is not defined in this specification.

SMBUS DE-FEATURING

Package Error Correction, Alarm function and the Address Resolution protocols are not supported by this device.

LX1977 REGISTER DEFINITIONS

Table 13: LX1977 Register Definitions

Register(hex)	R / W	Description	
00h	R / W	Command / Status	Device Control and Status
01h	R / W	Device Control	ALS ADC Control
02h	R / W	Low-Threshold LSB	Lower byte of the Interrupt low threshold window
03h	R / W	Low-Threshold MSB	Higher 4 bits of the Interrupt low threshold window
04h	R / W	High-Threshold LSB	Lower byte of the Interrupt high threshold window
05h	R / W	High-Threshold MSB	Higher 4 bits of the Interrupt high threshold window
06h	R	LSB of D_{COUNT}	Lower byte of the ADC result
07h	R	MSB of D_{COUNT}	Higher 4 bits of the ADC result
08h	R	ID Register	Part Identification

Detailed descriptions of the individual register are shown below.

Command Register 00h (R / W)

Table 14: Command Register 00h

7	6	5	4	3	2	1	0
ADC_FLAG	ALS_ENA	START_ADC	ADC_MOD	ADC_CLK	INT_FLAG	INT_ENA	OV
Read Only	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read Only

Index Address = 00000000b or 00h
Access = Read / Write
Default = 00000000b

This register contains bits for configuring and controlling LX1977 and also bits showing LX1977 operation status.

Bit Definitions:

ADC_FLAG (bit 7, R): This is a status bit and is a read only bit. When **START_ADC** is set to 1, 0 on this bit indicates ADC conversion is in process, 1 indicates conversion is done and the D_{COUNT} data is ready in register 06h & 07h. Setting **START_ADC** to 1 will clear **ADC_FLAG** bit and start a new conversion regardless the status of the ADC converter. The time needed to finish a conversion will depend on the **T_{INT}_SET** setting in Device Control Register 01h bit 0 & 1.

ALS_ENA (bit 6, R / W): 0 on this bit means power down ALS and ADC of this device, 1 means power up ALS and ADC.

START_ADC (bit 5, R / W): Writing 1 to this bit will start a new ADC conversion and clear the **ADC_FLAG** bit. Writing 0 to this bit stops (or disable) ADC conversion and also resets the internal interrupt persistent control counter when **ADC_MOD** bit is set to 1. When this bit is 0, **ADC_FLAG** bit will not be meaningful.

ADC_MOD (bit 4, R / W): 0 on this bit sets ADC to one time conversion mode and 1 sets ADC to continuous mode when **START_ADC** bit is set to 1.

Note:

These two bits should be controlled together. When these two bits are set to 11, LX1977 will be in continuous mode. When a restart of the continuous mode is need, 01 should be written to these bits and then 11 should be written afterwards. In this case, **ADC_FLAG**, **INT_FLAG** and the internal counter for **INT_PERSIST_CTRL** will be reset to 0.

Table 15: Bit 5 & 4 Definitions

START_ADC (Bit 5)	ADC_MOD (Bit 4)	Description
0	**0**	Disable ADC
0	**1**	Disable ADC and reset internal interrupt persistent control counter, ADC_FLAG and INT_FLAG
1	**0**	Set ADC to one time conversion mode and start the conversion. ADC_FLAG bit will indicate conversion status, 0 on this bit means conversion is in process, 1 means conversion is done and data is ready in register 06h and 07h. Interrupt persistent control function is not applicable to this mode. **Note:** 1) When this mode is set, the ADC_FLAG will be set to zero right away. 2) When conversion is done, Bit 5 and Bit 4 will be changed from 10 to 00 automatically. If a new conversion is needed, 10 should be written to Bit5 and Bit 4 again.

1	**1**	Set ADC to continuous conversion mode and start conversion. ADC_FLAG indicates conversion status, 0 means conversion is in process, 1 means previous conversion is done and data is ready in register 07h and 08h. Actually, after the first conversion, this bit will be always 1. Interrupt function applies to this mode. **Note:** When this mode is set, the ADC_FLAG will be set to zero right away.

ADC_CLK (bit 3, R / W): Selects the internal ADC clock speed when **CLK_SEL** (bit 7) of register 01h is 0
= 0, select clock speed to normal (40.96 kHz)
= 1, select clock speed to ¼ normal (10.24 kHz)

When clock speed is selected, the selectable integration time set will be determined automatically. For example, when **ADC_CLK = 1**, the selectable integration time will be 25ms, 100ms, 200ms or 400ms. Please refer to Table 24 for details.

INT_FLAG (bit 2, R / W): Interrupt Status Report
= 0, no interrupt or was cleared. This bit can be set to 1 or 0 by SMBus command. Setting zero to this bit will set the INT pin to high regardless of the previous state. When it is set to zero, the internal counter for **INT_PERSIST_CTRL** will be reset to 0.
= 1, interrupt triggered. When this bit is 1 and **INT_ENA = 1**, the INT pin will be asserted low and stay low until this bit is set to zero or **INT_ENA = 0**. Writing 1 to this bit will override any internal setting and generate an interrupt if **INT_ENA = 1**. This function is useful for testing user hardware and debugging software.

Note:
ADC will continue to run regardless of the interrupt status unless it is stopped by setting **START_ADC** bit to 0. Note that the ADC integration time is much longer than the interrupt response time. Data output of the ADC that generated the interrupt must be read immediately as the next sampled data by the ADC will write over the D_{COUNT} register during continuous conversion mode.

INT_ENA (bit 1, R / W): Interrupt Enable Bit
= 0, Disable interrupt pin function
= 1, Enable interrupt pin function

Note:
(1) When **INT_ENA = 0**, the INT pin function will be disabled. However, the **INT_FLAG** function could still be used as software interrupt to monitor the ALS readings. The user can still set the thresholds and read the **INT_FLAG** status periodically or when it is needed instead of reading the ALS data and calculating. If the **INT_FLAG = 1**, then it means the ALS reading is outside the boundaries. If this function is not needed, the user just simply ignores the **INT_FLAG** bit status.

(2) When **INT_ENA = 1**, the INT pin will perform the normal interrupt function.

(3) When **ALS_ENA = 0**, the INT pin will be set to high regardless of its previous status.

OV (bit 0, R): Overflow Indicator.
= 0, if D_{COUNT} has reached the maximum value and this bit is still 0, it means that the input light has reached the maximum range but not over.
= 1, 1 on this bit indicates that the D_{COUNT} has reached the maximum value and the input light is over the selected range limit. Bigger range should be selected.

Table 16: Maximum Count for Different T_{INT} Time

Full Scale ADC Output Value @ F_{OSC}= 40.96kHz, RANGE_SEL = 00b (0 ~ 500 lux)	D_{COUNT}	T_{INT} = 100 ms	4095	Counts
	D_{COUNT}	T_{INT} = 50 ms	2047	

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RANGE_SEL = 01b (0 ~ 1000 lux) RANGE_SEL = 10b (0 ~ 5000 lux) RANGE_SEL = 11b (0 ~ 2500 lux)	D_{COUNT}	T_{INT} = 25 ms	1023	
	D_{COUNT}	T_{INT} = 6.25 ms	255	

Note:

ADC output count will be always in the range as specified in the above table. For example, if the T_{INT} is set to 6.25ms, the ADC output count will be less or equal to 255

Register 00h and Send / Receive Byte Protocols application:

When host wants to send control command(s) that is contained in Register 00, for example Enable / Disable ALS or Start ADC conversion, the Send Byte Protocol could be used to simplify the communication. In Send Byte Protocol, bit 7 of the Data Byte field should be set to 1 indicating this is a direct command and this command should be put into Register 00h and executed. The example is shown in Table 17.

Table 17: Send Byte Protocol

1	7	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	1	1
S	**Slave Address**	**Wr**	**A**	**CMD_FLAG**								**A**	**P**
		0		**1**									

Write Byte Protocol could also be used to implement the same function but with a longer communication time.

When using Write Byte / Word protocol to send command / data to registers (including register 00h), bit 7 in command code field should be set to 0 to indicate this byte is for the register address. Bit 6, 5 & 4 except for the Register Address bits (bit 3, 2, 1 & 0) need to be set to zero also. These bits in this command are used for internal test purpose. The detailed Write Byte / Read Byte protocols are shown below.

Table 18: Write Byte Protocol

1	7	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	1	8		1
S	**Slave Address**	**Wr**	**A**	**CMD_FLAG**	**0**	**0**	**0**	**Register Address**				**A**	**Data Byte**	**A**	**P**
		0		**0**				**00 ~ 08h**							

Register 00h could be read back by the host via Receive Byte protocol or Read Byte protocol. When LX1977 receives a Receive Byte protocol, it will send a copy of register 00 data back to the host. When it receives Read Byte protocol, it will put register 00 data in the Data Byte field and send the data back to host. See Table 11 & Table 19 for details.

Table 19: Read Byte Protocol

1	7	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	1	1	7	1	1	8		1
S	**Slave Address**	**Wr**	**A**	**CMD_FLAG**	**0**	**0**	**0**	**Register Address**				**A**	**S**	**Slave Address**	**Rd**	**A**	**Data Byte**	**A**	**P**
		0		**0**				**00 ~ 08h**							**1**			**1**	

Examples of setting register 00h by using Send Byte Protocol

One of the sample LX1977 settings and Send Byte protocol could be as shown below.

Table 20: Sample Send Byte Protocol

1	7	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	1	1
S	**Slave Address**	**Wr**	**A**	**CMD_FLAG**								**A**	**P**
		0		**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**		

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This protocol will send commands to LX1977 and will write the command byte into register 00h for configuring the device settings.

1) Bit 6 will enable LX1977 ALS function
2) Bit 5, 4 will set ADC mode to Continuous Conversion Mode and start ADC
3) Bit 3 will select 40.96 kHz clock frequency as the Sigma-Delta ADC clock
4) Bit 2 will clear the interrupt flag no matter what it was
5) Bit 1 will enable the interrupt function
6) Bit 0 will be ignored since bit 0 of register 00h is a read only bit

Device Control Register 01h (R / W)

Table 21: Control Register 01h

7	6	5	4	3	2	1	0
CLK_SEL	RANGE_SEL		T_{INT}_SET		INT_PERSIST_SET		
Read / Write	Read / Write		Read / Write		Read / Write		

Index Address = 00000001b or 01h
Access = Read / Write
Default = 00000000b

Bit Definitions:

CLK_SEL (bit 7, R / W): Selects the source of the ADC clock
= 0, use internal clock (the actual speed will depend on bit 3 of register 00h setting)
= 1, use SMBus host SCL clock. Since the clock gap between protocols is inconsistent, this mode is not recommended.

RANGE_SEL (bit 6, 5, R / W): Selects the detectable input light range.

Table 22: ADC T_{INT}, Range and Resolution @ ADC Clock = 40.96 kHz

Bit 6	Bit 5	Full Scale Range (lux)	Resolution in Lux /Count			
			T_{INT} = 6.25 ms D_{COUNT} = 233	T_{INT} = 25 ms D_{COUNT} = 931	T_{INT} = 50 ms D_{COUNT} = 1861	T_{INT} = 100 ms D_{COUNT} = 3723
0	**0**	0 ~ 500	2.15	0.54	0.27	0.13
0	**1**	0 ~ 1000	4.29	1.07	0.54	0.27
1	**0**	0 ~ 5000	21.46	5.37	2.69	1.34
1	**1**	0 ~ 2500	10.73	2.68	1.34	0.67

Table 23: ADC T_{INT}, Range and Resolution @ ADC Clock = 10.24 kHz

Bit 6	Bit 5	Full Scale Range (lux)	Resolution in Lux /Count			
			T_{INT} = 25 ms D_{COUNT} = 233	T_{INT} = 100 ms D_{COUNT} = 931	T_{INT} = 200 ms D_{COUNT} = 1861	T_{INT} = 400 ms D_{COUNT} = 3723
0	**0**	0 ~ 500	2.15	0.54	0.27	0.13
0	**1**	0 ~ 1000	4.29	1.07	0.54	0.27
1	**0**	0 ~ 5000	21.46	5.37	2.69	1.34

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1	**1**	0 ~ 2500	10.73	2.68	1.34	0.67

When range is selected, the D_{COUNT} values with different input lux will also change. Please refer to the EC table for the values of 0 ~ 500 lux, 0 ~ 1000 lux, 0 ~ 5000 and 0 ~ 2500 lux light input. The equations for calculating between D_{COUNT} and lux are shown below.

T_{INT}_SET (bit 4, 3, R / W): ADC integration (conversion) time control. The relationship between bit settings and integration times are shown in table below.

Table 24: ALS ADC Integration Time

		Conversion Time / Reading					
		Register 00h, Bit 3 = 0, ADC Clock = 40.96kHz			Register 00h, Bit 3 = 1, ADC Clock = 10.24kHz		
Bit 4	**Bit 3**	**Integration Time**	**Nominal Full Range Reading**	**Max Reading**	**Integration Time**	**Nominal Full Range Reading**	**Max Reading**
0	0	6.25 ms	233	255	25 ms	233	255
0	1	25 ms	931	1023	100 ms	931	1023
1	0	50 ms	1861	2047	200 ms	1861	2047
1	1	100 ms	3723	4095	400 ms	3723	4095

Light input Lux and D_{COUNT} calculation:

LX1977 output D_{COUNT} is in a linear relationship with the light input lux. D_{COUNT} full scale values are determined by integration time as shown above. In the Electrical Characteristics table, D_{COUNT} values are listed in accordance with the specified light input at ADC Clock = 40.96 kHz, integration time = 100ms and at 0 ~ 500 lux, 0 ~ 1000 lux, 0 ~ 5000 lux and 0 ~ 2500 lux range. D_{COUNT} values are related to integration time and the measurement range selected. Below are the conversion methods between D_{COUNT} and light input lux at different integration time.

D_{COUNT} = (Input (lux) / Range) × (Nominal Full Range Reading) Refer to Table 24

For example: 0 ~ 500 lux range, 100 lux input, integration time = 50ms

D_{COUNT} = 100/500 × 1861 = 372 Refer to Table 24

For example: 0 ~ 1000 lux range, 500 lux input, integration time = 100ms

D_{COUNT} = 500/1000 × 3723 = 1862 Refer to Table 24

INT_PERSIST_CTRL (bit 2, 1, 0, R / W): Set the time duration before generating interrupt. **INT_ENA** should be set to 1 to enable the interrupt pin function. The actual time duration is determined by bit 3 of register 00h and bit 3 & 4 of this register. Please refer to **T_{INT}_SET** description.

= 000, generate interrupt after ADC conversion
= 001, generate interrupt if ADC result out of range
= 010, generate interrupt if ADC result out of range for 2 consecutive T_{INT} time
= 011, generate interrupt if ADC result out of range for 3 consecutive T_{INT} time
= 100, generate interrupt if ADC result out of range for 4 consecutive T_{INT} time
= 101, generate interrupt if ADC result out of range for 5 consecutive T_{INT} time
= 110, generate interrupt if ADC result out of range for 10 consecutive T_{INT} time

= 111, generate interrupt if ADC result out of range for 15 consecutive T_{INT} time

Note:

(1) When **INT_FLAG** of register 00h is cleared via SMBus command after an interrupt response, the internal counter for **INT_PERSIST_CTRL** will be reset to 0.

(2) For out-of-range conditions in the same direction, the persistence counter increments. If within the programmed T_{INT} time period, anytime an ADC conversion completes and the result is no longer out-of-range, the count starts over. If the output result is between the thresholds (in-range), then counter resets to '0'. If the value goes out of range in the other direction, the counter starts over at '1'.

(3) Note that once the interrupt is triggered and the INT pin is asserted low, the INT pin will stay low until INT_FLAG bit is set to zero or INT_ENA is set to 0.

(4) Generating an interrupt for x consecutive T_{INT} integration time only applies to continuous conversion mode.

Register 01h and Write / Read Byte Protocols application:

For programming register 01h, a Write Byte protocol should be used.

When using Write Byte / Word protocol to send command / data to registers (including register 00h), bit 7 in command code field should be set to 0 to indicate this byte is for the register address. Other bits (bit 6, 5 & 4) except for the Register Address bits (bit 3, 2, 1 & 0) need to be set to zero also. The detailed Write Byte / Read Byte protocols are shown below.

Note: Register 01h should be set prior to register 00h in order to get meaningful ALS read out.

Table 25: Write Byte Protocol:

1	7	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	1	8		1
S	**Slave Address**	**Wr**	**A**	**CMD_FLAG**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**A**	**Data Byte**	**A**	**P**
		0		**0**				**01h**							

Register 01h could be read back by the host by using a Read Byte protocol. When LX1977 receives a Read Byte protocol, it will put register 01h data into the Data Byte field and send the data back to the host. Please see Table 11 & Table 19 for details.

Table 26: Read Byte Protocol:

1	7	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	1	1	7	1	1	8		1
S	**Slave Address**	**Wr**	**A**	**CMD_FLAG**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**A**	**S**	**Slave Address**	**Rd**	**A**	**Data Byte**	**A**	**P**
		0		**0**				**01h**							**1**			**1**	

Examples of setting register 01h by using Write Byte Protocol

Write Byte protocol is shown below (only the Data Byte is in detail, please refer to Table 26).

Table 27: Write Byte Protocol:

1	7	1	1		1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	1	1
S	**Slave Address**	**Wr**	**A**	**Command Code**	**A**									**A**	**P**
		0				**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**		

The above example will write data byte 15h into register 01h to set the following configurations:

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1) Bit 7 will select the internal clock
2) Bit 6 & 5 will set detectable range to 0 ~ 500 lux
3) Bit 4, 3 will set the integration time or conversion time to either 50ms or 200ms depending on register 00h bit 3 setting. If bit 3 is 0, then the integration time is 50ms, otherwise it is 200ms
4) Bit 2, 1 & 0 will set LX1977 to generate interrupt after D_{COUNT} is above the high threshold for 5 consecutive times or below the low threshold for 5 consecutive times

Register 01h could be read back by the host by using Read Byte protocol. When LX1977 receives Read Byte protocol, it will put register 01 data in the Data Byte field and send back to host. See Table 11 for details.

Low Threshold Register 02h, 03h (R / W)

Table 28: Low Threshold Lower Byte Register 02h

7	6	5	4	3	2	1	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write

Table 29: Low Threshold Higher 4 bits Register 03h

7	6	5	4	3	2	1	0
0	0	0	0	Bit 11	Bit 10	Bit 9	Bit 8
N / A	N / A	N / A	N / A	Read / Write	Read / Write	Read / Write	Read / Write

Index Address = 00000010b, 00000011b or 02h, 03h
Access = Read / Write
Default = 00000000b, 00000000b

These two registers set the low threshold value of the interrupt function. If the ALS readout D_{COUNT} is lower than this value for the period of time set per **INT_PERSIST_CTRL (**register 01h bit 2, 1, 0**)**, the **INT_FLAG** will be set to 1 and if the **INT_ENA** is 1, the INT pin will be pulled low to indicate an interrupt on the INT pin.

For example, if **INT_ENA** is set to 1 and **INT_PERSIST_CTRL = 101** and the integration time is set to 100ms, and if the D_{COUNT} value is lower than this register value for consecutive five times, i.e. 5 x 100 = 500ms, then an interrupt flag **INT_FLAG** will be set and if **INT_ENA = 1**, the INT pin will be asserted low. If the **INT_PERSIST_CTRL** programmed time period is not reached and a new D_{COUNT} value is between this Low Threshold value and the High Threshold value, the counter for **INT_PERSIST_CTRL** will be reset to zero. If the **INT_PERSIST_CTRL** programmed time period is not reached and a new D_{COUNT} value is greater than the High Threshold value, the counter starts over at '1'.

Bit 7 to bit 4 in register 03h are always zero and can not be changed.

High Threshold Register 04h, 05h (R / W)

Table 30: High Threshold Lower Byte Register 04h

7	6	5	4	3	2	1	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write

Table 31: High Threshold Higher 4 bits Register 05h

7	6	5	4	3	2	1	0
0	0	0	0	Bit 11	Bit 10	Bit 9	Bit 8
N / A	N / A	N / A	N / A	Read / Write	Read / Write	Read / Write	Read / Write

Index Address = 00000100b, 00000101b or 04h, 05h
Access = Read / Write
Default = 11111111b, 00001111b

These two registers set the high threshold value of the interrupt function. If the ALS readout D_{COUNT} is higher than this value for the period of time set per **INT_PERSIST_CTRL (**register 01h bit 2, 1, 0**)**, The **INT_FLAG** will be set to 1 and if the **INT_ENA** is 1, the INT pin will be pulled low to indicate an interrupt on the INT pin.

For example, if **INT_PERSIST_CTRL = 101** and the integration time is set to 100ms, and if the D_{COUNT} value is higher than this register value for consecutive five times, i.e. 5 x 100 = 500ms, then an interrupt flag **INT_FLAG** will be set and if **INT_ENA = 1**, the INT pin will be asserted low. If the **INT_PERSIST_CTRL** programmed time period is not reached and a new D_{COUNT} value is between the Low Threshold value and this High Threshold value, the counter for **INT_PERSIST_CTRL** will be reset to zero. If the **INT_PERSIST_CTRL** programmed time period is not reached and a new D_{COUNT} value is lower than Low Threshold value, the counter starts over at '1'.

Bit 7 to bit 4 in register 05h are always zero and can not be changed.

ALS ADC Data Register 06h, 07h (R)

Table 32: ALS ADC D_{COUNT} Lower Byte Register 06h

7	6	5	4	3	2	1	0
Data bit 7	Data bit 6	Data bit 5	Data bit 4	Data bit 3	Data bit 2	Data bit 1	Data bit 0

Table 33: ALS ADC D_{COUNT} Higher Byte Register 07h

7	6	5	4	3	2	1	0
0	0	0	0	Data bit 11	Data bit 10	Data bit 9	Data bit 8

Index Address = 00000110b, 00000111b or 06h, 07h
Access = Read Only
Default = 00000000h, 00000000h

After each ADC conversion, the ADC output data will be stored in registers 06h and 07h. Once the data is stored, the ADC will start another conversion again. Note that registers 06h and 07h act as a buffer between the ADC output counter and the SMBus interface. Therefore, even when an ADC conversion is in process, the last conversion result will still be available in the registers to read.

Note that for the purpose of ADC data integrity control, when T_{INT} is greater than 6.25ms (in 40.96kHz Mode), or T_{INT} is greater than 25ms (in 10.24kHz Mode), Read Word Protocol should be used to read the two bytes of ADC data. If data is read by using Read Byte Protocol two consecutive times to read register 06h and 07h sequentially, the data in these registers might be updated before the time of executing the second Read Byte Protocol. Thus, the second read byte may not correspond to the original value

When T_{INT} is set to 6.25ms (in 40.96kHz Mode) or 25ms (in 10.24 kHz Mode), Read Byte Protocol could be used to read out the lower byte to reduce the communication time. Since for these integration times, the ADC results will be always less or equal to 255 and only data in register 06h will be relevant. The ADC result is updated per the integration time set by **T_{INT}_SET** (register 01h, bit 4, 3) when ADC is enabled by **START_ADC** (register 00h, bit 5).

These two registers can be read any time even while the ADC conversion is in process. When an ADC conversion is in process, the read data will correspond to the last conversion result.

Identification Register 08h (R)

Table 34: Identification Register 08h

7	6	5	4	3	2	1	0
MFG4	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0
0	0	0	0	1	1	0	0

Index Address = 00001000b or 08h
Access = Read Only
Default = 00001100b

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ALS D_{COUNT} VS LIGHT INPUT

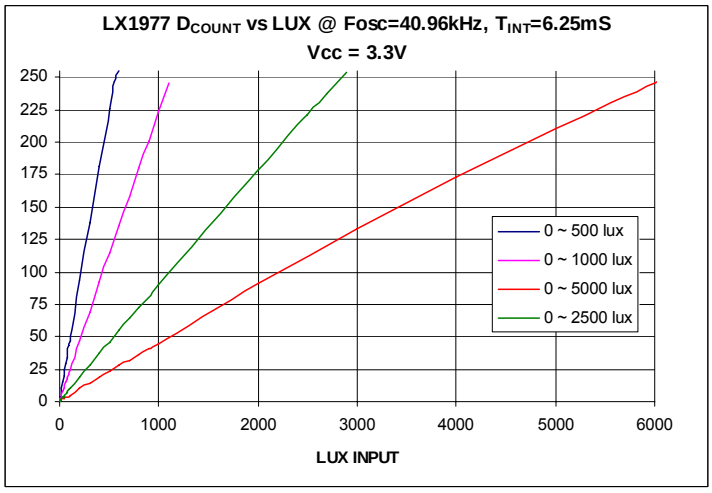

Chart 1 – D_{COUNT} vs Light Input, TINT=6.25mS @ Different Range

ALS D_{COUNT} VS LIGHT INPUT

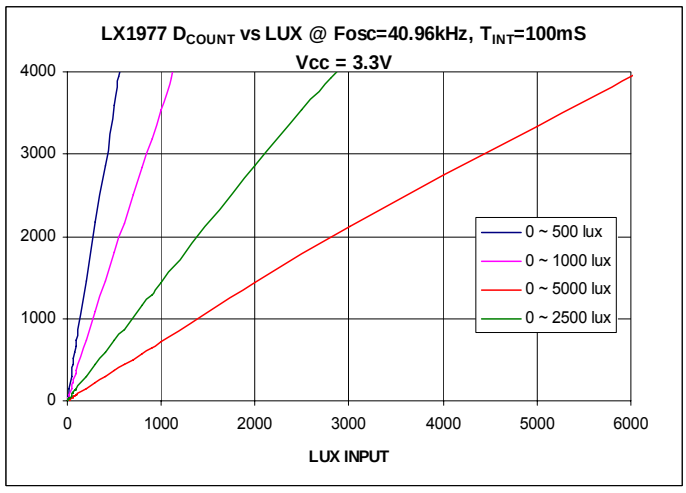

Chart 2 – D_{COUNT} vs Light Input, TINT=100mS @ Different Range

ALS D_{COUNT} VS LIGHT INPUT

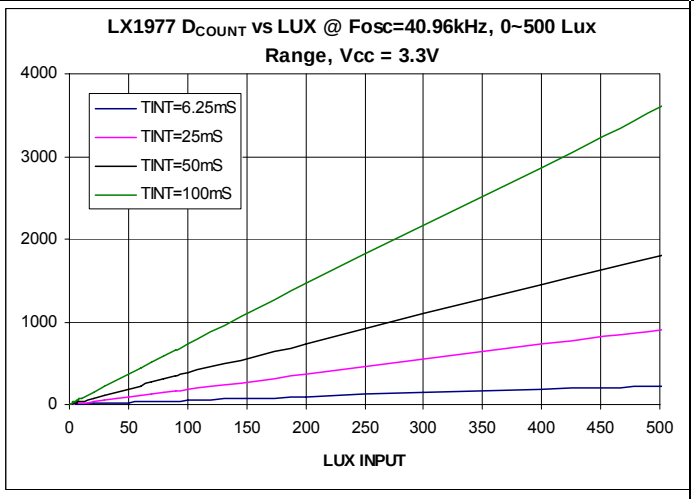

Chart 3 – D_{COUNT} vs Light Input @ Different T_{INT} for 0 ~ 500 lux Range

ALS D_{COUNT} VS LIGHT INPUT

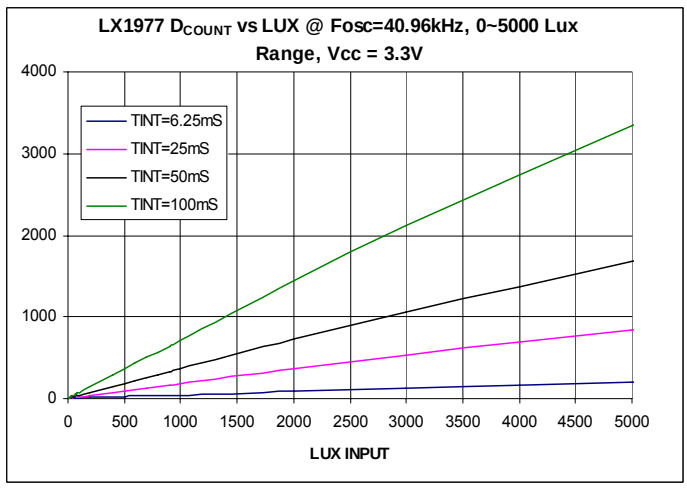

Chart 4 – D_{COUNT} vs Light Input @ Different T_{INT} for 0 ~ 1000 lux Range

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ALS, SPECTRAL RESPONSE

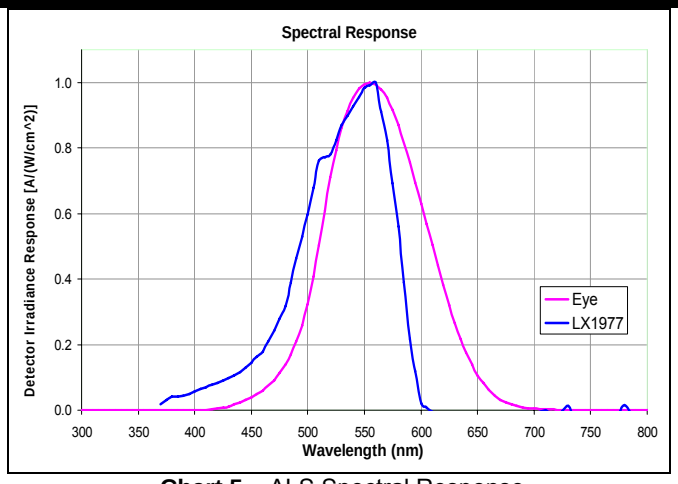

Chart 5 – ALS Spectral Response

DCOUNT VS TEMP

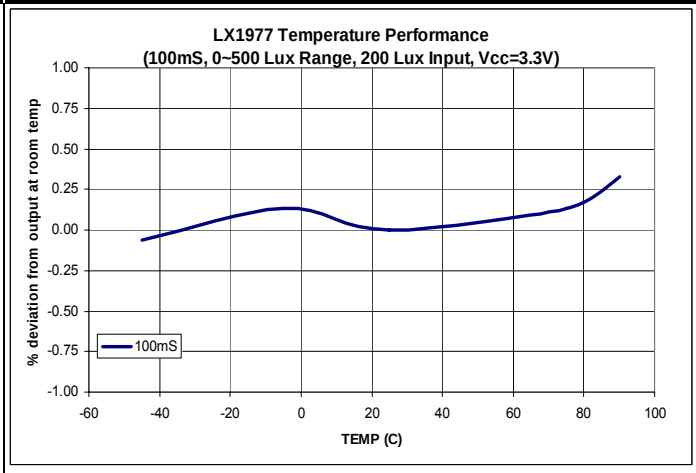

Chart 6 – D_{COUNT} vs Temperature

ALS DCOUNT VS VDD

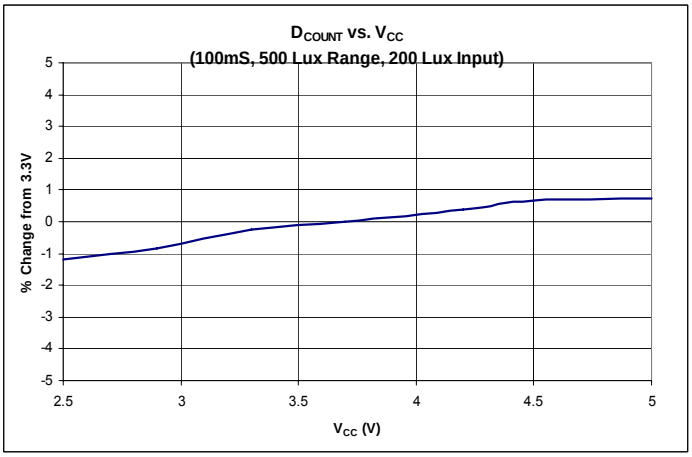

Chart 7 – ALS Output D_{COUNT} vs Supply Voltage

IDD VS TEMP

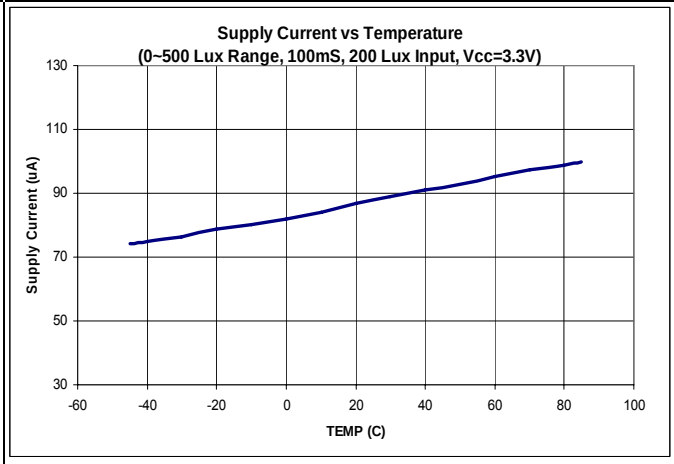

Chart 8 – Device Supply Current vs Temperature

ALS, ANGULAR RESPONSE

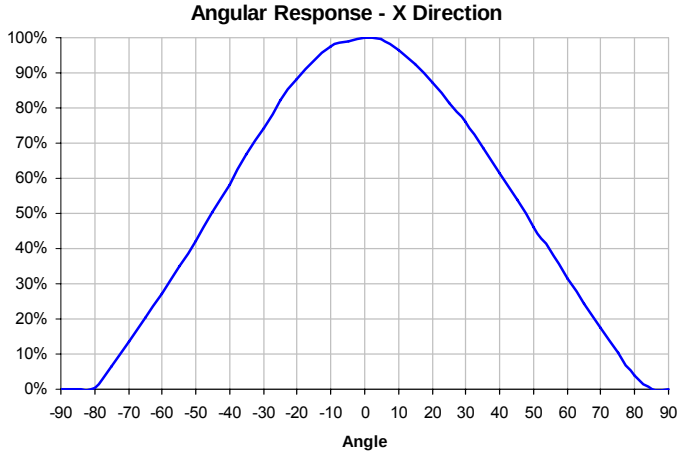

Chart 9 – Angular Response X Direction

ALS, ANGULAR RESPONSE

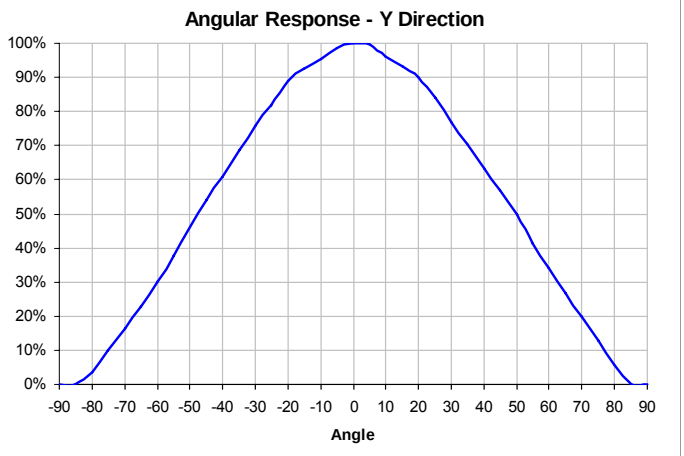

Chart 10 – Angular Response Y Direction

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11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

TYPICAL APPLICATION

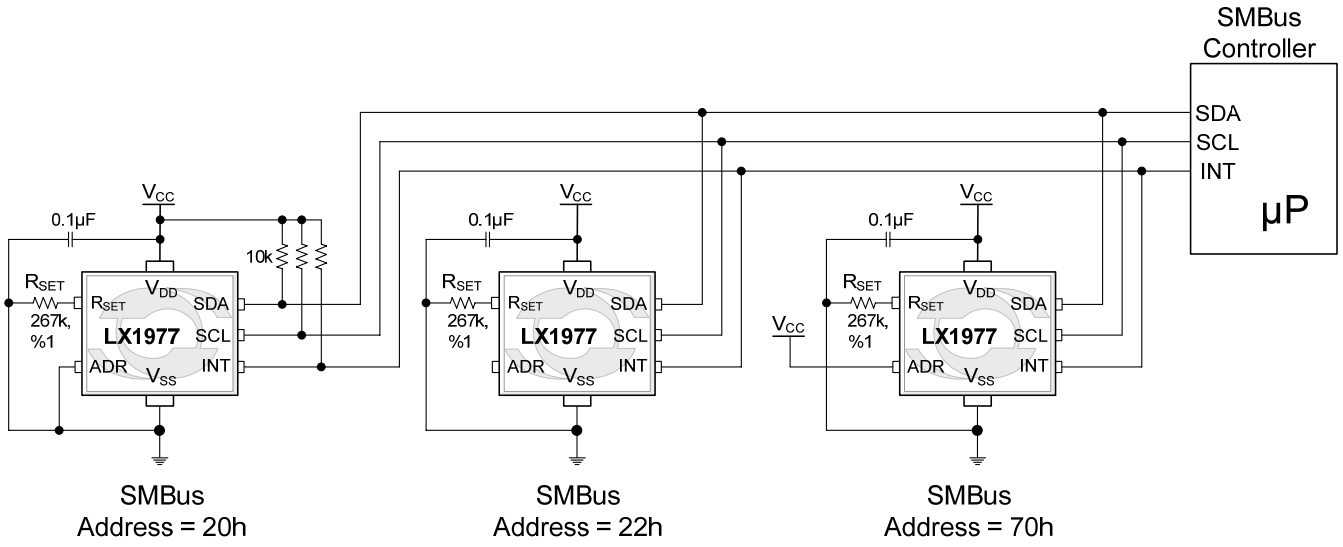


Figure 5 – Typical Application 1

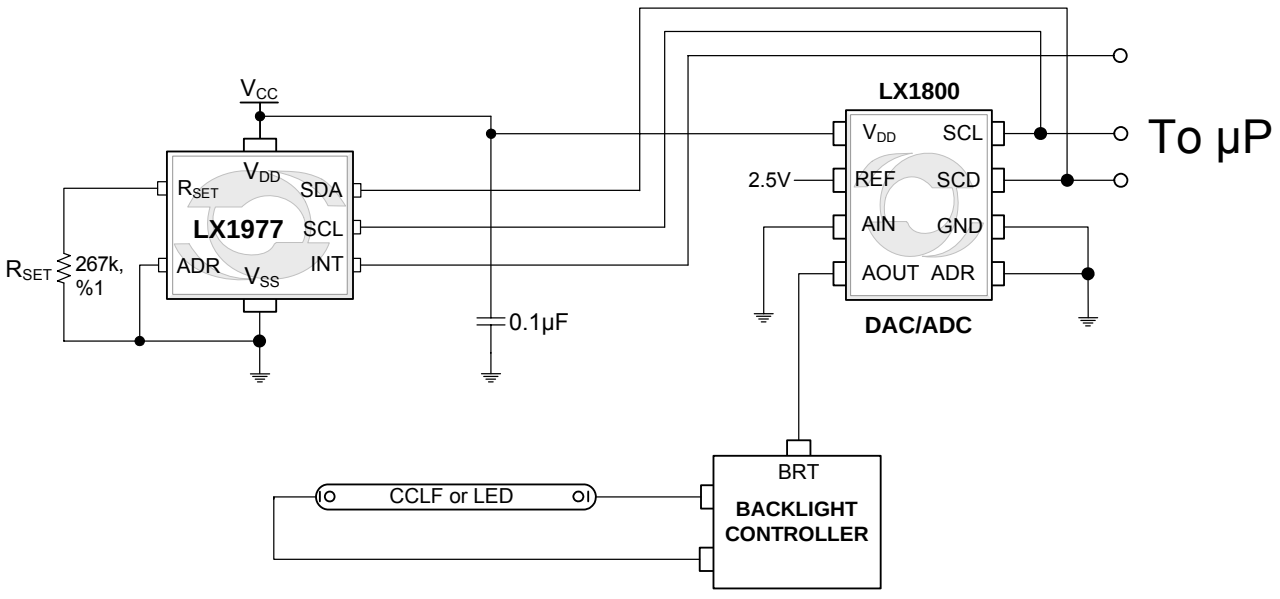
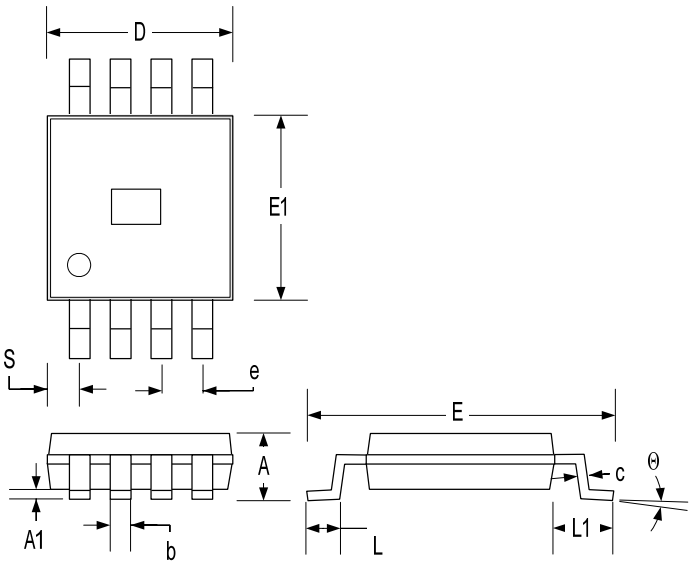


Figure 6 – Typical Application 2

PACKAGE DIMENSIONS

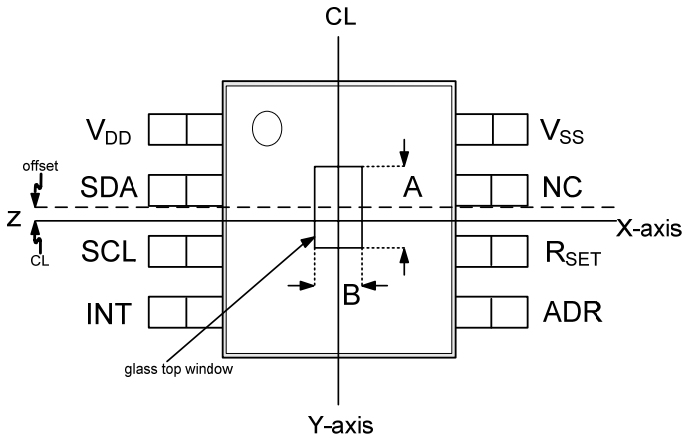
DU — Glass Top 8-Pin MSOP



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	1.10	–	0.043
A1	0.05	0.15	0.002	0.006
b	0.26	0.41	0.010	0.016
c	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
e	0.65 BSC		0.025 BSC	
E	4.75	5.05	0.187	0.198
E1	2.90	3.10	0.114	0.122
L	0.41	0.71	0.016	0.028
L1	0.95 BSC		0.037 BSC	
S	0.525 BSC		0.021 BSC	
Θ	3°		3°	

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.



Dim	MILLIMETERS	MILS
	Typ	Typ
A	0.76	30
B	0.5	20
Z	0.2	7.8

Note:

1. CL represents the centered X and Y axis of the package.
2. Z is the vertical offset from the X axis that centers the glass top window.
3. A and B are the dimensions of the glass top window.
4. Values listed in the table are typical numbers.

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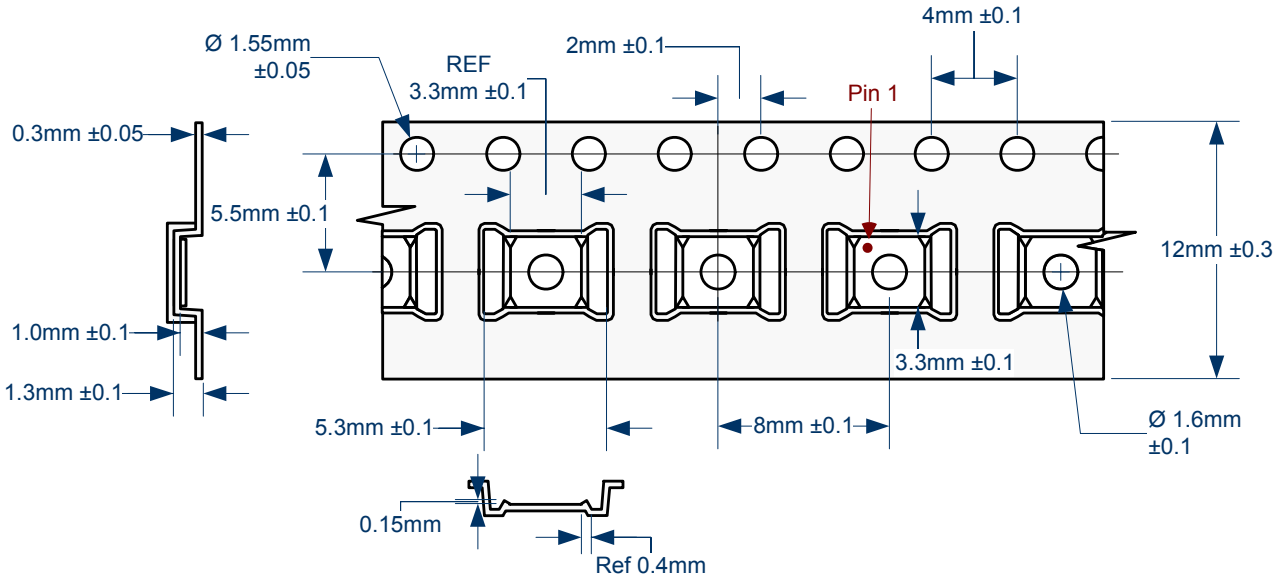
PACKAGE TAPE AND REEL INFORMATION



DU Package Tape and Reel Information