

System Motor Driver IC for CD/DVD players

5ch System Moter Driver

BD8203EFV

No.10011EAT02

Description

BD8203EFV is 5ch system motor driver for CD/DVD. A linear BTL method can be adopted for all 5ch and a low noise be designed. Built-in 5V regulator, a changeable regulator, and a general-purpose operational amplifier, and it is the best for the system design for car audio.

Features

- 1) Linear BTL method is adopted for the actuator driver and the DC motor driver and a low noise is achieved.
- 2) Loading driver 1CH
- 3) Built-in regulator 2CH (1ch output changeability)
- 4) MUTE function and Standby function
- 5) Built-in general-purpose operational amplifier 1CH
- 6) Built-in internal operational amplifier for the voltage detection between driver outputs and for Vc standard

Applications

Car Audio

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Power supply voltage	PREVCC,PVCC1,PVCC2, REGVARVCC	15	V
Input terminal voltage1	VIN1*1	PREVCC	V
Input terminal voltage2	VIN2*2	REG5	V
Output terminal voltage	VOUT*3	REG5	V
Operating temperature range	Topr	-40~85	°C
Storage temperature	Tstg	-55~150	°C
Junction temperature	Tjmax	150	°C

*1 Input terminal 1 : REGRST

*2 Input terminal 2 : REGCTL,MUTE123,MUTE4,VCI,RVS,FWD,IN1,IN2,IN3,IN4,OPIN+,OPIN-,VCTL

*3 Output terminal : VCO,TSDM,VSPDL

Power Dissipation

	Symbol	HTSSOP-B40	
Power dissipation	Pd (#1)	4.7W	

#1 Ta =25°C, Standard board mounting

(70mm×70mm×1.6mm,occupied copper foil is less than 3%, 4 glass epoxy layer substrate, 70mmx70mm of the back copper foil area) Reduce power by 34.6mW for each degree above 25°C.

●Recommended Operating Conditions (Ta=-40~+85°C)

(Set the power supply voltage taking allowable dissipation into considering.)

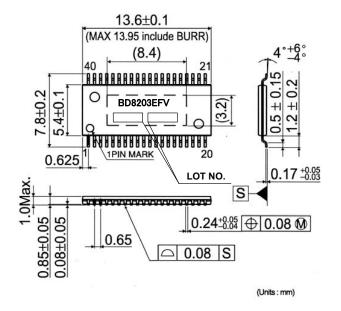
Parameter	Symbol	MIM.	TYP.	MAX.	Unit
Driver part Pre steps and regulator 1 power-supply voltage	PreVcc	7.5	8	14	V
Driver part power steps power-supply voltage	PVcc1,PVcc2	4.5	8	PreVcc	V
Power steps of two regulators power-supply voltage	REGVARVcc	4.5	5	PreVcc	V

•Electrical Characteristics

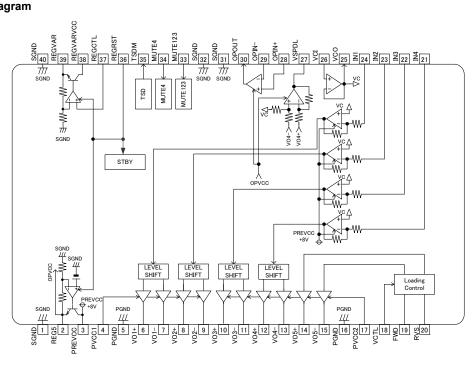
(Unless otherwise noted PREVCC=PVCC1=PVCC2 =8V, REGVARVCC=5V, VCO=1.65V, Ta=25°C)

(Unless otherw	vise noted PREVCC=PVCC1=P	VUUZ -0V, KEV	GVARVC	C = 5V,	vco-1.	000, 10	-23 0)
	Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Circuit current	Quiescent current	IQ	-	37	55	mA	MUTE123=MUTE4=H ,FWD=RVS=L
	Standby-on current	ISTBY	-	-	1	mA	Standby mode(REGRST=L)
	Input offset voltage	VIOBTL	-5	0	5	mV	
	Output offset voltage	VOFBTL	-75	-	75	mV	
3TL Driver	Output saturation voltage (vertical harmony)	VOSATBTL	-	1.5	2.3	V	IL=500mA
	Input output gain	GVBTL	16.8	18	19.2	dB	
	Input impedance	ZINBTL	20	40	80	kΩ	
	Slew rate	VSLBTL	1.0	-	-	V/usec	
	Input offset voltage	VIOOP1	-10	-	10	mV	
	Input bias voltage	IbOP1	-300	-	-	nA	
	H level output voltage	VOHOP1	4	-	-	V	
General-purpose	L level output voltage	VOLOP1	-	-	0.2	V	
perational amplifier	Output sink current ability	ISINKOP1	2	-	-	mA	
	Output source current ability	ISOUOP1	2	-	-	mA	
	Range of same phase input	VICMOP1	0		3.8	V	REG5=5.0V
	Slew rate	VSLOP1	0.5	-	-	V/usec	
	Output offset voltage	VOOOP2	-50	-	50	mV	Vo4+=Vo4-=3.4V
	H level output voltage	VOHOP2	4	-	-	V	
Descritional amplifica-	L level output voltage	VOLOP2	-	-	0.2	V	
Operational amplifier or the voltage	Output sink current ability	ISINKOP2	2	-	-	mA	
letection between	Output source current ability	ISOUOP2	2	-	-	mA	
friver outputs	Range of same phase input	VICMOP2	0		6.8	V	REG5=5.0V
	Input output gain	GVOP2	-6.2	-5	-3.8	dB	
	Slew rate	VSLOP2	0.5	-	-	V/usec	
	Output offset voltage	VOOOP3	-10	-	10	mV	
	Input bias voltage	IbOP3	-300	-	-	nA	
nternel en evetienel	H level output voltage	VOHOP3	3.5	-	-	V	
nternal operational amplifier for	L level output voltage	VOLOP3	-	-	0.2	v	
/c standard	Output sink current ability	ISINKOP3	0.5	_	-	mA	
	Output source current ability	ISOUOP3	10	-	-	mA	
	Range of same phase input	VICMOP3	1.1	-	3.5	V	REG5=5.0V BTL Range of operation
	Input terminal inflow current	IINLD	-	27	55	μA	FWD,RVS=3.3V
	VCTL terminal inflow current	IINVCTL	-1	-	-	μΑ	VCTL=2V
	Output offset voltage	VOFLD	-50	0	50	mV	
oading driver	Output saturation voltage H	VOHLD		1.1	1.4	V	IL=500mA
	Output saturation voltage L	VOLLD	-	0.45	0.8	V	IL=500mA
		GVLD	7.5	9.0	10.5	dB	VCTL=1V
	Input output gain	VOREG5	4.75	5.0	5.25	V	IL=100mA
	REG5 terminal output voltage REG5 terminal output current ability	REG5 I	4.75	5.0	- 5.25		
Regulator 1	, ,	-		-	-	mA	II -0 .: 100m A
	Load change regulation	VREG5_LOAD	-80	-	-		IL=0→100mA
	Input change regulation	VREG5_LINE	-20	-	30	mV	PREVCC=7.5→9V,IL=100mA
	Range of REGVAR output voltage setting	VREGVARR	0.5	-	4.1	V	IL=100mA
	REGVAR terminal output current ability	REGVAR_I	100	-	-	mA	
	REGVAR terminal output voltage	VREGVAR	3.4	3.6	3.8	V	IL=100mA,REGCTL=3.3V
Regulator 2	Input output gain	GV2	-	1.09	-	V/V	
output changeability)	Load change regulation	VREGVAR_LOAD	-80	-	-	mV	IL=0→100mA
	Input change regulation	VREGVAR_LINE	-20 REGVAR	-	30	mV	REGCTL=3.3V, REGVARVCC=4.5→5.5V, IL=100mA
	Range of REGVARVCC voltage	VREGVAR_ON	+0.9V	-	PREVCC	V	
	REGCTL terminal input current	REGCTL_I	-1	-	-	μA	REGCTL=3.3V
	Input voltage of input terminal H	VIHFUN	2.0	-	PREVCC	V	MUTE123,MUTE4,RVS,FWD
	Input voltage of input terminal L	VILFUN	-	-	0.8	V	MUTE123,MUTE4,RVS,FWD
	TSDM terminal L output voltage	VOL_TSDM	-	-	0.4	V	TSDM=33kΩ Pull-up3.3V)
unction	VCO drop mute voltage	VMVCO	0.4	0.7	1	V	
	PREVCC drop mute voltage	VMPREVCC	3.4	3.8	4.2	V	
	REGRST terminal reset ON voltage	RESON1	-	-	0.8	V	Turning off of regulator 1 and regulator

Package Outlines



Block Diagram



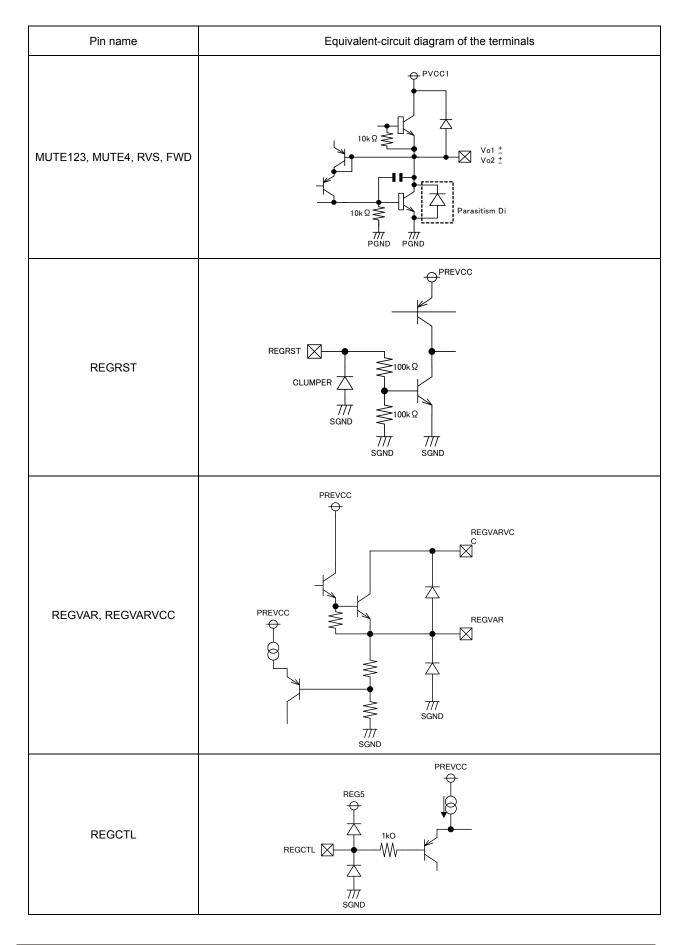
HTSSOP-B40

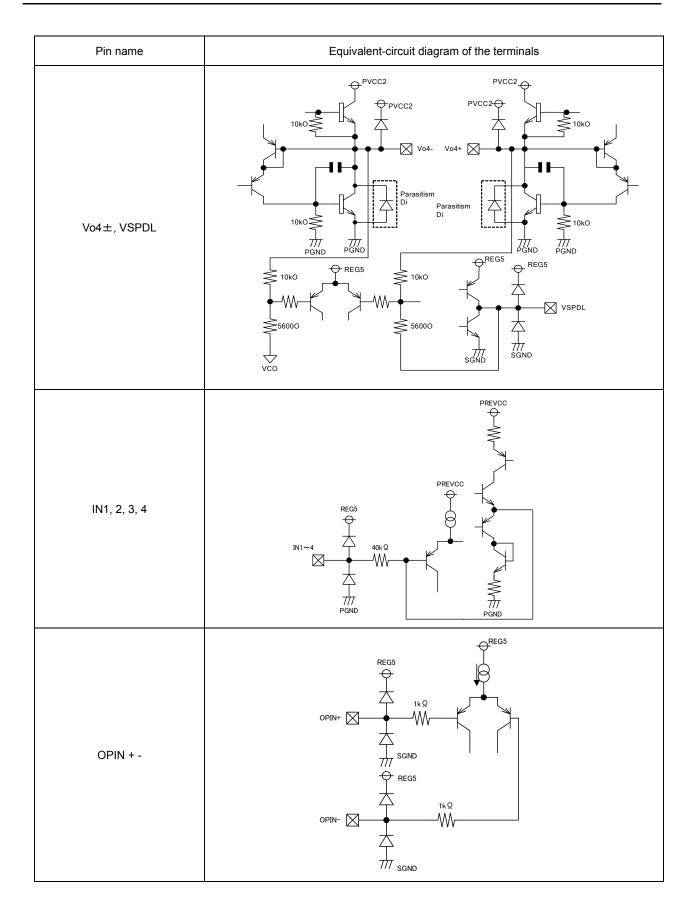
Pin Description

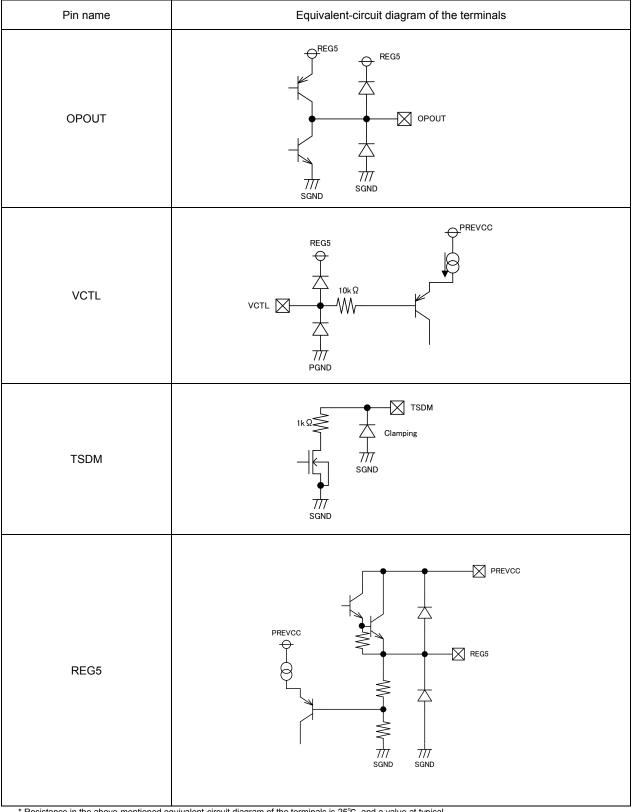
	escription				
No.	Symbol	Description	No.	Symbol	Description
1	SGNT	Signal GNT	40	SGNT	Signal GNT
2	REG5	REG5V Output	39	REGVAR	REGVAR output
3	PREVCC	PRE part, REG circuit, power supply terminal(+8V)	38	REGVARVCC	REGVAR Tr power supply terminal
4	PVCC1	Power supply 1	37	REGCTL	REGVAR Output changeability input terminal
5	PGNT	Power GNT	36	REGRST	REG Reset input
6	V01+	CH1(FCS) Positive output	35	TSDM	Thermal shutdown flag output
7	VO1-	CH1(FCS) Negative output	34	MUTE4	MUTE CH4(SPDL)
8	VO2+	CH2(TRK) Positive output	33	MUTE123	MUTE CH1,2,3
9	VO2-	CH2(TRK) Negative output	32	SGNT	Signal GNT
10	VO3+	CH3(SLD) Positive output	31	SGNT	Signal GNT
11	VO3-	CH3(SLD) Negative output	30	OPOUT	General purpose OP amplifier output
12	VO4+	CH4(SPDL) Positive output	29	OPIN-	General purpose OP amplifier reversing input
13	VO4-	CH4(SPDL) Negative output	28	OPIN+	General purpose OP amplifier non-reversing input
14	VO5+	CH5(LOAD) Positive output	27	VSPDL	Voltage detection value output between VO4 outputs
15	VO5-	CH5(LOAD) Negative output	26	VCI	Standard voltage (Vc) input
16	PGNT	Power GNT	25	VCO	Standard voltage (Vc) output
17	PVCC2	Power supply 2	24	IN1	CH1(FCS) input
18	VCTL	CH5(LOAD) Voltage control input	23	IN2	CH2(TRK)input
19	FWD	CH5(LOAD) FWD input	22	IN3	CH3(SLD)input
20	RVS	CH5(LOAD) RVS input	21	IN4	CH4(SPDL)input

●Equivalent-Circuit Diagram of the Terminals

Equivalent-Circuit Diagram of the Tern Pin name	Equivalent-circuit diagram of the terminals
Vo1± Vo2±	Vo1 ± 10k Ω Vo1 ± Vo2 ± 10k Ω Parasitism D PGND PGND
Vo3± Vo5±	PVCC2
VCI	REG5 VCI 1kQ VCI 1kQ SGND
VCO	PREVCC VCO W W W W W W W W W W W W W







Functional Description

Table for operation (PREVCC=PVCC1=PVCC2=8.0V,REGVARVCC=5.0V,VCO=1.65V)

		Input					Out	put		
REGRST	MUTE123	MUTE4	FWD	RVS	REG5	REGVAR	Operational amplifier	Vo1~Vo3	Vo4	Vo5
Low	-	-	-	-	STANDBY	STANDBY	STANDBY	STANDBY	STANDBY	STANDBY
High	Low	Low	-	-	ON	ON	ON	OFF	OFF	
High	High	Low	-	I	ON	ON	ON	ON	OFF	
High	Low	High	-	-	ON	ON	ON	OFF	ON	
High	High	High	-	-	ON	ON	ON	ON	ON	
High	-	-	Low	Low	ON	ON	ON			OFF
High	-	-	High	Low	ON	ON	ON			Forward
High	-	-	Low	High	ON	ON	ON		/	Reverse
High	-	-	High	High	ON	ON	ON			Brake

①BTL driver control

BTL driver's ON/OFF can control with MUTE123 and MUTE4 terminal.

	Input		Output mode	Vo1(FCS), Vo2(TRK), Vo3(SLD)	Vo4(SPDL)
REGRST	MUTE123	MUTE4	Output mode	VOI(FC3), VO2(TRR), VO3(3LD)	V04(SFDL)
Low	-	-	STANDBY	HI-Z	HI-Z
High	Low	Low	ALL OFF	HI-Z(M) *1	HI-Z(M) *1
High	High	Low	FCS, TRK, SLD,	ON	HI-Z(M) *1
High	Low	High	SPDL ON	HI-Z(M) *1	ON
High	High	High	ALL ON	ON	ON

*1 Vo1⁺ = Vo1⁻ = PVCC1/2 V (typ),Vo2⁺ = Vo2⁻ = PVCC1/2 [V] (typ)

Vo3⁺ = Vo3⁻ = (PVCC2-0.7)/2 V (typ),

Vo4^{*} = Vo4^{*} = [[(PVCC2-0.7)2] × 15.6 + VCO × 20] / (15.6 + 20) [V] (typ) at Hi-Z(M). (Example) Vo4^{*} = Vo4^{*} ≒ 2.53 [V](typ) at PVCC2=8V,VCO=1.65V

2 Loading driver

Only the loading can be independently operated with VCTL, FWD, and RVS terminal.

(ON/OFF by the function of MUTE123 and MUTE4 terminal is not controlled.)

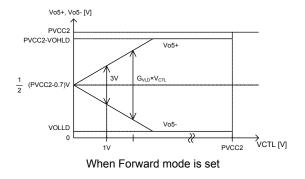
It operates according to the truth table below.

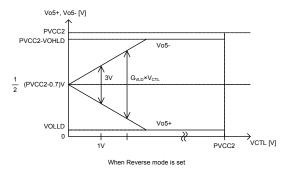
	Ir	iput			Voltage between	$\lambda = \Gamma^{+}(4.4 \text{ min})$	
REGRST	VCTL(18pin)	FWD(19pin)	RVS(20pin)	Output mode	outputs	Vo5 ⁺ (14pin)	Vo5 ⁻ (15pin)
Low	-	-	-	STANDBY	0	Hi-Z	Hi-Z
High	*2	L	L	OFF	0	Hi-Z(M) *3	Hi-Z(M) *3
High	*2	Н	L	Forward	$G_{VLD} \times V_{CTL}$	Н	L
High	*2	L	Н	Reverse	$G_{VLD} \times V_{CTL}$	L	Н
High	*2	Н	Н	Brake	0	M *4	M *4

*2 VCTL(18pin) is an arbitrary value of 0- REG5 (= 5.0V(typ)).

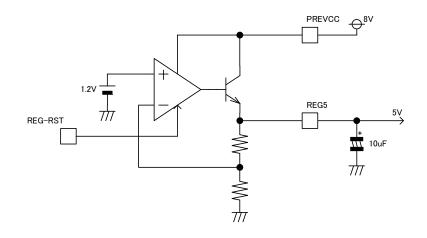
*3 Vo5+= Vo5-= (PVCC2-0.7)/2V (typ) at Hi-Z(M).

*4 Vo5⁺ = Vo5⁻ = (PVCC2-0.7)/2V (typ) at M.





③ 5V regulator 1

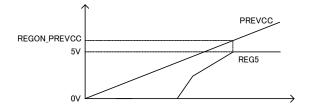


©Regulator 1 control

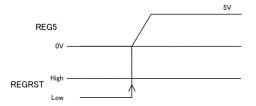
ON/OFF of regulator 1 can control with REGRST terminal.

REGRST	Regulator 1
Low	OFF
High	ON

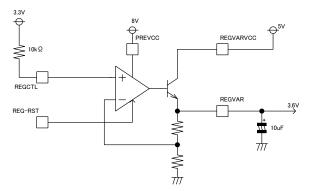
©Vcc−Vo Characteristic



©Timing chart



(4)3.6V changeable regulator 2

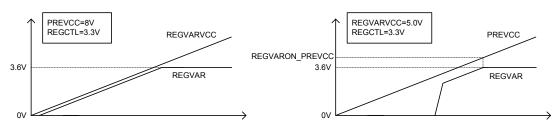


©Regulator 2 controls

ON/OFF of regulator 2 can control with REGRST terminal.

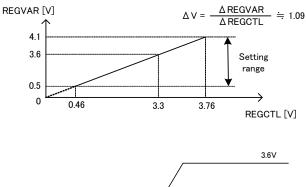
REGRST	Regulator 2
Low	OFF
High	ON

©Vcc-Vo Characteristic

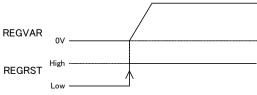


©REGCTL−Vo Characteristic

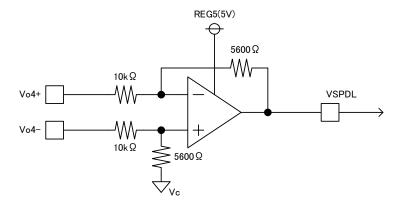
It is changeable according to the terminal REGCTL in linear as for the output voltage of REGVAR. The range of REGVAR of the output voltage setting is 0.5-4.1V(At REGVARVCC=5V (typ.)).





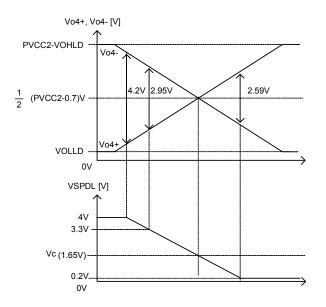


(5) OPAMP for the voltage detection between driver outputs



The voltage difference of Vo4+, Vo4- of the BTL driver for SPDL is detected and it outputs to VSPDL terminal.

$$V_{SPDL} = \frac{5600}{10k} (Vo4-Vo4+) + Vc$$

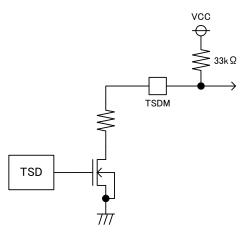


⑥ Thermal shutdown flag output function

TSDM = Hi-Z in operation usually

When a thermal shutdown operates, TSDM terminal becomes Low.

When a thermal shutdown operates, every driver output (Vo1-Vo5) and regulator output (REG5, REGVAR) is made to turn off (output HI-Z).



Thermal shutdown	TSDM
OFF	Hi-Z
ON	Low

⑦Power supply drop mute and VC drop mute function

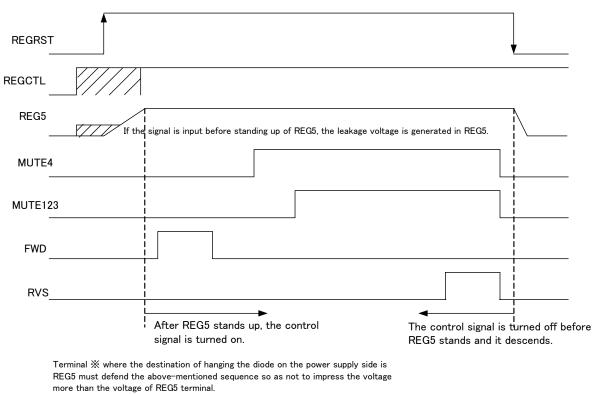
All driver outputs (Vo1-Vo5) are turned off (output HI-Z) by the power supply drop mute function at PREVCC<VMPREVCC(3.8Vtyp).

driver outputs (Vo1-Vo4) are turned off (output HI-Z) by the VC drop mute function at VCO<VMVCO(0.7Vtyp).

Mute function list (REGRST=MUTE123=MUTE4=FWD=High at the mode state of turning on)

Thermal shutdown	PREVCC	VCO	REG5,REGVAR	VO1~VO4	VO5
OFF	>VMPREVCC	>VMVCO	ON	ON	ON
ON	-	-	OFF	OFF	OFF
OFF	<vmprevcc< td=""><td>-</td><td>ON</td><td>OFF</td><td>OFF</td></vmprevcc<>	-	ON	OFF	OFF
OFF	>VMPREVCC	<vmvco< td=""><td>ON</td><td>OFF</td><td>ON</td></vmvco<>	ON	OFF	ON

⑧Start-up sequence regulations



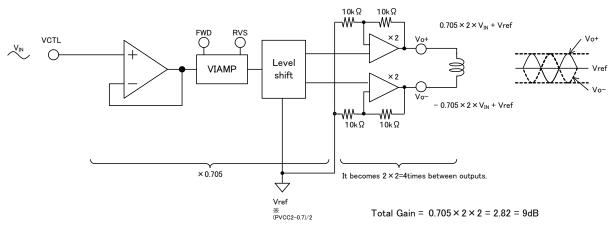
Please insert in the cereal and use the limit resistance for the terminal when you impress the voltage more than the voltage of REG5 terminal.

(Limit resistance $10k\,\Omega$ or more is inserted in the cereal about REGCTL terminal.)

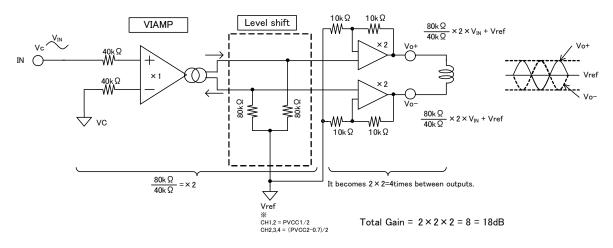
%Terminal where destination of hanging diode on power supply side is REG5 REGCTL, MUTE123, MUTE4, VCI, RVS, FWD, IN1, IN2, IN3, IN4, OPIN+, OPIN-, VCTL

(9) Method of calculating Gain

i) Loading



ii) Focus, Tracking, sled, spindle

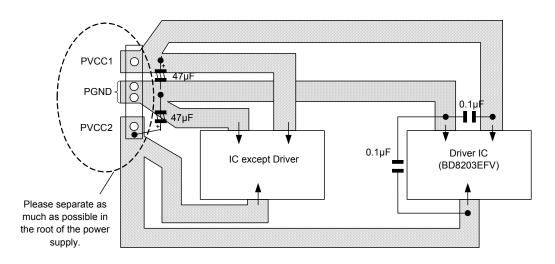


Noise measures

The cause of PWM driver's noise is the following. A.Noise from Vcc and GNT line B.Radiation noise

~Measures of A~

- ①Because a large current by the PWM output flows, driver's power supply (PVCC) and GNT line (PGNT) lower the wiring impedance. Please separate with the power supply line of other devices in the root without common impedance, and connect it in another line.
- ②Please stabilize it strongly for power supply pin (PVCC1,PVCC2,PREVCC) of drivers and GNT pin (PVCC) by the electrolytic capacitor that ESR is low. Please apply the ceramic capacitor with a high frequency characteristic to the root of IC.



③There is a method of inserting LC filter in the power supply line or GNT line, when not improved by ①②.

(Example

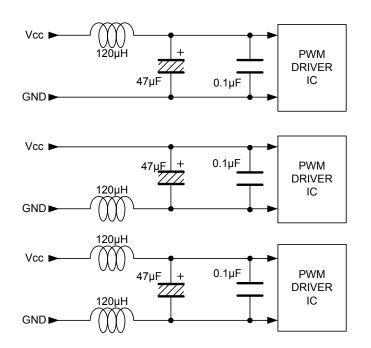


Figure LC filter chart

(4)In addition, there is a method of adding the capacitor of about 2200pF (arbitrary capacity) between each output and GNT in the PWM driver (Sled). In this case, the wiring for GNT must not have common impedances with other signals.

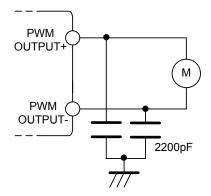
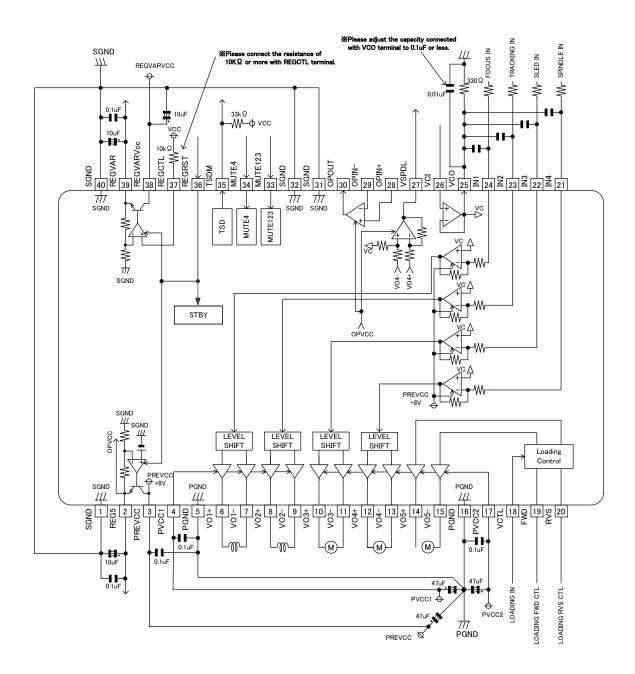


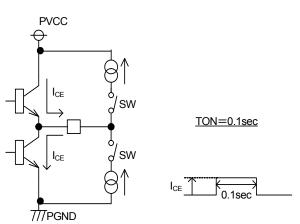
Figure Snaba circuit

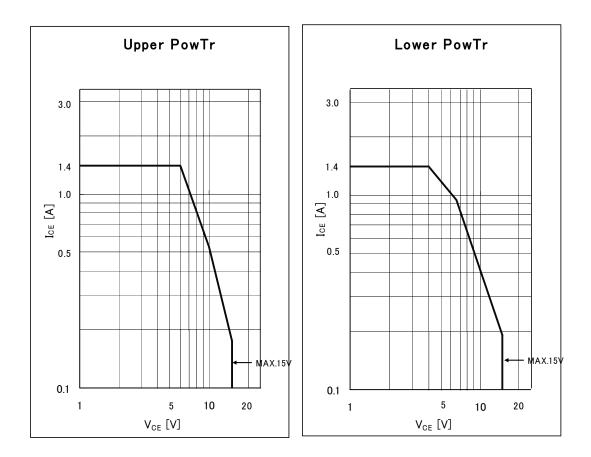
Application circuit chart



ASO

6~15pin ASO Data (TON=0.1sec) PREVCC=PVCC1=PVCC2=15V Ta=25℃





Notes for use

1.Absolute maximum ratings

We are careful enough for quality control about this IC. So, there is no problem under normal operation, excluding that it exceeds the absolute maximum ratings. However, this IC might be destroyed when the absolute maximum ratings, such as impressed voltages or the operating temperature range, is exceeded, and whether the destruction is short circuit mode or open circuit mode cannot be specified. Please take into consideration the physical countermeasures for safety, such as fusing, if a particular mode that exceeds the absolute maximum rating is assumed.

2.Reverse polarity connection

Connecting the power line to the IC in reverse polarity (from that recommended) will damage the part. Please utilize the direction protection device as a diode in the supply line and motor coil line.

3. Power supply line

Due to return of regenerative current by reverse electromotive force of external coil, using electrolytic and ceramic suppress filter capacitors (0.1μ F) close to the IC power input terminals (Vcc and GNT) are recommended. Please note the electrolytic capacitor value decreases at lower temperatures and examine to dispense physical measures for safety.

4.GNT line

Please keep the SGNT, PGNT, PGNT2 line the lowest potential always, and check the GNT voltage when transient voltages are connected to the IC.

5.Thermal design

Do not exceed the power dissipation (Pd) of the package specification rating under actual operation, and please design enough temperature margins. This product has exposed the frame to the back side of the package, but please note that it is assumed to use heat radiation efficiency by the heat radiation for this part. Please take the heat radiation pattern on not only the surface of the substrate but also the back of the substrate widely.

6.Short circuit mode between terminals and wrong mounting

Do not mount the IC in the wrong direction and displacement, and be careful about the reverse-connection of the power connector. Moreover, this IC might be destroyed when the dust short the terminals between them or GNT.

(The outputs of CH1(pin2,3) have NO protection circuit. So please especially be careful about them.)

7.Radiation

Strong electromagnetic radiation can cause operation failures.

8.ASO (Area of Safety Operation)

Do not exceed the maximum ASO and the absolute maximum ratings of the output driver.

9.TSD (Thermal Shut-Down)

The TSD is activated when the junction temperature (Tj) exceeds Tjmax, and the output terminal is switched to OPEN.

The guarantee and protection of set are not purpose. Therefore, please do not use this IC after TSD circuit operates, nor use it for assumption that operates the TSD circuit.

10.Capacitor between output and GNT

If a large capacitor is connected between the output and GNT, this IC might be destroyed when Vcc becomes 0V or GNT, because the electric charge accumulated in the capacitor flows to the output. Please set said capacitor to smaller than 0.1µF.

11.About the capacitor between the outputs

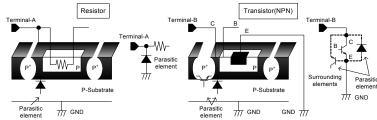
The output current increases compared with the change between the outputs when the capacitor is connected between the driver outputs. Therefore, please do measures such as putting bypass capacitor (0.1uF) in a nearest pin of power supply (PVCC) and GNT(PGNT) of this IC as the route of the output current. Please decide the capacity value after confirming there is no problem in various characteristics enough, it is possible to pull out capacity at the low temperature happening to the electrolytic capacitor more than the capacity value of the capacitor between the outputs.

12. Inspection by the set circuit board

The stress might hang to IC by connecting the capacitor to the terminal with low impedance. Then, please discharge electricity in each and all process. Moreover, when attaching or detaching from jig in the inspection process, please turn off the power before mounting the IC, and turn on after mounting the IC, and vice versa. In addition, please take into consideration the countermeasures for electrostatic damage, such as giving the earth in assembly process, transportation or preservation.

13. Input terminal

This IC is a monolithic IC, and has P⁺ isolation and P substrate for the element separation. Therefore, a parasitic PN junction is firmed in this P-layer and N-layer of each element. For instance, the resistor or the transistor is connected to the terminal as shown in the figure below. When the GNT voltage potential is greater than the voltage potential at Terminals A on the resistor, at Terminal B on the transistor, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the interference of circuit operation, then the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GNT (P substrate). Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed. Moreover, please impress each input terminal lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage is impressing.

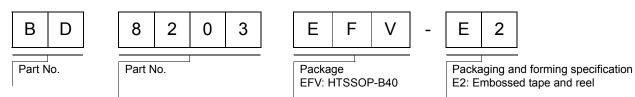


Example of IC of simple structure

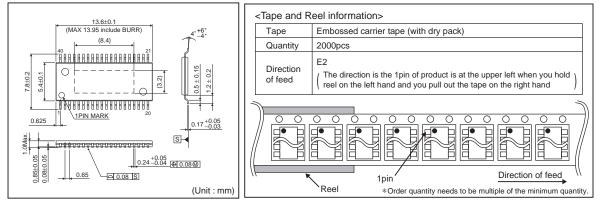
14. Earth wiring pattern

If small signal GNT and large current GNT exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GNT, each ground terminal of IC must be connected at the one point on the set circuit board. As for GNT of external parts, it is similar to the above-mentioned.

Ordering part number



HTSSOP-B40



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