1 nV/√Hz Low Noise 210°C Instrumentation Amplifier

Known Good Die

AD8229-KGD

FEATURES

- Designed for 210°C operation
- Low noise
  - 1 nV/√Hz input noise
  - 45 nV/√Hz output noise
- High CMRR
  - 126 dB CMRR (minimum), G = 100
  - 80 dB CMRR (minimum) to 5 kHz, G = 1
- Excellent ac specifications
  - 15 MHz bandwidth (G = 1)
  - 1.2 MHz bandwidth (G = 100)
  - 22 V/µs slew rate
  - THD: 130 dB (1 kHz, G = 1)
- Versatile
  - ±4 V to ±17 V dual supply
  - Gain set with single resistor (G = 1 to 1000)
  - Temperature range: −40°C to +210°C
- Known good die (KGD): these die are fully guaranteed to data sheet specifications

APPLICATIONS

- Down-hole instrumentation
- Harsh environment data acquisition
- Exhaust gas measurements
- Vibration analysis

FUNCTIONAL BLOCK DIAGRAM

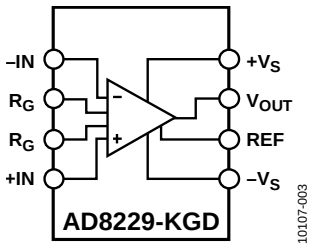

Figure 1.

GENERAL DESCRIPTION

The AD8229-KGD is an ultralow noise instrumentation amplifier designed for measuring small signals in the presence of large common-mode voltages and high temperatures.

The AD8229-KGD has been designed for high temperature operation. The process is dielectrically isolated to avoid leakage currents at high temperatures. The design architecture was chosen to compensate for the low V_{BE} voltages at high temperatures.

The AD8229-KGD excels at distinguishing tiny signals. It delivers industry leading 1 nV/√Hz input noise performance. The high CMRR of the AD8229-KGD prevents unwanted signals from corrupting the acquisition. The CMRR increases as the gain increases, offering high rejection when it is most needed.

The AD8229-KGD is one of the fastest instrumentation amplifiers available. Its current feedback architecture provides bandwidth that is quite high, even at high gains, for example, 1.2 MHz at G = 100. With the high bandwidth comes excellent distortion performance, allowing use in demanding applications such as vibration analysis.

Gain is set from 1 to 1000 with a single resistor. A reference pin allows the user to offset the output voltage. This feature is useful when interfacing with analog-to-digital converters.

Additional application and technical information can be found in the AD8229 standard product data sheet.

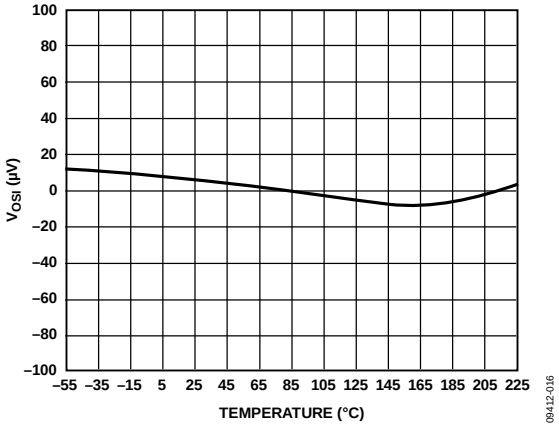

Figure 2. Typical Input Offset vs. Temperature (G = 100)

Rev. 0

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REVISION HISTORY

8/11—Revision 0: Initial Version

SPECIFICATIONS

$+V_S$ = 15 V, $-V_S$ = −15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = ±10 V				
G = 1		86			dB
Temperature Drift	T_A = −40°C to +210°C			300	nV/V/°C
G = 10		106			dB
Temperature Drift	T_A = −40°C to +210°C			30	nV/V/°C
G = 100		126			dB
Temperature Drift	T_A = −40°C to +210°C			3	nV/V/°C
G = 1000	T_A = −40°C to +210°C	134			dB
CMRR at 5 kHz	V_{CM} = ±10 V				
G = 1		80			dB
G = 10		90			dB
G = 100		90			dB
G = 1000		90			dB
VOLTAGE NOISE	V_{IN}+, V_{IN}− = 0 V				
Spectral Density[1]: 1 kHz					
Input Voltage Noise, e_{ni}			1	1.1	nV/√Hz
Output Voltage Noise, e_{no}			45	50	nV/√Hz
Peak to Peak: 0.1 Hz to 10 Hz					
G = 1			2		µV p-p
G = 1000			100		nV p-p
CURRENT NOISE					
Spectral Density: 1 kHz			1.5		pA/√Hz
Peak to Peak: 0.1 Hz to 10 Hz			100		pA p-p
VOLTAGE OFFSET	$V_{OS} = V_{OSI} + V_{OSO}/G$				
Input Offset, V_{OSI}				100	µV
Average TC	−40°C to +210°C		0.1	1	µV/°C
Output Offset, V_{OSO}				1000	µV
Average TC	−40°C to +210°C		3	10	µV/°C
Offset RTI vs. Supply (PSR)	V_S = ±5 V to ±15 V				
G = 1	−40°C to +210°C	86			dB
G = 10	−40°C to +210°C	106			dB
G = 100	−40°C to +210°C	126			dB
G = 1000	−40°C to +210°C	130			dB
INPUT CURRENT					
Input Bias Current				70	nA
High Temperature	T_A = 210°C			200	nA
Input Offset Current				35	nA
High Temperature	T_A = 210°C			50	nA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC RESPONSE					
Small Signal Bandwidth – 3 dB					
G = 1			15		MHz
G = 10			4		MHz
G = 100			1.2		MHz
G = 1000			0.15		MHz
Settling Time 0.01%	10 V step				
G = 1			0.75		µs
G = 10			0.65		µs
G = 100			0.85		µs
G = 1000			5		µs
Settling Time 0.001%	10 V step				
G = 1			0.9		µs
G = 10			0.9		µs
G = 100			1.2		µs
G = 1000			7		µs
Slew Rate					
G = 1 to 100			22		V/µs
GAIN[2]	$G = 1 + (6\ k\Omega/R_G)$				
Gain Range		1		1000	V/V
Gain Error	$V_{OUT} = \pm 10$ V				
G = 1			0.01	0.03	%
G = 10			0.05	0.3	%
G = 100			0.05	0.3	%
G = 1000			0.1	0.3	%
Gain Nonlinearity	$V_{OUT} = -10$ V to +10 V				
G = 1 to 1000	$R_L = 10\ k\Omega$		2		ppm
Gain vs. Temperature					
G = 1	−40°C to +210°C		2	5	ppm/°C
G > 10	−40°C to +210°C			−100	ppm/°C
INPUT					
Impedance (Pin to Ground)[3]			1.5||3		GΩ||pF
Input Operating Voltage Range[4]	$V_S = \pm 5$ V to ±18 V for dual supplies	$-V_S + 2.8$		$+V_S - 2.5$	V
Over Temperature	−40°C to +210°C	$-V_S + 2.8$		$+V_S - 2.5$	V
OUTPUT					
Output Swing	$R_L = 2\ k\Omega$	$-V_S + 1.9$		+Vs − 1.5	V
High Temperature	$T_A = 210°C$	$-V_S + 1.1$		+Vs − 1.1	V
Output Swing	$R_L = 10\ k\Omega$	$-V_S + 1.8$		+Vs − 1.2	V
High Temperature	$T_A = 210°C$	$-V_S + 1.1$		+Vs − 1.1	V
Short-Circuit Current			35		mA
REFERENCE INPUT					
R_{IN}			10		kΩ
I_{IN}	$V_{IN}+, V_{IN}- = 0$ V		70		µA
Voltage Range		$-V_S$		$+V_S$	V
Reference Gain to Output			1		V/V
Reference Gain Error			0.01		%

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		±4		±17	V
Quiescent Current			6.7	7	mA
High Temperature	T_A = 210°C			12	mA
TEMPERATURE RANGE					
For Specified Performance[5]		−40		+210	°C

[1] Total Voltage Noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2) + e_{RG}^2}$.
[2] These specifications do not include the tolerance of the external gain setting resistor, R_G. For G>1, R_G errors should be added to the specifications given in this table.
[3] Differential and common-mode input impedance can be calculated from the pin impedance: $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.
[4] Input voltage range of the AD8229-KGD input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage.
[5] Performance at 210°C is guaranteed for 1000 hours assuming that the maximum junction temperature listed in the Absolute Maximum Ratings, Table 2 is not exceeded.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±17 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at –IN, +IN[1]	$\pm V_S$
Differential Input Voltage[1]	
Gain ≤ 4	$\pm V_S$
4 > Gain > 50	±50 V/gain
Gain ≥ 50	±1 V
Maximum Voltage at REF	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +210°C
Maximum Junction Temperature	245°C

[1] For voltages beyond these limits, use input protection resistors.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PAD CONFIGURATION AND FUNCTION DESCRIPTIONS

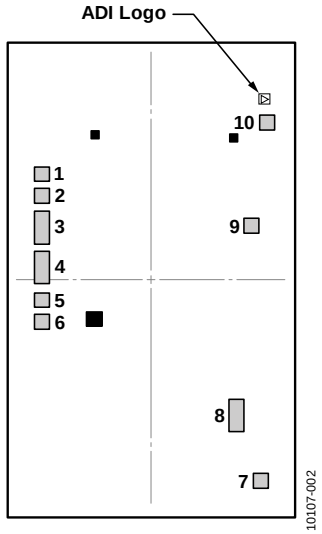

Figure 3. Pad Configuration

Table 3. Pad Function Descriptions[1]

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
1	−661	+665	−IN	Single	Negative Input Pad.
2	−661	+525	R_G	Single	Gain Setting Pad.
3	−661	+331	R_G	Double	Gain Setting Pad.
4	−661	+83	R_G	Double	Gain Setting Pad.
5	−661	−111	R_G	Single	Gain Setting Pad.
6	−661	−251	+IN	Single	Positive Input Pad.
7	+682	−1231	$-V_S$	Single	Negative Power Supply Pad.
8	+538	−839	REF	Double	Reference Voltage Pad.
9	+626	+337	V_{OUT}	Single	Output Pad.
10	+717	+979	$+V_S$	Single	Positive Power Supply Pad.

[1] To minimize gain errors introduced by the bond wires, use Kelvin connections between the chip and the gain resistor, RG, by connecting Pad 2 and Pad 3 in parallel to one end of RG, and connecting Pad 4 and Pad 5 in parallel to the other end of RG. For unity-gain applications where RG is not required, Pad 2 and Pad 3 must be bonded together as do Pad 4 and Pad 5.

OUTLINE DIMENSIONS

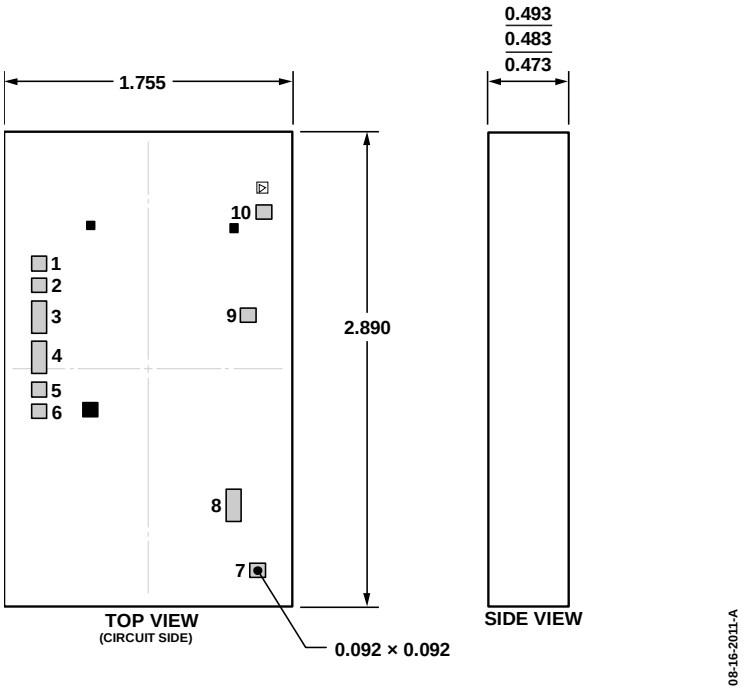

Figure 4. AD8229-KGD Die
1.755 mm × 2.890 mm Die Size
(Dimensions shown in millimeters)

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 4. Die Specifications

Parameter	Value	Unit[1]
Chip Size	1665 × 2800	µm
Scribe Line Width	90 × 90	µm
Die Size	1.755 × 2.890	mm (maximum)
Thickness	483 ± 10	µm
Bond Pad	92 × 92	µm (minimum)
Bond Pad Composition	0.5 AlCu	%
Backside	Bare	N/A
Passivation	Polymide	N/A

[1] N/A means not applicable.

Table 5. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	No special requirements
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Any

ORDERING GUIDE

Model	Temperature Range	Package Option
AD8229-KGD-CHIPS	−40°C to +210°C	Die Only