# Components
# for Entertainment Electronics

## Satellite Sound IF

## TDA6170X

## with Wegener Expander

Data Sheet 07.99

**Edition 07.99**
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**TDA6170X**
**Revision History:Current Version: 07.99**

Previous Version:

| old Page | new Page | Subjects (major changes since last revision) |
|---|---|---|
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**Data Classification**

**Maximum Ratings**
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

**Characteristics**
The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A$ = 25 °C and the given supply voltage.

**Operating Range**
In the operating range the functions given in the circuit description are fulfilled.
For detailed technical information about **"Processing Guidelines"** and
**"Quality Assurance"** for ICs, see our **"Product Overview"**.

# Satellite Sound IF with Wegener Expander

**TDA6170X**

**Data Sheet** **BIPOLAR**

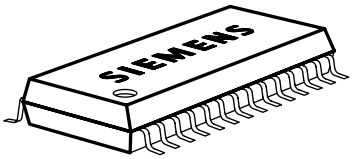
## 1 Features

- Fast $I^2C$-bus controlled (max. 400 kHz)
- PLL controlled sound IF tuning with 10 kHz stepwidth
- Second order high-pass mixer input
- IF MUX for 10.7 MHz broad / small IF filters
- Two identical high sensitive alignment free FM demodulators
- Original Wegener PANDA $1^{TM}$ expander
- Volume control for individual settings
- 50 µs / 75 µs / J17 de-emphasis for main sound reception
- Fully ESD protection

WEGENER COMMUNICATIONS®

PANDA®

NOISE REDUCTION




**P-DSO-28**

**Package**

## 2 Ordering Information

| Type | Package | Ordering Code |
|---|---|---|
| TDA6170X | P-DSO-28-1 | Q67001-A5214 |

## 3 General Description

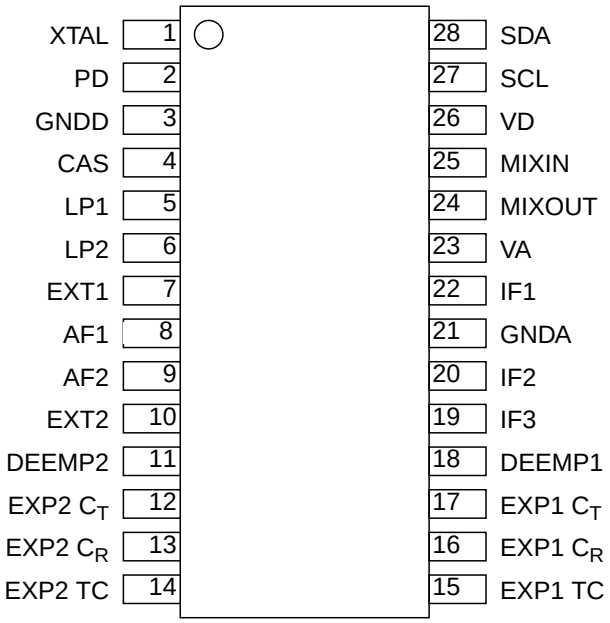
Multistandard satellite sound IF device consisting of a mixer and a voltage controlled oscillator (VCO) as a frequency converter that can be continuously tuned in 10 kHz increments with crystal accuracy by means of a PLL, two FM limiter amplifiers with PLL FM demodulators followed by two Wegener PANDA1$^{TM}$ expanders. The AF signal passes through two switches. Each switch can select the AF sources and the mono / stereo mode the de-emphasis networks together with the two following volume control stages with audio buffers. In front of one FM section an IF multiplexer is used to select the IF bandwidth.
The switching functions and settings of the PLL are controlled by an $I^2C$-bus.

### 3.1 Application

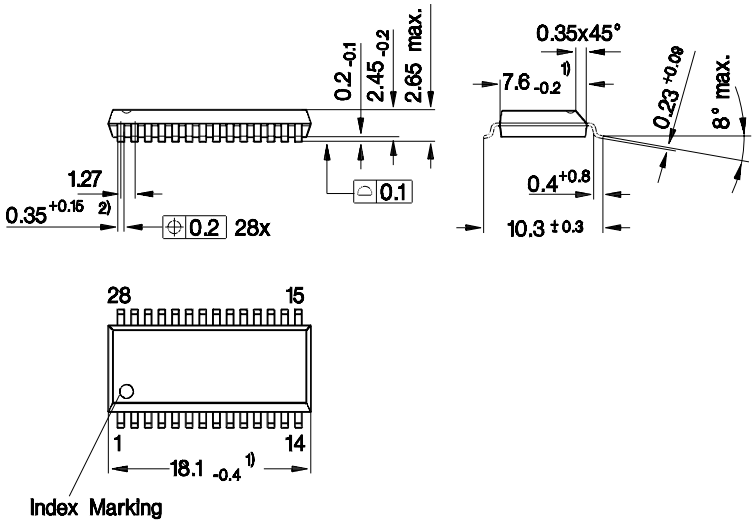
- For use in satellite receivers

# 4 Pinconfiguration

P-DSO 28-1




## 4.1 Package outline P-DSO-28-1

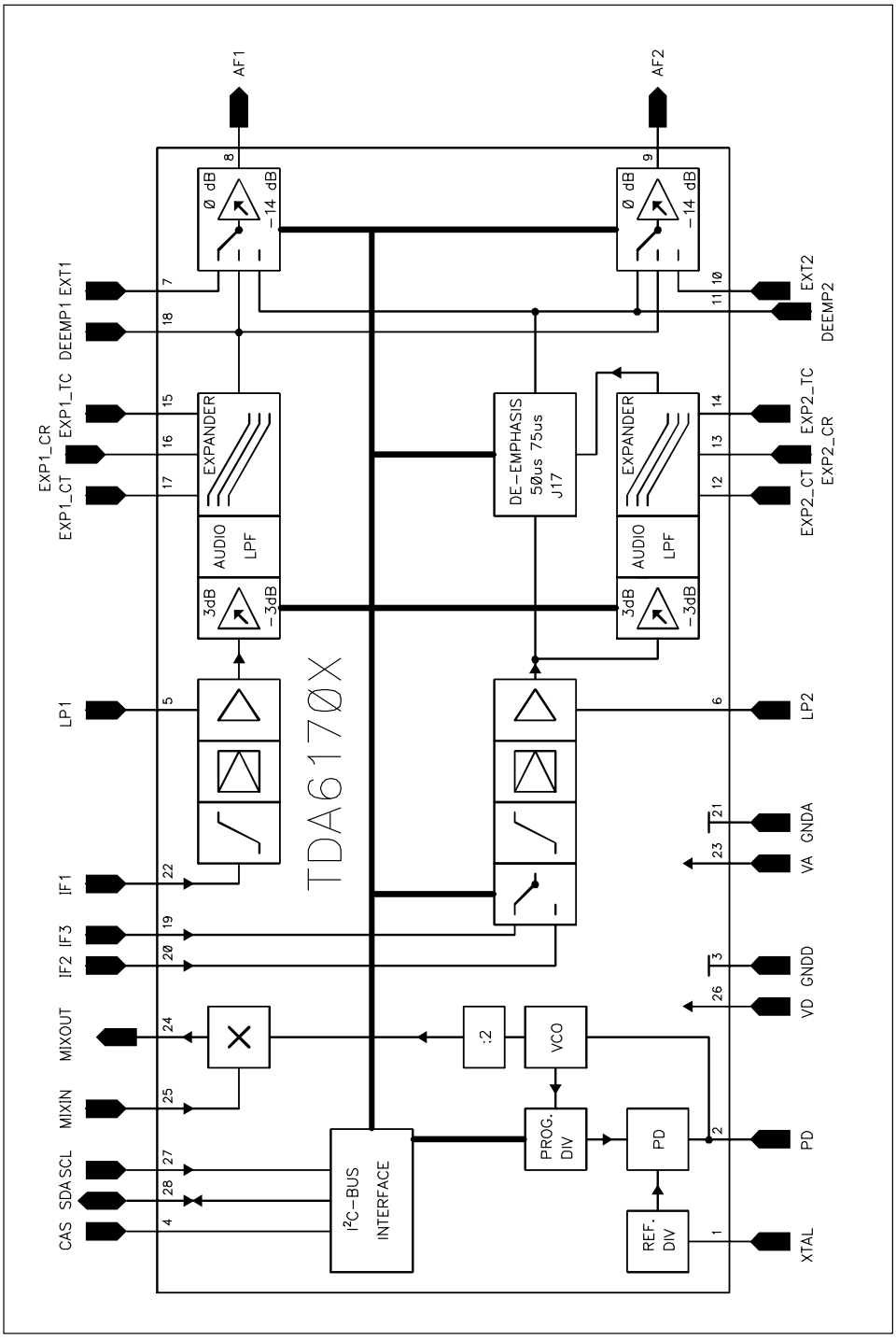



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

## 5 Pin Definitions and Functions

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | XTAL | crystal input for 4 MHz oscillator |
| 2 | PD | synthesizer loop-filter |
| 3 | GNDD | $I^2C$-bus and synthesizer ground |
| 4 | CAS | $I^2C$-bus address selection |
| 5 | LP1 | FM-PLL lowpass capacitor (channel 1) |
| 6 | LP2 | FM-PLL lowpass capacitor (channel 2) |
| 7 | EXT1 | external audio input (channel 1) |
| 8 | AF1 | audio output (channel 1) |
| 9 | AF2 | audio output (channel 2) |
| 10 | EXT2 | external audio input (channel 2) |
| 11 | DEEMP2 | de-emphasis capacitor (channel 2) |
| 12 | EXP2 $C_T$ | expander tracking capacitor (channel 2) |
| 13 | EXP2 $C_R$ | expander release capacitor (channel 2) |
| 14 | EXP2 TC | expander time constant (channel 2) |
| 15 | EXP1 TC | expander time constant (channel 1) |
| 16 | EXP1 $C_R$ | expander release capacitor (channel 1) |
| 17 | EXP1 $C_T$ | expander tracking capacitor (channel 1) |
| 18 | DEEMP1 | de-emphasis capacitor (channel 1) |
| 19 | IF3 | intercarrier input 3 |
| 20 | IF2 | intercarrier input 2 |
| 21 | GNDA | analog ground |
| 22 | IF1 | intercarrier input 1 |
| 23 | VA | analog supply voltage (+8V) |
| 24 | MIXOUT | intercarrier mixer output |
| 25 | MIXIN | mixer input |
| 26 | VD | $I^2C$-bus and synthesizer supply voltage (+5V) |
| 27 | SCL | $I^2C$-bus serial clock input |
| 28 | SDA | $I^2C$-bus serial data input/output |

# 6 Block Diagram



# 7 Circuit Description

## 7.1 General

The sound intermediate frequencies contained in the baseband of a demodulated FM satellite signal can lie between 5 and 9.9 MHz. This band of frequencies is applied rough filtered to the high-pass input of the converter mixer. The purpose of this mixer is to convert the different sound IF's in the baseband to fixed output frequencies (e.g. 10.7 / 10.72 MHz). These frequencies are then fed by external filters to the three sound IF inputs.
The VCO of the mixer can be continuously tuned between 29 and 40 MHz in 20 kHz increments with crystal accuracy by means of a PLL circuit.
The settings of the programmable divider and switching of the IF MUX and de-emphasis networks and volume control are done by the $I^2C$-bus.
Pin 5 (CAS) offers two switchable chip addresses to enable parallel operation of two devices.
All pins are guarded against electrostatic discharge. SCL and SDA include special protective structures to permit continued bus operation when the device is switched off.

## 7.2 PLL Description

The VCO signal is applied to the PLL input. It passes through a programmable divider (N=1024 to 2047) and then compared with a reference frequency ($f_{REF}$ = 20 kHz in a digital frequency / phase detector. This frequency is derived from a 4 MHz crystal oscillator whose signal is divided by 200.
The phase detector has a charge pump push-pull current output. If the negative edge of the divided VCO signal appears before the negative edge of the reference signal, the current source I+ will pulse for the duration of the phase difference. In the reverse case it is the current sink I-. If both signals are in phase, the output has a high impedance and the PLL is locked. The current pulses are filtered by means of an integrator.
The pump current can be switched between two values (1 and 5) by software with a control bit 5I. This permits a change in the control response during and after lock-in state.

## 7.3 Fast $I^2C$-Bus Interface

Information is exchanged between the processor and the sound IF device on an fast asynchronous bidirectional data bus. The timing for this comes from the processor (input SCL), while pin SDA functions as an I/O depending on the direction of the data (open collector; external pull-up resistor). The bus will work with clock frequencies up to 400 kHz.
The data from the processor goes to an $I^2C$-bus controller and are put into registers (latches 0 to x) according to their function. When the bus is not busy, both lines are in the marking state (SDA, SCL are high). Each telegram begins with the start condition: SDA goes low while SCL remains high. All further exchanges of information occur when SCL is low and are read by the controller with the positive clock edge. If SDA goes high while the clock is high, the $I^2C$-bus interface recognizes this as a stop condition and thus the end of the telegram.
For what follows, refer to the table of logic assignments below.
All telegrams are transferred byte for byte, followed by a ninth clock pulse during which the controller pulls the SDA line to low (i.e. acknowledge condition). The first byte consists of seven address bits with which the processor selects the PLL from among several other peripheral devices (chip select). The eighth bit is always low. The first bit of the first or third data byte in the data part of the telegram determines whether a divider ratio or control information for the IF or audio part will follow. In every case the first byte must be followed by a byte of the same data type (or stop condition). When the supply voltage is applied, a power-on reset circuit prevents the PLL from pulling the SDA line to low and thus blocking the bus.

### 7.3.1 Logic Allocation

| Byte | Data | | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| Address Byte | 0 | 1 | 0 | 0 | 0 | 0 | MA | R/W | A | |
| Progr. Divider Byte 1 | 0 | 0 | N11 | N10 | N9 | N8 | N7 | N6 | A | |
| Progr. Divider Byte 2 | 0 | 0 | N5 | N4 | N3 | N2 | N1 | N0 | A | |
| Control Byte 1 | 1 | 5I | Z2 | Z1 | Z0 | X | X | X | A | |
| Control Byte 2 | 1 | VL2 | VL1 | VL0 | VR2 | VR1 | VR0 | X | A | |
| Control Byte 3 | 1 | PVL2 | PVL1 | PVL0 | PVR2 | PVR1 | PVR0 | X | A | |
| Address Byte 1[1] | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | A | =H44 |
| Address Byte 2[2] | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | A | =H46 |

1. Chip address (CAS) Pin 5 grounded
2. Chip address (CAS) Pin 5 open

### 7.3.2 IF-Muting

| Control Bits | | | IF-Source | | | Function |
|---|---|---|---|---|---|---|
| Z2 | Z1 | Z0 | IF1 | IF2 | IF3 | |
| 0 | 0 | 0 | on | on | off | expanders are working, audio = stereo |
| 0 | 0 | 1 | off | on | off | expanders are working, audio = mono |
| 0 | 1 | 0 | on | off | off | expanders are working, audio = mono |
| 0 | 1 | 1 | off | off | on | de-emphasis = 50µ; audio = mono |
| 1 | 0 | 0 | off | off | on | de-emphasis = 75µ; audio = mono |
| 1 | 0 | 1 | off | off | on | de-emphasis = J17; audio = mono |
| 1 | 1 | 0 | off | off | off | External audio |
| 1 | 1 | 1 | off | off | off | Mute |

## 7.4 Converter Mixer

In the converter mixer the sound subcarriers (frequency band approx. 5 to 9.9 MHz) contained in the base-band of the received composite satellite signal are converted to an output frequency of 10.52 MHz and 10.7 MHz for example. The converter consists of a high-pass input filter followed by a double balanced mixer and a low impedance output.
The signal of the on chip voltage controlled oscillator (VCO) is applied to the PLL input.

## 7.5 IF Limiter with Demodulator

The two limiter amplifiers are implemented as balanced five stage, capacitively coupled differential amplifiers. The three inputs are designed as high-pass inputs. The load resistors for the IF filters are connected to ground.
The output signals of the limiter amplifiers are fed directly to the internal PLL FM demodulators.
The demodulated AF signals are fed to the input of a pre volume control part in front of the expander the de-emphasis networks and audio switches.

## 7.6 Expander Description

The demodulated and level controlled audio signals are fed via low-pass filters to the inputs of two identical expander circuits. The IF3 audio signal is also applied in parallel via different de-emphasis networks to the input of the audio switch for broadband mono reception. The expander circuits have the reverse characteristics of the audio compressor of the TV station. A 3 bit pre volume control (control byte 3: PVL2...PVL0 and PVR2...PVR0) for each audio channel enables a correct adjustment of the expander characteristics and allows the possibility to align to the right level for both broadband and smallband sound IF reception.

## 7.7 AF Switch and Volume Control

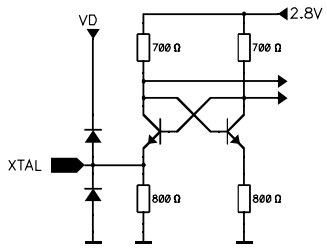
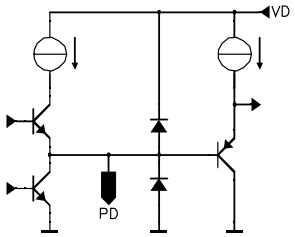
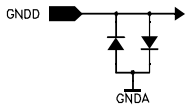
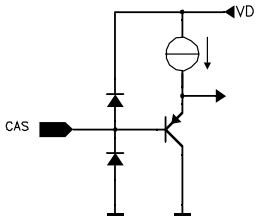
The input signals of the AF switch can be derived from the external audio input pair. However, these signals can also be derived from either the different de-emphasis networks or from both expanders. The selection of the output signals from IF1, IF2 or IF3 is done by using the $I^2C$-bus interface. The switches are followed by a volume control section with buffered outputs Ch1 and Ch2.

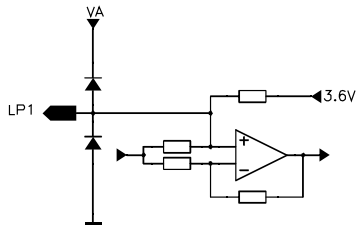
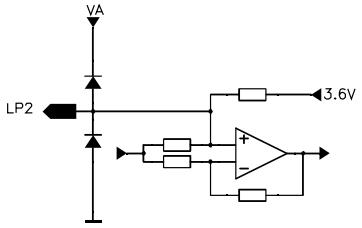
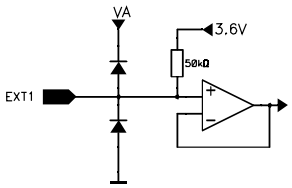
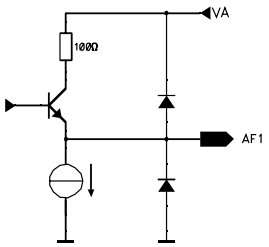
In case of small-band reception the demodulated signals of IF1 and IF2 are processed in both expanders and fed to the switches. So it is possible to select one of each or both in the audio switches for both AF outputs Ch1 and Ch2.

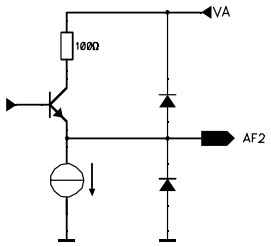
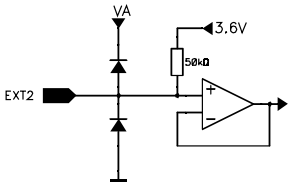
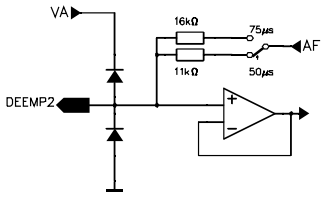
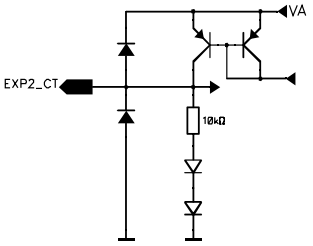
In the case of broad-band audio transmission with 50µs, 75µs or J17 pre-emphasis the IF3 input is active and with the audio switch the demodulated audio signals are selected after the three de-emphasis networks and fed to both AF outputs in mono mode.

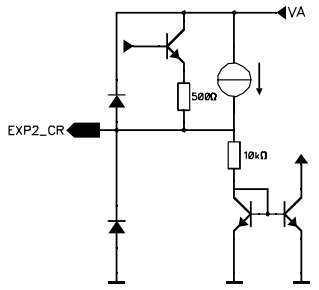
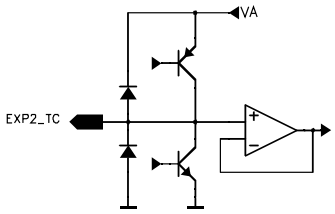
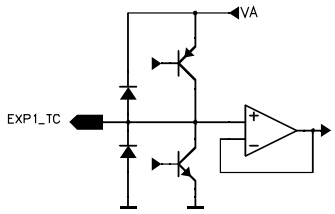
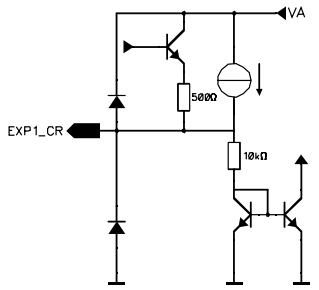
The 3 bit volume control (control byte 2: VL2...VL0 and VR2...VR0) in front of each AF output enables the same audio level for different FM deviations of several satellite transponders.

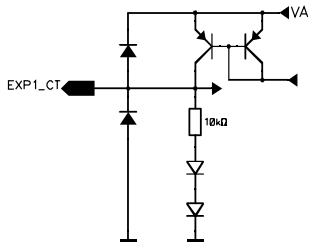
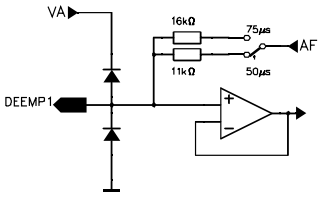
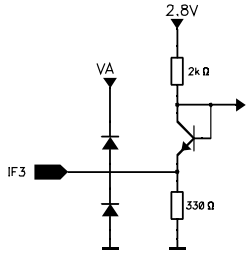
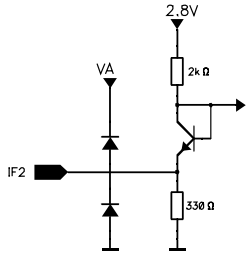
# 8 Pinning

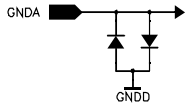
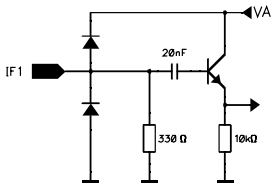
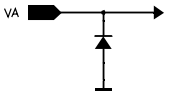
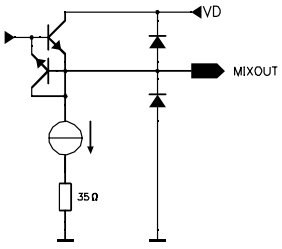
| Pin No. | Symbol | Equivalent Circuit |
|---|---|---|
| 1 | XTAL |  |
| 2 | PD |  |
| 3 | GNDD |  |
| 4 | CAS |  |

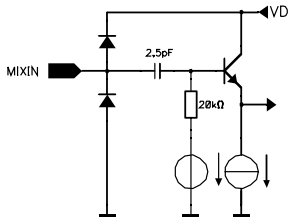
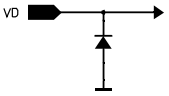
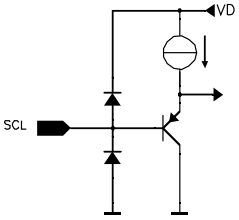
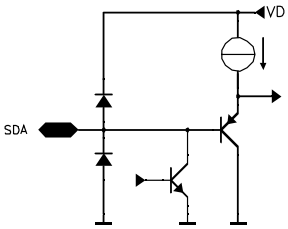
| Pin No. | Symbol | Equivalent Circuit |
|---|---|---|
| 5 | LP1 |  |
| 6 | LP2 |  |
| 7 | EXT1 |  |
| 8 | AF1 |  |

| Pin No. | Symbol | Equivalent Circuit |
|---|---|---|
| 9 | AF2 |  |
| 10 | EXT2 |  |
| 11 | DEEMP2 |  |
| 12 | EXP2 $C_T$ |  |

| Pin No. | Symbol | Equivalent Circuit |
|---|---|---|
| 13 | EXP2 $C_R$ |  |
| 14 | EXP2 TC |  |
| 15 | EXP1 TC |  |
| 16 | EXP1 $C_R$ |  |

| Pin No. | Symbol | Equivalent Circuit |
|---|---|---|
| 17 | EXP1 $C_T$ |  |
| 18 | DEEMP1 |  |
| 19 | IF3 |  |
| 20 | IF2 |  |

| Pin No. | Symbol | Equivalent Circuit |
|---|---|---|
| 21 | GNDA |  |
| 22 | IF1 |  |
| 23 | VA |  |
| 24 | MIXOUT |  |

| Pin No. | Symbol | Equivalent Circuit |
|---|---|---|
| 25 | MIXIN |  |
| 26 | VD |  |
| 27 | SDA |  |
| 28 | SCL |  |

# 9 Absolute Maximum Ratings

*The maximal ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.*

Ambient Temperature under bias: $T_A$=0 to 70°C

| Parameter | Symbol | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | min | max | | |
| Supply voltage (digital) | $V_{VD}$ | 0 | 6 | V | |
| Supply voltage (analog) | $V_{VA}$ | 0 | 13.2 | V | |
| Mixer input | $V_{MIXIN}$ | -0.3 | 13.2 | V | |
| IF inputs | $V_{IF}$ | -0.3 | 1 | V | |
| Crystal oscillator | $V_{XTAL}$ | 0 | 1.5 | V | |
| SDA; SCL; CAS | V | -0.3 | 6 | V | |
| Junction temperature | $T_j$ | 0 | 150 | °C | |
| Storage temperature | $T_{stg}$ | 0 | 125 | °C | |
| Thermal resistance | $R_{th\ j\text{-}a}$ | | 75 | K/W | |
| ESD-Protection | $V_{ESD}$ | | 2 | kV | all pins |

All values are referred to ground (pin), unless stated otherwise.
All currents are designated according to the source and sink principle, i.e. if the device pin is to be regarded as a sink (the current flows into the stated pin to internal ground), it has a negative sign, and if it is a source (the current flows from Vs across the designated pin), it has a positive sign.

# 10 Operating Range

*Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.*

| Parameter | Symbol (Name) | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | min | max | | |
| Supply voltage (digital) | $V_{VD}$ | 4.5 | 5.5 | V | |
| Supply voltage (analog) | $V_{VA}$ | 7.2 | 13.2 | V | |
| Input frequency range of converter mixer | $f_{MIXIN}$ | 5 | 10 | MHz | |
| Input frequency range of sound IF amplifier | $f_{IF}$ | 10 | 12 | MHz | |
| VCO frequency | $f_{VCO}$ | 29 | 42 | MHz | |
| Ambient temperature | $T_A$ | 0 | 70 | °C | |

# 11 Electrical Characteristics

*AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.*

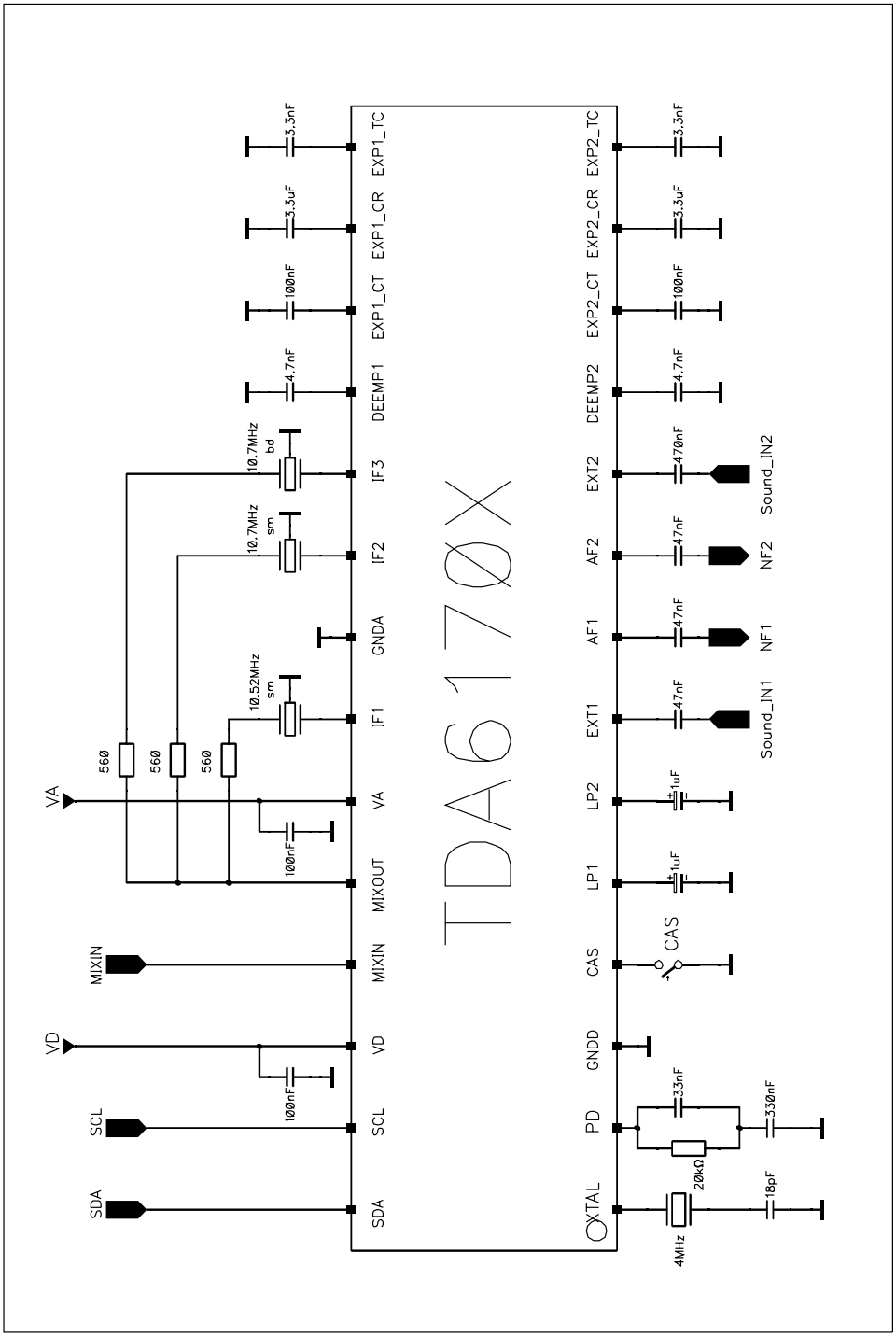
| Parameter | Symbol | Limit Values | | | Unit | Test conditions |
|---|---|---|---|---|---|---|
| | | min | typ | max | | |
| **Power Supply** | | | | | | |
| Current consumption $V_{digital}$ | $I_{VD}$ | 30 | 40 | 50 | mA | |
| Current consumption $V_{analog}$ | $I_{VA}$ | 30 | 40 | 50 | mA | |
| **Mixer** | | | | | | |
| Mixer input voltage | $V_{MIXIN(rms)}$ | | | 200 | mV | |
| Mixer output current | $I_{MIXOUT}$ | 4 | 6 | 8 | mA | |
| Input impedance | $R_{MIXIN}$ | 3.5 | | | kΩ | |
| Output frequency range | $f_{MIXOUT}$ | 10 | 10.7 | 11.5 | MHz | |
| Mixer gain | $G_{MIX}$ | 2 | 3 | 4 | dB | RL = 100 Ω |
| **Charge pump** | | | | | | |
| Phase detector charge current | $I_{PD}$ | 32 | 50 | 75 | µA | I |
| Phase detector charge current | $I_{PD}$ | 160 | 250 | 360 | µA | 5I |
| repetition time of charge pump pulses | t | | 50 | | µs | |
| **VCO** | | | | | | |
| Frequency range VCO | $\Delta f_{VCO}$ | 29 | | 43 | MHz | |
| VCO frequency | $f_{VCO}$ | | 35.5 | | MHz | $V_{PD}$ = 2.5V |
| VCO sensitivity | $S_{VCO}$ | | -16 | | MHz/V | |
| **Cyrstal oscillator (4 MHz)** | | | | | | |
| crystal oscillator frequency | $f_{xtal}$ | | 4 | | MHz | |
| resonance resistance of crystal | $R_{xtal}$ | | | 60 | W | |
| parallel capacitance of crystal | $C_{xtal}$ | | 4.5 | 10 | pF | |
| input current from external source | $I_i$ | 50 | | | µA | |
| **Sound IF** | | | | | | |
| Sound IF input resistance | $R_{IF}$ | 260 | 330 | 400 | W | |
| Input frequency range | $f_{IF}$ | 10 | | 11.5 | MHz | |
| Input sensitivity | $V_{IF(rms)}$ | | 0.3 | 1 | mV | S/N(A) > 40 dB; $f_{IF}$ = 10.7 MHz; $\Delta f$ = 27 kHz; $f_{mod}$ = 1 kHz |
| AM rejection | $a_{AM}$ | 45 | | | dB | $f_{IF}$ = 10.7 MHz; $V_{IF}$ = 5 to 100mV; $f_{mod}$ = 30% |

| Parameter | Symbol | Limit Values | | | Unit | Test conditions |
|---|---|---|---|---|---|---|
| | | min | typ | max | | |
| **FM PLL demodulators** | | | | | | |
| free-running frequency | $f_{cco}$ | | 10.6 | | MHz | |
| lock range of PLL | $\Delta f_{CCO}$ | 10 | | 11.5 | MHz | |
| **Expander** | | | | | | |
| Pre volume control range | ΔPV | 2.5<br>-3.5 | 3<br>-3 | 3.5<br>-2.5 | dB | PVL = 000<br>PVL = 111 |
| Control resolution | δV | 0.6 | 0.8 | 1 | dB | |
| Low-pass filter response | | 16 | 20 | 24 | kHz | |
| **AF Switch and Volume Control** | | | | | | |
| Max. external input voltage | $V_{EXT(rms)}$ | | | 2 | V | |
| Volume control range | ΔV | -1<br>-12 | 0<br>-14 | 1<br>-16 | dB | VL = 000<br>VL = 111 |
| Control resolution | δV | 1.6 | 2 | 2.4 | dB | |
| **Output Buffer** | | | | | | |
| Output DC level | $V_{AF}$ | | 3.6 | | V | |
| Output resistance | $R_{AF}$ | 100 | 125 | 150 | W | |
| total harmonic distortion | THD | | 0.01 | 0.2 | % | |
| signal to noise ratio | S/N (A) | 80 | | | dB | A-weighted<br>$V_{EXT}$ = 500 $mV_{rms}$<br>Control Byte = 110 |
| crosstalk between channels | $\alpha_{L/R}$;<br>$\alpha_{R/L}$ | 80 | | | dB | $V_{EXT}$ = 2 $V_{rms}$<br>f = 1 kHz<br>Control Byte = 110 |
| **Overall performance** | | | | | | |
| Input voltage | $V_{MIXIN}$ | | 0.5 | 1 | mV | S/N > 40 dB<br>Δf = 27kHz,<br>Control Byte = 000 |
| | | | 1.5 | 3 | mV | S/N > 40 dB<br>Δf = 50kHz,<br>Control Byte = 011 |
| Output voltage | $V_{AF}$ | 400 | 500 | 600 | mV | Δf = 27kHz,<br>$f_{mod}$ = 1kHz,<br>Control Byte = 000 |
| | | 400 | 500 | 600 | mV | Δf = 50kHz,<br>$f_{mod}$ = 1kHz,<br>Control Byte = 011 |

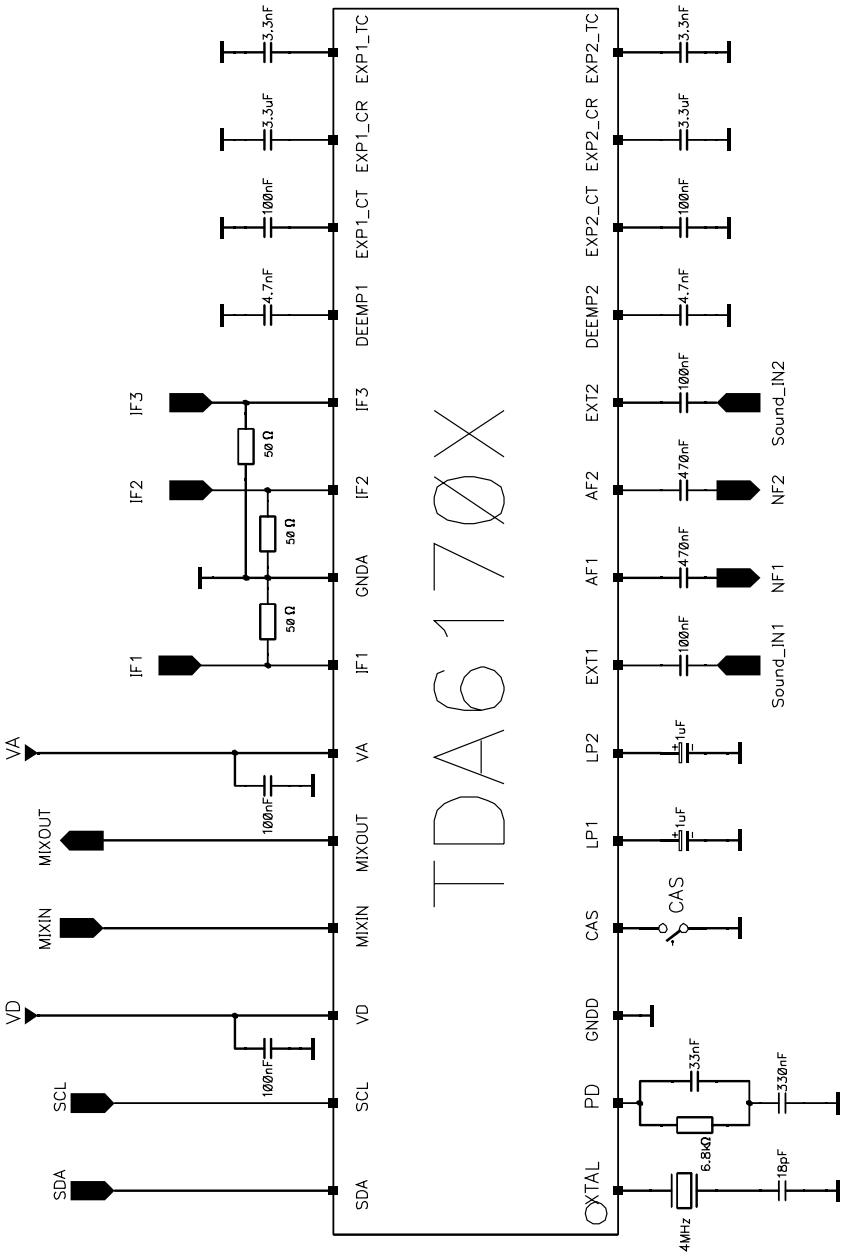
| Parameter | Symbol | Limit Values | | | Unit | Test conditions |
|---|---|---|---|---|---|---|
| | | min | typ | max | | |
| total harmonic distortion | THD | | 0.2 | 0.5 | % | $V_{MIXIN}$ > 2 mV<br>Δf = 27kHz,<br>$f_{mod}$ = 1kHz,<br>Control Byte = 000 |
| | | | 0.2 | 0.5 | % | $V_{MIXIN}$ > 2 mV<br>Δf = 50kHz,<br>$f_{mod}$ = 1kHz,<br>Control Byte = 011 |
| signal to noise ratio | S/N | 70 | 75 | | dB | A-weighted,<br>Δf = 27kHz,<br>$f_{mod}$ = 1kHz,<br>Control Byte = 000 |
| Mute attenuation | $a_{MUTE}$ | 75 | 90 | | dB | Control Byte = 111 |
| **I²C-Bus Interface** | | | | | | |
| LOW level input voltage for both SDA and SCL | $V_{IL}$ | -0.5 | | 1.5 | V | |
| HIGH level input voltage for both SDA and SCL | $V_{IH}$ | 3 | | $V_{VD}$ + 0.5 | V | |
| Hysteresis of Schmitt trigger inputs | $V_{hys}$ | 0.2 | | | V | |
| Pulse width of spikes which must be suppressed by the input filters | $t_{SP}$ | | | 50 | ns | |
| LOW level output voltage (open collector) | $V_{OL1}$<br>$V_{OL2}$ | 0<br>0 | | 0.4<br>0.6 | V | 3 mA sink current<br>6 mA sink current |
| Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance from 10 pF to 400 pF | $t_{OF}$ | 20 + 0.1$C_b$ | | 250 | ns | |
| Input current for both SDA + SCL | $I_i$ | -10 | | 10 | µA | |
| SCL clock frequency | $f_{SCL}$ | 0 | | 400 | kHz | |
| Bus free time between a STOP and START condition | $t_{BUF}$ | 1.3 | | | µs | |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD,STA}$ | 0.6 | | | µs | |
| LOW period of the SCL clock | $t_{LOW}$ | 1.3 | | | µs | |
| HIGH period of the SCL clock | $t_{HIGH}$ | 0.6 | | | µs | |
| Set-up time for repeated START condition | $t_{SU,DAT}$ | 0.6 | | | µs | |
| Data hold time:<br>for I²C-bus devices | $t_{HD,DAT}$ | 0 | | 0.9 | µs | |
| Data set-up time | $t_{SU,DAT}$ | 100 | | | ns | |
| Rise time of both SDA + SCL | $t_R$ | 20 + 0.1$C_b$ | | 300 | ns | |

| Parameter | Symbol | Limit Values | | | Unit | Test conditions |
|---|---|---|---|---|---|---|
| | | min | typ | max | | |
| Fall time of both SDA + SCL | $t_F$ | 20 + 0.1$C_b$ | | 300 | ns | |
| Set-up time for STOP condition | $t_{SU,STO}$ | 0.6 | | | µs | |
| Capacitive load for each bus line | $C_b$ | | | 400 | pF | |

## 12 Application Circuit



## 13 Test circuit



# 14 Diagrams

## 14.1 I²C-Bus Timing