Specification, Version 1.4, 2004-05-17

TDA 6190
DVB-IF Mixer

Wireless Components

Infineon technologies

Never stop thinking.

Edition 2004-05-17

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Specification

Revision History: **2004-05-17** TDA 6190

Previous Version: Specification Version 1.3, 2002-06-10

Page (in prev. version)	Page (in current version)	Subjects (major changes since last revision)
		TDA 6190X and TDA 6190S removed (all pages):
5	5	Product Info and Features adapted.
7	7	Overview and Features adapted
10	10	Pin 8 adapted
12	12	AGC description adapted
13	13	2.5.2 adapted
15	15	TDA 6190T and Ordering Code adapted
16, 17	16, 17	TDA 6190T only
19	19	“This value is guaranteed by design” replaced with “This value is not subject to production test - verified by design/ characterisation”
21	21	input levels only for TDA 6190T
23	23	Static, Dynamic Characteristics for TDA 6190T only “This value is guaranteed by design” replaced with “This value is not subject to production test - verified by design/ characterisation”
24	24	TDA 6190T only
25	25	conversion gain for Evaluation Board, single ended
28	28	Intermodulation measurement result added
29	29	TDA 6190T only
30	30	frequency response adapted

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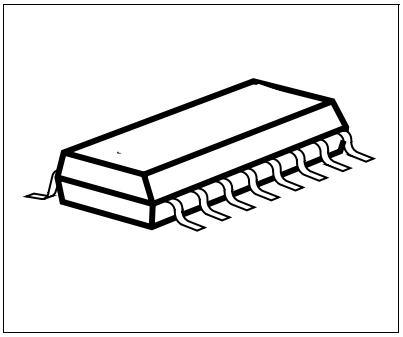
Product Info

General Description

The TDA 6190T is a bipolar integrated circuit for amplification and down conversion of modulated IF signals used for DVB on cable or for terrestrial transmission.



Features

- Input frequency range of 30 to 70 MHz
- External gain control for integrated variable gain amplifier
- Output for adjustable delayed tuner AGC
- Integrated low noise VCO circuitry with external varactor diode or crystal
- Broadband outputs for the down converted IF signal
- Internal low noise reference voltage source
- Full ESD protection

Application

- For use in TV or cable set-top receivers for Digital Video Broadcast.

Type	Ordering Code	Package
TDA 6190T	Q67036-A1073 (tape and reel)	P-DSO-16

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1 Product Description

1.1 Overview

The TDA 6190T is a bipolar integrated circuit for amplification and down conversion of modulated IF signals used for DVB on cable or for terrestrial transmission.

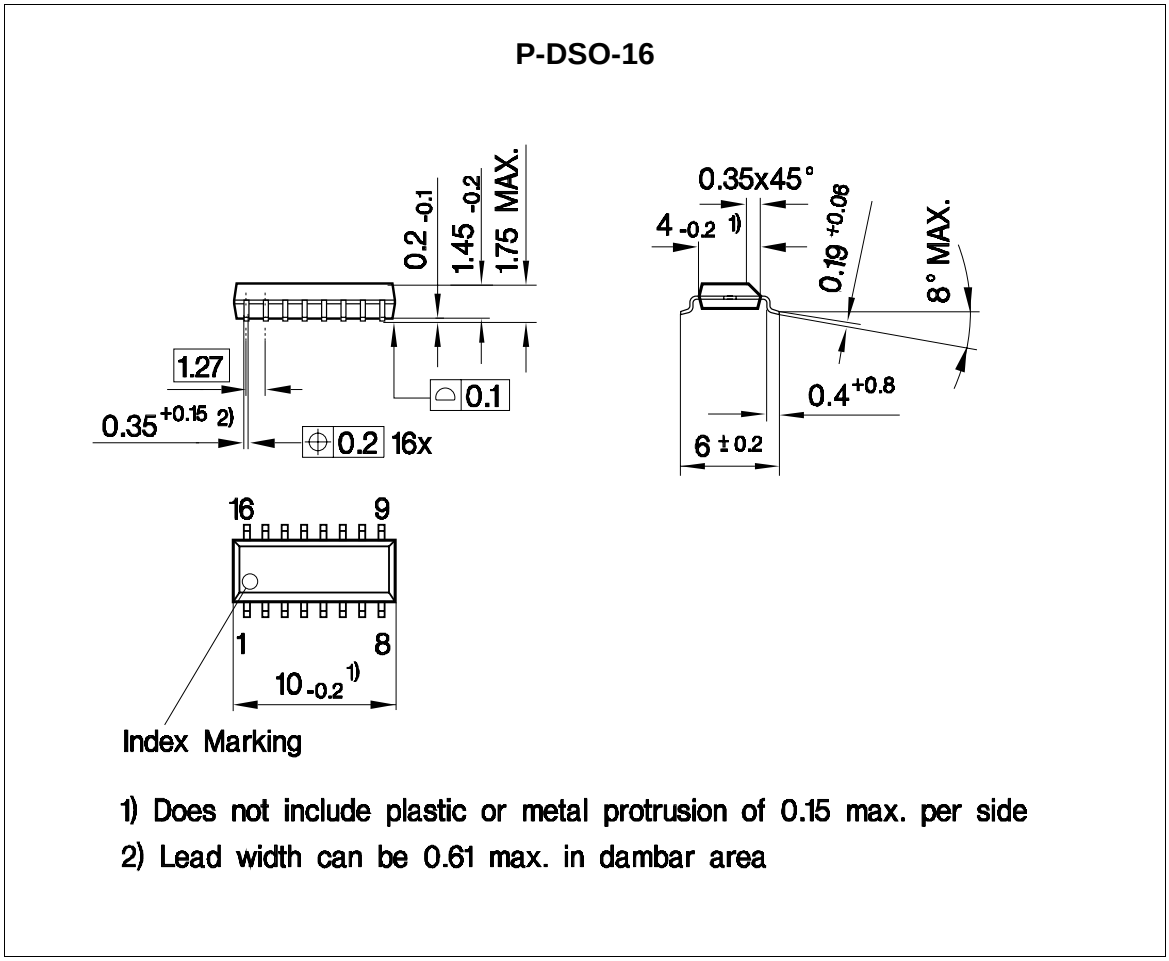
1.2 Features

- Input frequency range of 30 to 70 MHz
- External gain control for integrated variable gain amplifier
- Output for adjustable delayed tuner AGC
- Integrated low noise VCO circuitry with external varactor diode or crystal
- Broadband outputs for the down converted IF signal
- Internal low noise reference voltage source
- Full ESD protection

1.3 Application

- For use in TV or cable set-top receivers for Digital Video Broadcast.

1.4 Package Outlines



P-DSO_16.eps

Figure 1-1 Package Outline P-DSO-16

2 Functional Description

2.1 Pin Configuration

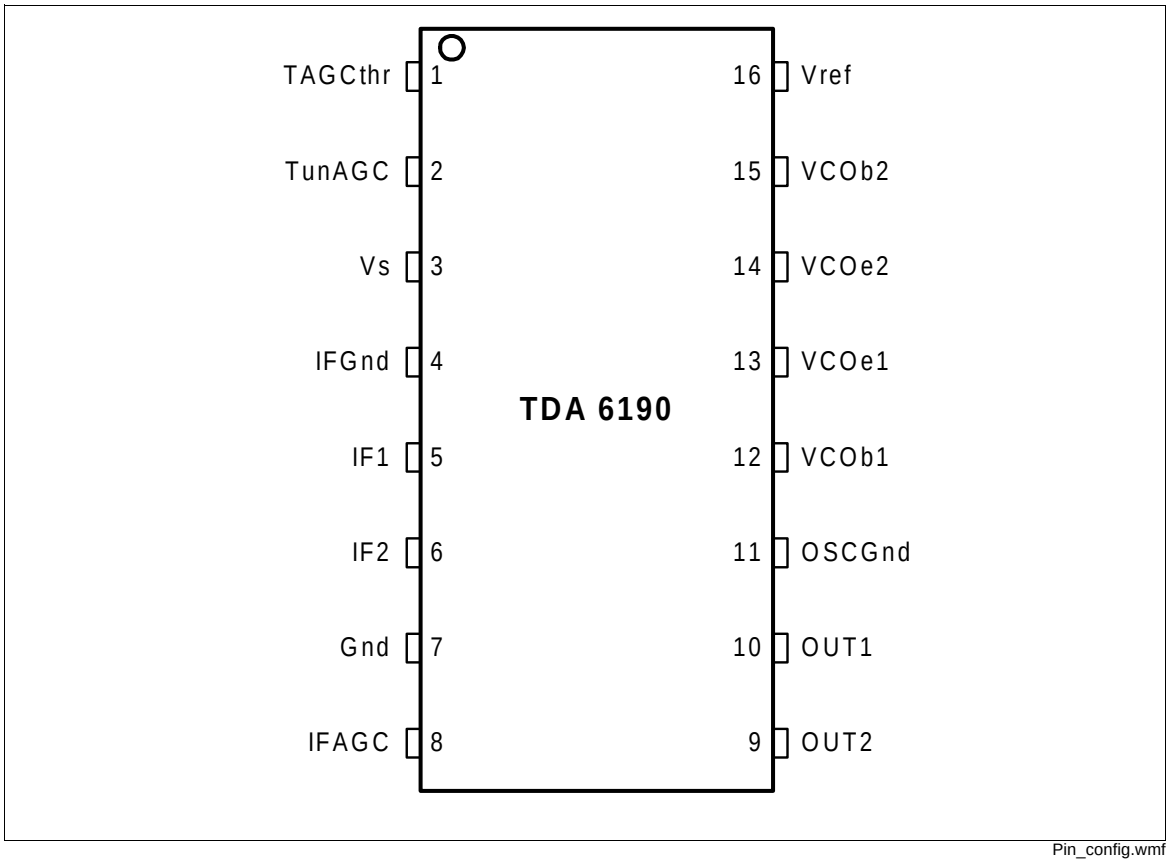


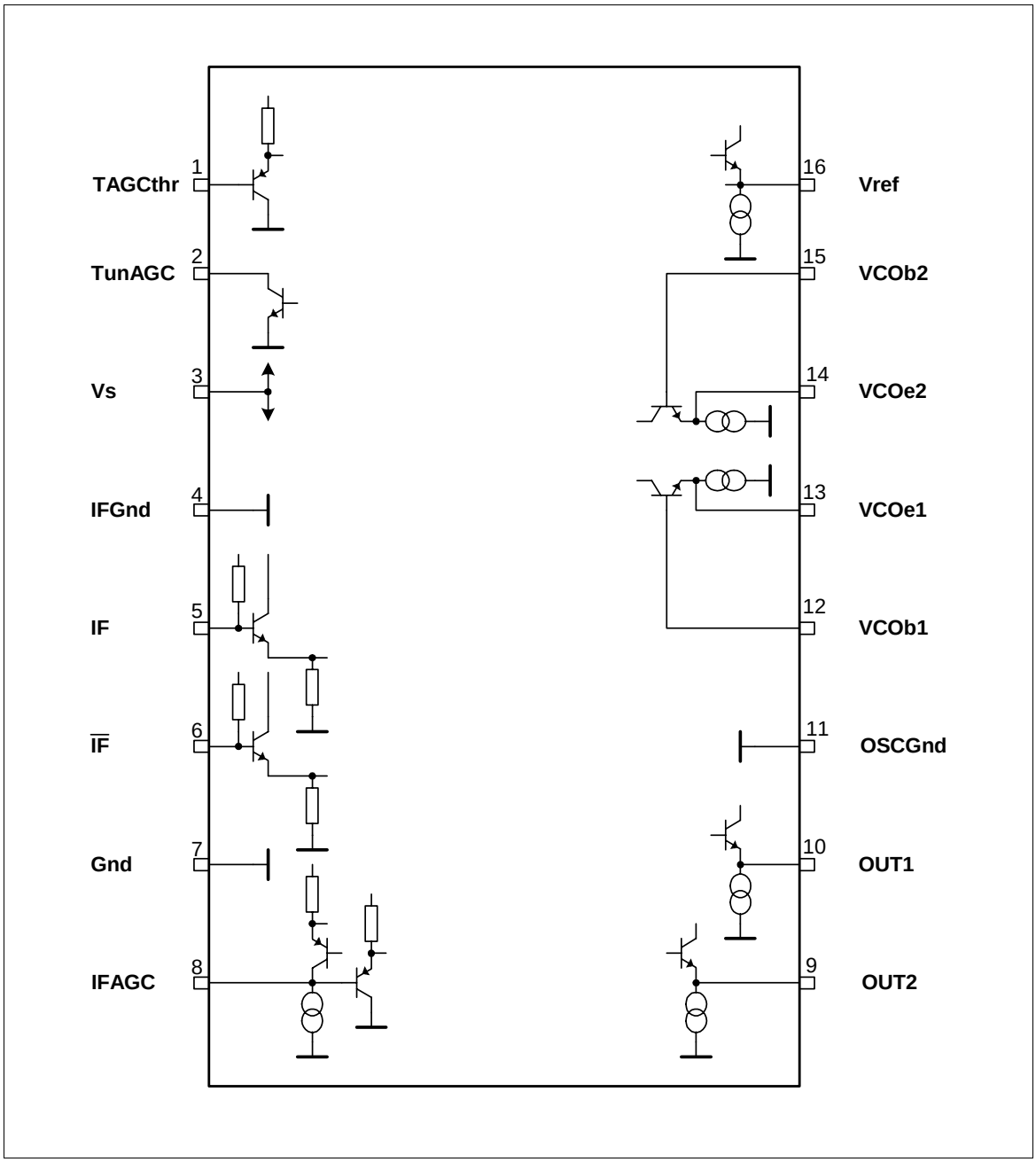
Figure 2-1 Pin Configuration

2.2 Pin Definitions and Functions

Table 2-1 Pin Definition and Function

Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	TAGCthr		Tuner AGC threshold; delayed tuner AGC adjust input; if not required, connect to reference voltage Vref
2	TunAGC		Delayed tuner AGC output; open npn transistor collector
3	Vs		Supply voltage
4	IFGnd		IF input ground
5	IF1		IF input IF1; balanced to IF2
6	IF2		IF input IF2; balanced to IF1
7	Gnd		Ground
8	IFAGC		IF amplifier gain control input pin, low voltage corresponds to maximum gain
9	OUT2		buffered mixer output OUT2; balanced to OUT1
10	OUT1		buffered mixer output OUT1; balanced to OUT2
11	OSCGnd		Oscillator Ground
12	VCOb1		VCO base 1; balanced to VCOb2
13	VCOe1		VCO emitter 1; balanced to VCOe2
14	VCOe2		VCO emitter 2; balanced to VCOe1
15	VCOb2		VCO base 2; balanced to VCOb1
16	Vref		Reference voltage

2.3 Equivalent I/O Schematic



I_O_Schematic.wmf

Figure 2-2 Equivalent I/O Schematic

2.4 Functional Block Diagram

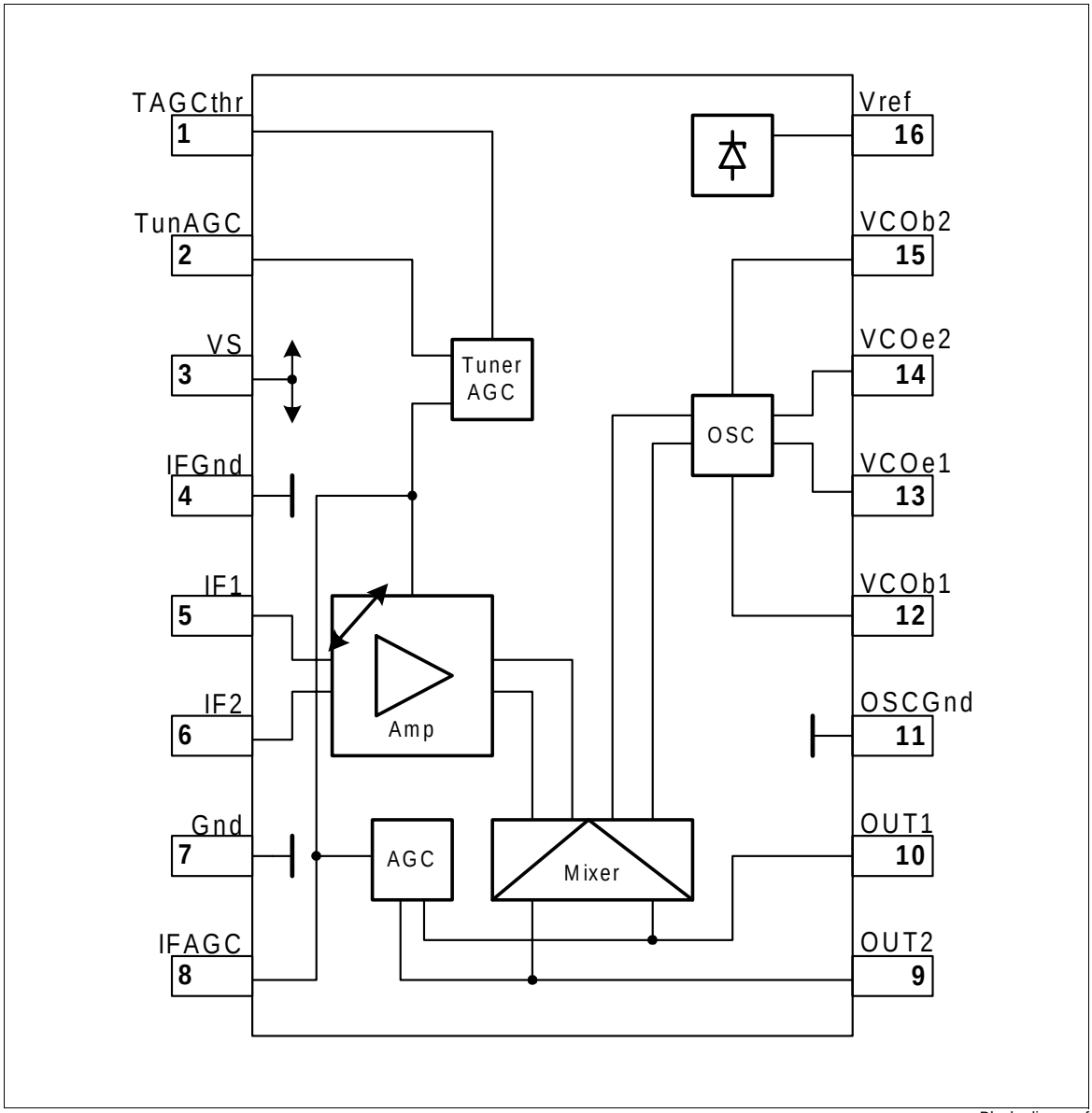


Figure 2-3 Block Diagram

TDA 6190T: AGC is disabled, external gain control voltage to Pin 8

2.5 Functional Block Description

2.5.1 Power Supply, Reference Voltage

The 3.6 V low noise reference voltage Vref is used as a reference for the adjustment of the delayed tuner AGC. The reference voltage has a low temperature coefficient and high line regulation.

2.5.2 DVB-IF Input Amplifier, AGC

The filtered IF signal is fed to the balanced input pins IF1 / IF2 of the gain controlled amplifier, where it is amplified and then down converted to the output frequency signals.

The control voltage for the gain-controlled amplifier at pin IFAGC is applied from external source.

If the IFAGC control voltage level exceeds an adjustable value (TAGCthr), a sink current at TunAGC is generated which controls the tuner gain.

2.5.3 Oscillator

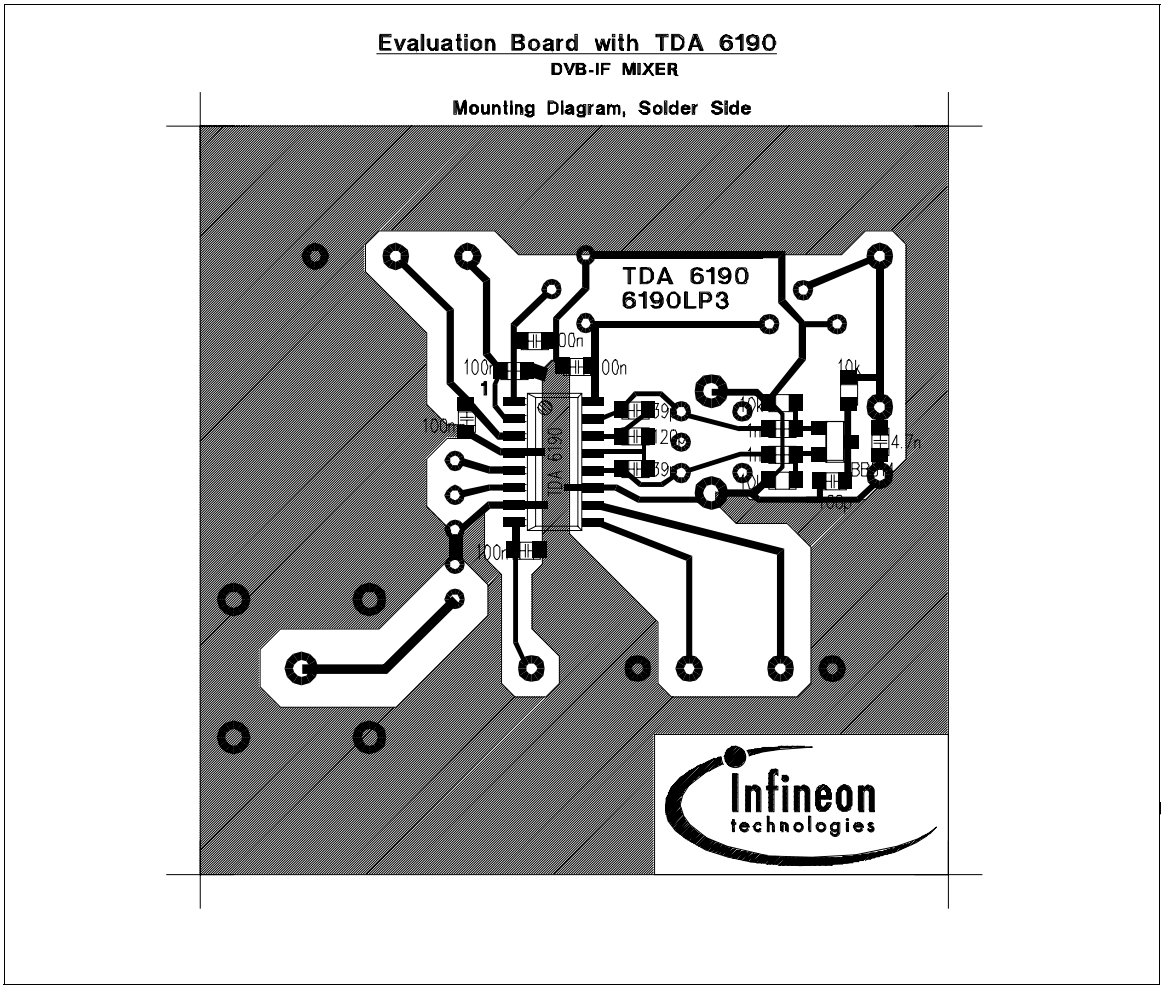
The symmetrical 4 pin voltage controlled oscillator feeds the mixer to generate the down converted DVB-IF signals.The frequency of the VCO is below or above the input frequency of the AGC amplifier. The control voltage for the external varactor diode is derived from the DVB processor.

2.5.4 Mixer and Output Buffers

The mixer converts the filtered and amplified IF signal down to the low IF frequency. This frequency is fed to a balanced output pair OUT1 and OUT2.

3 Application

3.1 Evaluation Board Layout



6190lp3_2.pdf

Figure 3-1 Evaluation Board Layout

3.2 Bill of material

Table 3-1 Bill of material for Application Circuit 1

Component	Type / Value	Material / Raster	Outline / Case	Supplier	Ordering Code Nr.
R01	10k		0805	S&M	
R02	10k		0805	S&M	
R03	10k		0805	S&M	
C01	100n	X7R	0805	S&M	
C02	100n	X7R	0805	S&M	
C03	100n	X7R	0805	S&M	
C04	100n	X7R	0805	S&M	
C05	100n	X7R	0805	S&M	
C06	39p	COG	0805	S&M	
C07	120p	COG	0805	S&M	
C08	39p	COG	0805	S&M	
C09	1n	X7R	0805	S&M	
C10	1n	X7R	0805	S&M	
C11	1µF	5mm	MKT	S&M	
C12	100p	COG	0805	S&M	
C13	4n7	X7R	0805	S&M	
Tr01	10k		Potentiom.		
Tr02	10k		Potentiom.		
SAW01	X6966M		SAW Filter	S&M	
D01	BB814		Var. Diode		
L01	330nH		Filter adjust.	TOKO	T1369Z
IC01	TDA6190T		P-DSO-16-1	Infineon	Q67036-A1073

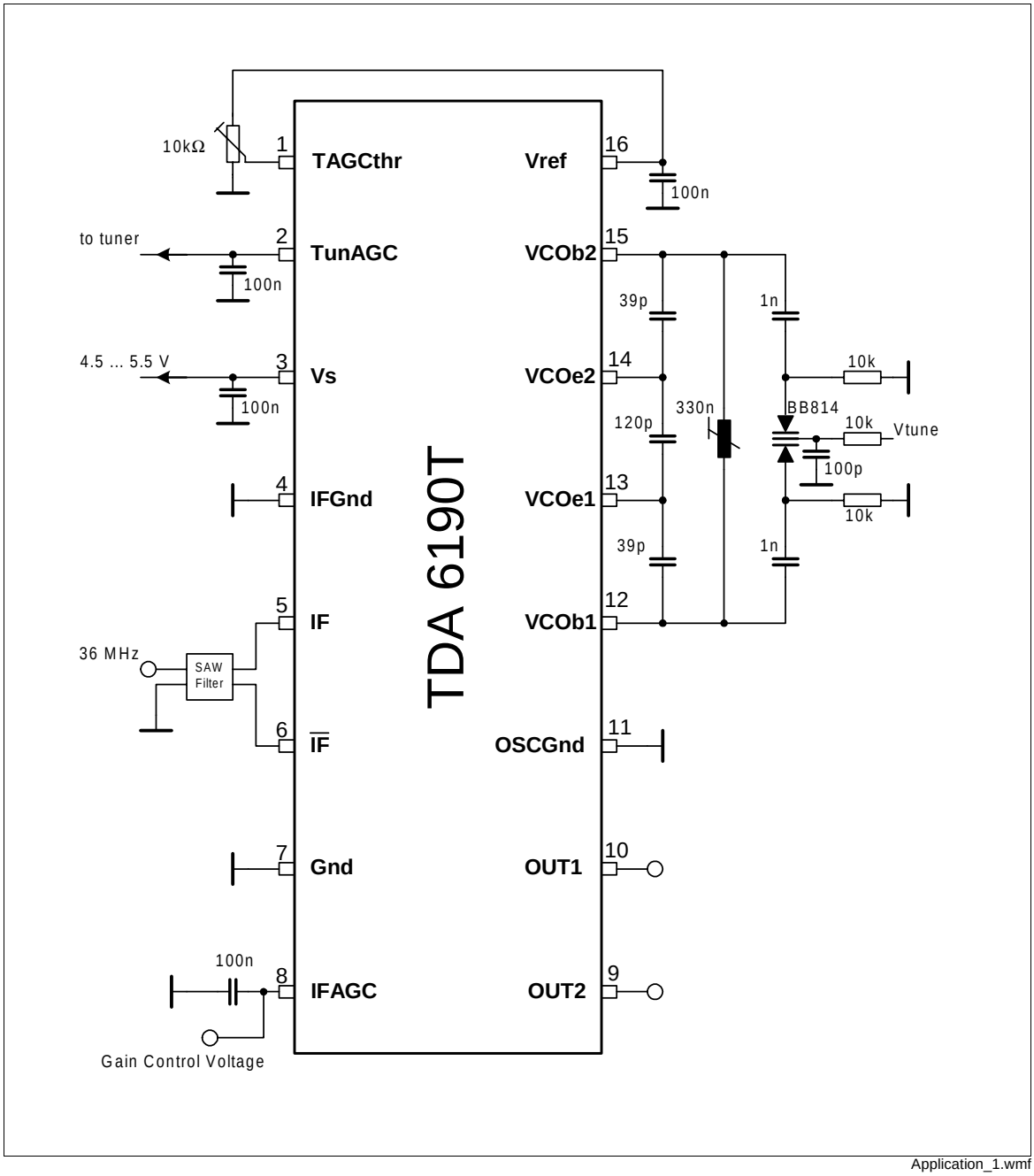
Mechanical Parts

1 x PCB

8 x Soldering Pin 1 mm (Stocko)

1 x BNC-Jack (PCB Mounting)

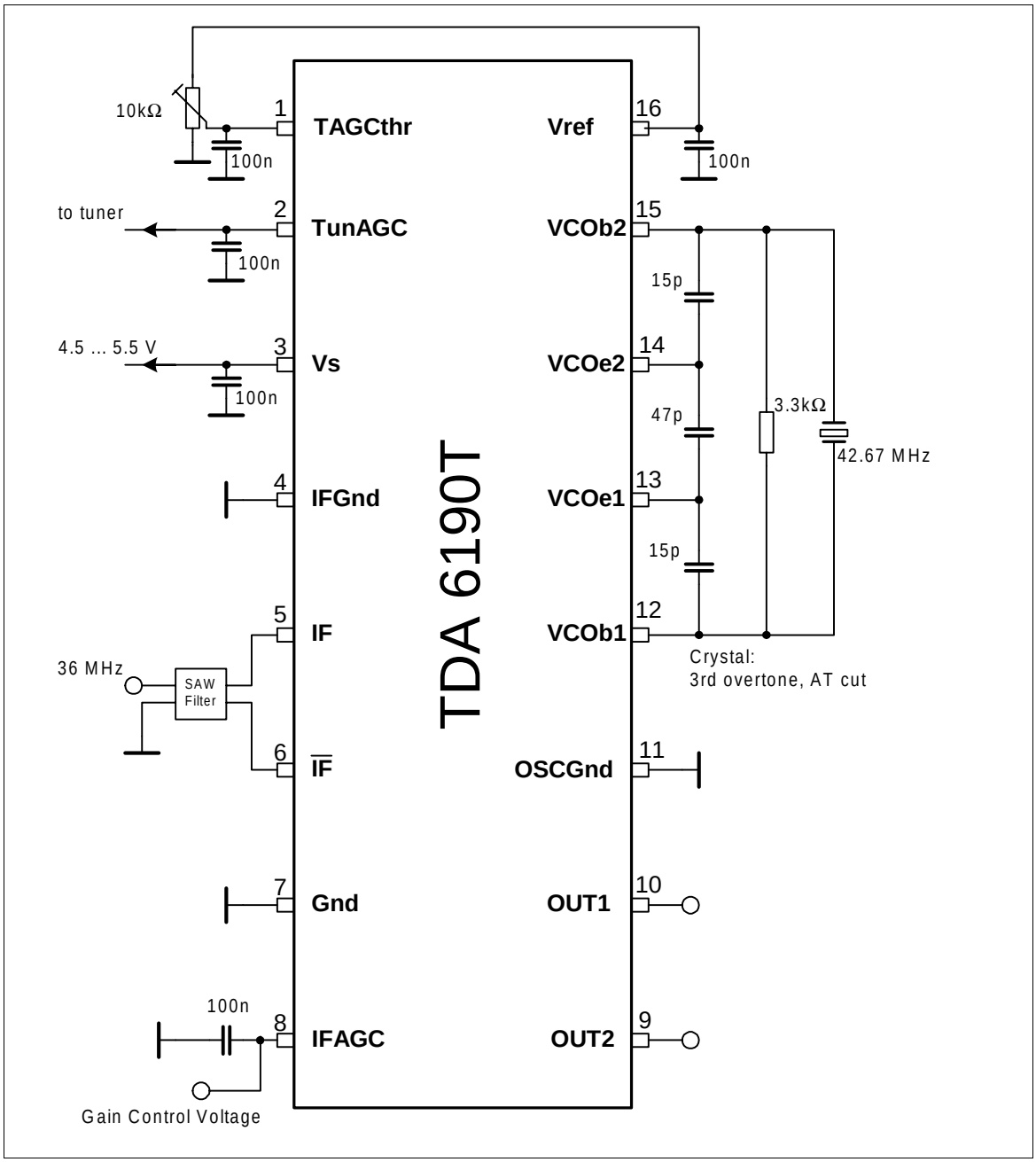
3.3 Application Circuit 1 (Evaluation Board)



Application_1.wmf

Figure 3-2 Application Circuit 1 (Evaluation Board)

3.4 Application Circuit 2



Application_2.wmf

Figure 3-3 Application Circuit 2

4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Ambient Temperature under bias: T_A= -40 to +85°C

Table 4-1 Absolute Maximum Ratings

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min	max		
1	Reference current	I_{Vref}	-10	1	mA	
2	Tuner AGC output	V_{TunAGC}	-0.3	13,2	V	
3	IFAGC	V_{IFAGC}	-0.3	Vref	V	
4	IF input	$V_{IF1/IF2}$	-0.3	4	V	
5	Supply voltage	V_{Vs}	-0.3	6	V	
6	Mixer outputs	$I_{OUT1\ /OUT2}$	-5	1	mA	
7	VCO	V_{VCO}	-0.3	4	V	
8	VCO	I_{VCO}	-3		mA	
9	Tuner AGC threshold	$V_{TAGCthr}$	-0.3	Vref	V	
10	Junction temperature	T_j		125	°C	
11	Storage temperature	T_{stg}	-40	125	°C	
12	Thermal resistance	$R_{th\ SA}$		110	K/W	
13	ESD protection ***)**	V_{ESD}	-4	+4	kV	HBM

*) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993

All values are referred to Ground (pin), unless stated otherwise.
All ground pins must be connected externally.
All currents flowing into the IC are positive, out of the IC are negative.

4.1.2 Operating Range

Table 4-2 Operating Range

#	Parameter	Symbol	Limit Values		Unit	Test Conditions	■	Item
			min	max				
1	Supply voltage	V_{Vs}	4.5	5.5	V			
2	Input frequency range of IF Amplifier (-3 dB)	$f_{IF1/IF2}$	30	70	MHz			
3	Mixer output bandwidth (-1 dB)	$B_{OUT1/OUT2}$	11		MHz			
	VCO frequency range	f_{VCO}	25	80	MHz	depends on application		
	Ambient temperature	T_A	-40	85	°C			

■ This value is not subject to production test - verified by design/characterisation.

4.1.3 AC/DC Characteristics

Table 4-3 AC/DC Characteristics with T_A = 25 °C, V_S = 5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■	Item
			min	typ	max				
1.	Power Supply, Reference Voltage								
	Current consumption Vs	I_{Vs}	35	50	65	mA			
	Reference voltage Vref	V_{Vref}	3.3	3.6	3.8	V			
	Vref line regulation	$\Delta V_{refLine}$			30	mV	V_{Vs} = 4.5 to 5.5 V		
	Vref load regulation	$\Delta V_{refLoad}$			30	mV	I_{Vref} = -0.5 to 0.5mA		
	Vref vs temperature	$\Delta V_{refTemp}$	-30	10	30	mV	T_A = 0 to 70 °C		
2.	DVB-IF Input Amplifier, AGC								
	Static Characteristics								
	IF input voltage	$V_{IF1/IF2}$	3.2	3.6	3.9	V			
	IFAGC voltage (AGC_{min}= $gain_{max}$)	$V_{IFAGCgmax}$	0		0.5	V			
	IFAGC voltage (AGC_{max}= $gain_{min}$)	$V_{IFAGCgmin}$	2.5		3.9	V			
	Tuner AGC threshold active	$V_{TAGCthr}$	0		2.0	V			
	Tuner AGC threshold disable	$V_{TAGCthrdis}$	3.0		V_{Vs}	V			
	Tuner AGC threshold current	$I_{TAGCthr}$	-1		1	µA	$V_{TAGCthr}$ = 0 V		
	Tuner AGC output current	$I_{TunAGCon}$	2.5	3.5	5	mA	V_{TunAGC} = 0.5 V; V_{IFAGC} =1.5V; $V_{TAGCthr}$ = 1V		
	Tuner AGC output current	$I_{TunAGCoff}$	0		10	µA	V_{TunAGC}= 13.2 V; V_{IFAGC} =1.5V; $V_{TAGCthr}$ = 2V		

Table 4-3 AC/DC Characteristics with T_A = 25 °C, V_S = 5 V (cont'd)

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■	Item
			min	typ	max				
Dynamic Characteristics									
	Minimum IF input level (max. gain)	V_{min} IF1/IF2	42	45	48	dBµV	$f_{IF1/IF2}$= 36 MHz(sine); V_{IFAGC} = 0.4 V V_{OUT1}-V_{OUT2} set to 2 x 1V_{pp}		
	Maximum IF input level (min. gain)	V_{max} IF1/IF2	90	93	96	dBµV	$f_{IF1/IF2}$= 36 MHz(sine); V_{IFAGC} = 2.4 V V_{OUT1}-V_{OUT2} set to 2 x 1V_{pp}		
	Input impedance	$R_{IF1/IF2}$ $C_{IF1/IF2}$	1.5	2.0 1.5	2.5	kΩ pF	balanced input	■	
	maximum slope of delayed tuner AGC	ΔI_{TunAGC} / ΔV_{IFAGC}	27	40	54	mA/V	V_{IFAGC}=1.8 to 2.1V $V_{TAGCthr}$=1.9V V_{TunAGC}=0.5V		

Table 4-3 AC/DC Characteristics with T_A = 25 °C, V_S = 5 V (cont'd)

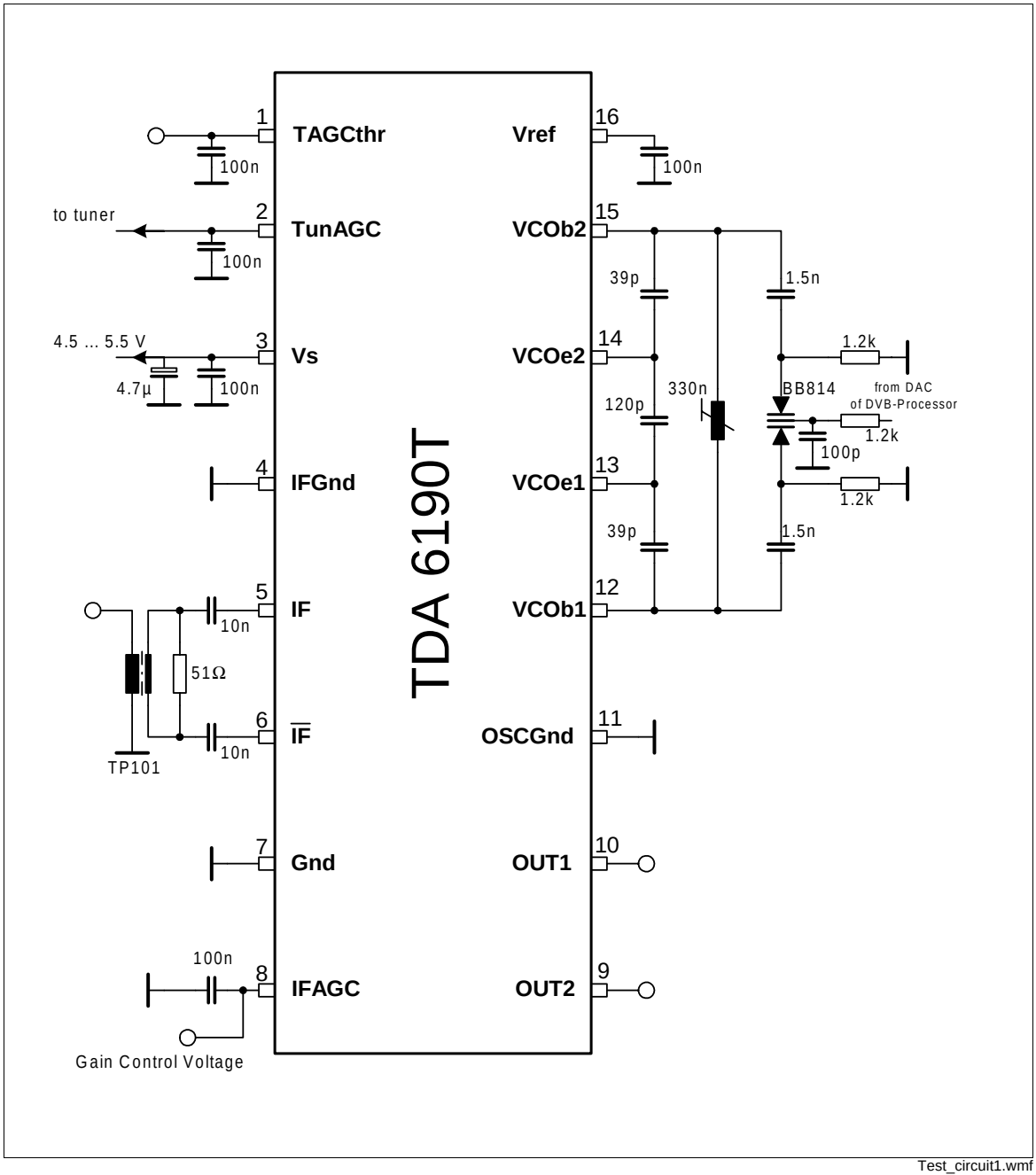
#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■	Item
			min	typ	max				
3. Oscillator									
Static Characteristics									
	VCO voltage	$V_{VCOb1/VCOb2}$	2.1	2.4	2.7	V			
Dynamic Characteristics									
	VCO input admittance [a]	Y=G+jB					VCO, 39/120/39pF		
	Real part	$G_{VCOb1/b2}$		-1.3		mS	f_{VCO} = 25 MHz	■	
	Imag. part	$B_{VCOb1/b2}$		1.8		mS	f_{VCO} = 25 MHz	■	
	Real part	$G_{VCOb1/b2}$		-1.9		mS	f_{VCO} = 55 MHz	■	
	Imag. part	$B_{VCOb1/b2}$		5.8		mS	f_{VCO} = 55 MHz	■	
	Oscillator level	$V_{VCOb1/b2}$		107		dBµV	f_{VCO} = 43 MHz	■	
	Oscillator range	f_{VCO}	25		80	MHz	depends on application	■	
	Oscillator frequency variation range	Δf_{VCO}	4	6		MHz	Application Circuit 1 V_{tune} = 0.5 to 3 V		
	Oscillator phase noise @ 10 kHz	$\Delta\Phi_{VCO}$		-105		dBc/Hz	Application Circuit 1 f_{VCO} = 43 MHz	■	

Table 4-3 AC/DC Characteristics with T_A = 25 °C, V_S = 5 V (cont'd)

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■	Item
			min	typ	max				
4. Mixer, Output Buffers									
Static Characteristics									
	Demodulator output DC level	$V_{OUT1/OUT2}$	V_{Vs} - 2.5	V_{Vs} - 2.0	V_{Vs} - 1.5	V			
	Demodulator output sink current	$I_{OUT1/OUT2}$	1.4	2.0	2.8	mA			
Dynamic Characteristics									
output voltage V_{OUT1}-V_{OUT2} set to 2 x 1Vpp									
	Mixer output bandwidth (-1 dB)	$B_{OUT1/B_{OUT2}}$	11			MHz	f_{VCO} = 43 MHz; $R_L \geq$ 10 kΩ; CL≤10 pF; $V_{IF1/IF2}$= 60dBµV		
	Intermodulation	a_{IM}	45	48		dB	f_{VCO} = 43 MHz; $R_L \geq$ 10 kΩ; CL≤10 pF; V_{f1}=V_{f2}=60 dBµV $f_{1\ IF1/IF2}$=37 MHz; $f_{2\ IF1/IF2}$=38 MHz; OUT1/OUT2:balanced		
	Harmonic distortion	THD		-60	-50	dB	f_{VCO} = 43 MHz; $R_L \geq$ 10 kΩ; CL≤10 pF; $V_{IF1/IF2}$= 70 dBµV $f_{IF1/IF2}$= 39.5 MHz OUT1/OUT2:balanced		
	Buffer output impedance	R_{OUT1}		25	100	Ω	$f_{OUT1/OUT2}$= 11 MHz		
	Buffer output impedance	R_{OUT2}		25	100	Ω	$f_{OUT1/OUT2}$= 11 MHz		

■ This value is not subject to production test - verified by design/characterisation.

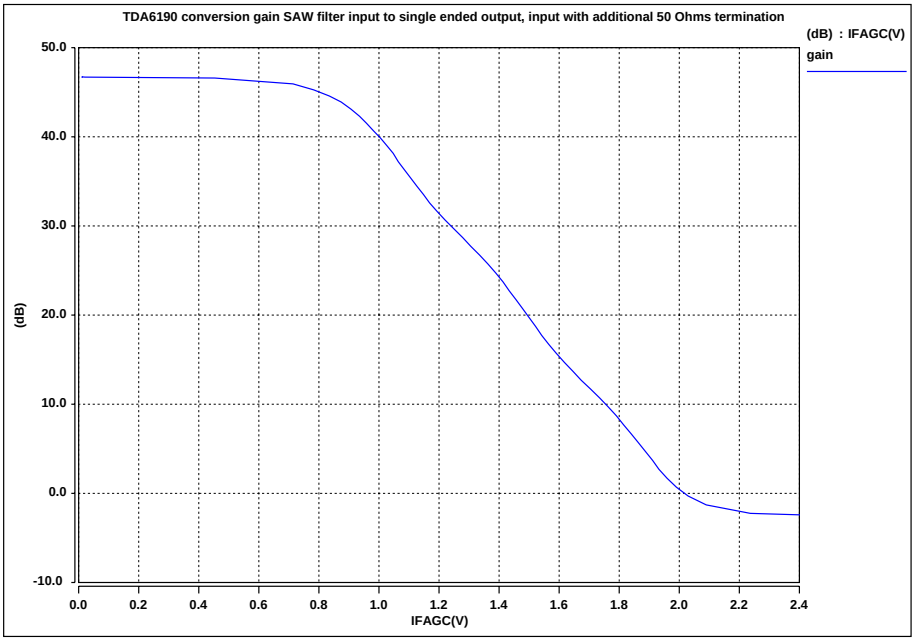
4.2 Test Circuit



Test_circuit1.wmf

Figure 4-1 Test Circuit

4.3 Typical Characteristics



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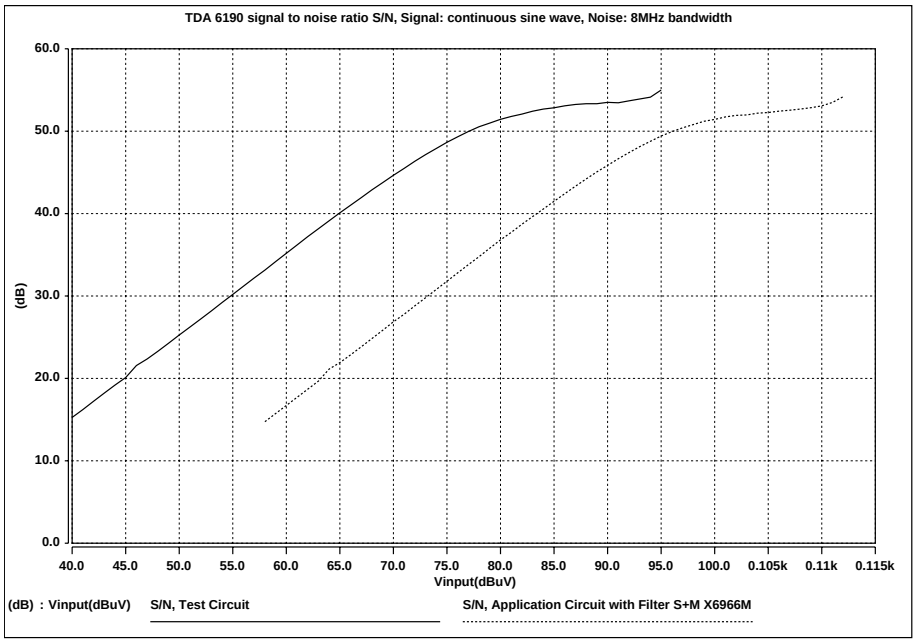

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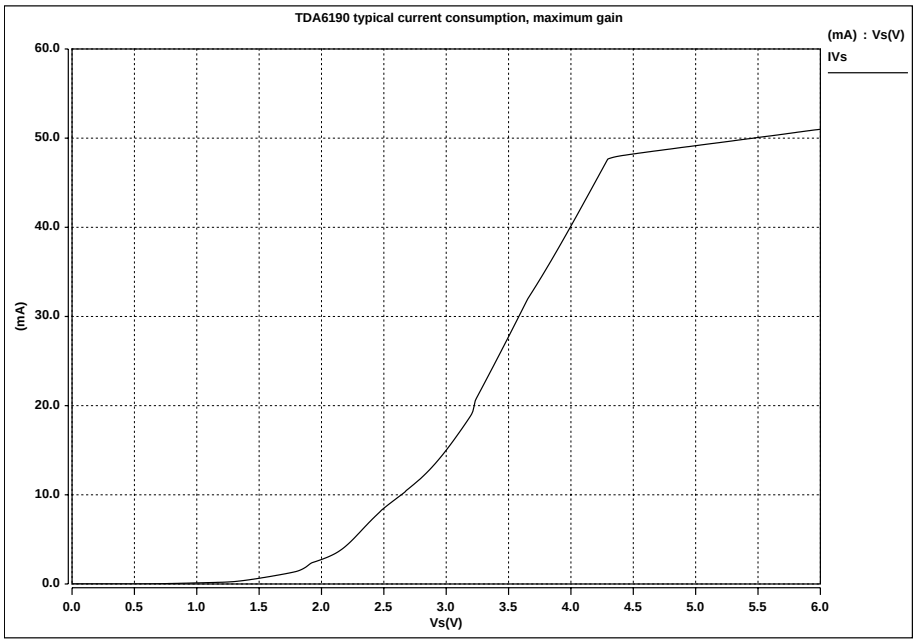

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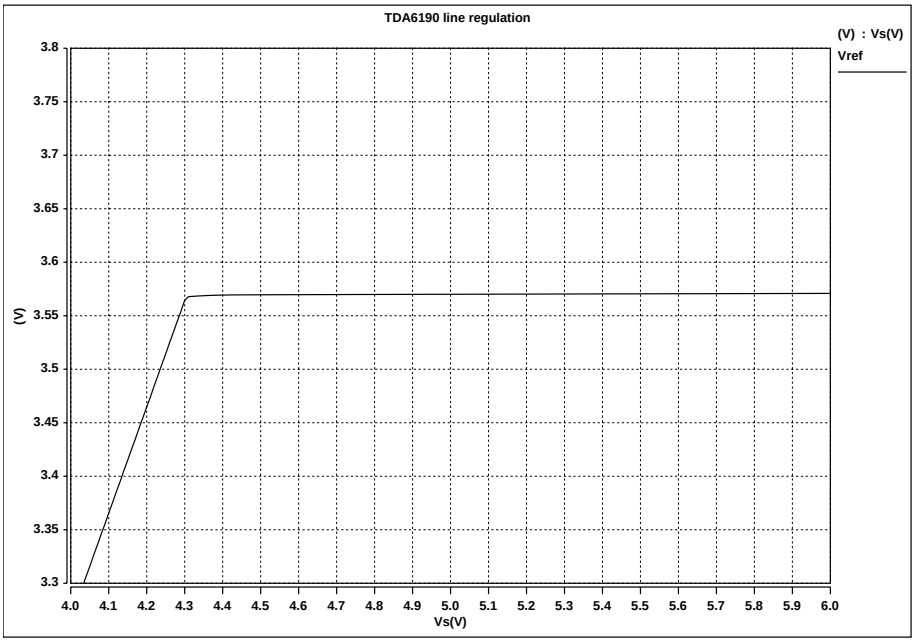

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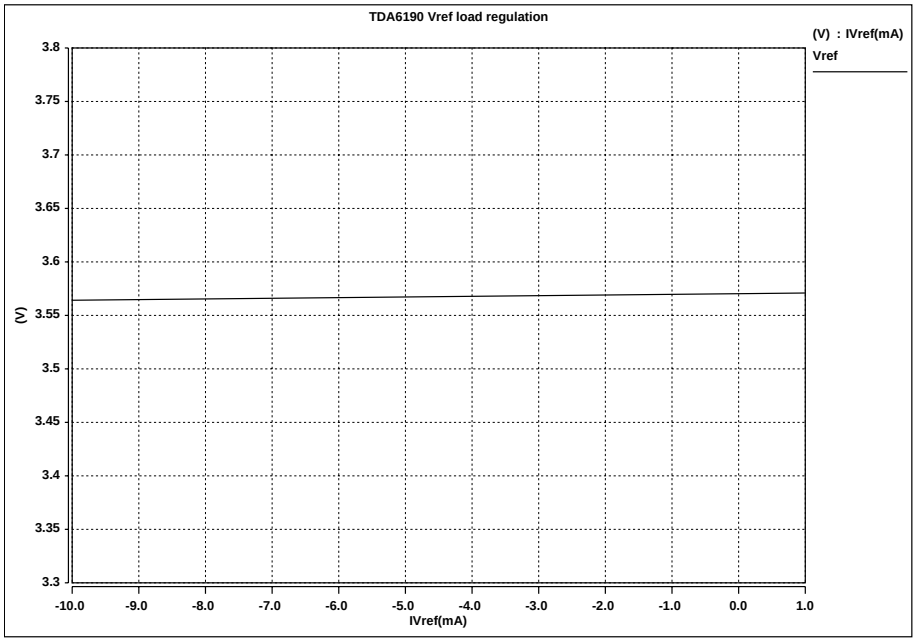

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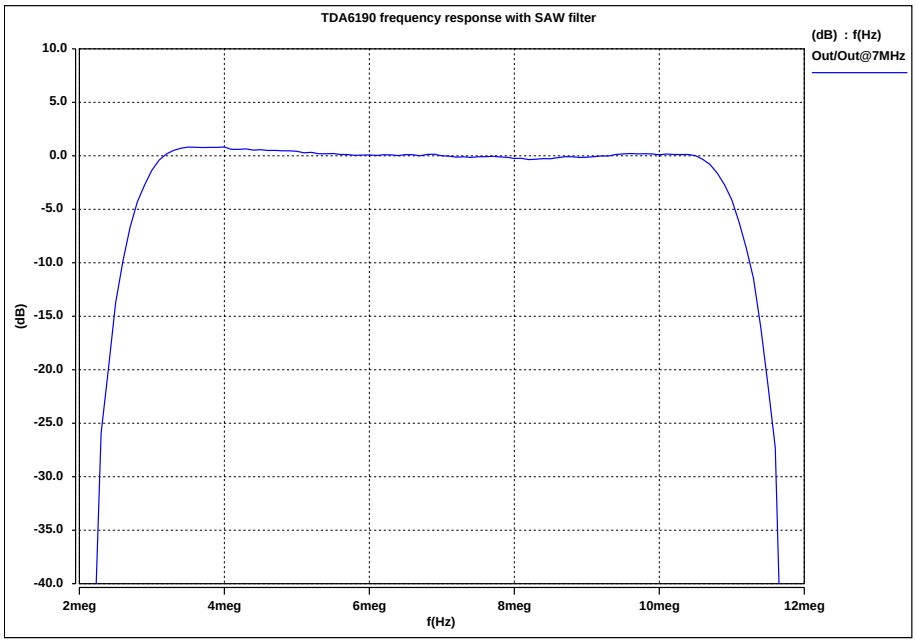
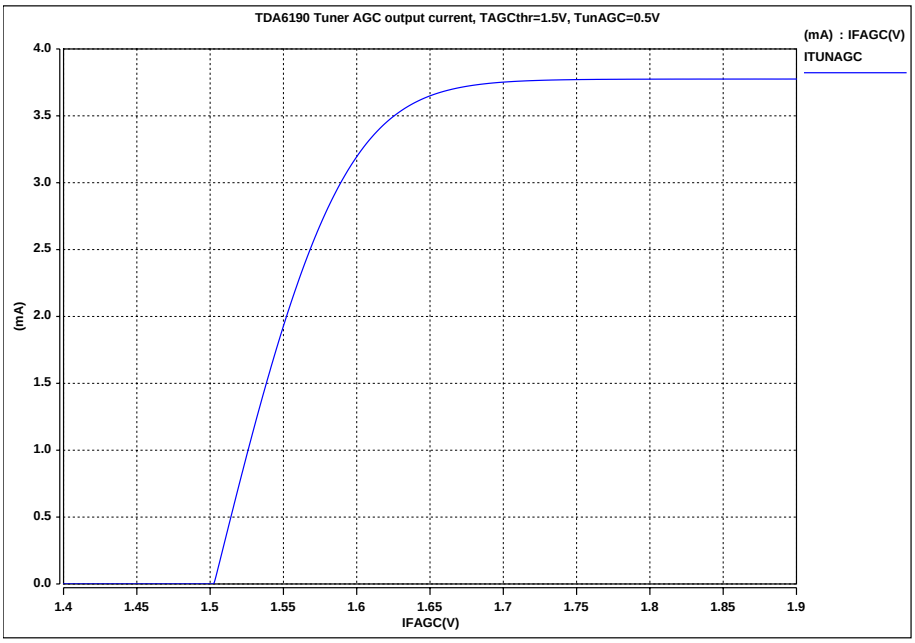
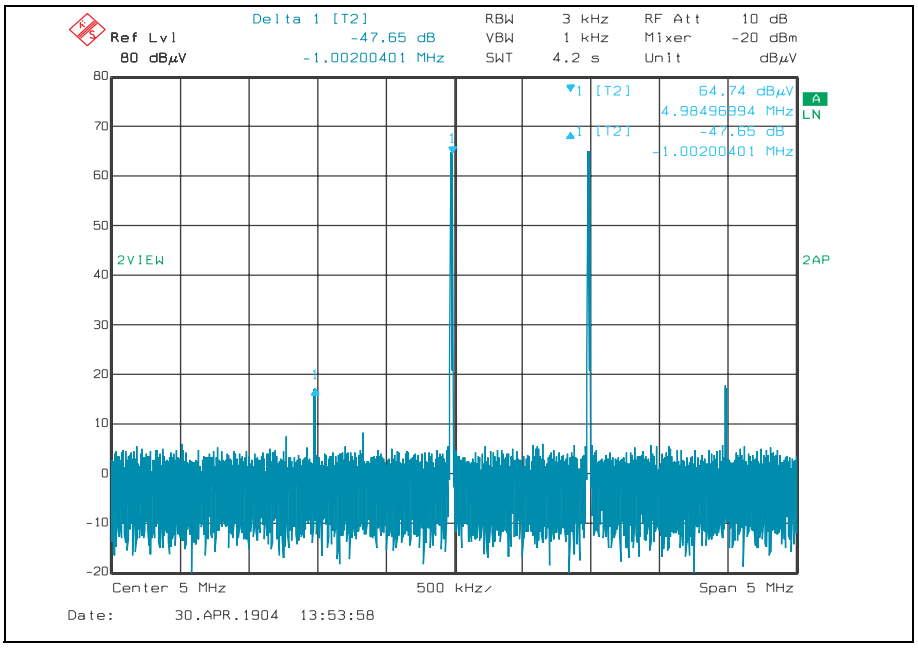


TDA6190_FrequencyResponse.pdf



TDA6190_TunerAGC.pdf

Intermodulation, measured single ended using Evaluation Circuit for frequency response



TDA6190_IM3.pdf

4.4 Evaluation Circuit for frequency response

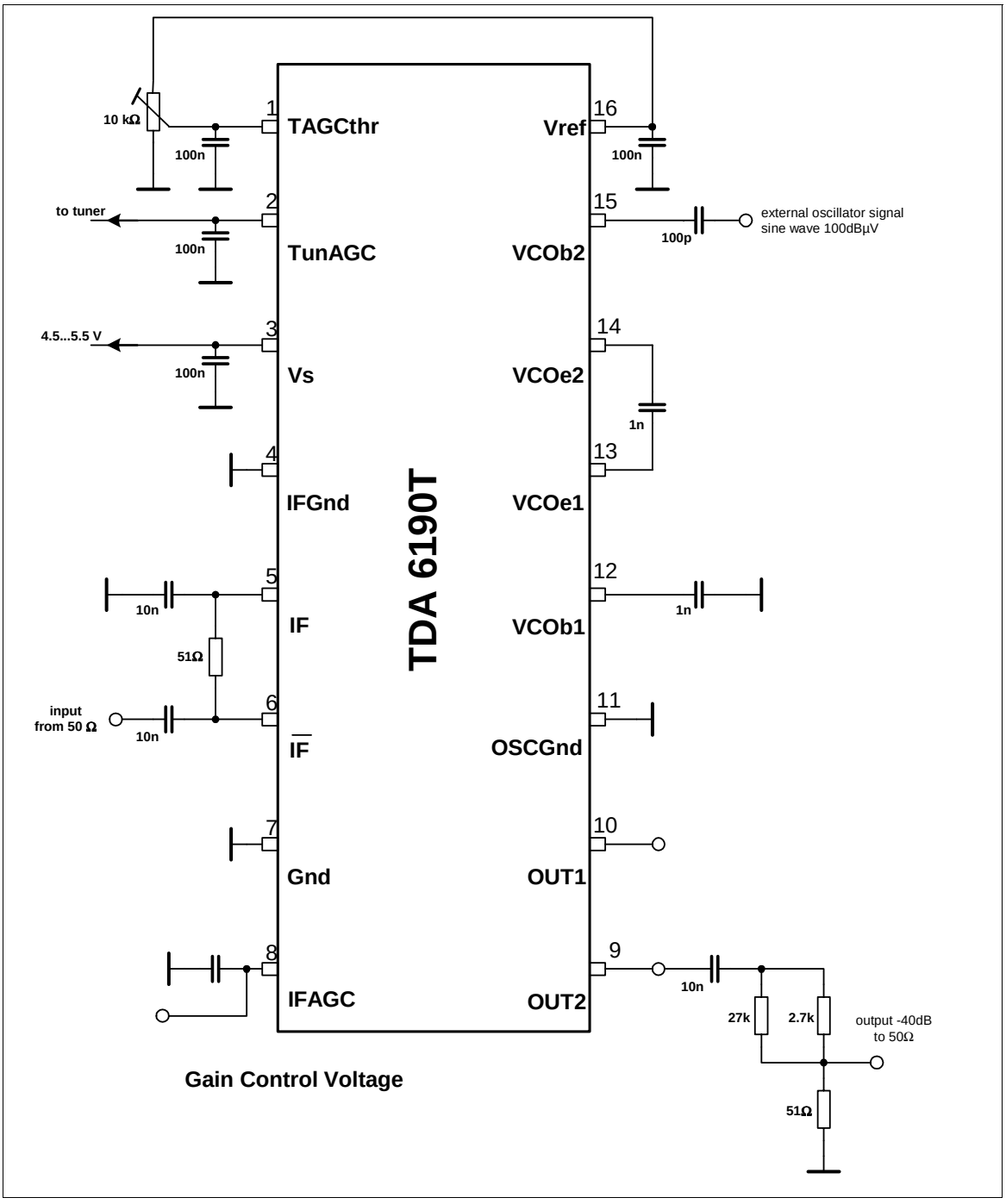
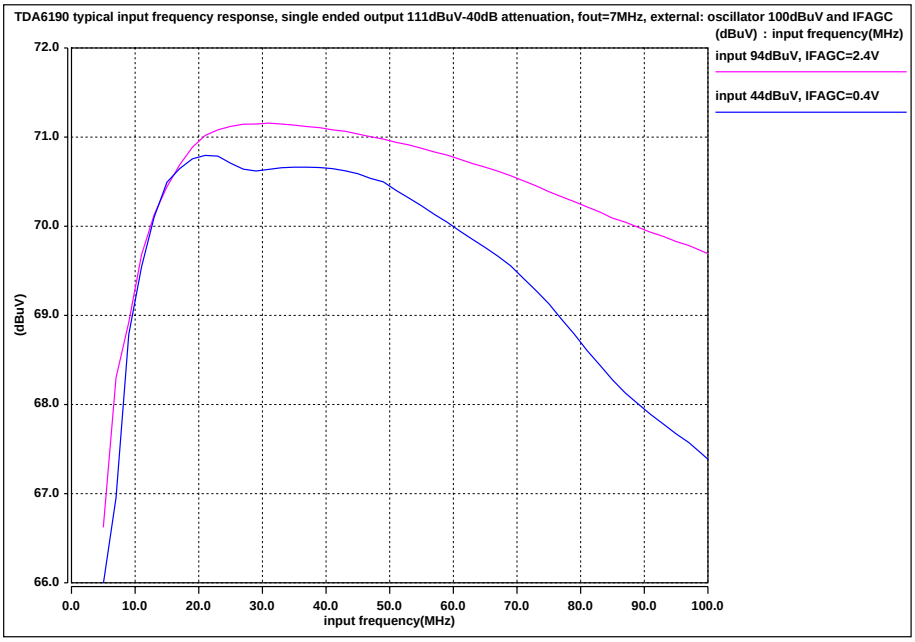
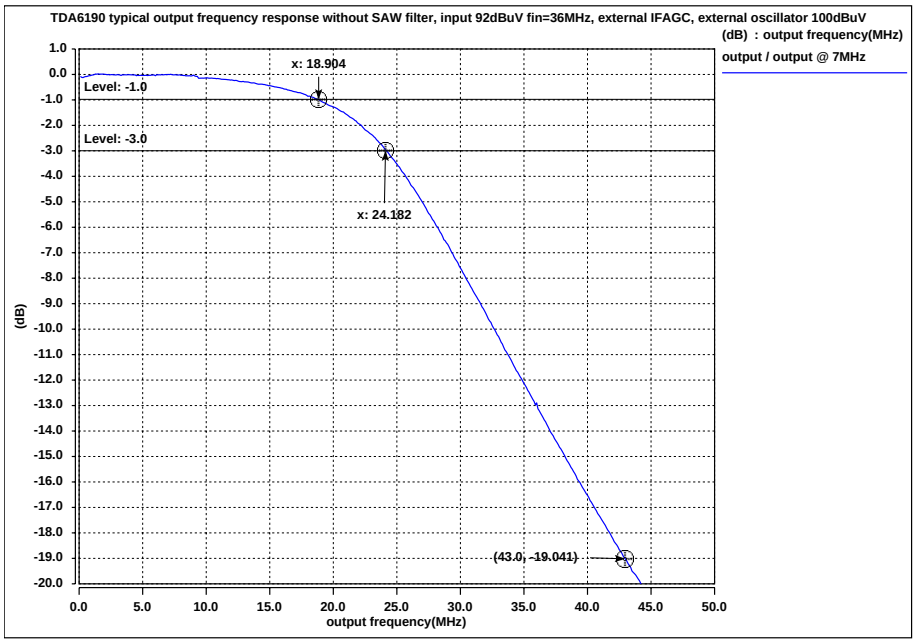


Figure 4-2 Evaluation Circuit



TDA6190_FR_input_2.pdf



TDA6190_FR_output.pdf