SIEMENS

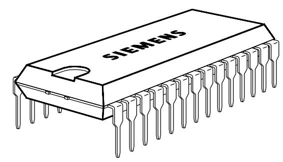
TV-Stereo Processor

TDA 6610-5

Bipolar IC

Features

- All functions are I^2C Bus controlled
- Suitable for multistandard including NICAM SCART-interface
- Independent headphones output high signal noise ratio
- Extremely low total harmonic distortion
- High security of detection of the stereo decoder part because of the digital interference suppression and the very narrow bandwidth



P-DIP-28-3

Type	Ordering Code	Package
TDA 6610-5	Q67000-A5126	P-DIP-28-3

General

The TDA 6610-5 represents a complete TV-stereo sound system controlled via the I^2C Bus. The IC is divided into three functional blocks:

1. **Stereo Sound Processing with High Quality (exceeds DIN 45500; suitable for NICAM and CD)**
   a) Matrix for G-standard
   b) Additional single-channel AF-input (for e.g. AF-signal according to L-standard)
   c) Stereo SCART-interface is in accordance with FTZ-official specification
   d) Stereo loudspeaker signal section with Ch1/Ch2 switch, treble/bass control, quasi-stereo/stereo base width control and separate left/right loudspeaker volume control
   e) Signal section with Ch1/Ch2 switch and volume control for stereo headphones

2. TV-Sound Identification Signal Decoder Consisting of:

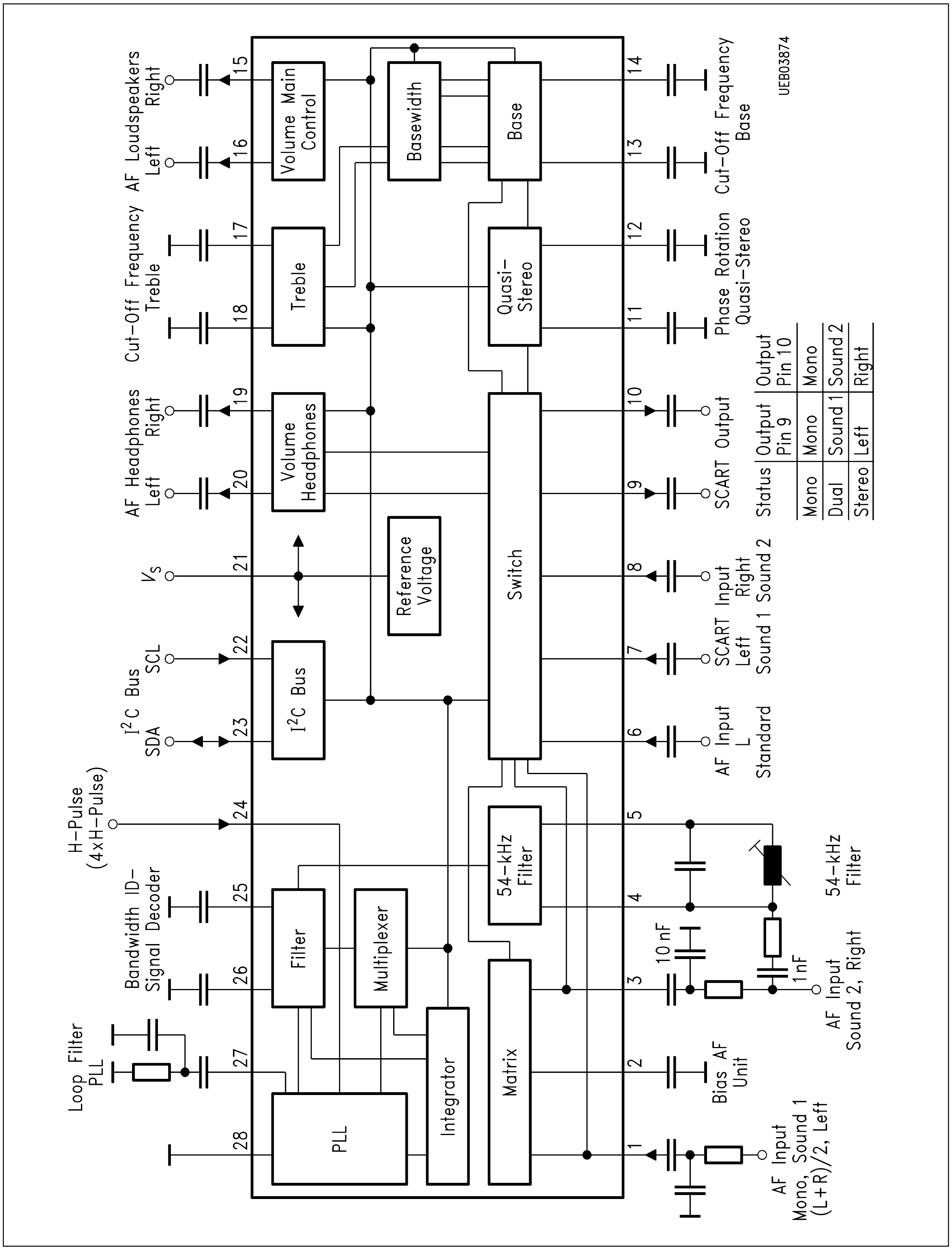
a) Active pilot signal filter
b) Phase-independent rectifier with very narrow bandwidth for evaluation of the identification signal
c) Digital integrator to reduce interference
d) Multiplexer for cyclical switch over between "stereo" or "dual" recognition
e) PLL for the generation of the reference signal. External synchronization with either the fly-back pulse or external reference clock signals of 62.5 kHz

3. Control Section for:

a) I^2C Bus interface with listen/talk function
b) Control of the complete AF-sound processing
c) Control of the identification signal decoder
d) Reading of the identification signal decoder status
e) Test modes

Pin Functions

Pin No.	Function
1	AF-input mono, left, sound 1
2	Bias for AF-unit
3	AF-input right, sound 2
4	54-kHz input
5	54-kHz filter
6	AF-input (L-standard)
7	AF-input SCART left (sound 1)
8	AF-input SCART right (sound 2)
9	AF-output SCART (mono, sound 1, left)
10	AF-output SCART (mono, sound 2, right)
11	Phase-shifter quasi-stereo
12	Phase-shifter quasi-stereo
13	Cut-off frequency base (base-width) left
14	Cut-off frequency base (base-width) right
15	AF-output, loudspeaker left
16	AF-output, loudspeaker right
17	Cut-off frequency treble left
18	Cut-off frequency treble right
19	AF-output, headphones left
20	AF-output, headphones right
21	+ V_S (supply voltage)
22	I^2C Bus SCL
23	I^2C Bus SDA
24	Input H-pulse (4 x H-pulse)
25	Filter ID-signal decoder
26	Filter ID-signal decoder
27	PLL-filter ID-signal decoder
28	Ground



Block Diagram

Circuit Description

Signal Section

The audio signal processing in the matrix and the switch-over for multichannel TV-sound signals according to the two-carrier system used in Germany takes place in the matrix and switching sections. In addition to the two inputs for the demodulated sound carrier a two-channel SCART-input and an additional mono input (e.g. for demodulated L-standard sound) are provided. The two AF-inputs can be by-passed internally in such a way that decoded stereo sound signals of other audio systems (NICAM) can be processed. The switching section is terminated with the SCART-output and an independently switchable Ch1/Ch2 switch for the loudspeaker and headphone outputs.

In the loudspeaker signal path a switchable quasi-stereo section follows the Ch1/Ch2 switch. This section gives a special audio effect with mono signals due to a 180˚ phase shift at medium frequencies (about 1 kHz) in one channel. The following bass control exhibits a step of 3 dB with an adjustment range of + 15/– 12 dB. The cutoff frequency is set for each channel with an external capacitor.

A circuit for stereo base-width expansion, switchable if stereo signals are recognized, provides a more spatial audio effect due to 50 % of frequency dependent crosstalk in opposing phases. The circuit operates with the same cut-off frequency as the bass control, but the function is largely independent. Likewise the treble control, whose cut-off frequency is also controlled by a capacitor in each channel, has a step of 3 dB with an adjustment range of ± 12 dB. The volume control can be adjusted independently for the right and left loudspeaker signal path. Using 57 steps of 1.25 dB each, a 70 dB adjustment range is available, where the 57th step activates the "MUTE" function. Functions such as "balance" or "loudness" are realized by software adjustment of the appropriate tone and volume controls.

In the signal path for the headphones after the Ch1/Ch2 switch a volume control circuit is used for the simultaneous left/right adjustment. Thirty-two steps of 2 dB each allow an adjustment range of 62 dB (31 x 2 dB = 62 dB, while the 32nd step activates the "MUTE” function).

Identification Sound Decoder

The input of the identification sound decoder consists of an op-amp for the pilot signal with its sidebands. An external LC-circuit is used to select the pilot carrier and his sidebands. The signal is then passed to a phase-independent active band-pass filter wih a very narrow bandwidth (adjustable externally). This filter detects whether the lower side-band of the pilot carrier, modulated with the identification signal, is present. The center frequency of the filter is switched between "dual" and "stereo" by a multiplexer. The multiplexing frequency is adjustable by software. If a side-band is detected, the multiplexer stops. The first "detected" criterion is processed by a digital integrator and a following comparator in order to suppress interferences due to noise. The decoder status caw can be read out via I^2C Bus (talk mode) as the "stereo" or "dual" mode. The control of the corresponding signal path can take place either directly internally or through the µC . All required clock signals are derived from a fast lowding PLL synchronized by a external reference frequency. This reference frequency has to be sufficiently close to the horizontal frequency, but **a rigid phase coupling is not required**. Therefore, alternatively to the line frequency the use of a crystal-controlled 62.5 kHz frequency commonly available in PLL-tuning systems is possible.

Control Section

All functions are controlled via I²C Bus interface with listen/talk functions. The actual valid data are stored in a latch block.

The telegram structure is:

start condition - chip address - any number of data bytes - stop condition

The following conditions apply to the data bytes:

Before a data byte (with the adjustment information) is transmitted, a subaddress byte has **always** to be transmitted.

Example: The headphone volume (HP vol) has to be increased in several (i.e. 3) steps.

Right		**Wrong**	
Start condition		Start condition	
Chip address	84 (Hex)	Chip address	84 (Hex)
Subaddr. vol	03 (Hex)	Subaddr. vol	03 (Hex)
Volume step 8	08 (Hex)	Volume step 8	08 (Hex)
Subaddr. vol	03 (Hex)	Volume step 9	09 (Hex)
Volume step 9	09 (Hex)	Volume step 10	0A (Hex)
Subaddr. vol	03 (Hex)	Stop condition	
Volume step 10	0A (Hex)		
Stop condition			

Within a telegram (i.e. without a new start condition) any different subaddresses can be accessed. The changeover between "listen" and "talk" however has always to be initialized via the sequence "stop condition - start condition - chip address". Before each readout always a start condition and chip address (talk) has to be transmitted. The data to be read out are loaded into the I²C Bus interface after this sequence and are available for the transfer to the µC.

Chip Address

MSB	•	•	•	•	•	•	LSB
1	0	0	0	0	1	0	R/W

R/W = 0 → Read (Listen)

R/W = 1 → Write (Talk)

Subaddress Bytes

	MSB	•	•	•	•	•	•	LSB
Loudspeaker volume left	X	X	X	X	X	0	0	1
Loudspeaker volume right	X	X	X	X	X	0	1	0
Headphone volume	X	X	X	X	X	0	1	1
Treble/bass	X	X	X	X	X	1	0	1
Switch byte **I**	X	X	X	X	X	1	1	1
Switch byte **II**	X	X	X	X	X	0	0	0

Setting Bytes

a) Loudspeaker Volume Left / Right

	MSB	•	•	•	•	•	•	LSB
Maximum volume	X	X	1	1	1	1	1	1
Max – 1 step	X	X	1	1	1	1	1	0
Max – 15 steps	X	X	1	1	0	0	0	0
Max – 55 steps	X	X	0	0	1	0	0	0
MUTE	X	X	0	0	0	1	1	1
MUTE	X	X	0	0	0	0	0	0
MUTE	X	X	0	0	0	X	X	X
Power ON	0	0	0	0	0	0	0	1

b) Headphone Volume

	MSB	•	•	•	•	•	•	LSB
Max. volume	T2	T1	T0	1	1	1	1	1
Max – 1 step	T2	T1	T0	1	1	1	1	0
Max – 15 steps	T2	T1	T0	1	0	0	0	0
Max – 31 steps	T2	T1	T0	0	0	0	0	1
MUTE	T2	T1	T0	0	0	0	0	0
Power ON	0	0	0	0	0	0	0	1

T0 - T2 are test bits; these have to be set to 0 for normal operation.

c) Treble / Bass

	MSB	•	•	•	•	•	•	LSB
Linear	1	0	0	0	1	0	0	0
Max. treble, lin. bass	1	1	0	0	1	0	0	0
Max. treble, lin. bass	1	1	X	X	1	0	0	0
Min. treble, lin. bass	0	1	0	0	1	0	0	0
Min. treble, lin. bass	0	0	X	X	1	0	0	0
Lin. treble, max. bass	1	0	0	0	1	1	0	1
Lin. treble, max. bass	1	0	0	0	1	1	X	1
Lin. treble, max. bass	1	0	0	0	1	1	1	X
Lin. treble, min. bass	1	0	0	0	0	1	0	0
Lin. treble, min. bass	1	0	0	0	0	0	X	X
Max. treble, max. bass	1	1	X	X	1	1	X	1
Min. treble, min. bass	0	0	X	X	0	0	X	X
Power ON	0	0	0	0	0	0	0	1
	MSB treble			LSB treble	MSB bass			LSB bass

d) Switch Byte I

MSB	•	•	•	•	•	•	LSB
MUTE I	MUTE II	$Ch1/Ch2_{vol}$	$Ch1/Ch2_{HP}$	Mono	SCART	SCART-D	AM

MUTE I	= 0	All AF-outputs are muted (loudspeakers, headphones, SCART); power ON
MUTE I	= 1	All AF-outputs ON
MUTE II	= 0	Loudspeaker outputs muted; power ON
MUTE II	= 1	Loudspeaker outputs ON

MUTE I and MUTE II are OR gated with respect to the loudspeaker outputs

MUTE I	MUTE II	Loudspeaker outputs	Headphones, SCART-outputs
0	0	muted	muted
0	1	muted	muted
1	0	muted	ON
1	1	ON	ON

$CH1/Ch2_{vol}$	=	0	Sound 1 on the loudspeaker outputs; power ON
$CH1/Ch2_{vol}$	=	1	Sound 2 on the loudspeaker outputs
$CH1/Ch2_{HP}$	=	0	Sound 1 on the headphone outputs; power ON
$CH1/Ch2_{HP}$	=	1	Sound 2 on the headphone outputs

$CH1/Ch2_{vol}$ and $CH1/Ch2_{HP}$ are only effective if the matrix is set to the position "dual sound".

Mono	=	0	identification signal decoder is set to mono position and held; power ON
Mono	=	1	normal operation of identification signal decoder
SCART	=	0	normal TV-operation; power ON
SCART	=	1	SCART-playback; connection of SCART-inputs - AF-outputs. SCART = 1 has priority over AM = 1 (loudspeaker and headphones)
SCART-D	=	0	SCART-playback stereo (mono); power ON
SCART-D	=	1	Enable for the Ch1/Ch2 switch during SCART-playback (only effective when SCART = 1)
Standard L	=	0	normal operation (G-standard)
Standard L	=	1	AM AF-input is activated; power ON AM = 1 has priority over bypass = 1

e) Switch Byte II

MSB	•	•	•	•	•	•	LSB
MPX0	MPX1	Quasi-st	Be	H-pul	Matrix 0	Matrix 1	Bypass

MPX0	MPX 1	MPX period		recommended $C_{25, 26}$
0	0	2 s	power ON	1 µF
0	1	4 s		2.2 µF
1	0	8 s		4.7 µF

MPX-period = 2 s signifies: Identification (ID) signal decoder searches 1 s for dual and 1 s for stereo transmission

Quasi-st	=	0	Quasi-stereo OFF; Power ON
Quasi-St	=	1	Quasi-stereo ON
Be	=	0	Stereo basewidth expansion OFF; Power ON
Be	=	1	Stereo basewidth expansion ON
H pul	=	0	ID-signal decoder synchronization with f_H = 15.625 kHz; power ON
H pul	=	1	ID-synchronization with 4 x f_H

Matrix 0	Matrix 1	Matrix status	
0	0	mono	power ON
0	1	stereo	
1	0	dual	
1	1	automatic according to ID-signal decoder	

Bypass	=	0	Normal operations (G-standard)
Bypass	=	1	Matrix is bridged so that left/right signals can be fed in; power ON (AM = 1 has priority over bypass = 1)

Priority List of Setting Bits

1. MUTE I
2. MUTE II (only with regard to the loudspeaker outputs)
3. SCART
4. Standard L
5. Bypass
6. Matrix 0, 1

h) Talk Mode

MS	•	•	•	•	•	•	LSB
St	D	T5	T4	T3	X	X	X
0	0	decoder detects mono					
1	0	decoder detects stereo					
0	1	decoder detects dual					
1	1	internally inhibited					

T3 - T5 are test bits

Absolute Maximum Ratings

T_A = 0 to 70 °C; all voltages relatives to V_{SS}

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{21}	0	14	V
Max. DC-voltage	V_1	0	V_{21}	V
Max. DC-voltage	V_2	0	V_{21}	V
Max. DC-voltage	V_3	0	V_{21}	V
Max. DC-voltage	V_4	0	V_{21}	V
Max. DC-voltage	V_6	0	V_{21}	V
Max. DC-voltage	V_7	0	V_{21}	V
Max. DC-voltage	V_8	0	V_{21}	V
Max. DC-voltage	V_{11}	0	V_{21}	V
Max. DC-voltage	V_{12}	0	V_{21}	V
Max. DC-voltage	V_{13}	0	V_{21}	V
Max. DC-voltage	V_{14}	0	V_{21}	V
Max. DC-voltage	V_{17}	0	V_{21}	V
Max. DC-voltage	V_{18}	0	V_{21}	V
Max. DC-voltage	V_{22}	0	V_{21}	V
Max. DC-voltage	V_{23}	0	V_{21}	V
Max. DC-voltage	V_{24}	0	V_{21}	V
Max. DC-voltage	V_{25}	0	V_{21}	V
Max. DC-voltage	V_{26}	0	V_{21}	V
Max. DC-current	I_5	0	2	mA
Max. DC-current	I_9	0	2	mA
Max. DC-current	I_{10}	0	2	mA
Max. DC-current	I_{15}	0	2	mA
Max. DC-current	I_{16}	0	2	mA
Max. DC-current	I_{19}	0	2	mA
Max. DC-current	I_{20}	0	2	mA
Max. DC-current	I_{27}	0	1	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance system ambient	$R_{th\ SA}$		53	K/W

Operating Range

Parameter	Symbol	min.	max.	Unit
Supply voltage	V_6	10	13.2	V
Ambient temperature	T_A	0	70	°C
Input frequency range	f_I	0.01	20	kHz

Characteristics

V_S = 12 V; T_A = 25 ^oC, in accordance with test circuit 1

I²C Bus present: start - 84 - 01,3F - 0 2,3F - 0 3,1F - 0 5,88 - 0 6,10 - 07,C8 - 00,01 - stop

Chip address - *Vol* $_{LSl}$ *63 - Vol* $_{LSr}$ *63 - Vol* $_{HP}$ *31 - tone lin - adj 0dB - MUTE I, MUTE II, Mono - Bypass*

The basic setting for each point in the specification is always preset; only settings which deviate from this are given in the test conditions. Details in *italics* only provide explanation of the hexadecimal code and with switch bits on the set bits and features are stated.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_{21}		50		mA	

Signal Section

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Max. gain	$V_{16\text{-}1}$	– 2	0	2	dB	
Max. gain	$V_{15\text{-}3}$	– 2	0	2	dB	
Max. gain	$V_{20\text{-}1}$	– 2	0	2	dB	
Max. gain	$V_{19\text{-}3}$	– 2	0	2	dB	
Max. gain	$V_{16\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 01 *Matrix: Stereo*
Max. gain	$V_{15\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 01 *Matrix: Stereo*
Max. gain	$V_{20\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 *Matrix: Stereo*
Max. gain	$V_{19\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 *Matrix: Stereo*
Max. gain	$V_{16\text{-}1}$	4	6	8	dB	00,02; V_3 = 0 *Matrix: Stereo*
Max. gain	$V_{20\text{-}1}$	4	6	8	dB	00,02; V_3 = 0 *Matrix: Stereo*
Max. gain	$V_{16\text{-}7}$	– 5	– 3	– 1	dB	07,CC, *SCART*
Max. gain	$V_{15\text{-}8}$	– 5	– 3	– 1	dB	07,CC, *SCART*
Max. gain	$V_{20\text{-}7}$	– 5	– 3	– 1	dB	07,CC, *SCART*
Max. gain	$V_{19\text{-}8}$	– 5	– 3	– 1	dB	07,CC, *SCART*
Max. gain	$V_{16\text{-}6}$	– 2	0	2	dB	07,C9, Standard L
Max. gain	$V_{15\text{-}6}$	– 2	0	2	dB	07,C9, Standard L
Max. gain	$V_{20\text{-}6}$	– 2	0	2	dB	07,C9, Standard L
Max. gain	$V_{19\text{-}6}$	– 2	0	2	dB	07,C9, Standard L

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Gain	V_{9-1}	– 2	0	2	dB	
Gain	V_{10-3}	– 2	0	2	dB	
Gain	V_{9-3}	– 2	0	2	dB	00,02; V_1 = 0 *Matrix: Stereo*
Gain	V_{10-3}	– 2	0	2	dB	00,02; V_1 = 0 *Matrix: Stereo*
Gain	V_{9-1}	4	6	8	dB	00,02; V_3 = 0 *Matrix: Stereo*
Gain	V_{10-6}	– 2	0	2	dB	07,C9 Standard L
Gain	V_{9-6}	– 2	0	2	dB	07,C9 Standard L
Min. gain	V_{16-1}	– 65	– 70		dB	01,08-02,08 *Vol* $_{LSl}$ *8-Vol* $_{LSr}$ *8*
Min. gain	V_{15-3}	– 65	– 70		dB	01,08-02,08 *Vol* $_{LSl}$ *8-Vol* $_{LSr}$ *8* 01,08-02,08
Min. gain	V_{20-1}	– 57	– 62		dB	03,01 *Vol* $_{HP}$ *1*
Min. gain	V_{19-3}	– 57	– 62		dB	03,01 *Vol* $_{HP}$ *1*
Min. gain	V_{16-7}	– 68	– 73		dB	07,CC-01,08-02,08 *SCART-Vol* $_{LSl}$ *8-Vol* $_{LSr}$ *8*
Min. gain	V_{15-8}	– 68	– 73		dB	07,CC-01,08-02,08 *SCART-Vol LSl 8-Vol* $_{LSr}$ *8*
Min. gain	V_{20-7}	– 60	– 65		dB	07,CC-03,01 *SCART-Vol* $_{KH}$ *1*
Min. gain	V_{19-8}	– 60	– 65		dB	07,CC-03,01 *SCART-Vol* $_{KH}$ *1*
Min. gain	V_{16-6}	– 60	– 70		dB	07,C9-01,08-02,08 Standard L *Vol* $_{LSl}$ *8-Vol* $_{LSr}$ *8*
Min. gain	V_{15-6}	– 60	– 70		dB	07,C9-01,08-02,08 Standard L *Vol* $_{LSl}$ *8-Vol* $_{LSr}$ *8*
Min. gain	V_{20-6}	– 57	– 62		dB	07,C9-03,01 Standard L *Vol* $_{KH}$ *1*
Min. gain	V_{19-6}	– 57	– 62		dB	07,C9-03,01 Standard L *Vol* $_{KH}$ *1*
Flutter and wow	ΔV_{15-16}			± 2	dB	01,3F to 01,24 02,3F to 02,24 *Vol* $_{LSl}$ *63-36-Vol* $_{LSr}$ *63-36*
Flutter and wow	ΔV_{19-20}			± 2	dB	03,1F to 03,13 *Vol* $_{KH}$ *31-19*

Characteristics (cont'd)

V_S = 12 V; T_A = 25 ^{o}C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Step width Vol$_{15}$	ΔV_{15}	0	1.25	2.5	dB	01,X-01, (X ± 1) *Vol $_{LSl}$ X-Vol $_{LSl}$ (X 1)*
Step width Vol$_{16}$	ΔV_{16}	0	1.25	2.5	dB	02,X-02,(X±1) *Vol $_{Lsr}$ X-Vol $_{LSr}$ (X 1)*
Step width Vol$_{19}$	ΔV_{19}	0	2	4	dB	03,X-03, (X ± 1) *Vol $_{KH}$ X-Vol $_{KH}$ (X 1)*
Step width Vol$_{20}$	ΔV_{20}	0	2	4	dB	03,X-03, (X ± 1) *Vol $_{KH}$ X-Vol $_{KH}$ (X 1)*
Bass boost	V_{16-1}	13	15		dB	05,8F; f_l = 40 Hz *Bass max, treble lin.*
Bass boost	V_{15-3}	13	15		dB	05,8F; f_l = 40 Hz *Bass max, treble lin.*
Bass boost	V_{16-1}	– 10	– 12		dB	05,8F; f_l = 40 Hz *Bass max, treble lin.*
Bass boost	V_{15-3}	– 10	– 12		dB	05,8F; f_l = 40 Hz *Bass max, treble lin.*
Step wide bass	ΔV_{15}	1	3	5	dB	05,8X-05,8 (X ± 1) *Bass X – bass (X ± 1)*
Step wide bass	ΔV_{16}	1	3	5	dB	05,8X-05,8 (X ± 1) *Bass X – bass (X ± 1)*
High frequency emphasis	V_{16-1}	10	12		dB	05,8F; f_l = 15 kHz *Treble max, bass lin.*
High frequency emphasis	V_{15-3}	10	12		dB	05,8F; f_l = 15 kHz *Treble max, bass lin.*
High frequency emphasis	V_{16-1}	– 10	– 12		dB	05,8F; f_ll = 15 kHz *Treble max, bass lin.*
High frequency emphasis	V_{15-3}	– 10	– 12		dB	05,8F; f_l = 15 kHz *Treble max, bass lin.*
Step wide treble	ΔV_{15}	1	3	5	dB	05,X8-0,5 (X ± 1) 8 *Treble X – treble (X ± 1)*
Step wide treble	ΔV_{16}	1	3	5	dB	05,X8-0,5 (X ± 1) 8 *Treble X – treble (X ± 1)*
Linearity sound	ΔV_{15}			± 2	dB	05,88; f_l = 40 Hz – 15 kHz *Treble, bass lin.*
Linearity sound	ΔV_{16}			± 2	dB	05,88; f_l = 40 Hz – 15 kHz *Treble, bass lin.*
Channel separation	ΔV_{15-16}	50			dB	V_3 or V_1 = 600 mVrms
Channel separation	ΔV_{19-20}	50			dB	V_3 or V_1 = 600 mVrms
Channel separation	ΔV_{9-10}	50			dB	V_3 or V_1 = 600 mVrms

Characteristics (cont'd)
V_S = 12 V; T_A = 25 ^oC, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Cross talk attenuation switch	$\alpha_{inputinterf / Output\,rms}$	60			dB	$V_{I\,rms}$ = 0 $V_{I\,Int1,3,6}$ = 600 mVrms $V_{I\,Int7,8}$ = 2 Vrms
Attenuation MUTE	$\alpha_{1\text{-}16}$	80			dB	01,00-02,00 *Vol* $_{LSl}$ *0-Vol* $_{LSr}$ *0* V_1 = 600 mVrms
Attenuation MUTE	$\alpha_{1\text{-}16}$	80			dB	07,48; V_1 = 600 mVrms *MUTE I: 0*
Attenuation MUTE	$\alpha_{1\text{-}16}$	80			dB	07,88; V_1 = 600 mVrms *MUTE II: 0*
Attenuation MUTE	$\alpha_{3\text{-}15}$	80			dB	01,00-02,00 *Vol* $_{LSl}$ *0-Vol* $_{LSr}$ *0* V_3 = 600 mVrms
Attenuation MUTE	$\alpha_{3\text{-}15}$	80			dB	07,48; V_3 = 600 mVrms *MUTE I: 0*
Attenuation MUTE	$\alpha_{3\text{-}15}$	80			dB	07,88; V_3 = 600 mVrms *MUTE II: 0*
Attenuation MUTE	$\alpha_{1\text{-}20}$	80			dB	03,00; V_1 = 600 mVrms *Vol* $_{KH}$ *0*
Attenuation MUTE	$\alpha_{1\text{-}20}$	80			dB	07,48; V_1 = 600 mVrms *MUTE I: 0*
Attenuation MUTE	$\alpha_{3\text{-}19}$	80			dB	03,00; V_3 = 600 mVrms *Vol* $_{KH}$ *0*
Attenuation MUTE	$\alpha_{3\text{-}19}$	80			dB	07,48; V_3 = 600 mVrms *MUTE I: 0*
Analog values are valid for feed-in at the pin 6, 7, 8; $V_{7,\,8}$ = 2 Vrms; V_6 = 600 mVrms						
Attenuation MUTE	$\alpha_{3\text{-}10}$	80			dB	07,48; V_3 = 600 mVrms *MUTE I: 0*
Attenuation MUTE	$\alpha_{1\text{-}9}$	80			dB	07,48; V_3 = 600 mVrms *MUTE I: 0*
Attenuation MUTE	$\alpha_{6\text{-}10}$	80			dB	07,49; V_6 = 600 mVrms *MUTE I: 0*, Standard L
Attenuation MUTE	$\alpha_{6\text{-}9}$	80			dB	07,49; V_6 = 600 mVrms *MUTE I: 0*, Standard L

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Max. input voltage	V_6	600			mVrms	$THD_{15,16}$ = 1 %
Max. input voltage	V_3	600			mVrms	THD_{15} = 1 %
Max. input voltage	V_1	600			mVrms	THD_{16} = 1 %
Max. input voltage	V_1	300			mVrms	THD_{16} = 1 %; 00,02 *Matrix: Stereo*
Max. input voltage	V_7	2			Vrms Vrms	THD_{16} = 1 % 07, CC, SCART
Max. input voltage	V_8	2			%	THD_{15} = 3 % 07, CC, SCART
Distortion	THD_{19}	0	0.01	0.1	%	V_3 = 250 mVrms
Distortion	THD_{20}		0.01	0.1	%	V_1 = 250 mVrms
Distortion	THD_{19}		0.01	0.1	%	V_3 = 250 mVrms; 03,15 *Vol*$_{KH}$ *21*
Distortion	THD_{20}		0.01	0.1	%	V_1 = 250 mVrms; 03,15 *Vol*$_{KH}$ *21*
Analog values are valid for feed-in at the pin 6, 7, 8; $V_{7,8}$ = 2 Vrms; V_6 = 250 mVrms						
Distortion	THD_{16}		0.01	0.1	%	V_1 = 250 mVrms
Distortion	THD_{15}		0.01	0.1	%	V_3 = 250 mVrms
Distortion	THD_{16}		0.01	0.2	%	V_1 = 250 mVrms; 01 2F-02,2F *Vol* $_{LSl}$ *47-Vol* $_{LSr}$ *47*
Distortion	THD_{15}		0.01	0.2	%	V_3 = 250 mVrms; 01 2F-02,2F *Vol* $_{LSl}$ *47-Vol* $_{LSr}$ *47*
Distortion	THD_{16}		0.01	0.4	%	V_1 = 250 mVrms; 05,XX *any sound*
Distortion	THD_{15}		0.01	0.4	%	V_3 = 250 mVrms; 05,XX *any sound*
Analog values are valid for feed-in at the pin 6, 7, 8; $V_{7,8}$ = 2 Vrms; V_6 = 250 mVrms						
Distortion	THD_{10}		0.01	0.1	%	V_3 = 250 mVrms
Distortion	THD_9		0.01	0.1	%	V_1 = 250 mVrms
Distortion	THD_{10}		0.01	0.1	%	V_6 = 250 mVrms 07,C9, Standard L
Distortion	THD_9		0.01	0.1	%	V_1 = 250 mVrms 07,C9, Standard L
Antiphase Cross talk atten. Base width	ΔV_{16-15}	0.5	0.55			 V_3 = 600 mVrms f_l = 2 kHz; 00,11, *Basis width*

Characteristics (cont'd)
V_S = 12 V; T_A = 25 ^{o}C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Antiphase Cross talk atten. Base width	$\Delta V_{16\text{-}15}$	0.5	0.55			 V_3 = 600 mVrms f_l = 2 kHz; 00,11, *Basis width*
Base width phase	$\Phi_{16\text{-}15}$	150	180	210	deg	V_1 = 600 mVrms; 00,11 *Basis width*, f = 2 kHz
Base width phase	$\Phi_{15\text{-}16}$	150	180	210	deg	V_1 = 600 mVrms; 00,11 *Basis width*, f = 2 kHz
Phase rotation quasi stereo	$\Phi_{16\text{-}15}$	0	10	40	deg	$V_{3,1}$ = 600 mVrms; 00,21 *Quasi stereo*, f = 40 Hz
Phase rotation quasi stereo	$\Phi_{16\text{-}15}$	130	180	230	deg	$V_{3,1}$ = 600 mVrms; 00,21 *Quasi stereo*, f = 1 kHz
Phase rotation quasi stereo	$\Phi_{16\text{-}15}$	– 30	10	0	deg	$V_{3,1}$ = 600 mVrms; 00,21 *Quasi stereo*, f = 15 kHz
Unweighted signal-to-noise ratio	$\alpha_{S / N16}$	1	90	97	dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms
Unweighted signal-to-noise ratio	$\alpha_{S / N15}$	1	90	97	dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0.6 Vrms
Unweighted signal-to-noise ratio	$\alpha_{S / N16}$	70	80		dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms 01,27-02,27 *Vol* $_{LSl}$ *39-Vol* $_{LSr}$ *39*
Unweighted signal-to-noise ratio	$\alpha_{S / N15}$	70	80		dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0.6 Vrms 01,27-02,27 *Vol* $_{LSl}$ *39-Vol* $_{LSr}$ *39*
External voltage	V_{N15}		2	10	µVrms	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$ 01,00-02,00 *Vol* $_{LSl}$ *0-Vol* $_{LSr}$ *0*
External voltage	V_{N16}		2	10	µVrms	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$ 01,00-02,00 *Vol* $_{LSl}$ *0-Vol* $_{LSr}$ *0*

Characteristics (cont'd)

V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Unweighted signal-to-noise ratio	$\alpha_{S/N20}$	90	97		dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms
Unweighted signal-to-noise ratio	$\alpha_{S/N19}$	1	90	97	dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0.6 Vrms
Unweighted signal-to-noise ratio	$\alpha_{S/N20}$	70	80		dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms 03,10, *Vol* $_{KH}$ *16*
Unweighted signal-to-noise ratio	$\alpha_{S/N19}$	70	80		dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0.6 Vrms 03,10, *Vol* $_{KH}$ *16*
External voltage	V_{N20}		2	10	µVrms	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; 03,00 *Vol* $_{KH}$ *0*
External voltage	V_{N19}		2	10	µVrms	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; 03,00 *Vol* $_{KH}$ *0*
Unweighted signal-to-noise ratio	$\alpha_{S/N9}$	1	90	97	dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms
Unweighted signal-to-noise ratio	$\alpha_{S/N10}$	1	90	97	dB	$V_{N\ rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0.6 Vrms
Change of DC-switch Δ1 Bit	ΔV_{16}			± 10	mV	01,X-01,X ± 1 *Vol* $_{LSl}$ *X-Vol* $_{LSl}$ *(X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{15}			± 10	mV	02,X-02,X ± 1 *Vol* $_{LSr}$ *X-Vol* $_{LSr}$ *(X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{16}			± 10	mV	05,X-05,X ± 1 *Sound X-Sound (X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{15}			± 10	mV	05,X-05,X ± 1 *Sound X-Sound (X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{19}			± 10	mV	03,X-03,X ± 1 *Vol* $_{KH}$*X-Vol* $_{KH}$ *(X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{20}			± 10	mV	03,X-03,X ± 1 *Vol* $_{KH}$*X-Vol* $_{KH}$ *(X ± 1)*

Characteristics (cont'd)

V_S = 12 V; T_A = 25 ^oC, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Design-Related Data						
Input resistance	R_7	35			kΩ	
Input resistance	R_8	35			kΩ	
Input resistance	R_6	20			kΩ	
Input resistance	R_3	20			kΩ	
Input resistance	R_1	20			kΩ	
Output resistance	R_{19}			200	Ω	
Output resistance	R_{20}			200	Ω	
Output resistance	R_{15}			200	Ω	
Output resistance	R_{16}			200	Ω	
Output resistance	R_9			200	Ω	
Output resistance	R_{10}			200	Ω	

Characteristics (cont'd)

V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
ID-Signal Decoder							
Gain Filter OP-amp	V_5	13	14	15	dB	V_{IF} = 80 mVpp	1
Max. input voltage	V_5	600			mVpp	Function	2
VCO voltage PLL	V_{27}	1.3			V	f_{24} = 14.6 kHz; V_{24} = 2.5 V	2
VCO voltage PLL	V_{27}	2	3	4	V	f_{24} = 15.625 kHz; V_{24} = 2.5 V	2
VCO voltage PLL	V_{27}			4.7	V	f_{24} = 16.6 kHz; V_{24} = 2.5 V	2
VCO voltage PLL	V_{27}	1.3			V	f_{24} = 58.4 kHz; V_{24} = 2.5 V 00,09, *H-Imp*	2
VCO voltage PLL	V_{27}			4.7	V	f_{24} = 66.4 kHz; V_{24} = 2.5 V 00,09, *H-Imp*	2

$$V_{KT\ FILTER} = \frac{\sqrt{(V_{25} - V_{25}^*)^2 + (V_{26} - V_{26}^*)^2}}{V_5}$$

V_{25} or V_{26} when V_5 = 0
V_{25}* or V_{26}* when V_5 = 400 mVpp

ID-filter gain	$V_{KT\ Filter}$	3.4		6.8		f_5 = Pilot signal: dual I²C-talk: dual	
ID-filter gain	$V_{KT\ Filter}$	3.4		6.8		f_5 = Pilot signal: stereo I²C-talk: stereo	

$V_{25\ test} = V_{25}\ (V_5 = 0) \pm \Delta V_{25}$; $V_{26\ test} = V_{26}\ (V_5 = 0) \pm \Delta V_{26}$

Detection threshold	ΔV_{25}	900			mV	I²C-talk: stereo or dual	3
Detection threshold	$-\Delta V_{25}$	900			mV	I²C-talk: stereo or dual	3
Detection threshold	ΔV_{26}	900			mV	I²C-talk: stereo or dual	3
Detection threshold	$-\Delta V_{26}$	900			mV	I²C-talk: stereo or dual	3

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

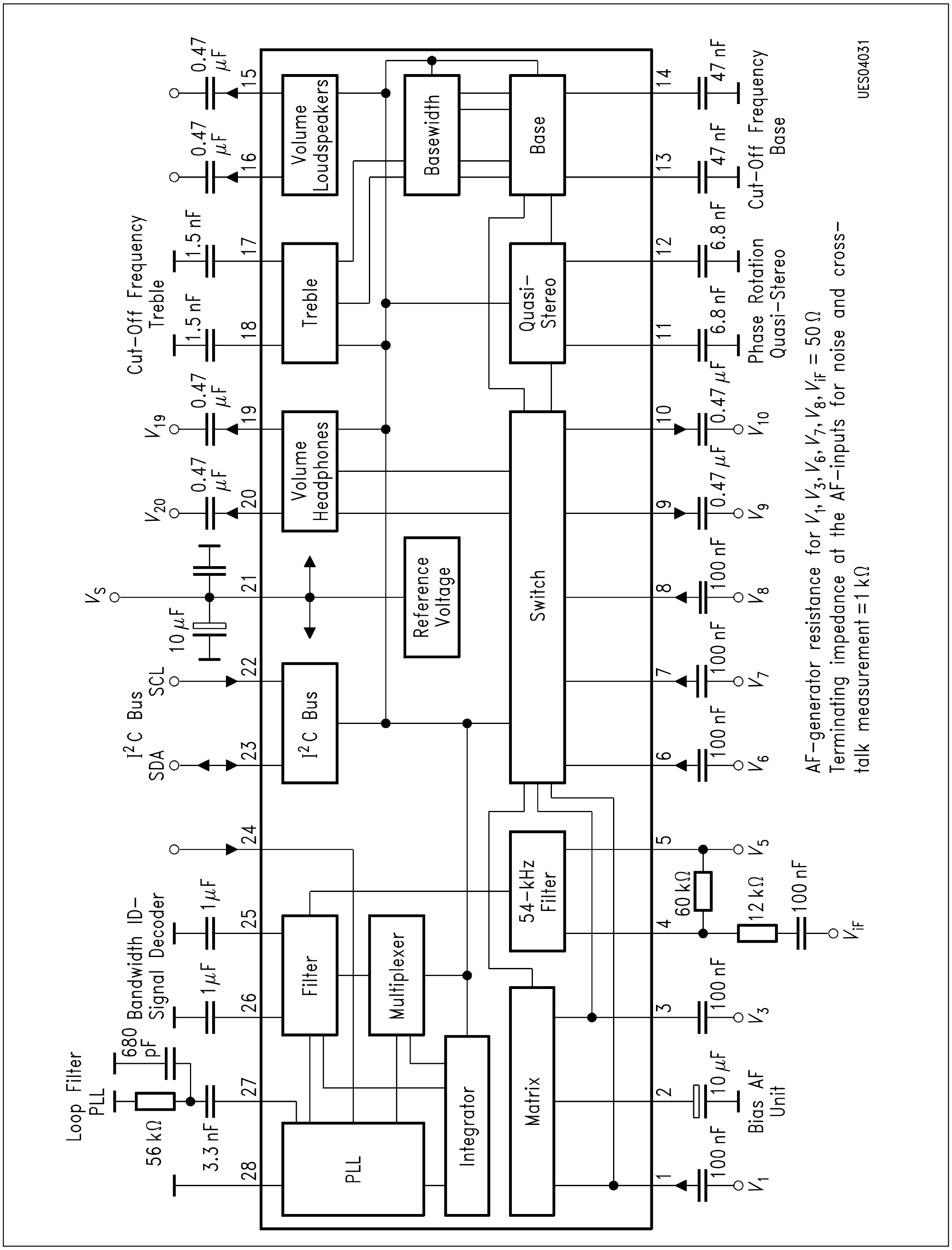
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Mono threshold	ΔV_{25}	0		100	mV	I^2C-talk: mono	3
Mono threshold	$- \Delta V_{25}$	0		100	mV	I^2C-talk: mono	3
Mono threshold	ΔV_{26}	0		100	mV	I^2C-talk: mono	3
Mono threshold	$- \Delta V_{26}$	0		100	mV	I^2C-talk: mono	3
Detection response	t_{det}	1/4		1/2	t_{MPX}	I^2C-talk: stereo or dual $\pm \Delta V_{25}$ = 1 V	3
Detection response	t_{det}	1/4		1/2	t_{MPX}	I^2C-talk: stereo or dual $\pm \Delta V_{25}$ = 1 V	3
Switching threshold f_{REF}-input	V_{24L}	0		1.5	V		2
Switching threshold f_{REF}-input	V_{24L}	3.5		V_{21}	V		2
Multiplexer clock	t_{MPX}		1.08		s	00,C0, *MPX = 1 s*	
Multiplexer clock	t_{MPX}		2.17		s	00,C0, *MPX = 2 s*	
Multiplexer clock	t_{MPX}		4.34		s	00,C0, *MPX = 4 s*	
Multiplexer clock	t_{MPX}		8.68		s	00,C0, *MPX = 8 s*	

Design-Related Data

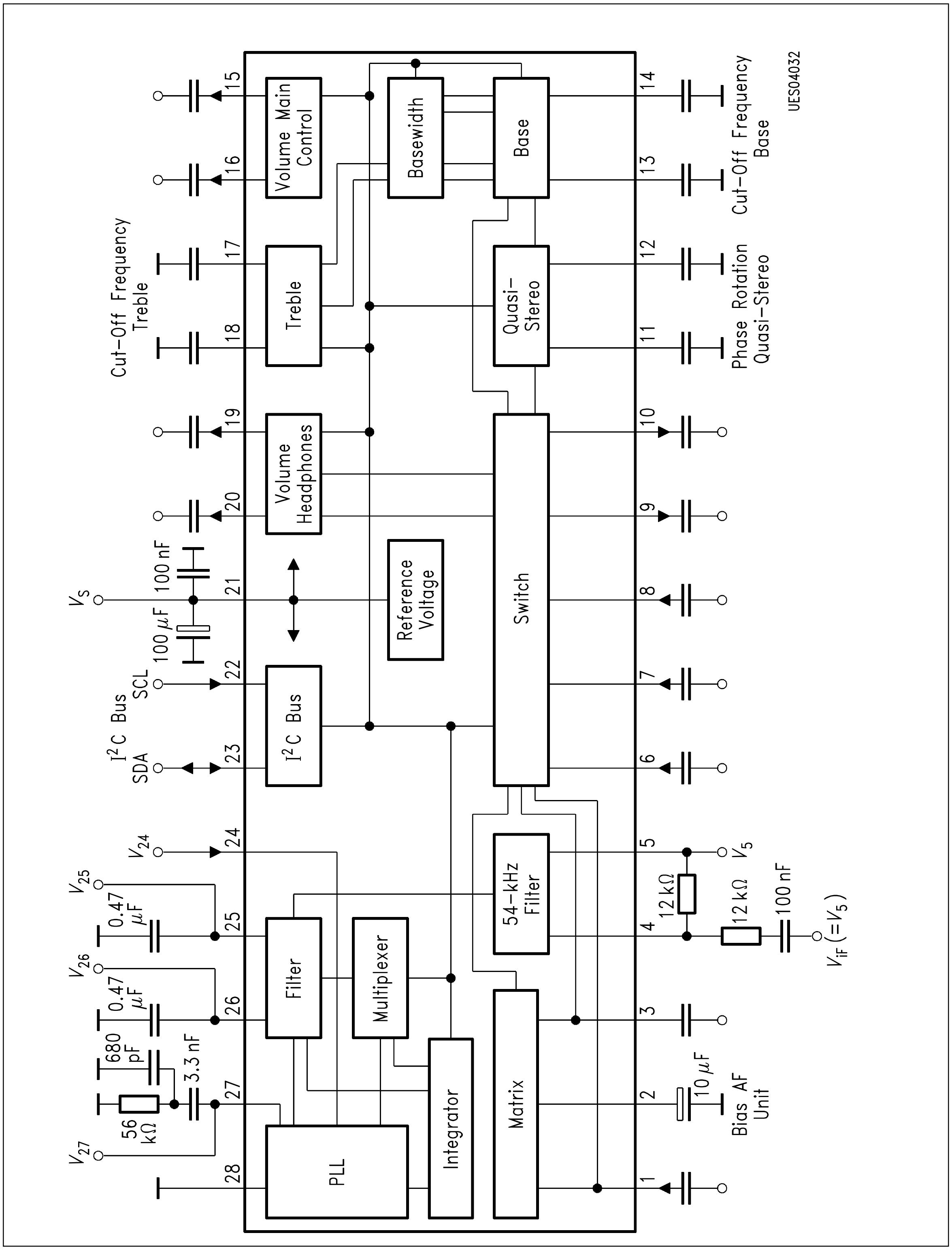
Filter output resistance	$R_{25, 26}$	110			kΩ		
f_{REF}-input resistance	R_{24}	7			kΩ		

Characteristics
V_S = 12 V; T_A = 25 ^oC

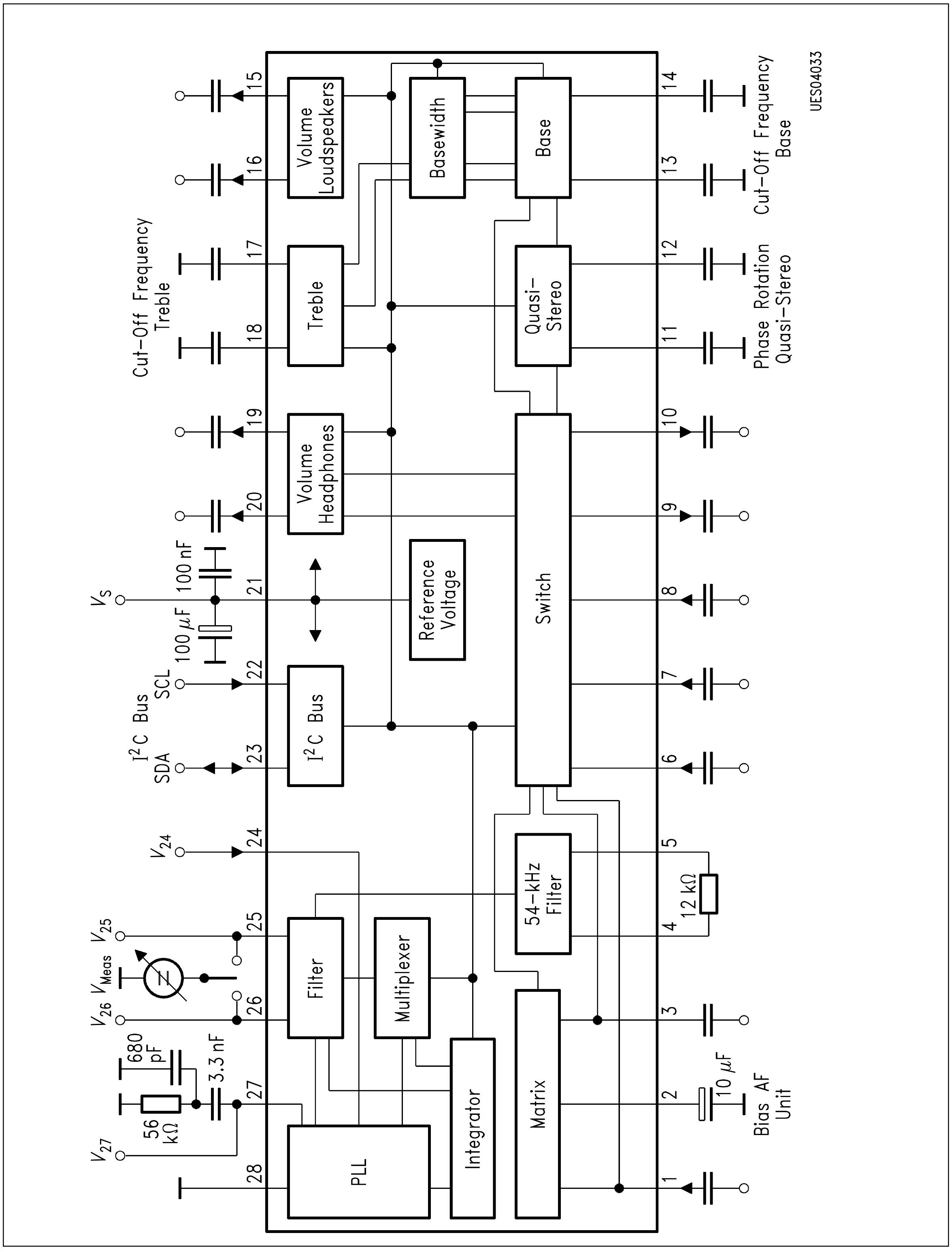
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
I²C Bus (SCL, SDA)					
SCL, SDA edges					
Rise time	t_R			1	µs
Fall time	t_F			300	ns
Shift register clock pulse SCL					
Frequency	f_{SCL}	0		100	kHz
H-pulse width	t_{HIGH}	4			µs
L-pulse width	t_{LOW}	4			µs
Start					
Setup time	t_{SUSTA}	4			µs
Hold time	t_{HDSTA}	4			µs
Stop					
Setup time	t_{SUSTO}	4			µs
Bus free time	t_{BUF}	4			µs
Data transfer					
Setup time	t_{SUDAT}	1			µs
Hold time	t_{HDDAT}	1			µs
Input SCL, SDA					
Input voltage	V_{QH}	2.4		5.5	V
	V_{QL}			1	V
Input current	I_{QH}			20	µA
	I_{QL}			20	µA
Output SDA (open collector)					
Output voltage	V_{QH}	5.4			V
R_L = 2.5 kΩ	V_{QL}			0.4	V
I_{QL} = 3 mA					



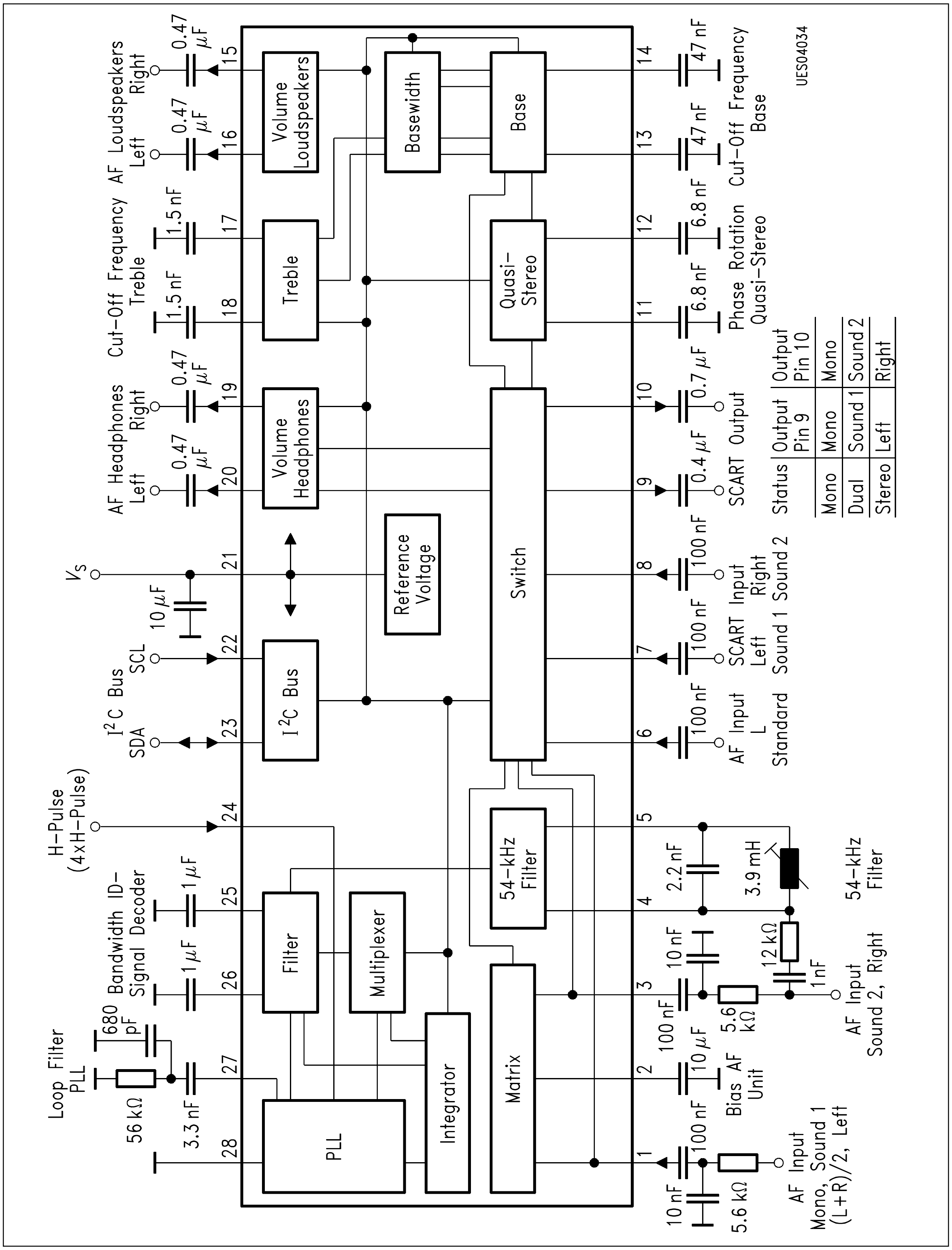
Test Circuit 1



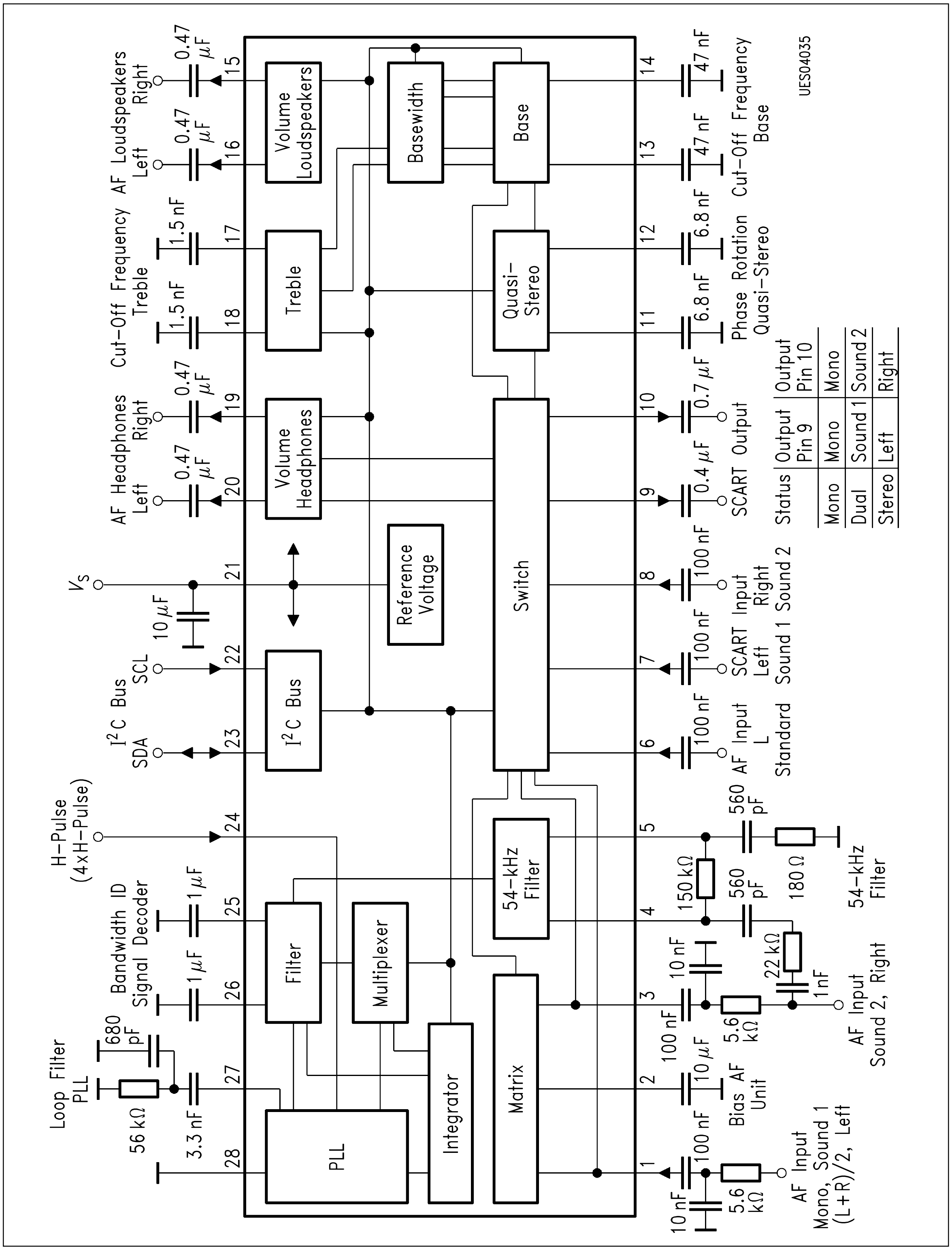
Test Circuit 2



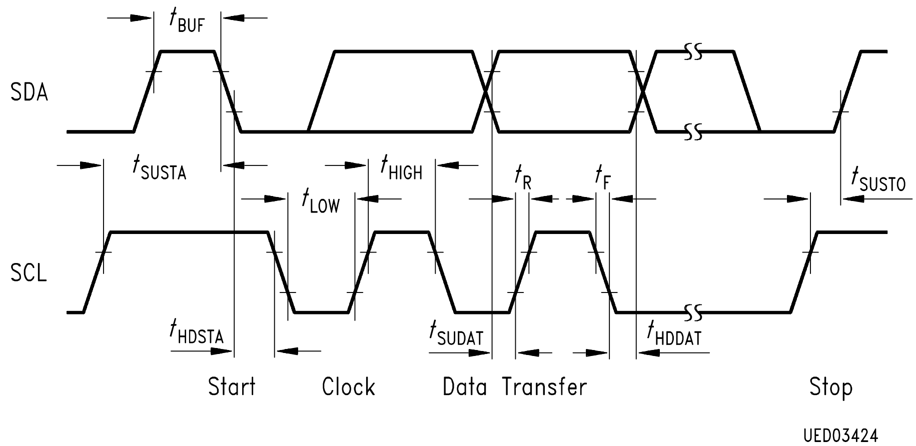
Test Circuit 3



Application Circuit 1



Application Circuit 2



I[2]C Bus Timing Diagram

t_{SUSTA}	Setup time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	H-pulse width (clock)
t_{LOW}	L-pulse width (clock)
t_{SUDAT}	Setup time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Setup time (stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

All times referred to V_{IH} and V_{IL} values.