

# **LM6142QML**

# 17 MHz Rail-to-Rail Input-Output Operational Amplifiers

# **General Description**

Using patented new circuit topologies, the LM6142 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of 2.7V to over 24V, the LM6142 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with 650µA/Amplifier supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.

## **Features**

At  $V_S = 5V$ . Typ unless noted.

- Rail-to-rail input CMVR -0.25V to 5.25V
- Rail-to-rail output swing 0.005V to 4.995V
- Wide gain-bandwidth: 17MHz (typ)
- Slew rate:

Small signal, 5V/µs Large signal, 30V/µs

- Low supply current 650µA/Amplifier
- Wide supply range 2.8V to 24V
- CMRR 107dB
- Gain 108dB with R<sub>I</sub> = 10k
- PSRR 87dB

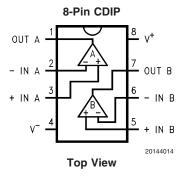
## **Applications**

- Battery operated instrumentation
- Portable sonar
- Barcode scanners
- Wireless communications
- Rail-to-rail in-out instrumentation amps

## **Ordering Information**

NS Part Number	JAN Part Number	NS Package Number	Package Description
LM6142AMJ-QML	5962-9550301QPA	J08A	8LD CERDIP

# **Connection Diagram**



# **Absolute Maximum Ratings** (Note 1)

Differential Input Voltage 15V

Voltage at Input/Output Pin  $(V^+) + 0.3V$ ,  $(V^-) - 0.3V$ 

Supply Voltage (V<sup>+</sup> – V<sup>-</sup>) 35VCurrent at Input Pin  $\pm 10 \text{mA}$ Current at Output Pin (Note 4)  $\pm 25 \text{mA}$ Current at Power Supply Pin 50 mALead Temperature (soldering, 10 sec)  $260 ^{\circ}\text{C}$ 

Storage Temp. Range  $-65^{\circ}C \le T_{A} \le +150^{\circ}C$ 

Maximum Junction Temperature (T<sub>Jmax</sub>)(Note 2) 150°C

Thermal Resistance

 $\theta_{\mathsf{JA}}$ 

 $\begin{array}{ccc} \text{still Air} & 125^{\circ}\text{C/W} \\ 500\text{LF / Min Air Flow} & 63^{\circ}\text{C/W} \\ \theta_{\text{JC}} & 12^{\circ}\text{C/W} \\ \text{ESD Tolerance (Note 3)} & 3\text{KV} \end{array}$ 

# Recommended Operating Conditions(Note 1)

Supply Voltage  $2.8 \text{V} \leq 24 \text{V}$  Operating Temperature Range  $-55 \, ^{\circ}\text{C} \leq T_{\text{A}} \leq +125 \, ^{\circ}\text{C}$ 

# **Quality Conformance Inspection**

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

# **5.0V Electrical Characteristics**

## **DC Parameters**

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V+ = 5.0V, V^ = 0V, V  $_{CM}$  = V  $_{O}$  = V+/2 and R  $_{L} \geq 100 K \Omega$  to V+/2

Symbol	Parameter	Conditions	Notes	Min	Max	μnit	Sub- group
V <sub>IO</sub>	Input Offset Voltage				1.0	mV	1
					2.5	mV	2, 3
I <sub>IB</sub>	Input Bias Current	t Bias Current $0V \le V_{CM} \le 5V$		280	nA	1	
					526	nA	2, 3
I <sub>IO</sub>	Input Offset Current				30	nA	1
					80	nA	2, 3
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 4V$		84		dB	1
				78		dB	2, 3
		$0V \le V_{CM} \le 5V$		66		dB	1
				64		dB	2, 3
PSRR Power Supply R	Power Supply Rejection Ratio	Supply Rejection Ratio 5V ≤ V+ ≤ 24V		80		dB	1
				78		dB	2, 3
V <sub>CM</sub>	Input Common-Mode Voltage Range		(Note 5)	0	5.0	V	1, 2, 3
A <sub>V</sub>	Large Signal Voltage Gain	$R_L = 10K\Omega$		100		V/mV	4
				33		V/mV	5, 6
V <sub>O</sub>	Output Swing	R <sub>L</sub> = 100KΩ		4.98	0.01	V	4
				4.93	0.014	V	5, 6
	Output Swing	$R_L = 2K\Omega$		4.86	0.1	V	4
				4.77	0.133	V	5
				4.8	0.133	V	6
I <sub>sc</sub>	Output Short Circuit Current	Sourcing		10		mA	1
				2.0	35	mA	2, 3
		Sinking		10		mA	1
				4.0	35	mA	2, 3
Is	Supply Current	Per Amplifier			800	μΑ	1
					880	μΑ	2, 3

## **AC Parameters**

The following conditions apply to all the following parameters, unless otherwise specified.

AC: V+ = 5.0V, V- = 0V, V\_{CM} = V\_O = V+/2 and  $R_L \geq 100 K\Omega$  to V+/2

Symbol	Parameter	Conditions	Notes	Min	Max	μnit	Sub- group
+SR	Slew Rate	$-4V \le V_1 \le +4V$ ,		15		V/µS	4
		$+V_{CC} = 6V, -V_{CC} - 6V,$		9.5		V/µS	5
		$R_S = 1K\Omega$ , $R_L = 2K\Omega$ $C_O = 0F$		11		V/µS	6
-SR	Slew Rate	$+4V \ge V_1 \ge -4V$ ,		15		V/µS	4
		$+V_{CC} = 6V, -V_{CC} - 6V,$		9.5		V/µS	5
		$R_S = 1K\Omega$ , $R_L = 2K\Omega$ $C_O = 0F$		11		V/µS	6
GBW	Gain-Bandwidth Product	f = 50Khz		10		MHz	4
				6.0		MHz	5, 6

# 2.8V Electrical Characteristics

## **DC Parameters**

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V+ = 2.8V, V^ = 0V, V\_{CM} = V\_O = V+/2 and R\_L  $\geq$  100K $\Omega$  to V+/2

Symbol	Parameter	Conditions	Notes	Min	Max	μnit	Sub- group
V <sub>IO</sub>	Input Offset Voltage				1.8	mV	1
					4.3	mV	2, 3
I <sub>IB</sub>	Input Bias Current				250	nA	1
					526	nA	2, 3
I <sub>IO</sub>	Input Offset Current				30	nA	1
					80	nA	2, 3
CMRR Common Mode Rejection Ratio	0V ≤ V <sub>CM</sub> ≤ 1.9V		72		dB	1	
				63		dB	2, 3
		0V ≤ V <sub>CM</sub> ≤ 2.8V		62		dB	1
				58		dB	2, 3
PSRR	Power Supply Rejection Ratio	3V ≤ V <sup>+</sup> ≤ 5V		72		dB	1
				58		dB	2, 3
V <sub>CM</sub>	Input Common-Mode Voltage Range		(Note 5)	0.0	2.8	V	1, 2, 3
A <sub>V</sub>	Large Signal Voltage Gain	$R_L = 100K\Omega, V_O = \pm 1.1V$		10		V/mV	4
				1.5		V/mV	5, 6
V <sub>O</sub>	Output Swing	$R_L = 100 \text{K}\Omega$		2.76	0.08	V	4
				2.35	0.112	V	5, 6
Is	Supply Current	Per Amplifier			800	μΑ	1
					880	μΑ	2, 3

# **AC Parameters**

The following conditions apply to all the following parameters, unless otherwise specified.

AC:  $V^+$  = 2.8V,  $V^-$  = 0V,  $V_{CM}$  =  $V_O$  =  $V^+/2$  and  $R_L \ge 100 K\Omega to~V^+/2$ 

Symbol	Parameter	Conditions	Notes	Min	Max	μnit	Sub- group
GBW	Gain-Bandwidth Product	f = 50KHz		3		MHz	4
				1.5		MHz	5, 6

## 24V Electrical Characteristics

#### **DC Parameters**

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V+ = 24V, V- = 0V, V\_{CM} = V\_O = V+/2 and  $R_L \geq 100 K\Omega$  to V+/2

Symbol	Parameter	Conditions	Notes	Min	Max	μnit	Sub- group
V <sub>IO</sub>	Input Offset Voltage				2.0	mV	1
					4.8	mV	2, 3
Vo	Output Swing	$R_L = 10K\Omega$		23.81	0.15	V	4
				23.62	0.185	V	5, 6
I <sub>S</sub>	Supply Current	Per Amplifier			1100	μΑ	1
					1150	μΑ	2, 3

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{Jmax}$  (maximum junction temperature),  $\theta_{JA}$  (package junction to ambient thermal resistance), and  $T_A$  (ambient temperature). The maximum allowable power dissipation at any temperature is  $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$  or the number given in the Absolute Maximum Ratings, whichever is lower.

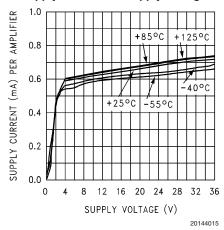
Note 3: Human body model,  $1.5k\Omega$  in series with 100pF.

Note 4: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

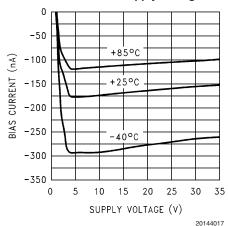
Note 5: Input common-mode voltage range is guaranteed by CMRR.

# Typical Performance Characteristics $T_A = 25^{\circ}C$ , $R_L = 10 \text{ k}\Omega$ Unless Otherwise Specified

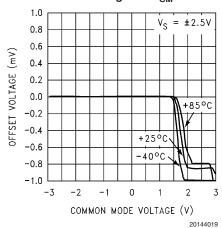
#### Supply Current vs. Supply Voltage



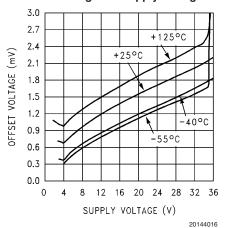
### Bias Current vs. Supply Voltage



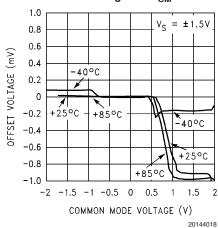
## Offset Voltage vs. $V_{\rm CM}$



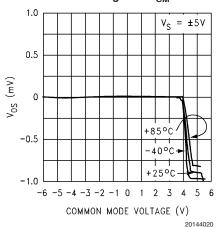
#### Offset Voltage vs. Supply Voltage



#### Offset Voltage vs. V<sub>CM</sub>

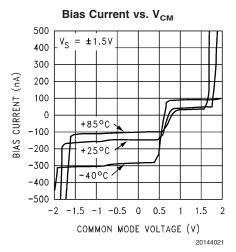


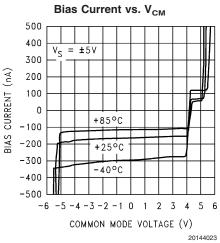
#### Offset Voltage vs. V<sub>CM</sub>

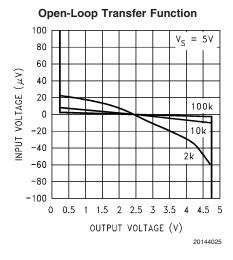


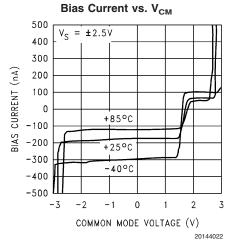
# Typical Performance Characteristics $T_A$ = 25°C, $R_L$ = 10 $k\Omega$ Unless Otherwise

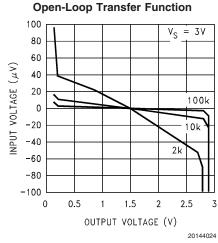
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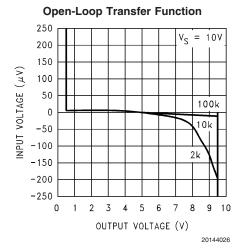








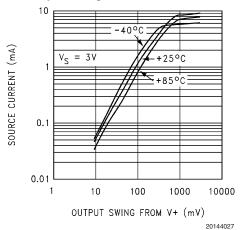




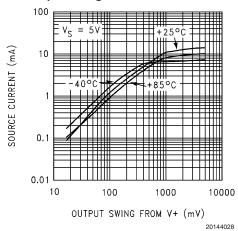
# Typical Performance Characteristics $T_A = 25^{\circ}C$ , $R_L = 10 \text{ k}\Omega$ Unless Otherwise

Specified (Continued)

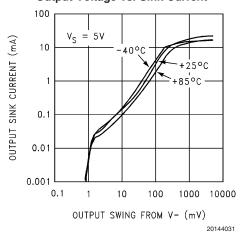
#### **Output Voltage vs. Source Current**



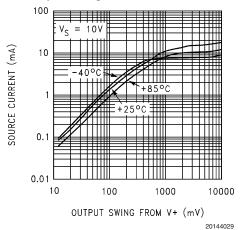
#### **Output Voltage vs. Source Current**



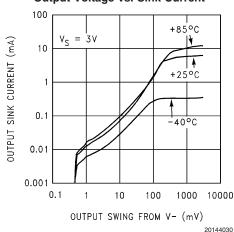
#### Output Voltage vs. Sink Current



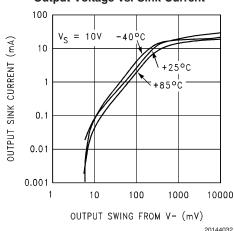
#### **Output Voltage vs. Source Current**



## Output Voltage vs. Sink Current

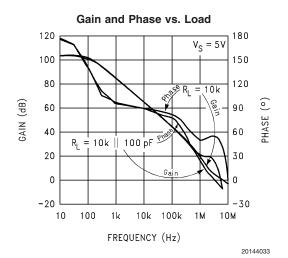


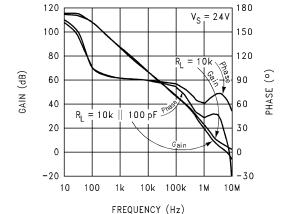
## Output Voltage vs. Sink Current



# Typical Performance Characteristics $T_A$ = 25°C, $R_L$ = 10 $k\Omega$ Unless Otherwise

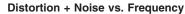
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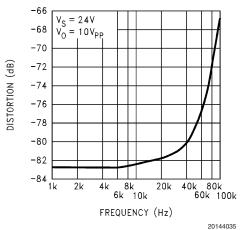


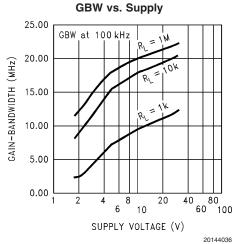


Gain and Phase vs. Load

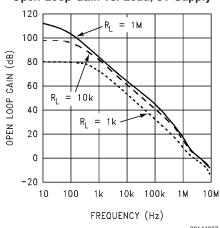
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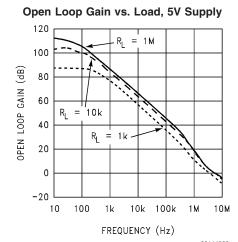






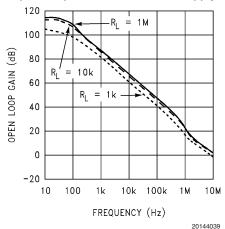
### Open Loop Gain vs. Load, 3V Supply



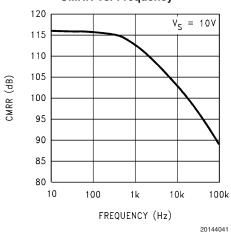


# **Typical Performance Characteristics** $T_A = 25^{\circ}C$ , $R_L = 10 \text{ k}\Omega$ Unless Otherwise Specified (Continued)

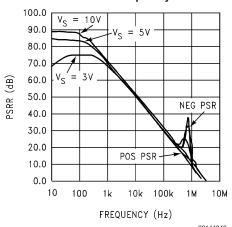
#### Open Loop Gain vs. Load, 24V Supply



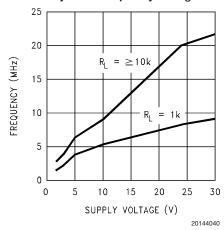
#### CMRR vs. Frequency



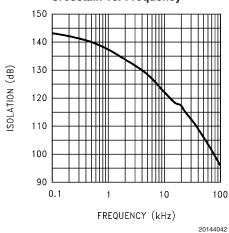
### PSRR vs. Frequency



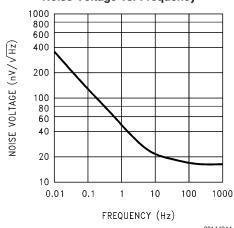
## Unity Gain Frequency vs. $V_{\rm S}$



#### Crosstalk vs. Frequency



#### Noise Voltage vs. Frequency

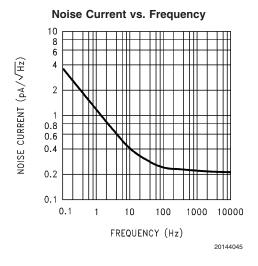


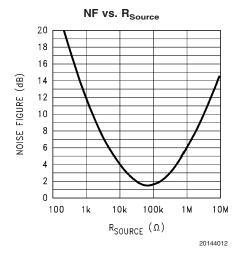
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## **Typical Performance Characteristics** $T_A = 25^{\circ}C$ , $R_L = 10 \text{ k}\Omega$ Unless Otherwise

Specified (Continued)





# LM6142 Application Ideas

The LM6142 brings a new level of ease of use to op amp system design.

With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption, previously reduced battery life to unacceptable levels.

To take advantage of these features, some ideas should be kept in mind.

#### **ENHANCED SLEW RATE**

Unlike most bipolar op amps, the unique phase reversal prevention/speed-up circuit in the input stage causes the slew rate to be very much a function of the input signal amplitude.

Figure 2 shows how excess input signal, is routed around the input collector-base junctions, directly to the current mirrors.

The LM6142 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1–Q2, Q3–Q4 when the input levels are normal.

If the input signal exceeds the slew rate of the input stage, the differential input voltage rises above two diode drops. This excess signal bypasses the normal input transistors, (Q1-Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.

This rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See *Figure 1*.)

As the overdrive increases, the op amp reacts better than a conventional op amp. Large fast pulses will raise the slew-rate to around 30V to  $60V/\mu s$ .

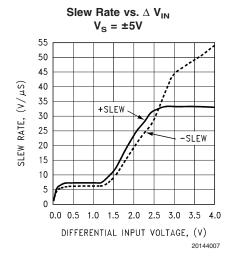


FIGURE 1.

This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large.

This new input circuit also eliminates the phase reversal seen in many op amps when they are overdriven.

This speed-up action adds stability to the system when driving large capacitive loads.

#### **DRIVING CAPACITIVE LOADS**

Capacitive loads decrease the phase margin of all op amps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most op amps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6142, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.

# LM6142 Application Ideas (Continued)

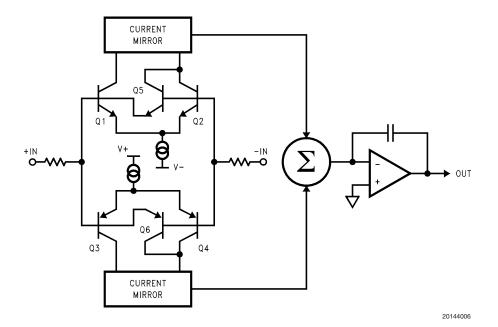


FIGURE 2.

These features allow the LM6142 to drive capacitive loads as large as 1000pF at unity gain and not oscillate. The scope photos (Figure 3 and Figure 4) above show the LM6142 driving a l000pF load. In Figure 3, the upper trace is with no capacitive load and the lower trace is with a 1000pF load. Here we are operating on  $\pm 12$ V supplies with a 20  $V_{PP}$  pulse. Excellent response is obtained with a  $C_f$  of l0pF. In Figure 4, the supplies have been reduced to  $\pm 2.5$ V, the pulse is 4  $V_{PP}$  and  $C_f$  is 39pF. The best value for the compensation capacitor is best established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.

Another effect that is common to all op amps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.

The circuit shown in *Figure 5* was used for these scope photos.

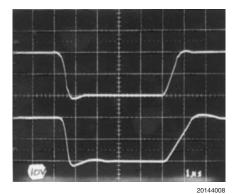


FIGURE 3.

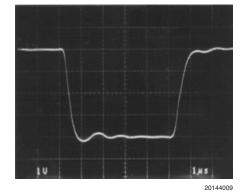


FIGURE 4.

## LM6142 Application Ideas (Continued)

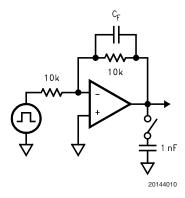


FIGURE 5.

## **Typical Applications**

#### **ANALOG TO DIGITAL CONVERTER BUFFER**

The high capacitive load driving ability, rail-to-rail input and output range with the excellent CMR of 82 dB, make the LM6142a good choice for buffering the inputs of A to D converters.

# 3 OP AMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using two LM6142 amplifiers, a 3 op amp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these preci-

sion resistors reduces the CMR as well. Using two LM6142 amplifiers, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage (*Figure 6*). These buffers assure that the input impedance is over  $100M\Omega$  and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.

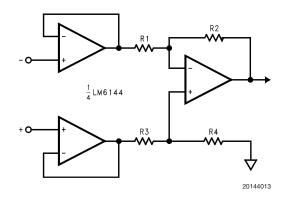


FIGURE 6.

The gain is set by the ratio of R2/R1 and R3 should equal R1 and R4 equal R2. Making R4 slightly smaller than R2 and adding a trim pot equal to twice the difference between R2 and R4 will allow the CMR to be adjusted for optimum.

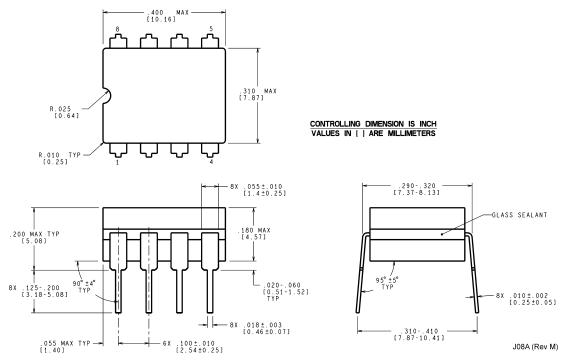
With both rail to rail input and output ranges, the inputs and outputs are only limited by the supply voltages. Remember that even with rail-to-rail output, the output can not swing past the supplies so the combined common mode voltage plus the signal should not be greater than the supplies or limiting will occur.

#### SPICE MACROMODEL

A SPICE macromodel of this and many other National Semiconductor op amps is available at no charge from the NSC Customer Response Group at 800-272-9959.

Date Released	Revision	Section	Originator	Changes
1/08/05	A	New release to the corporate format	L. Lytle	1 MDS datasheet converted into standard corporate format. MNLM6142-X Rev 4A1 to be archived.

# Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Cerdip Dual-In-Line Package NS Package Number J08A

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at www.national.com.

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National Semiconductor Americas Customer Support Center

Email: new.feedback@nsc.com Tel: 1-800-272-9959

www.national.com

National Semiconductor Europe Customer Support Center Fax: +49 (0) 180-530 85 86

Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center Email: ap.support@nsc.com National Semiconductor Japan Customer Support Center Fax: 81-3-5639-7507 Email: jpn.feedback@nsc.com Tel: 81-3-5639-7560