100 MHz to 9 GHz 60 dB TruPwr™ Detector

Preliminary Technical Data

ADL5902

FEATURES

Accurate RMS-to-DC conversion from 100 MHz to 9 GHz
Single ended input dynamic range of 60 dB
No balun or external input tuning required
Waveform and modulation independent, such as GSM/CDMA/WCDMA/TD-SCDMA/WiMAX/LTE
Linear-in-decibels output, scaled 50 mV/dB
Temperature stability of <±0.3 dB
All functions temperature and supply stable
Operates from 4.5 V to 5.5 V from −40°C to +125°C
Power-down capability
Small footprint, 4 mm x 4 mm, LFCSP
Pin-compatible with the AD8363 TruPwr™ Detector

APPLICATIONS

Power amplifier linearization/control loops
Transmitter power controls
Transmitter signal strength indication (TSSI)
RF instrumentation

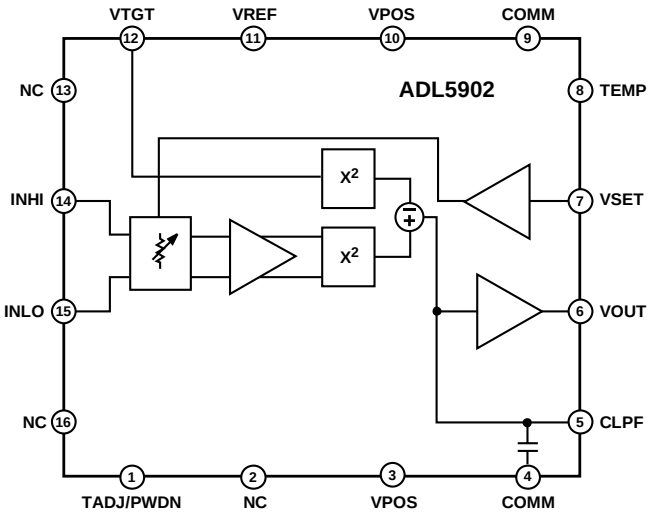

Figure 1 FUNCTIONAL BLOCK DIAGRAM.

GENERAL DESCRIPTION

The ADL5902 is a true RMS responding power detector that has a 60 dB measurement range when driven with a single-ended 50 Ω source. This feature makes the ADL5902 extremely frequency versatile by eliminating the need for a balun, or any other form of external input tuning, for operation up to 9 GHz.

The ADL5902 provides a solution in a variety of high frequency communication systems and in instrumentation requiring an accurate response to signal power. Requiring only a single supply of 5 V and a few capacitors, it is easy to use and capable of being driven single-ended or with a balun (for differential input drive). The ADL5902 can operate from less than 100 MHz to 9 GHz and can accept inputs that have RMS values from 1 mV to at least 1 V, with large crest factors, exceeding the requirements for accurate measurement of WiMAX, CDMA, WCDMA, TD-SCDMA, multi-carrier GSM, and LTE signals.

The ADL5902 can determine the true power of a high frequency signal having a complex low frequency modulation envelope, or as a simple low frequency RMS voltmeter.

Used as a power measurement device, VOUT is connected to VSET. The output is then proportional to the logarithm of the RMS value of the input. In other words, the reading is presented directly in decibels and is conveniently scaled 50 mV/dB; other slopes are easily arranged. In controller modes, the voltage applied to VSET determines the power level required at the input to null the deviation from the set point. The output buffer can provide high load currents.

The ADL5902 has a typical operating current of 65 mA at 25°C. It is supplied in a 4 mm x 4 mm 16-lead LFCSP for operation over the temperature range of −40°C to +125°C. A fully populated RoHS-compliant evaluation board is also available.

Rev. PrD

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SPECIFICATIONS

V_S = 5 V, T = 25°C, Z_O = 50 Ω, Single ended input drive, VOUT tied to VSET, Error referred to best-fit line (linear regression), unless otherwise noted. VTGT = 1V, two point calibration at-42 dBm and -2 dBm

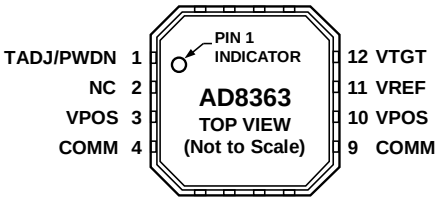
Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range			100-9000		MHz
RF INPUT INTERFACE	INHI (Pin 14), INLO (Pin 15), ac-coupled				
Input Impedance	Single-ended drive		2/TBD		KΩ/pF
Common Mode Voltage			TBD		V
900 MHz					
Output Voltage: High Power in	P_{IN} = 0 dBm		3.17		V
Output Voltage: Low Power in	P_{IN} = -50 dBm		0.58		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C,		55		dB
±2.0 dB Dynamic Range	CW input, T_A = +25°C,		60		dB
Maximum Input Level, ±1.0 dB			4		dB
Minimum Input Level, ±1.0 dB			-51		dB
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; TADJ = 0.5 V, P_{IN} = -5 dBm		±0.3		dB
	-40°C < T_A < +85°C; TADJ = 0.5 V, P_{IN} = -40 dBm		±0.3		dB
Logarithmic Slope			50		mV/dB
Logarithmic Intercept			-60		dBm
Deviation from CW Response	13 dB peak-to-RMS ratio (WCDMA)		±0.1		dB
	12 dB peak-to-RMS ratio (WiMAX)		±0.1		dB
	14.0 dB peak-to-RMS ratio (16C CDMA2K)		±0.1		dB
	8 dB peak-to-RMS ratio 256 QAM		±0.1		dB
Input Impedance	Single-ended drive		2/TBD		KΩ/pF
1900 MHz					
Output Voltage: High Power in	P_{IN} = 0 dBm		3.10		V
Output Voltage: Low Power in	P_{IN} = -45 dBm		0.80		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C,		57		dB
±2.0 dB Dynamic Range	CW input, T_A = +25°C,		61		dB
Maximum Input Level, ±1.0 dB			6		dB
Minimum Input Level, ±1.0 dB			-51		dB
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; TADJ = 0.5 V, P_{IN} = 0 dBm		±0.3		dB
	-40°C < T_A < +85°C; TADJ = 0.5 V, P_{IN} = -35 dBm		±0.3		dB
Logarithmic Slope			51		mV/dB
Logarithmic Intercept			-60		dBm
Deviation from CW Response	13 dB peak-to-RMS ratio (WCDMA)		±0.1		dB
	12 dB peak-to-RMS ratio (WiMAX)		±0.1		dB
	14.0 dB peak-to-RMS ratio (16C CDMA2K)		±0.1		dB
	8 dB peak-to-RMS ratio 256 QAM		±0.1		dB
2350 MHz					
Output Voltage: High Power in	P_{IN} = -5 dBm		2.78		V
Output Voltage: Low Power in	P_{IN} = -45 dBm		0.79		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C,		57		dB
±2.0 dB Dynamic Range	CW input, T_A = +25°C,		62		dB
Maximum Input Level, ±1.0 dB			7		dB
Minimum Input Level, ±1.0 dB			-50		dB
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; TADJ = 0.5 V, P_{IN} = -5 dBm		±0.3		dB
	-40°C < T_A < +85°C; TADJ = 0.5 V, P_{IN} = -35 dBm		±0.3		dB
Logarithmic Slope			50		mV/dB

Parameter	Conditions	Min	Typ	Max	Unit
Logarithmic Intercept			-60		dBm
Deviation from CW Response	13 dB peak-to-RMS ratio (WCDMA)		±0.1		dB
	12 dB peak-to-RMS ratio (WiMAX)		±0.1		dB
	14.0 dB peak-to-RMS ratio (16C CDMA2K)		±0.1		dB
	8 dB peak-to-RMS ratio 256 QAM		±0.1		
4 GHz					
Output Voltage: High Power in	P_{IN} = 0 dBm		2.76		V
Output Voltage: Low Power in	P_{IN} = -45 dBm		0.69		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C,		57		dB
±2.0 dB Dynamic Range	CW input, T_A = +25°C,		60		dB
Maximum Input Level, ±1.0 dB			7		dB
Minimum Input Level, ±1.0 dB			-50		dB
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; TADJ = 0.3 V, P_{IN} = 0 dBm		±0.5		dB
	-40°C < T_A < +85°C; TADJ = 0.3 V, P_{IN} = -35 dBm		±0.5		dB
Logarithmic Slope			46		mV/dB
Logarithmic Intercept			-59		dBm
Deviation from CW Response	13 dB peak-to-RMS ratio (WCDMA)		±0.1		dB
	12 dB peak-to-RMS ratio (WiMAX)		±0.1		dB
	14.0 dB peak-to-RMS ratio (16C CDMA2K)		±0.1		dB
	8 dB peak-to-RMS ratio 256 QAM		±0.1		
6 GHz					
Output Voltage: High Power in	P_{IN} = -5 dBm		2.04		V
Output Voltage: Low Power in	P_{IN} = -45 dBm		0.43		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C,		52		dB
±2.0 dB Dynamic Range	CW input, T_A = +25°C,		58		dB
Maximum Input Level, ±1.0 dB			5		dB
Minimum Input Level, ±1.0 dB			47		dB
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; TADJ = 0.7 V, P_{IN} = -5 dBm		±0.5		dB
	-40°C < T_A < +85°C; TADJ = 0.7 V, P_{IN} = -35 dBm		±0.6		dB
Logarithmic Slope			40.6		mV/dB
Logarithmic Intercept			-55		dBm
Deviation from CW Response	13 dB peak-to-RMS ratio (WCDMA)		±0.1		dB
	12 dB peak-to-RMS ratio (WiMAX)		±0.1		dB
	14.0 dB peak-to-RMS ratio (16C CDMA2K)		±0.1		dB
	8 dB peak-to-RMS ratio 256 QAM		±0.1		
OUTPUT INTERFACE	VOUT (Pin 6)				
Output Swing, Controller Mode	Swing Range Min RL≥200 to ground		0.03		V
	Swing Range Max RL≥200 to ground		Vs – 0.15		V
	Source/Sink Current Out held at Vs/2K, to 1%change		10/10		mA
SETPOINT INPUT	VSET (Pin 7)				
Voltage Range	Log conformance error ≤1 dB Min @ 1900 MHz		0.52		V
	Log conformance error ≤1 dB Max@ 1900 MHz		3.46		V
Input Resistance			30		kΩ
Logarithmic Scale Factor	f = 2140 MHz, −40°C ≤ T_A ≤ +85°C		50		mV/dB
Logarithmic Intercept	f = 2140 MHz, −40°C ≤ T_A ≤ +85°C, referred to 50 Ω		-60		dBm
TEMPERATURE COMPENSATION	TADJ (Pin1)				
Input Voltage Range			0-2		V
Input Resistance			2		KΩ
VOLTAGE REFERENCE	VREF (Pin 11)				
Output Voltage	RF in = −55 dBm		2.3		V
Current Limit Source/Sink	1% change			4/0.1	mA
Voltage Regulation	I_{LOAD} = 3 mA		–0.6		%

Parameter	Conditions	Min	Typ	Max	Unit
TEMPERATURE REFERENCE	TEMP (Pin 8)				
Output Voltage	T_A = 25°C, $R_L \geq 10$ kΩ		1.4		V
Temperature Coefficient	−40°C ≤ T_A ≤ +85°C, $R_L \geq 10$ kΩ		5		mV/°C
Current Source/Sink	T_A = 25°C to 1% change			4/0.05	mA
Voltage Regulation	I_{LOAD} = 3 mA		−0.1		%
RMS TARGET INTERFACE	VTGT (Pin 12)				
Input Voltage Range		.2		2.5	V
Input Resistance			70		kΩ
POWER-DOWN INTERFACE	TADJ (Pin1)				
Logic Level to Enable	Logic LO enables Max		<3.8		V
Logic Level to Disable	Logic HI disables Min		>4.5		V
Input Current	Logic HI PWDN = 5 V		63		µA
	Logic LO PWDN = 0 V		63		µA
POWER SUPPLY INTERFACE	Pin VPOS (Pin 3, Pin 10)				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	25C RF in =-55 dBm		65		mA
	+85 C		74		
Power Down Current	When disabled		0.3		mA

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT

Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	TADJ/PWDN	This is a dual function pin used for controlling the amount of intercept temperature compensation at voltages <2.5 V and/or for shutting down the device at voltages >4 V. If the shutdown function is not used, this pin can be connected to the VREF pin through a voltage divider.
2, 13, 16	NC	No Connect.
3, 10	VPOS	Supply for the Device. Connect this pin to a 5 V power supply. Pin 3 and Pin 10 are not internally connected; therefore, both must connect to the source.
4, 9, 17	COMM	System Common Connection. Connect this pin via low impedance to system common. The exposed paddle is also COMM and should have both a good thermal and good electrical connection to ground.
5	CLPF	Connection for Loop Filter Integration (Averaging) Capacitor. Connect a ground-referenced capacitor to this pin. A resistor can be connected in series with this capacitor to improve loop stability and response time.
6	VOUT	Output Pin in Measurement Mode (Error Amplifier Output). In measurement mode, this pin is normally connected directly to VSET. This pin can be used to drive a gain control when the device is used in controller mode.
7	VSET	The voltage applied to this pin sets the decibel value of the required RF input voltage that results in zero current flow in the loop integrating capacitor pin, CLPF. This pin controls the variable gain amplifier (VGA) gain such that a 50 mV change in VSET reduces the gain by approximately 1 dB.
8	TEMP	Temperature Sensor Output.
11	VREF	General-Purpose Reference Voltage Output of 2.3 V.
12	VTGT	The voltage applied to this pin determines the target power at the input of the RF squaring circuit. The intercept voltage is proportional to the voltage applied to this pin. The use of a lower target voltage increases the crest factor capacity; however, this may affect the system loop response. This is nominally set to 1V.
14	INHI	This is a RF input pin. For a 50 ohm input impedance, use a 60.4 ohm resistor to ground. There must be a series (DC block) capacitor between the pin and the 60.4 ohm termination resistor. If using INLO as RF input, place a DC block capacitor on INHI to ground.
15	INLO	This is a RF input pin. For a 50 ohm input impedance, use a 60.4 ohm resistor to ground. There must be a series (DC block) capacitor between the pin and the 60.4 ohm termination resistor. If using INHI as RF input, place a DC block capacitor on INLO to ground.
17 (EPAD)	Exposed Pad (EPAD)	The paddle should be connected to both a thermal and electrical ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, Z_O = 50 Ω, single-ended input drive, VOUT connected to VSET, VTGT = 1V, CLPF = 3.9 nF,, T_A = +25°C (black), −40°C (blue), +85°C (red), where appropriate. Error referred to best-fit line (linear regression), unless otherwise indicated. Input RF signal is a sine wave unless otherwise indicated.

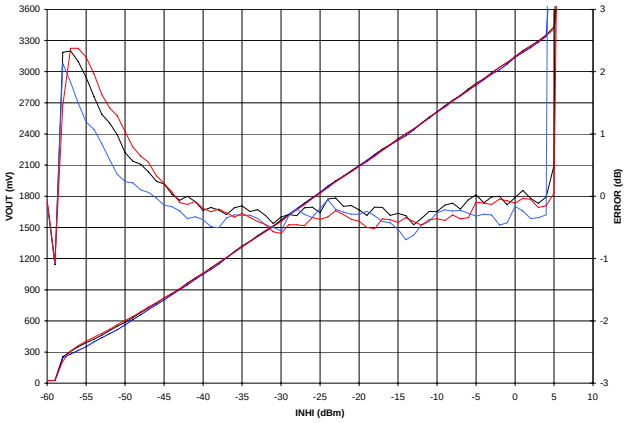


Figure 3. VOUT Voltage and Log Conformance Error vs. Input Amplitude at 900 MHz, Typical Device, TADJ =0.5V

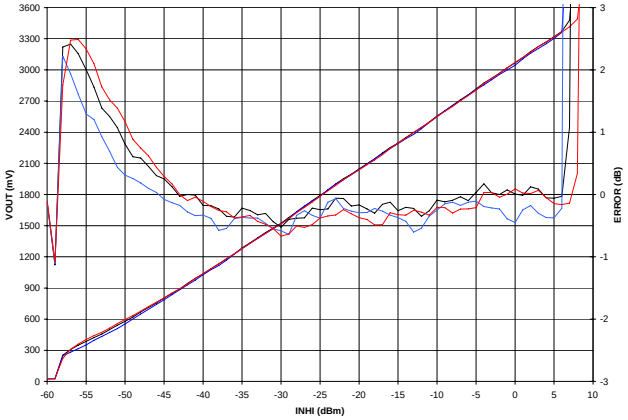


Figure 4. VOUT Voltage and Log Conformance Error vs. Input Amplitude at 1900 MHz, Typical Device, TADJ =0.5V

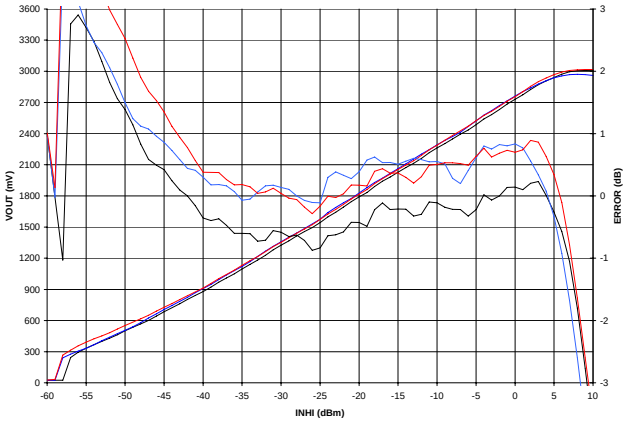


Figure 5. VOUT Voltage and Log Conformance Error vs. Input Amplitude at 4000 MHz, Typical Device, TADJ =0.3V

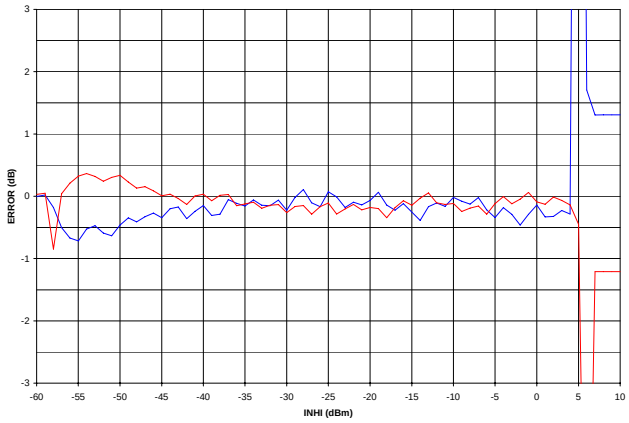


Figure 6. Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency = 900 MHz, Typical Device, TADJ =0.5V

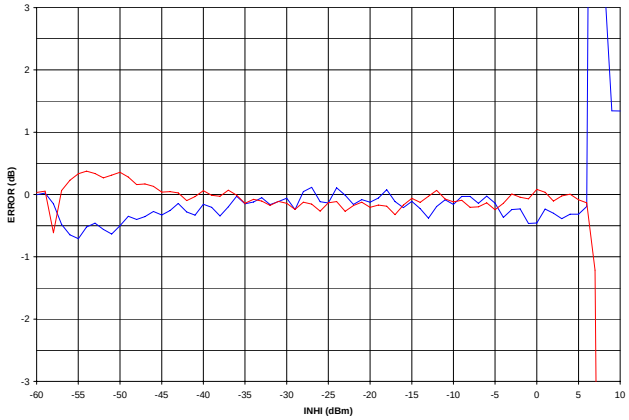


Figure 7. Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency =1 900 MHz, Typical Device, TADJ =0.5V

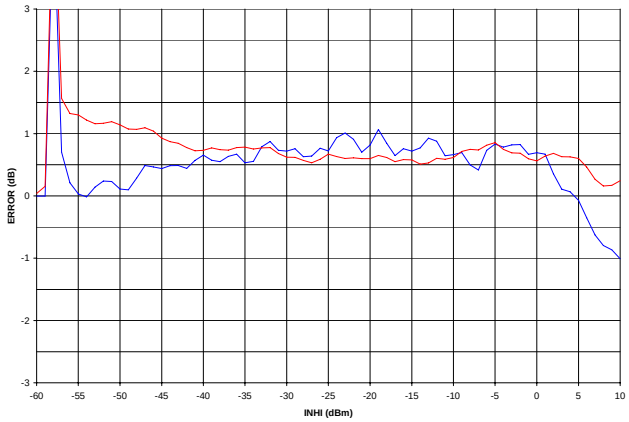


Figure 8. Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency =4000 MHz, Typical Device, TADJ =0.3V

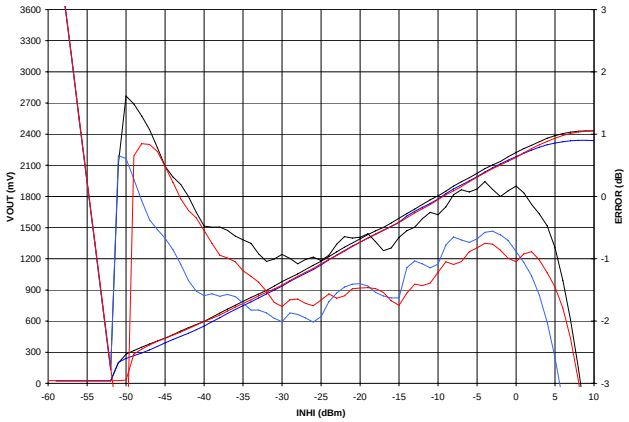


Figure 9. VOUT Voltage and Log Conformance Error vs. Input Amplitude at 6000 MHz, Typical Device, TADJ =0.7V

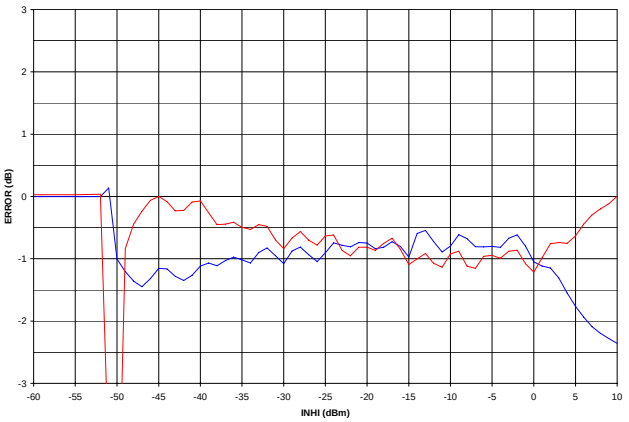


Figure 12. . Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency =6000 MHz, Typical Device, TADJ =0.7V

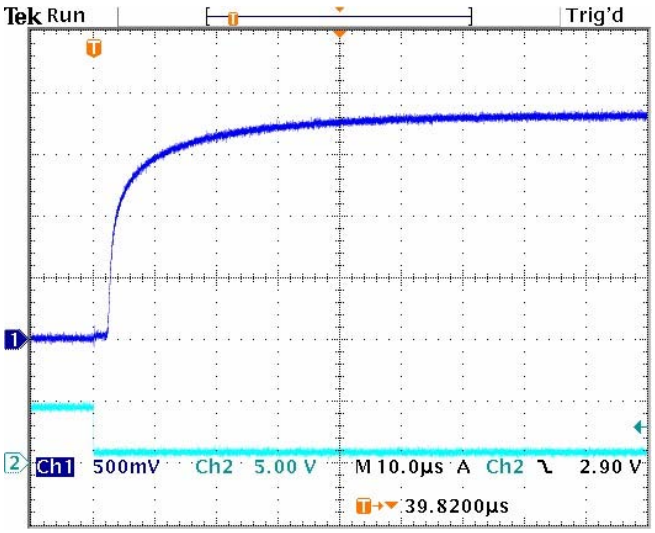


Figure 10. Output Response to enable pulse for RF Input Level of -30 dBm, Carrier Frequency 900 MHz, CLPF = 3.9 nF

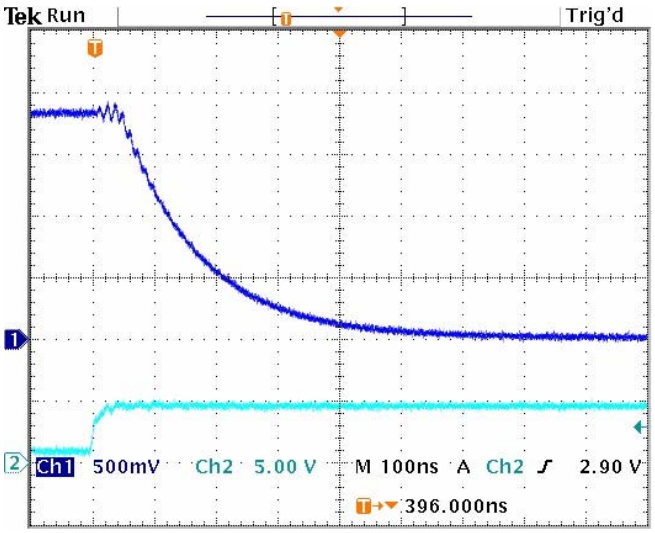


Figure 13. Output Response to shutdown pulse for RF Input Level of -30 dBm, Carrier Frequency 900 MHz, CLPF = 3.9 nF

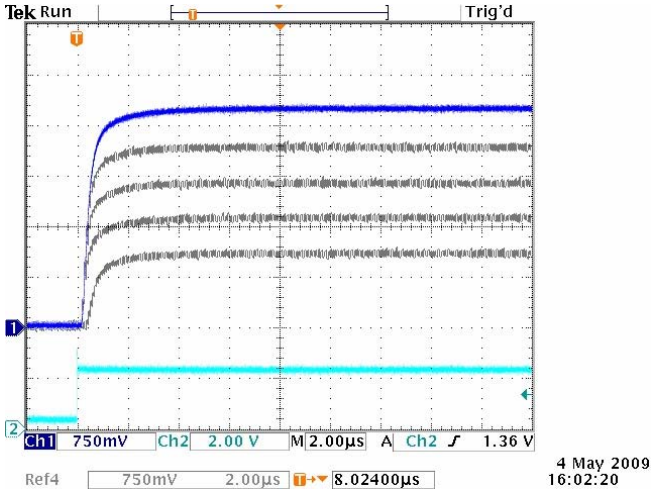


Figure 11. Output Response to RF Burst Input for RF Input Levels of –40 dBm, –30 dBm, –20 dBm, –10 dBm, and 0 dBm, Carrier Frequency 900 MHz, CLPF = 470 pF

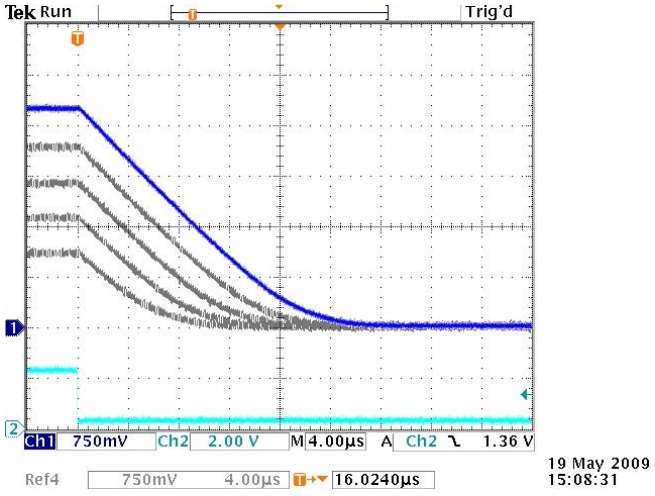


Figure 14. Output Response to RF Burst Input for RF Input Levels of –40 dBm, –30 dBm, –20 dBm, –10 dBm, and 0 dBm, Carrier Frequency 900 MHz, CLPF = 470 pF

EVALUATION AND CHARACTERIZATION CIRCUIT BOARD LAYOUTS

Figure 15 to Figure 19 show the evaluation board for the ADL5902.

Table 3. Bill of Materials

Component	Function/Notes	Default Value
C6, C10, C11, C12, R3	Input. The ADL5902 is single ended driven from either INHI or INLO. When driving INHI, populate C10 and C12 with an appropriate capacitor value for the frequency of operation and leave C6 and C11 open. When driving INLO, populate C6 and C11 with an appropriate capacitor value for the frequency of operation and leave C10 and C12 open. R3 is the input termination resistor and is chosen to give a 50 ohm input impedance over a broad frequency range.	C6 = open, C10=C12=0.1 µF C11 = open, R3 = 60.4 Ω,
R7, R8, R10, R11	VTGT. R10 and R11 are set up to provide 1V to VTGT from VREF. If R10 and R11 are removed, an external voltage can be used. Alternatively, R7 and R11 can be used to form a voltage divider for an external reference.	R7=R8=0 Ω, R10 = 953 Ω, R11 = 1.69 kΩ,
C4, C5, C7, C13, R14, R16	Power Supply Decoupling. The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the ADL5902, a 0 Ω series resistor, and a 0.1 µF capacitor placed close to the power supply input pin. The 0 Ω resistor can be replaced with a larger resistor to add more filtering; however, it is at the expense of a voltage drop.	C4 = C5 = 100 pF, C7 = C13 = 0.1µF, R14 = R16 = 0 Ω
R1, R2, R6, R13, R15	Output Interface (Default Configuration) in Measurement Mode. In this mode, a portion of the output voltage is fed back to the VSET pin via R6. Using the voltage divider created by R6 and R2, the magnitude of the slope at VOUT is increased by reducing the portion of VOUT that is fed back to VSET. If a fast responding output is expected, the 0 Ω resistor on R15 can be removed to reduce parasitics on the output. Output Interface in Controller Mode. In this mode, R6 must be open and R13 must have a 0 Ω resistor. In controller mode, the ADL5902 can control the gain of an external component. A set point voltage is applied to the VSET pin, the value of which corresponds to the desired RF input signal level applied to the ADL5902. If a fast responding output is expected, the 0 Ω resistor on R15 can be removed to reduce parasitics on the output.	R1= R6 = R15 = 0 Ω R2 = R13 = open,
C8, C9, R5	Low-Pass Filter Capacitors. The low-pass filter capacitors reduce the noise on the output and affect the pulse response time of the ADL5902. This capacitor should be as large as possible.	C8 = open, C9 = 0.1 µF, R5 = 0 Ω
R9, R12	TADJ/PWDN. The TADJ/PWDN pin controls the amount of intercept temperature compensation and/or shuts down the device. The evaluation board is configured to control this from a test loop, but VREF can also be used with a voltage divider created by R9 and R12.	R9 = R12 = open
Paddle	The paddle should be tied to both a thermal and electrical ground	

EVALUATION BOARD ARTWORK AND SCHEMATICS

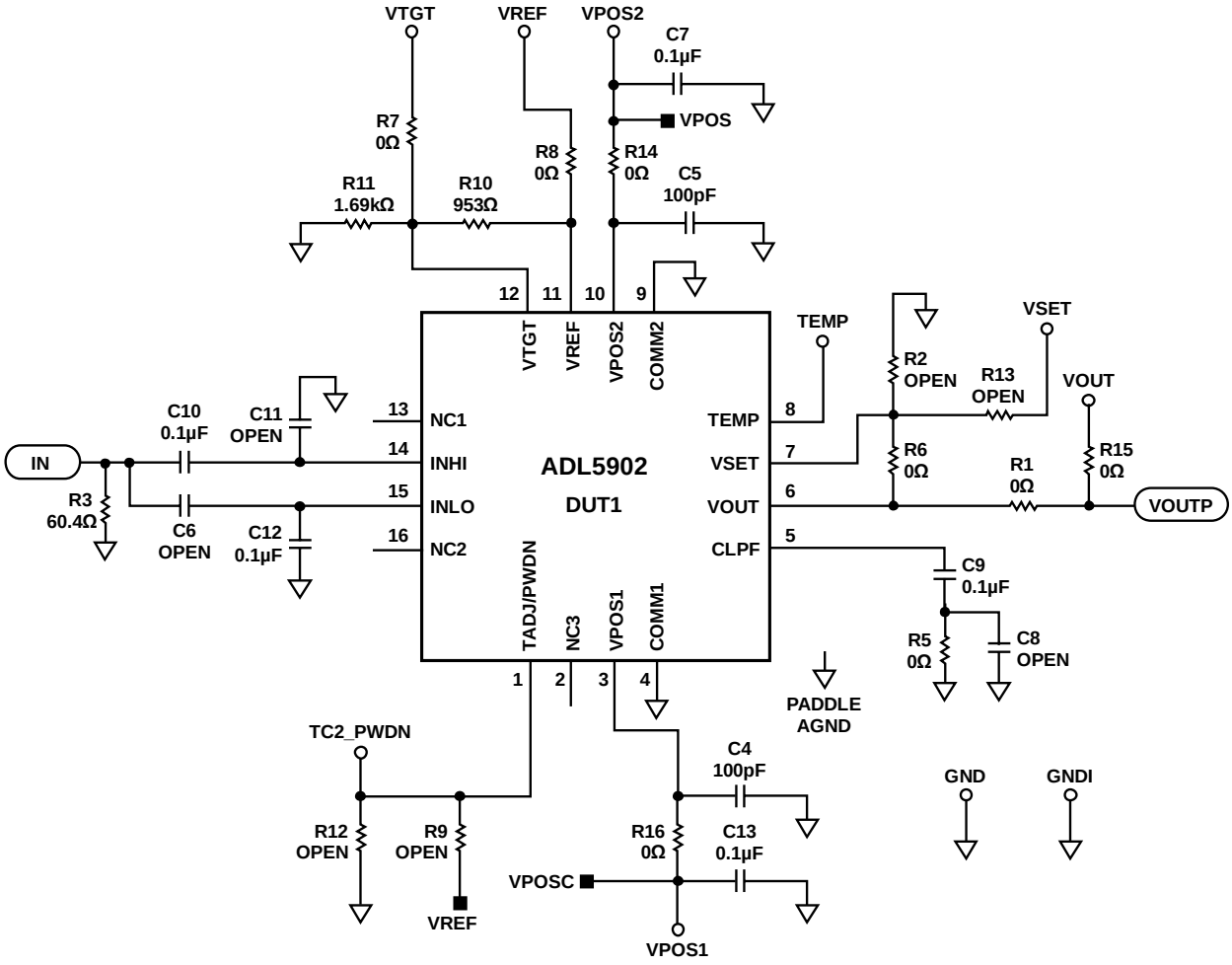


Figure 15. Evaluation Board Schematic

ASSEMBLY DRAWINGS

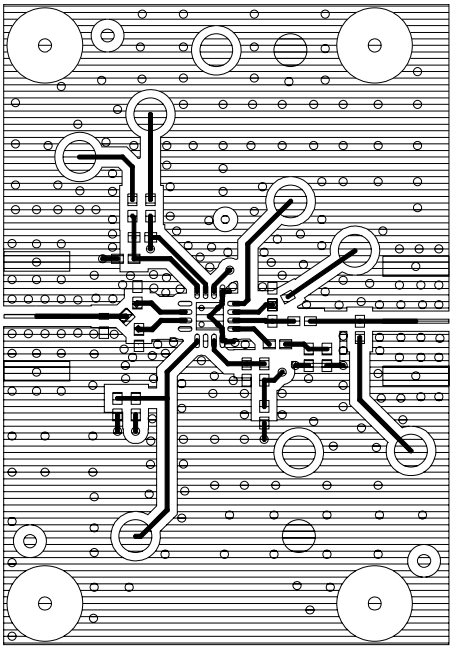


Figure 16. Evaluation Board Layout, Top Side

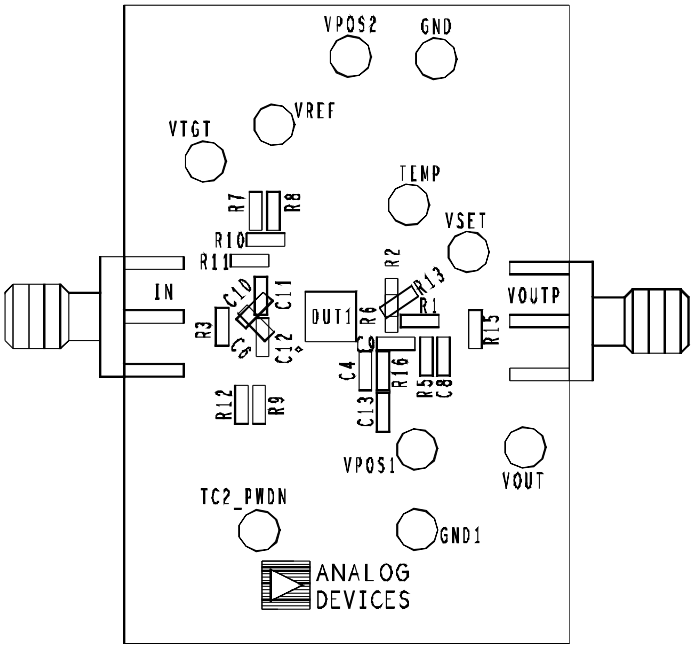


Figure 18. Evaluation Board Assembly, Top Side

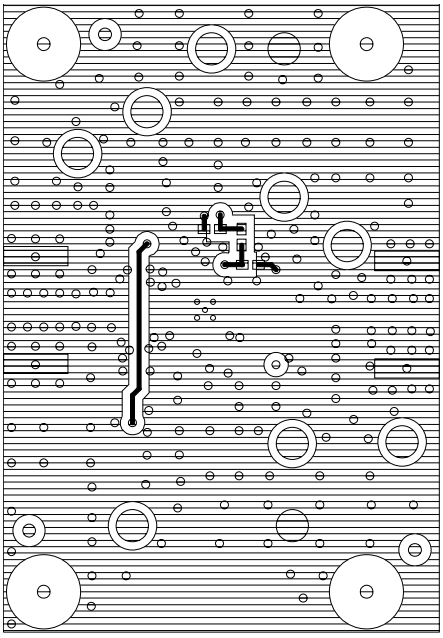


Figure 17. Evaluation Board Layout, Bottom Side

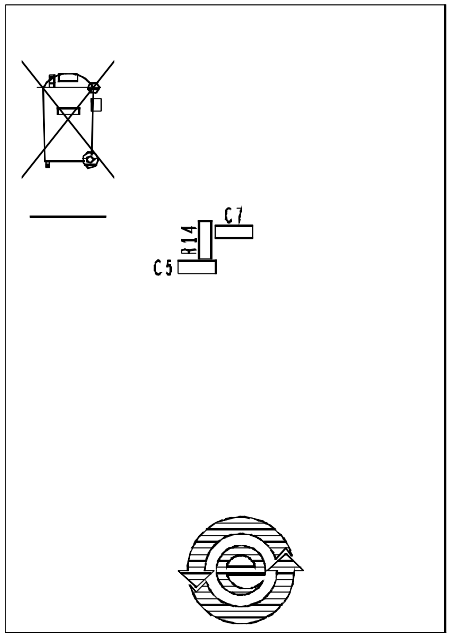


Figure 19. Evaluation Board Assembly, Bottom Side

OUTLINE DIMENSIONS

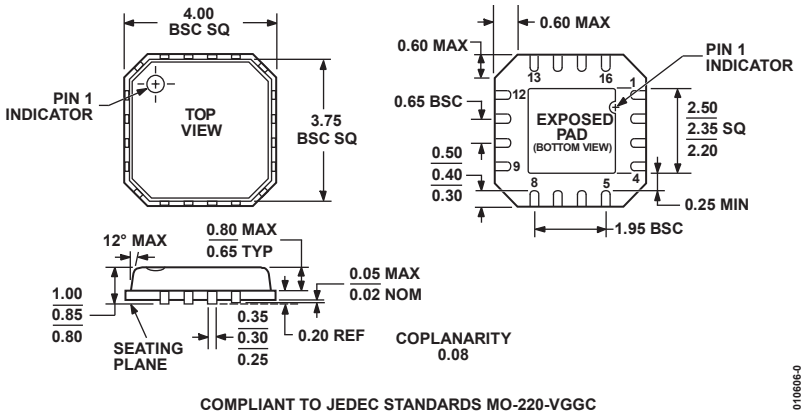


Figure 20. X-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
mm × mm Body, Very Thin Quad
(CP-16-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5902ACPZ-R7[1]	40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-10	1,500
ADL5902ACPZ-R2[1]	40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-10	250
ADL5902ACPZ-WP[1]	40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-10	64
ADL5902-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

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