DATA SHEET

Part No.	AN30181A
Package Code No.	HQFN024-P-0404

Contents

AN30181A

General-purpose power management LSI

■ Overview

AN30181A is a power management LSI which has step-down DC-DC converters (2-ch) that employs hysteretic control system.
By this system, when load current changes suddenly, it responds at high speed and minimizes the changes of output voltage.
Since it is possible to use capacitors with small capacitance and it is unnecessary to use parts for phase compensation, this IC realizes downsizing of set and reducing in the number of external parts.
Output voltages are 1.2 V and 1.8 V. Each maximum current is 0.8 A.
This LSI has a LDO circuit, external Pch-MOSFET gate drive circuits and a reset circuit of input power supply voltage.

■ Features

- High-speed response step-down DC-DC converter circuit that employs hysteretic control system : 2-ch (1.2 V, 0.8 A / 1.8 V, 0.8 A)
- LDO : 1-ch (0.9 V, 10 mA)
- Built-in external Pch MOSFET gate drive circuits
- Built-in Reset function
- Built-in Under Voltage Lockout function (UVLO)

■ Applications

- SSD (Solid State Drive), Portable phone, etc.

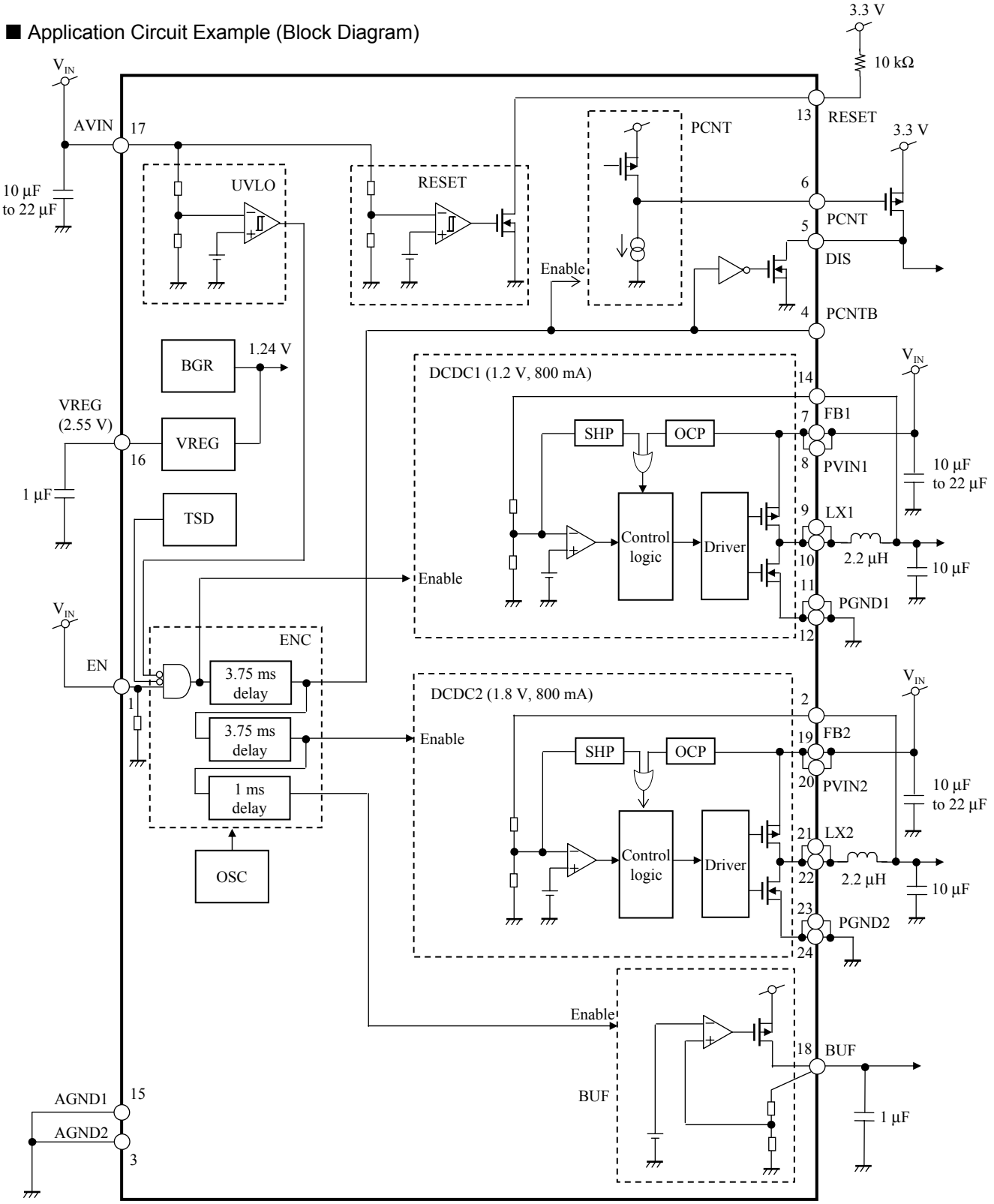
■ Package

- 24pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)
  (Size : 4 × 4 mm, 0.5 mm pitch)

■ Type

- Bi-CMOS IC

■ Application Circuit Example (Block Diagram)



Notes) • This application circuit is an example. The operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

• This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	EN	Input	ON/OFF control pin
2	FB2	Input	Feed Back pin (for 1.8 V DCDC)
3	AGND2	Ground	Ground pin
4	PCNTB	Output	External devices control output pin
5	DIS	Input	Discharge pin (open drain)
6	PCNT	Output	External Pch MOSFET gate control pin
7	PVIN1	Power supply	Power supply pin (for 1.2 V DCDC)
8	PVIN1	Power supply	Power supply pin (for 1.2 V DCDC)
9	LX1	Output	Driver output pin (for 1.2 V DCDC)
10	LX1	Output	Driver output pin (for 1.2 V DCDC)
11	PGND1	Ground	Ground pin (for 1.2 V DCDC)
12	PGND1	Ground	Ground pin (for 1.2 V DCDC)
13	RESET	Output	Reset output pin (open drain)
14	FB1	Input	Feed Back pin (for 1.2 V DCDC)
15	AGND1	Ground	Ground pin
16	VREG	Output	LDO output pin (Power supply for internal control circuit / 2.55 V)
17	AVIN	Power supply	Power supply pin
18	BUF	Output	LDO output pin (0.9 V)
19	PVIN2	Power supply	Power supply pin (for 1.8 V DCDC)
20	PVIN2	Power supply	Power supply pin (for 1.8V DCDC)
21	LX2	Output	Driver output pin (for 1.8 V DCDC)
22	LX2	Output	Driver output pin (for 1.8 V DCDC)
23	PGND2	Ground	Ground pin (for 1.8 V DCDC)
24	PGND2	Ground	Ground pin (for 1.8 V DCDC)

■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which do not result in damages to this IC, and IC operation is not guaranteed at these limit values.

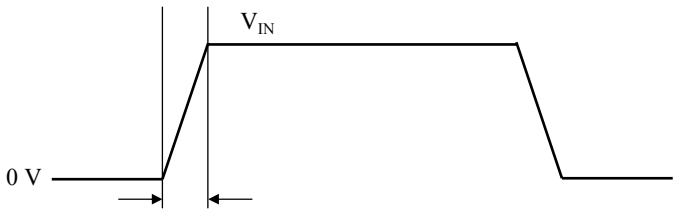
A No.	Parameter	Symbol	Rating	Unit	Notes
1	Supply voltage	V_{IN}	6.0	V	*1
2	Supply current	I_{IN}	—	A	—
3	Power dissipation	P_D	187.9	mW	*2
4	Operating ambient temperature	T_{opr}	–40 to +85	°C	*3
5	Storage temperature	T_{stg}	–55 to +150	°C	*3

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
V_{IN} is voltage for AVIN, PVIN1 and PVIN2.
*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) IC package without a heat sink.
When using this IC, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.
*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Notes
Supply voltage range	V_{IN}	2.9 to 5.5	V	*1 *2

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
V_{IN} is voltage for AVIN, PVIN1 and PVIN2.
*2 : Please set the rising time of power input pin to the following range.
In addition, please input the voltage with the rising time which has margin enough in consideration of the variation in external parts.



100 µs < Tr < 1.5 ms
(Tr is the rise time from 0 V to the setup voltage of V_{IN}.)

■ Allowable Current and Voltage Range

Notes)
- Allowable current and voltage ranges are limit ranges which do not result in damages to this IC, and IC operation is not guaranteed within these limit ranges.
- Voltage values, unless otherwise specified, are with respect to GND.
  GND is voltage for AGND1, AGND2, PGND1and PGND2. GND = AGND1 = AGND2 = PGND1 = PGND2.
- V_{IN} is voltage for AVIN, PVIN1 and PVIN2. AVIN = PVIN1 = PVIN2.
- Do not apply external currents or voltages to any pin not specifically mentioned.

Pin No.	Pin name	Rating	Unit	Notes
1	EN	−0.3 to (V_{IN} + 0.3)	V	*1

Note) *1 : (V_{IN} + 0.3) V must not be exceeded 6 V.

■ Electrical Characteristics at V_{IN} = 3.3 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Notes
				Min	Typ	Max		
[DCDC1] (1.2 V step-down DC-DC converter) C = 10 µF (Murata : GRM21BB31A106K), L = 2.2 µH (Taiyo Yuden : NR3012T2R2M) [DCDC2] (1.8 V step-down DC-DC converter) C = 10 µF (Murata : GRM21BB31A106K), L = 2.2 µH (Taiyo Yuden : NR3012T2R2M)								
1	Consumption current at active	IACT	EN = 3.3 V, I_{OUT1}, I_{OUT2}, $I_{OUT(BUF)}$ = 0 A	—	200	300	µA	—
2	EN pin Low-level input voltage	VENL	V_{IN} = 3.3 V	—	0	0.3	V	—
3	EN pin High-level input voltage	VENH	V_{IN} = 3.3 V	1.5	3.3	—	V	—
4	EN pin leak current	ILEAKEN	EN = 3.3 V	—	2.4	10	µA	—
5	DCDC1 output voltage	DD1VOUT	I_{OUT1} = 450 mA	1.176	1.200	1.224	V	—
6	DCDC2 output voltage	DD2VOUT	I_{OUT2} = 500 mA	1.764	1.800	1.836	V	—
7	UVLO start voltage	VUVLODET	V_{IN} = 3.3 V → 0 V	2.4	2.5	2.6	V	—
8	UVLO stop voltage	VUVLORMV	V_{IN} = 0 V → 3.3 V	2.45	2.6	2.8	V	—
9	Reset detection voltage	VRSTDET	V_{IN} = 3.3 V → 0 V	2.740	2.810	2.880	V	—
10	Reset cancel voltage	VRSTRMV	V_{IN} = 0 V → 3.3 V	2.847	2.920	2.993	V	—
11	Reset ON resistance	RONRST	EN = 0 V RESET inflowing current = 330 µA (10 kΩ pull-up resistor to 3.3 V)	—	140	240	Ω	—
12	DIS discharge resistance	RONDIS	EN = 0 V	—	90	190	Ω	—
13	BUF output voltage	BUFVOUT	$I_{OUT(BUF)}$ = 10 µA	0.873	0.900	0.927	V	—

■ Electrical Characteristics (Reference values for design) at V_{IN} = 3.3 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Reference values			Unit	Notes
				Min	Typ	Max		
[DCDC1] (1.2 V step-down DC-DC converter) C = 10 µF (Murata : GRM21BB31A106K) L = 2.2 µH (Taiyo Yuden : NR3012T2R2M or TDK : MLP2520S2R2S or FDK : MIPSA2520D2R2) [DCDC2] (1.8 V step-down DC-DC converter) C = 10 µF (Murata : GRM21BB31A106K) L = 2.2 µH (Taiyo Yuden : NR3012T2R2M or TDK : MLP2520S2R2S or FDK : MIPSA2520D2R2)								
14	Consumption current at standby	ISTB	EN = 0 V	—	0	10	µA	—
15	DCDC1 line regulation	DD1REGIN	V_{IN} = 2.9 V → 5.5 V I_{OUT1} = 450 mA	—	6	18	mV	—
16	DCDC2 line regulation	DD2REGIN	V_{IN} = 2.9 V → 5.5 V I_{OUT2} = 500 mA	—	8	24	mV	—
17	DCDC1 load regulation	DD1REGLD	I_{OUT1} = 10 µA → 800 mA	—	10	30	mV	—
18	DCDC2 load regulation	DD2REGLD	I_{OUT2} = 10 µA → 800 mA	—	15	40	mV	—
19	DCDC1 output current limit	DD1ILMT	FB1 = 1.2 V → 0.6 V	0.8	1.6	2.0	A	—
20	DCDC2 output current limit	DD2ILMT	FB2 = 1.8 V → 0.9 V	0.8	1.6	2.0	A	—
21	DCDC1 efficiency 1	DD1EFF1	V_{IN} = 3.3 V → 5 V I_{OUT1} = 10 mA	69	75	—	%	—
22	DCDC1 efficiency 2	DD1EFF2	V_{IN} = 3.3 V I_{OUT1} = 450 mA	77	83	—	%	—
23	DCDC1 efficiency 3	DD1EFF3	V_{IN} = 5 V I_{OUT1} = 450 mA	74	80	—	%	—
24	DCDC2 efficiency 1	DD2EFF1	V_{IN} = 3.3 V → 5 V I_{OUT2} = 10 mA	74	80	—	%	—
25	DCDC2 efficiency 2	DD2EFF2	V_{IN} = 3.3 V I_{OUT2} = 500 mA	79	85	—	%	—
26	DCDC2 efficiency 3	DD2EFF3	V_{IN} = 5 V I_{OUT2} = 500 mA	75	81	—	%	—
27	DCDC1 output ripple voltage 1	DD1VRPL1	I_{OUT1} = 10 mA	—	30	50	mV[p-p]	—
28	DCDC1 output ripple voltage 2	DD1VRPL2	I_{OUT1} = 450 mA	—	7	50	mV[p-p]	—
29	DCDC2 output ripple voltage 1	DD2VRPL1	I_{OUT2} = 10 mA	—	30	50	mV[p-p]	—
30	DCDC2 output ripple voltage 2	DD2VRPL2	I_{OUT2} = 500 mA	—	7	50	mV[p-p]	—

■ Electrical Characteristics (Reference values for design) (continued) at V_{IN} = 3.3 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Reference values			Unit	Notes
				Min	Typ	Max		
[DCDC1] (1.2 V step-down DC-DC converter) C = 10 µF (Murata : GRM21BB31A106K) L = 2.2 µH (Taiyo Yuden : NR3012T2R2M or TDK : MLP2520S2R2S or FDK : MIPSA2520D2R2) [DCDC2] (1.8 V step-down DC-DC converter) C = 10 µF (Murata : GRM21BB31A106K) L = 2.2 µH (Taiyo Yuden : NR3012T2R2M or TDK : MLP2520S2R2S or FDK : MIPSA2520D2R2)								
31	DCDC1 load transient response	DD1DVAC	I_{OUT1} = 50 mA ↔ 200 mA Δt = 1 µs	—	—	50	mV	—
32	DCDC2 load transient response	DD2DVAC	I_{OUT2} = 10 mA ↔ 250 mA Δt = 1 µs	—	—	50	mV	—
33	DCDC1 operating frequency	DD1FSW	I_{OUT1} = 450 mA	0.96	1.2	1.44	MHz	—
34	DCDC2 operating frequency	DD2FSW	I_{OUT2} = 500 mA	0.96	1.2	1.44	MHz	—
35	DCDC1 discharge resistance	DD1RDIS	EN = 0 V	—	100	150	Ω	—
36	DCDC2 discharge resistance	DD2RDIS	EN = 0 V	—	150	225	Ω	—
37	DCDC1 Pch-MOS ON resistance	DD1RONP	—	—	0.25	0.375	Ω	—
38	DCDC2 Pch-MOS ON resistance	DD2RONP	—	—	0.3	0.45	Ω	—
39	DCDC1 Nch-MOS ON resistance	DD1RONN	—	—	0.2	0.3	Ω	—
40	DCDC2 Nch-MOS ON resistance	DD2RONN	—	—	0.25	0.375	Ω	—
41	DCDC1 start time	DD1TSTU	Capacitive load : 26 µF I_{OUT1} = 0 A The time until 90% from 10% of target value.	—	0.1	1	ms	—
42	DCDC2 start time	DD2TSTU	Capacitive load : 24 µF I_{OUT2} = 0 A The time until 90% from 10% of target value.	—	0.15	1	ms	—

■ Electrical Characteristics (Reference values for design) (continued) at V_{IN} = 3.3 V

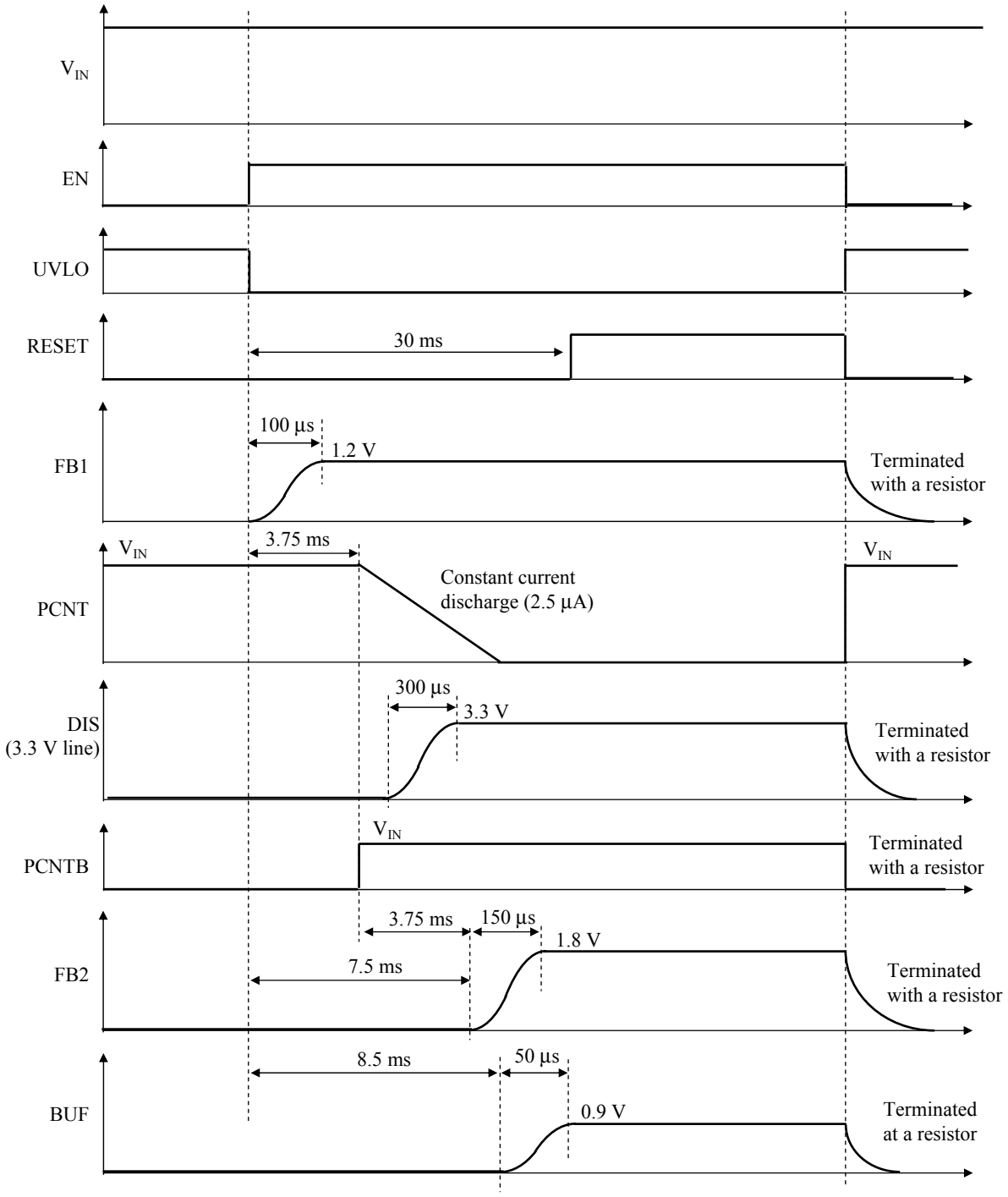
Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Reference values			Unit	Notes
				Min	Typ	Max		
[DCDC1] (1.2 V step-down DC-DC converter) C = 10 µF (Murata : GRM21BB31A106K) L = 2.2 µH (Taiyo Yuden : NR3012T2R2M or TDK : MLP2520S2R2S or FDK : MIPSA2520D2R2) [DCDC2] (1.8 V step-down DC-DC converter) C = 10 µF (Murata : GRM21BB31A106K) L = 2.2 µH (Taiyo Yuden : NR3012T2R2M or TDK : MLP2520S2R2S or FDK : MIPSA2520D2R2)								
43	BUF line regulation	BUFREGIN	V_{IN} = 2.9V → 5.5V $I_{OUT(BUF)}$ = 10 µA	—	0	10	mV	—
44	BUF load regulation	BUFREGLD	$I_{OUT(BUF)}$ = 10 µA → 10 mA	—	5	20	mV	—
45	BUD output current limit	BUFILMT	BUF = 0V	5	10	20	mA	—
46	BUF PSRR	BUFPSR	$I_{OUT(BUF)}$ = 10 µA f = 10 kHz	—	–50	–20	dB	—
47	BUF load transient response 1	BUFDVAC1	$I_{OUT(BUF)}$ = 10 µA → 10 mA Δt = 1 µs	—	160	300	mV	—
48	BUF load transient response 2	BUFDVAC2	$I_{OUT(BUF)}$ = 10 mA → 10 µA Δt = 1 µs	—	100	200	mV	—
49	BUF discharge resistance	BUFRDIS	EN = 0 V	—	80	120	Ω	—
50	BUF start time	BUFTSTU	$I_{OUT(BUF)}$ = 0 A The time until 90% from 10% of target value.	—	50	200	µs	—
51	Reset delay	RSTDLY	—	20	30	40	ms	—
52	PCNT sink current	IPCNT	PCNT = 3.3 V	1.25	2.5	3.75	µA	—
53	Timer latch time	TLATCH	—	0.6	1	1.4	ms	—
54	DCDC1 Ground-short detection voltage	DD1SCP	FB1 = 1.2 V → 0 V	0.5	0.6	0.7	V	—
55	DCDC2 Ground-short detection voltage	DD2SCP	FB2 = 1.8 V → 0 V	0.8	0.9	1.0	V	—
56	TSD operating temperature	TJSO	Temperature error detection	130	160	190	°C	—

■ Technical Data

1. Start / Stop sequence

Start / Stop control of AN30181A is performed by EN pin.
The start / stop sequence is as follows.

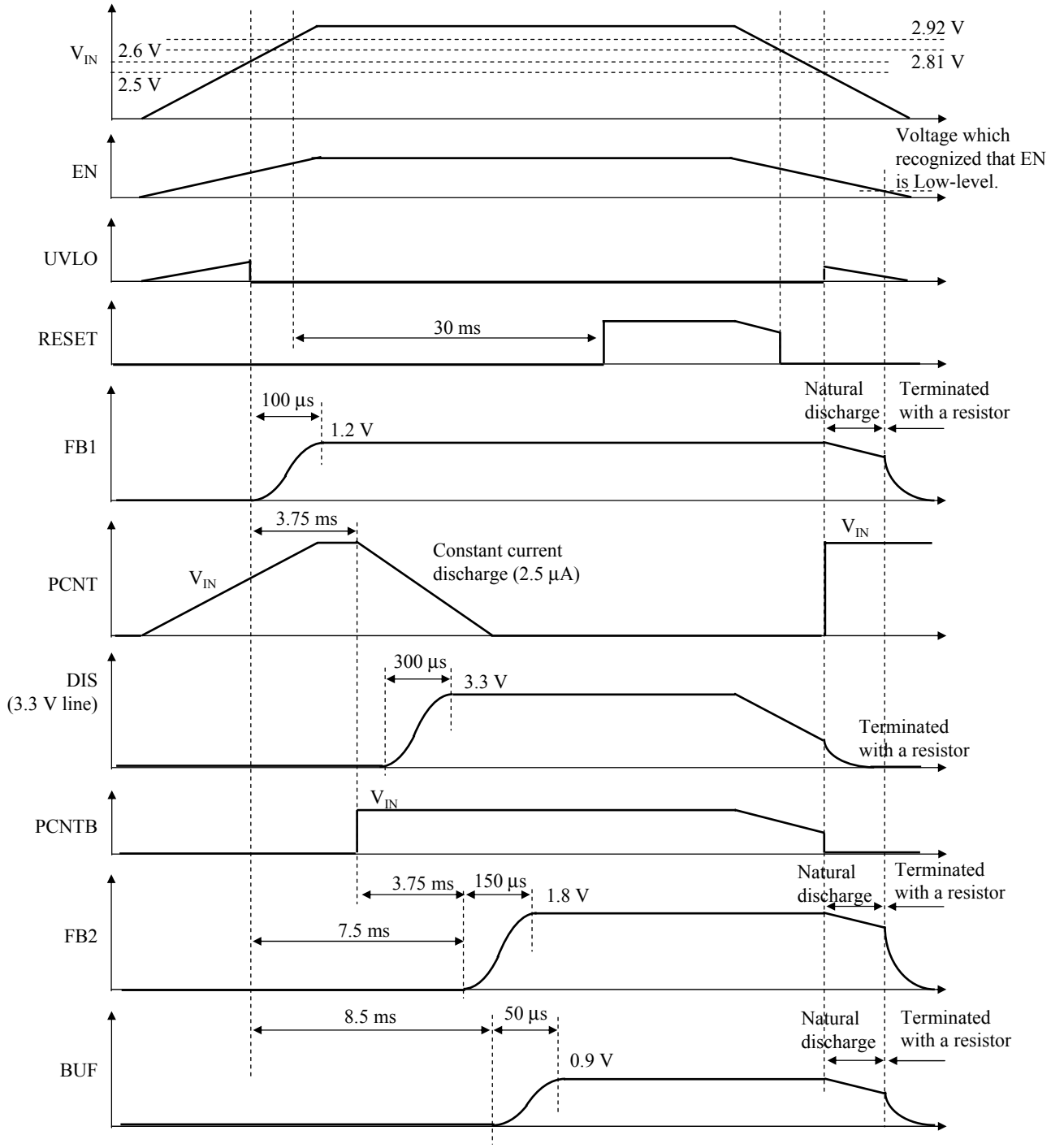


Note) All values given in the above figure are typical values.

■ Technical Data (continued)

1. Start / Stop sequence (continued)

Start / Stop sequence in case that EN pin is connected to power supply (V_{IN}) is as follows.



Note) All values given in the above figure are typical values.

■ Technical Data (continued)

1. Start / Stop sequence (continued)

The operation of each block is as follows.

- UVLO function
  When power supply rises to 2.6 V or higher at EN = High, UVLO is released, and the operation of each function starts.
  Since this function's hysteresis is 100 mV, UVLO detects when power supply falls to 2.5 V or lower, then each function shuts down.

- Reset function
  RESET pin shifts to High at 30 ms delay after power supply rises to 2.92 V or higher.
  (Output type : Nch MOS open drain)
  Since this function's hysteresis is 110 mV, RESET pin shifts to Low when power supply falls to 2.81 V or lower.
  (No delay in case of High → Low)

- DCDC1 (Output voltage : 1.2 V)
  When UVLO is released, DCDC1 starts and outputs 1.2 V. Soft-start function operates for 1 ms after startup. Since output voltage rises slowly, limiting input current, it is possible to prevent rush current and overshoot.
  When UVLO detects, DCDC1 turns off. When EN pin shifts to Low, an output pin (FB1) is terminated with a resistor.

- External Pch-MOSFET gate control function
  PCNT pin is discharged by the constant current (2.5 μA) at 3.75 ms delay after UVLO is released.
  By connecting the gate of Pch MOSFET to PCNT pin, it is possible to turn on this FET softly.
  At the same time, the termination with a resistor of DIS pin is released.
  Just after UVLO detects, PCNT pin voltage becomes V_{IN} and DIS pin is terminated with a resistor.

- External synchronization signal output function
  PCNTB pin outputs the signal which synchronized with the above-mentioned PCNT pin. Therefore, PCNTB pin outputs High at 3.75 ms delay after UVLO is released. PCNTB pin outputs Low just after UVLO detects.

- DCDC2 (Output voltage : 1.8 V)
  DCDC2 starts and outputs 1.8 V at 7.5 ms delay after UVLO is released. DCDC2 has the same soft-start function as DCDC1 and starts, preventing rush current and overshoot.
  DCDC2 stops because UVLO detects. When EN pin shifts to Low, an output pin (FB2) is terminated with a resistor.

- BUF (Output voltage : 0.9 V)
  BUF pin outputs 0.9 V at 8.5 ms delay after UVLO is released. BUF starts, preventing rush current and overshoot.
  BUF stops because UVLO detects. BUF is terminated with a resistor when EN pin shifts to Low.

■ Technical Data (continued)

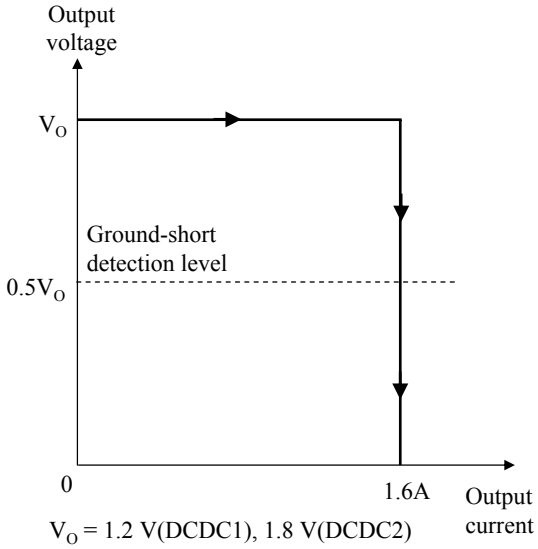
2. Protection function

2.1 Ground-short protection function

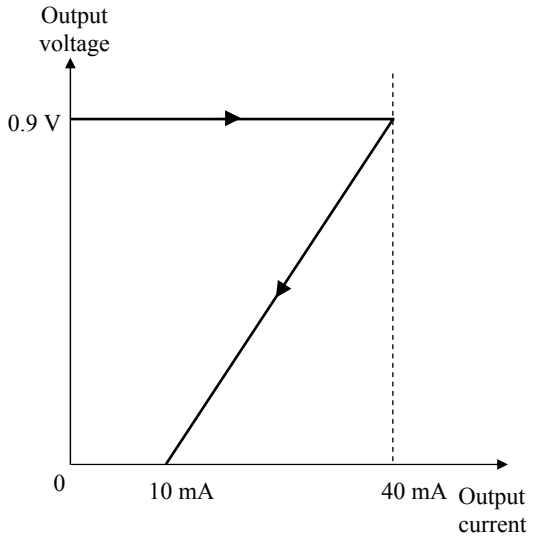
DCDC1 and DCDC2 have ground-short detection circuits respectively. When output voltage falls to 50% or lower of target value (DCDC1 : 0.6 V, DCDC2 : 0.9 V), it shifts to the protection sequence shown in 2.3.
However, even if BUF pin shorts to GND, BUF does not shift to the protection sequence.

2.2 Over-current limit function

DCDC1, DCDC2 and BUF have over-current limit circuits respectively. This function limits the output current which exceeds the setup value. The over-current limit characteristics are as follows.



a) DCDC1/2



b) BUF

The output currents of DCDC1 and DCDC2 are limited to 1.6 A(typ) regardless of the output voltage.
BUF has limit characteristics, which the output current decreases as the output voltage falls.
The peak input current is 40 mA(typ). The input current at BUF = 0 V is 10 mA(typ).

■ Technical Data (continued)

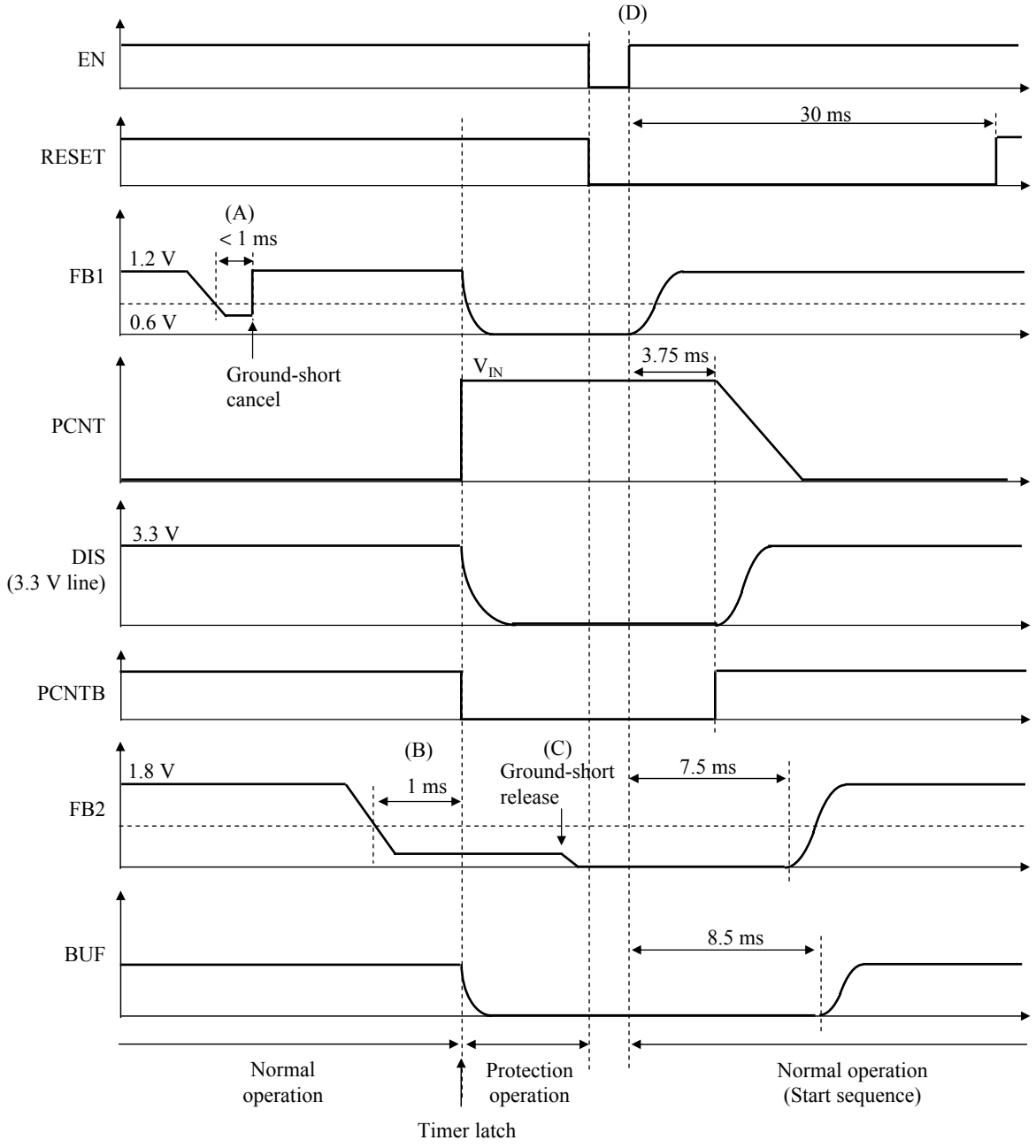
2. Protection function (continued)

2.3 Protection sequence

When the following state continues for 1 ms(typ), AN30181A shifts to the protection sequence.

- Any of DCDC1 and DCDC2 shorts to GND. (Output voltage is 50% or lower of target value.)
- TSD circuit detects abnormal state.

When this LSI shifts to the protection sequence, it is latched to the state at which each function is shut down. It recovers from the protection sequence by applying to EN pin again or releasing UVLO again.
The protection sequence example is as follows.



■ Technical Data (continued)

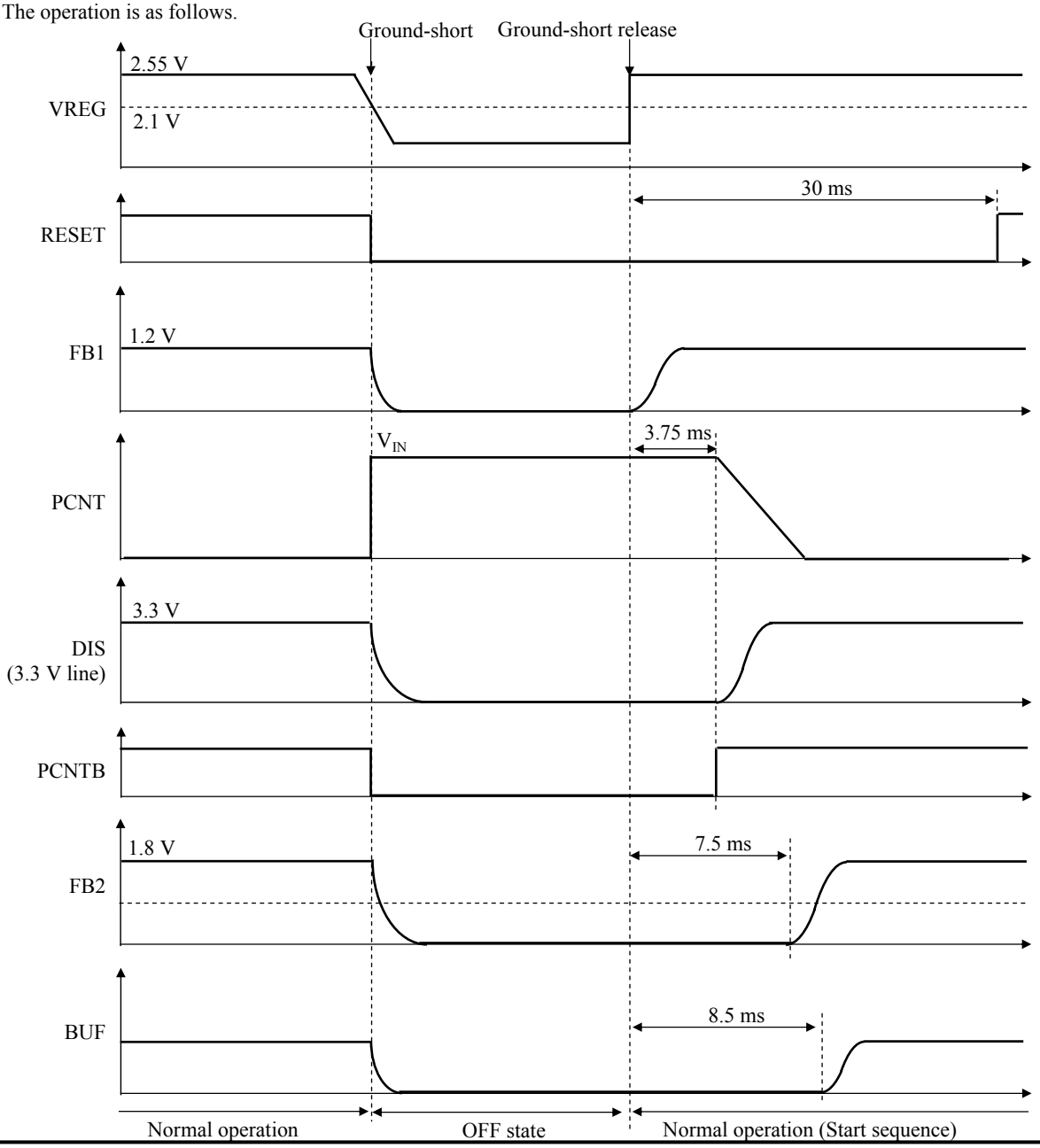
2. Protection function (continued)

2.3 Protection sequence (continued)

In (A) of the following figure, DCDC1 output shorts to GND. However, this LSI doesn't shift to protection sequence because the term of ground-short is 1 ms or shorter.
In (B) of the following figure, DCDC2 output shorts to GND. After ground-short state continues for 1 ms, this LSI shifts to protection sequence, DCDC1, DCDC2, external Pch-MOSFET gate drive circuits and BUF shift to OFF state and are latched. Even if ground-short is released, the operation of each circuit does not recover (C). During the protection sequence, RESET pin is not set to Low.
In (D) of the following figure, they recover to normal start sequence after EN is input again.

2.4 VREG pin ground-short operation

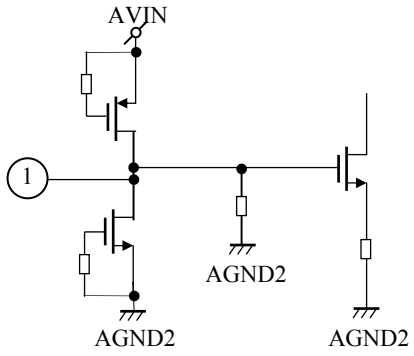
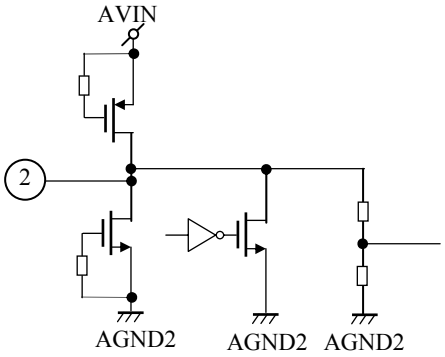
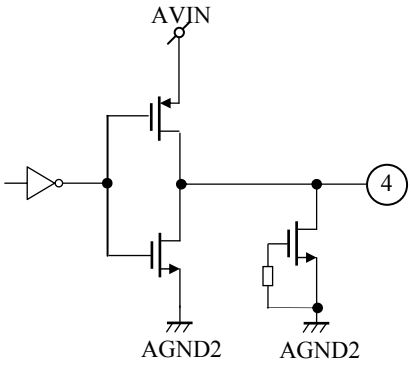
VREG pin is an output pin of LDO used in internal circuits. The operation of each function stops just after VREG pin is shorted to GND. Since each function is not latched unlike the case of 2.3 Protection sequence, it recovers by the release of ground-short. The operation is as follows.



■ Technical Data (continued)

3. I/O block circuit diagrams and pin function descriptions

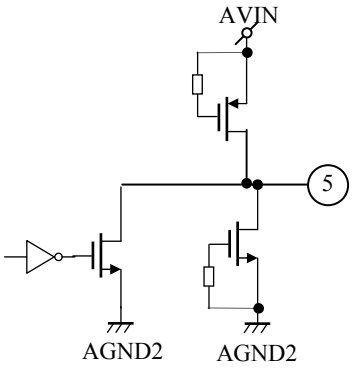
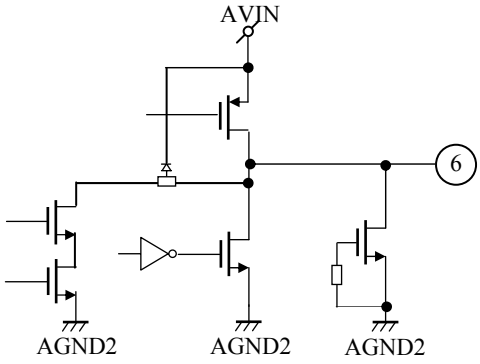
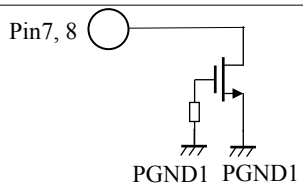
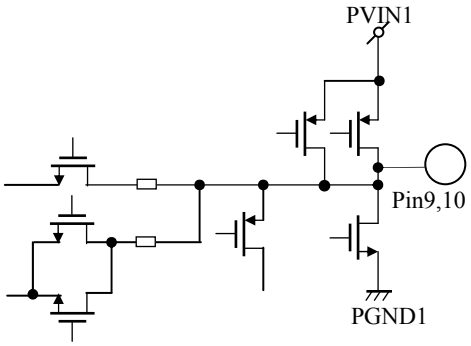
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Pin name	Waveform and voltage	Internal circuit	Impedance	Description
1	EN	V_{IN} 0 V		1.36 MΩ	ON/OFF control pin
2	FB2	1.8 V		430 kΩ	Output voltage control input pin
3	AGND2	0 V		—	GND
4	PCNTB	V_{IN} 0V		—	Logic output pin

■ Technical Data (continued)

3. I/O block circuit diagrams and pin function descriptions (continued)

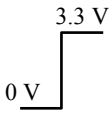
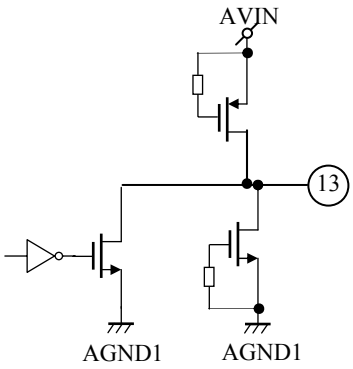
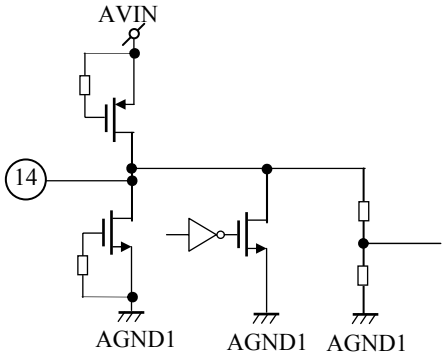
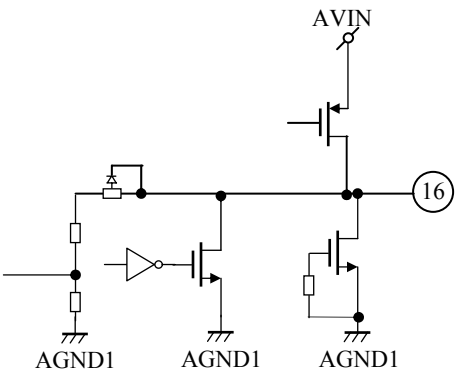
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Pin name	Waveform and voltage	Internal circuit	Impedance	Description
5	DIS	0 V to 3.3 V		90 Ω	Discharge pin
6	PCNT	V_{IN} 0 V		—	External PMOS control pin
7, 8	PVIN1	V_{IN}		—	Power supply pin
9, 10	LX1	V_{IN} 0 V 0 Hz to 1.2 MHz		—	Switching output pin

■ Technical Data (continued)

3. I/O block circuit diagrams and pin function descriptions (continued)

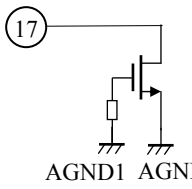
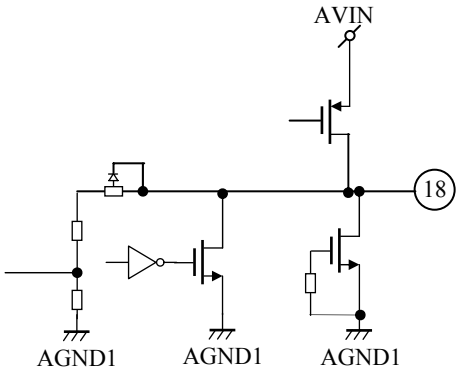
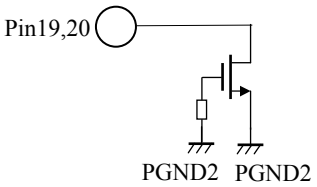
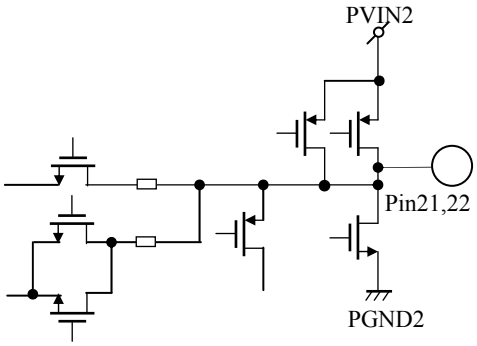
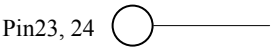
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Pin name	Waveform and voltage	Internal circuit	Impedance	Description
11,12	PGND1	0 V		—	GND
13	RESET			140 Ω	Comparator output pin (open drain)
14	FB1	1.2 V		430 kΩ	Output voltage control input pin
15	AGND1	0 V		—	GND
16	VREG	2.55 V		1.8 MΩ	LDO output pin

■ Technical Data (continued)

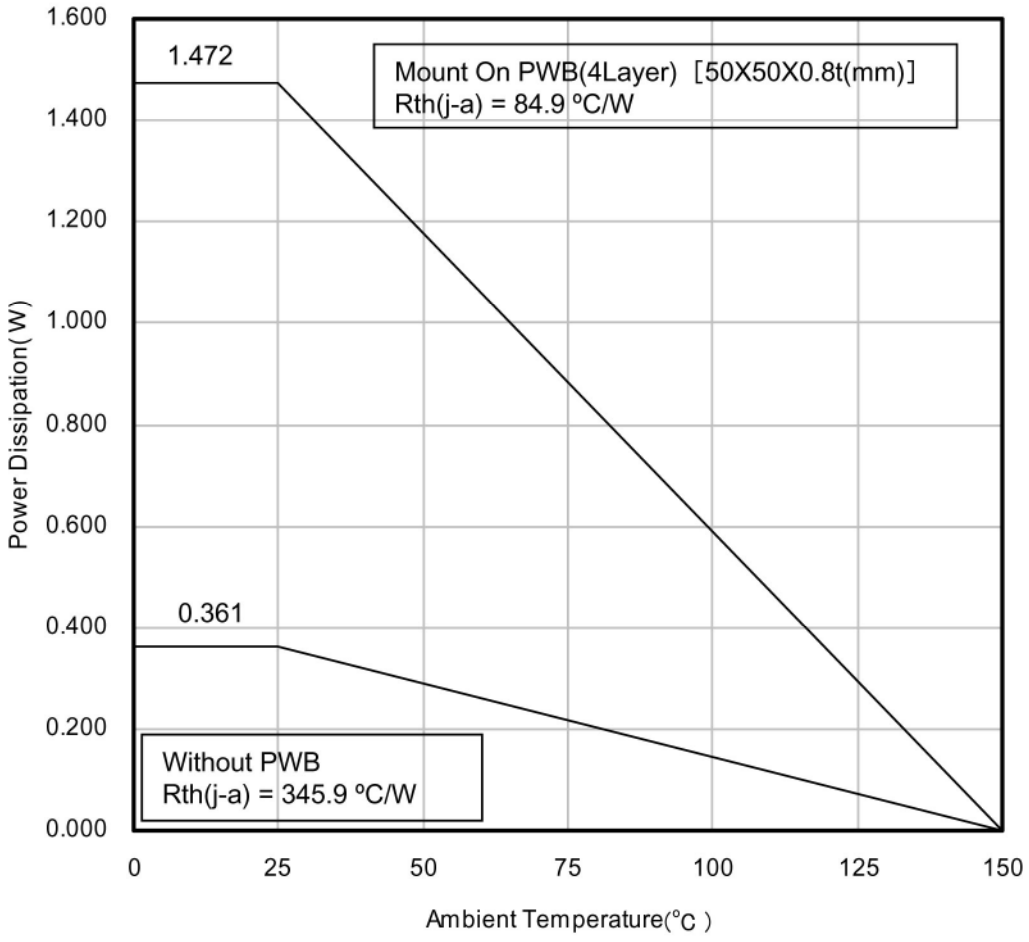
3. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Pin name	Waveform and voltage	Internal circuit	Impedance	Description
17	AVIN	V_{IN}		—	Power supply pin
18	BUF	0.9 V		900 kΩ	LDO output pin
19, 20	PVIN2	V_{IN}		—	Power supply pin
21, 22	LX2	V_{IN} 0 V 0 Hz to 1.2 MHz		—	Switching output pin
23, 24	PGND2	0 V		—	GND

■ Technical Data (continued)

4. P_D — T_a diagram



■ Usage Notes

• Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications:
   - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   - Any applications other than the standard applications intended.
     (1) Space appliance (such as artificial satellite, and rocket)
     (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
     (3) Medical equipment for life support
     (4) Submarine transponder
     (5) Control equipment for power plant
     (6) Disaster prevention and security device
     (7) Weapon
     (8) Others : Applications of which reliability equivalent to (1) to (7) is required

   It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the IC described in this book for any special application, unless our company agrees to your using the IC in this book for any special application.
2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-V_{CC} short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
7. When using the LSI for new models, verify the safety including the long-term reliability for each product.
8. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

20100202