TZA3054A
100 Mbit/s to 3.2 Gbit/s A-rate™ limiting amplifier
Rev. 01 — 12 August 2004　　　　　　　　**Objective data sheet**

1. General description

The TZA3054A is a highly sensitive A-rate™ Limiting amplifier featuring ACE (Automatic Current Engine) functionality, Logarithmic Level Detect (LLD), Loss-of-Signal (LOS) detector and output jam function. The ACE functionality provides a limiting amplifier which achieves optimum performance (sensitivity, bandwidth, jitter and output eye pattern) for any bit rate with very low power consumption. This is achieved through automatic adjustment of the input bandwidth and the output slew rate by using built-in performance monitors. Manual adjustment is possible by programming the I^{2}C-bus registers.

The integrated I^{2}C-bus controller allows for flexible configuration with a microcontroller, which minimizes the number of external connections and external components needed.

Adjustment of the LOS threshold can be done either via the I^{2}C-bus or with an external resistor. The output amplitude is selectable between a high or low value, or adjustable via the I^{2}C-bus. The detected logarithmic signal level is indicated directly by a voltage on pin LLD, or by a binary value of an I^{2}C-bus register. Furthermore, the junction temperature, the internal supply voltage and an external voltage can all be monitored through a built-in Analog-to-Digital Converter (ADC) which supports several diagnostic functions.

These features make the TZA3054A ideally suited for application in modules, including Small Form Factor (SFF/SFP/iSFP) modules.

The TZA3054A comes in a compact 3×4 mm^2 HVQFN20 package, with the exposed die pad serving as the main ground connection.

2. Features

- A-rate™ limiting amplifier; supporting any data rate between 100 Mbit/s and 3.2 Gbit/s, including data rates such as OC3, OC48, FC, 2FC and GE
- Very low power
- I^{2}C-bus programmable
- Highly sensitive data input with 2.5 mV sensitivity
- On-chip DC offset compensation without external capacitor
- Automatic bandwidth and slew rate adjustment (ACE)
- Pin selectable output level, 500 mV or 1500 mV (p-p) differential
- Rise and fall times 40 ps typical at 3.2 Gbit/s
- Deterministic Jitter typically below 10 ps (p-p)
- Logarithmic Level Detect (LLD) from 1 mV to 1200 mV
- Input amplitude related Loss Of Signal (LOS) indicator with adjustable threshold
- 2.9 V to 3.5 V supply voltage
- SFF-8074i and SFF-8472 compliant

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- Additional features with I^{2}C-bus:
    - ◆ Microcontroller controllable
    - ◆ Temperature readout
    - ◆ Supply voltage readout
    - ◆ Logarithmic level detect readout
    - ◆ External voltage readout
    - ◆ Readout calibration
    - ◆ Adjustable output level from 0 mV to 2000 mV (p-p) differential
    - ◆ Adjustable LOS threshold without external components
    - ◆ Programmable LOS hysteresis
    - ◆ Offset compensation disable
    - ◆ Status and interrupt reporting
    - ◆ Polarity inversion
    - ◆ Configurable LOS and JAM I/Os
    - ◆ Auto Jam
    - ◆ Adjustable bandwidth and slew rate.

3. Applications

- Fiber optic modules: SFP, SFF, GBIC, 1 × 9 and 2 × 9
- Digital fiber optic receivers for Fiber Channel (FC), gigabit ethernet, infiniband and telecom applications.

4. Ordering information

Table 1:   Ordering information

Type number	Package		
	Name	**Description**	**Version**
TZA3054AHN	HVQFN20	plastic heat sink bottom chip carrier; 20 leads; body 3 × 4 × 0.65 mm	SOT797-1

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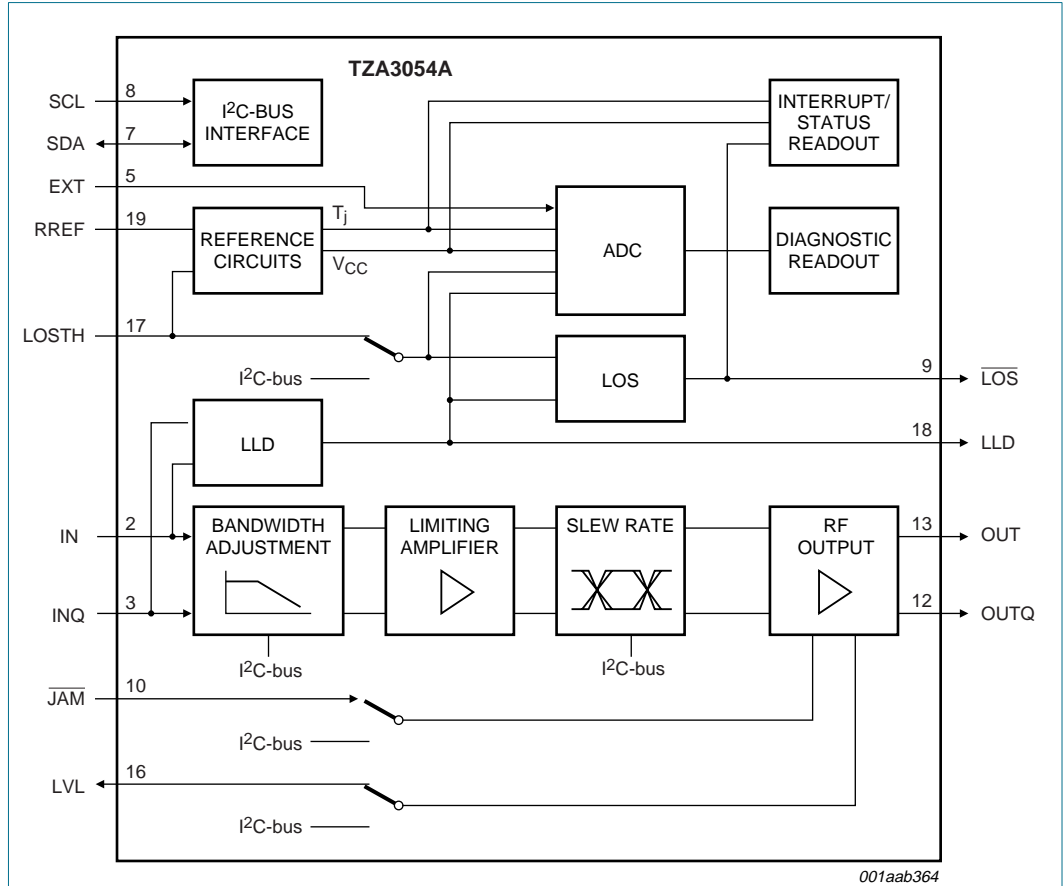
5. Block diagram

Fig 1.   Block diagram.
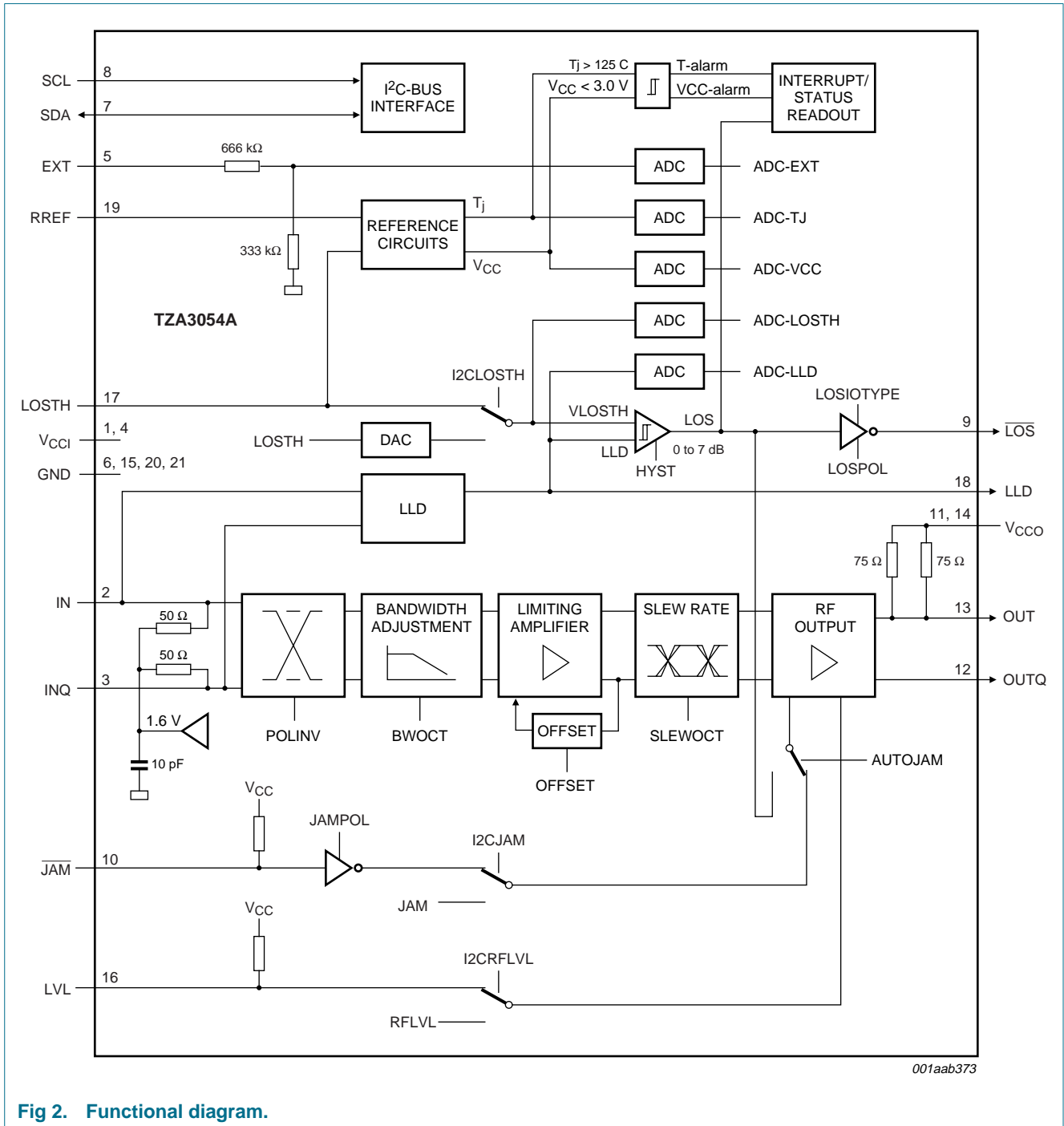
6. Functional diagram

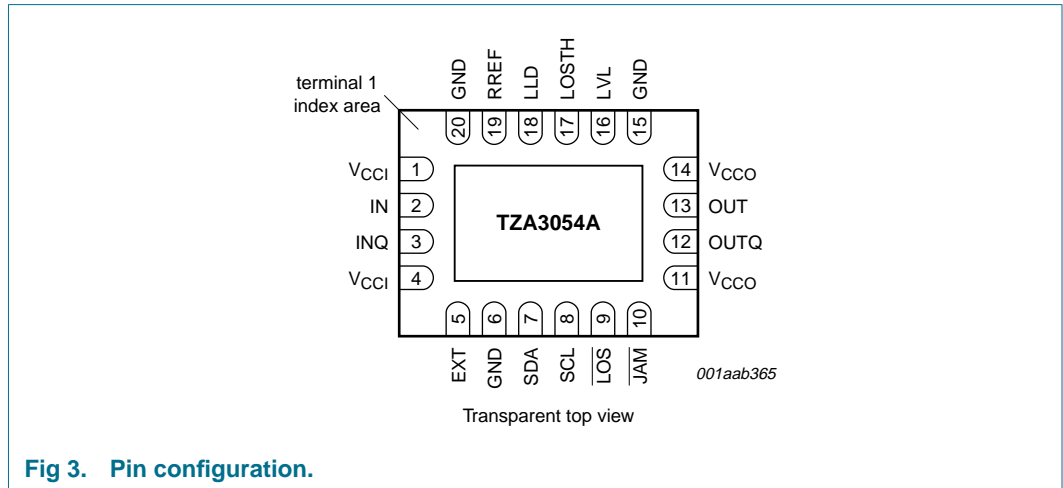**Fig 2. Functional diagram.**

7. Pinning information

7.1 Pinning

Fig 3. Pin configuration.

7.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
V_{CCI}	1	supply voltage for RF input part
IN	2	non-inverted RF input
INQ	3	inverted RF input
V_{CCI}	4	supply voltage for RF input part
EXT	5	external voltage input
GND	6	ground
SDA	7	I²C-bus data signal bi-directional
SCL	8	I²C-bus clock signal input
$\overline{LOS}$	9	LOS open-drain output (active LOW)
$\overline{JAM}$	10	jam input (active LOW)
V_{CCO}	11	supply voltage for RF output part; analog part and digital part
OUTQ	12	inverted RF output
OUT	13	non-inverted RF output
V_{CCO}	14	supply voltage for RF output part; analog part and digital part
GND	15	ground
LVL	16	RF output signal level select
LOSTH	17	loss of signal threshold adjustment
LLD	18	logarithmic level detection
RREF	19	reference pin; for generating an external resistor related precision current
GND	20	ground
	21	RF ground plus die pad

8. Functional description

8.1 RF input

The TZA3054A is a highly sensitive limiting amplifier with an input voltage range from 2.5 mV to 1200 mV (p-p) Single-Ended (SE). It is assumed that the inputs, requiring AC-coupling, carry a complementary signal with the specified peak-to-peak value (true differential excitation).
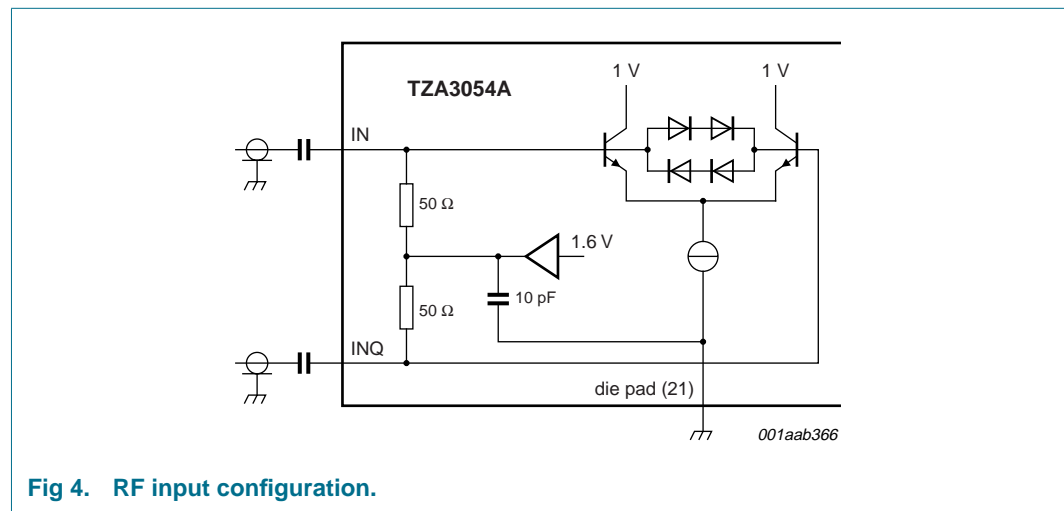

Fig 4.   RF input configuration.

The TZA3054A includes a DC offset cancellation loop with a very low bandwidth of approximately 1 kHz. The TZA3054A can support transmission standards allowing extremely long sequences of consecutive identical bits by disabling the DC offset cancellation, but at the expense of reduced sensitivity. The DC offset cancellation can be disabled with I2C-bus bit OFFSET in I2C-bus register LIMCNF (12H). This also allows for burst mode applications.

As part of the ACE functionality, the TZA3054A has an automatic bandwidth adjustment loop to achieve optimum performance over temperature at all bit rates. This means that the input bandwidth is reduced automatically at lower bit rates. Wide band noise of the optical front-end (photo detector and transimpedance amplifier) is thus reduced for lower bit rates.

The automatic bandwidth adjustment of the input stage can be overruled by manual settings via the I2C-bus. This may be needed in the event of non-randomized or burst-mode signals; see Section 8.6.

8.2 Logarithmic level detect

The signal strength at the input is measured with a Logarithmic Level Detector (LLD) and presented at pin LLD. The LLD reading has a sensitivity (S_{LLD}) of typically 17 mV/dB for a $V_{i(p-p)(SE)}$ range of 1 mV to 1200 mV, which is available as a voltage on pin LLD, or can be retrieved from the I2C-bus register 0Ah in binary form.

$$V_{LLD} = V_{LLD} = V_{LLD(10\,mV)} + S_{LLD} \times 20 LOG\left[\frac{V_{IN(p-p)}}{10\,mV}\right], \text{ (expressed in mV)}.$$
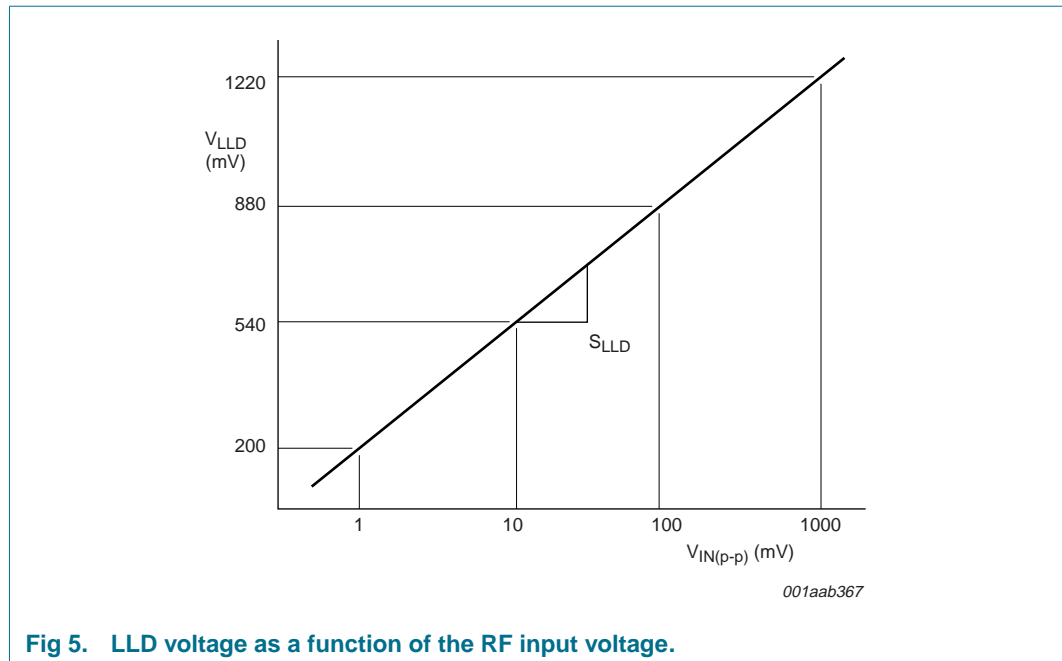
Fig 5.   LLD voltage as a function of the RF input voltage.

8.3 Loss of signal indicator

Besides the analog LLD output, a digital LOS indication circuit is also incorporated in the TZA3054A. The LLD level is internally compared with a loss of signal threshold, which can be set via an external resistor connected to pin LOSTH (this is the default mode after power-up) or by means of an internal Digital-to-Analog Converter (DAC). If the DAC is used, programmed with I^2C-bus bit I2CLOSTH in I^2C-bus register LOSCNF (10h), the value of the required threshold needs to be programmed into the I^2C-bus register LOSTH (11h). The default value is 00h, so no LOS can be generated.

If the received signal strength is **below** the threshold value the LOS open-drain output will be pulled LOW. The LOS open-drain output requires an external pull-up resistor in the range of 4.7 kΩ to 10 kΩ. A default hysteresis of 3 dB is applied in the comparator.

I^2C-bus register LOSCNF (10h) provides more flexibility, e.g. a programmable hysteresis of 0 dB to 7 dB in steps of 1 dB, a CMOS style LOS output instead of the default open-drain configuration and programmable LOS polarity. These features provide "any-interface" in the application; see Figure 6.
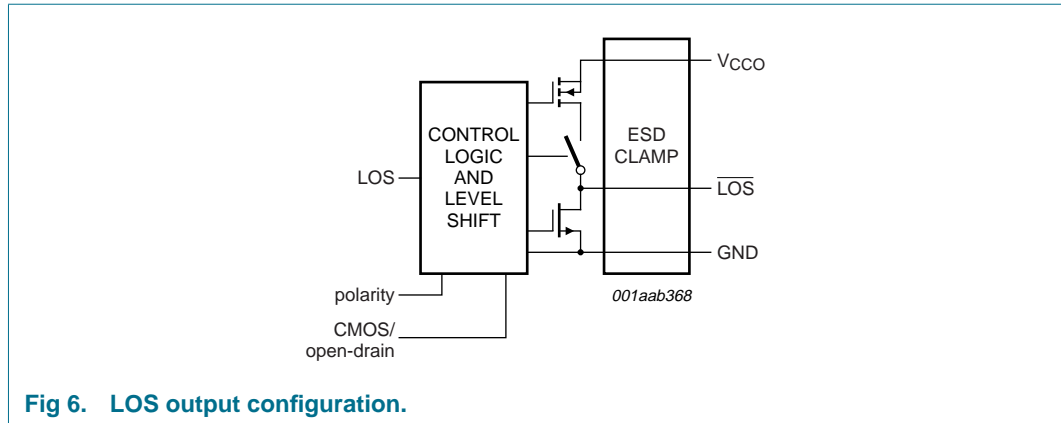
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Fig 6.   LOS output configuration.

8.4   Setting LOSTH reference level by external resistor
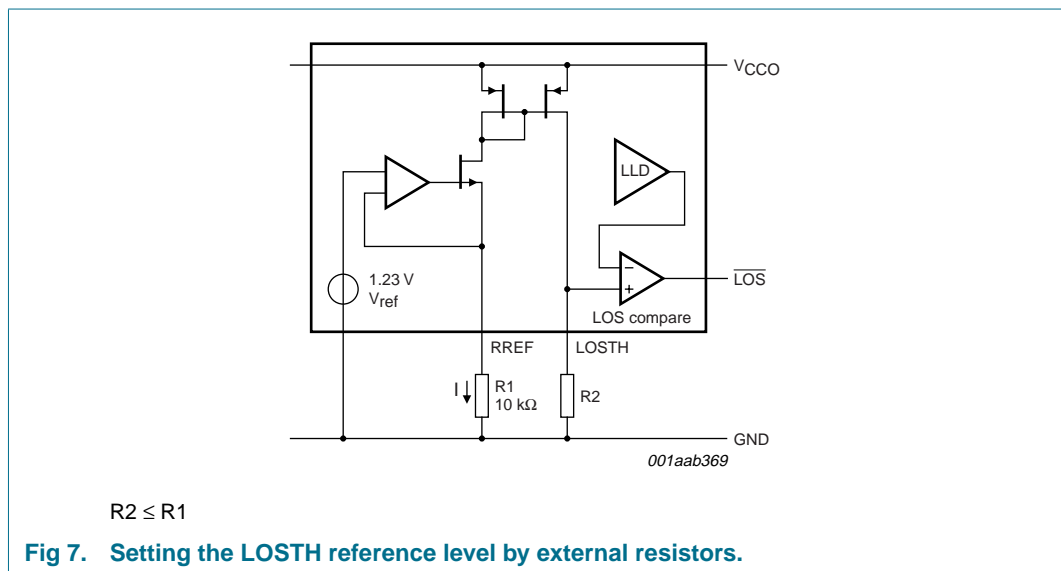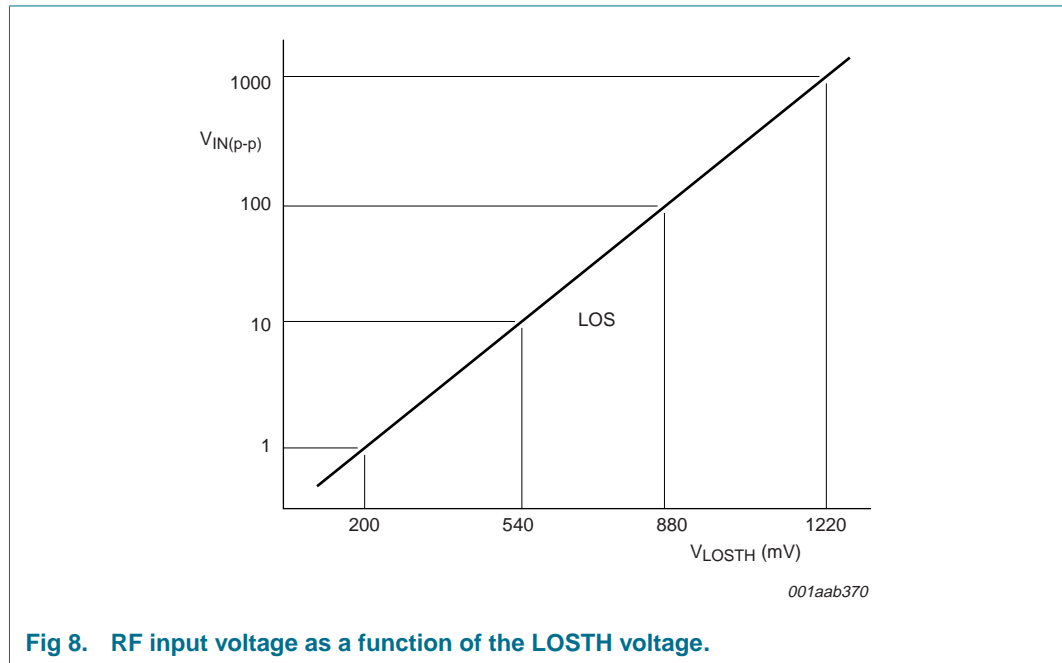

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R2 ≤ R1

Fig 7.   Setting the LOSTH reference level by external resistors.

The loss of signal threshold can also be programmed by applying an external voltage to pin LOSTH (this is the default mode after power-up). The reference voltage level at pin LOSTH can be set by connecting an external resistor (R2) from the pin to ground. The voltage on the pin is determined by the resistor ratio between R2 and R1; see Figure 7. For resistor R1 the value must be 10 kΩ, with 1 % accuracy, thus yielding a current of

123 μA. The LOSTH voltage equals $\frac{R2}{R1} \times V_{ref}$.

Voltage V_{ref} represents a temperature stabilized and accurate reference voltage of 1.23 V. The minimum threshold level corresponds to 0 V and the maximum to 1.23 V. Hence, the value of R2 may not be higher than R1. The accuracy of the LOSTH voltage depends mainly on the matching of the two external resistors.

Apart from using resistors (R1 and R2) to set the LOS threshold an accurate external voltage source can also be used, provided that it has a low output impedance.

The omission of R2 results in maximum LOS threshold, thereby generating LOS constantly. LOSTH may be short-circuited to ground to circumvent this situation. If the I²C-bus DAC is used, R2 may be omitted or connected to ground.

Fig 8.   RF input voltage as a function of the LOSTH voltage.

8.5 RF output

Fig 9.   RF output configuration.
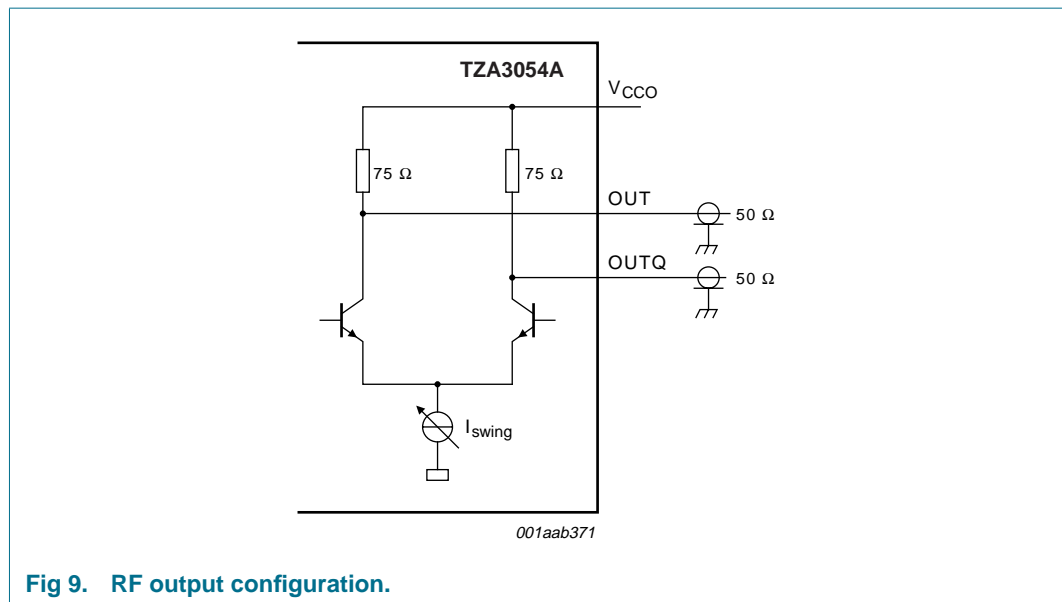
The RF CML output has a programmable signal amplitude between 500 mV to 2000 mV (p-p) (differential) in 7 steps of 250 mV, by I²C-bus bits RFLVL[2:0] (I²C-bus register RFLVL; 13h). The output can also be switched off using this RFLVL register: this might be useful to save power in case only the LLD and LOS functions of the TZA3054A are used in the application. The default amplitude is 1500 mV (p-p, differential). Furthermore, the termination scheme can be either DC or AC-coupled.

If the I^{2}C-bus setting for the output level is set to pin selection, the signal amplitude of the output buffer can be selected from two fixed values. By applying a HIGH level to pin LVL 1570 mV (p-p, differential) is selected (this is the default mode after power-up due to the internal pull-up resistor). By applying a LOW level to pin LVL 500 mV (p-p, differential) is selected.

As part of the ACE functionality, the slew rate of the output is adjusted automatically for any bit rate to approximately 10 % of the corresponding Unit Interval time, by a built-in slew rate control loop. The slew rate control loop eases ElectroMagnetic Compatibility (EMC) and ElectroMagnetic Interference (EMI) compliance of the final module design, as well as dramatic power saving, especially for lower bit rates. To estimate the power dissipation use Figure 17 Core supply current as a function of bit rate, and Figure 18 RF output supply current as a function of output voltage swing. By adding both independent currents the total supply current can be calculated.

The automatic slew rate adjustment can be overruled by manual setting of the output stage via the I^{2}C-bus. This may be required in the event of non-randomized or burst-mode signals; see the Section 8.6.

8.5.1 JAM

The RF output can be forced into the logic 0 state by applying a LOW-level to the JAM pin (pin JAM is active LOW). Hence in the event of a loss of signal situation, the output can be jammed to suppress the amplified noise from the optical front-end. The JAM pin has an internal pull-up, to prevent jamming of the output if the JAM pin is not connected.

If CMOS compatibility is required, pin JAM can be programmed to be active HIGH with I^{2}C-bus bit JAMPOL (I^{2}C-bus register RFLVL; 13h).

Jamming can also be done via the I^{2}C-bus, using I^{2}C-bus bit I2CJAM to enable this function and I^{2}C-bus bit JAM to actually jam the output (I^{2}C-bus register RFLVL; 13h).

JAM can also be programmed to work automatically when loss of signal occurs. This can be done by connection pin LOS to pin JAM directly or with I^{2}C-bus bit AUTOJAM (I^{2}C-bus register RFLVL; 13h).
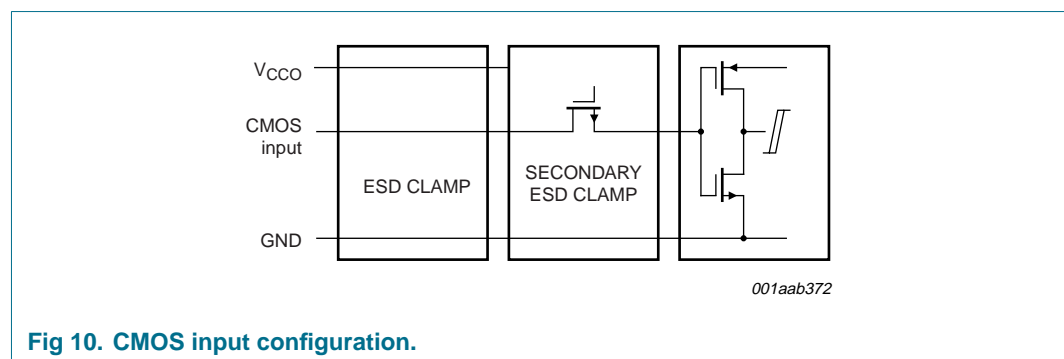

Fig 10. CMOS input configuration.

8.5.2 Diagnostic support

The TZA3054A supports several diagnostic functions, including:

- Junction temperature
- Supply voltage
- Input signal strength (LLD)
- External voltage (EXT input).

The junction temperature, supply voltage, LLD voltage and an external voltage (EXT input) can be measured with a built-in 8-bit ADC, based on the successive approximation principle. The value of the measured quantity can then be read in the appropriate ADC result register. A supervisory algorithm can be implemented in a microcontroller, to realize the required diagnostic functionality e.g. the i-SFP standard, SFF-8472.

8.5.2.1 Junction temperature

The junction temperature can be measured in a range of −40 °C to +85 °C with approximately 3 °C resolution. The result can be read from ADC register 08h. The following formula can be applied to convert the ADC reading into a temperature:
$T = 478.43 - 2.93 \times ADC_{value}$.

8.5.2.2 Supply voltage

The supply voltage can be measured in a range of 2.4 V to 3.7 V with approximately 5 mV resolution. The result can be read from ADC register 09h. The formula to convert the ADC reading into the supply voltage is: $V_{CC} = 2.4 + 4.82 \times 10^{-3} \times ADC_{value}$.

8.5.2.3 LLD voltage

The LLD voltage can be measured from 0 mV to 1200 mV with approximately 5 mV resolution. The result can be read from ADC register 0Ah. The formula to convert the ADC reading into the supply voltage is: $V_{LLD} = 4.82 \times 10^{-3} \times ADC_{value}$. The LLD voltage can be converted to an input voltage by using Figure 5.

8.5.2.4 External voltage

The external input voltage (EXT) can be measured between 0 V and 3.6 V with approximately 15 mV resolution. The result can be read from ADC register 0Bh. The formula to convert the ADC reading into the supply voltage is:
$V_{EXT} = 14.45 \times 10^{-3} \times ADC_{value}$.

8.5.3 Power supply connections

Two separate supply domains (V_{CCI} and V_{CCO}) provide isolation between the various functional blocks of the TZA3054A. Each supply domain should be connected to a common V_{CC} via a separate filter. **All supply and ground pins, including the exposed die pad, must be connected**. The die pad should be connected with the lowest inductance possible. Since the die pad is also used as the **main** ground return of the chip, the connection should also have a low DC impedance. The voltage supply levels should be in accordance with the values specified in Section 11.

All external components should be surface mounted devices, preferably of size 0603 or smaller. The components must be mounted as close to the IC as possible, especially supply decoupling capacitors.

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8.5.4 Power-up

At power-up an internal safe condition signal is generated once the V_{CC} voltage is sufficiently high for proper operation and the internal reference voltage has settled. This signal is used to generate a Power-On-Reset (POR) signal that resets all internal circuits to their default value.

8.5.5 Default at power-up

All I²C-bus registers are reset to their default setting at power-up, which are:

- DC offset compensation: on
- Automatic bandwidth adjustment (ACE on)
- Automatic slew rate adjustment (ACE on)
- Pin adjustable / selectable LOSTH, JAM and LVL
- LOS hysteresis 3 dB
- LOS output open drain (active LOW)
- JAM active LOW.

8.5.6 Interrupt controller

The TZA3054A features an interrupt controller, based on status flags. These flags are:

- Loss of signal
- Temperature alarm (> 125 °C with a hysteresis of approximately 4 °C)
- Supply voltage alarm (< 2.85 V with a hysteresis of approximately 50 mV).

The controller contains two I²C-bus registers, namely the I²C-bus interrupt register (INTERRUPT at address 00h) and the I²C-bus status register (STATUS at address 01h).

The I²C-bus interrupt register stores the history, while the I²C-bus status register always shows the present state of the receiver.

The I²C-bus interrupt and status registers can be polled by an I²C-bus read action. The read action of the I²C-bus interrupt register clears all interrupt flags. If the alarm condition is still present, the flag is immediately reset in the I²C-bus interrupt register. The I²C-bus status register is not reset since it always shows the present state of the TZA3054A.

8.5.7 I²C-bus

The chip can be configured by using the I²C-bus connections SDA and SCL.

The I²C-bus address of the TZA3054A is D2h for writing and D3h for reading.

A detailed list of all I²C-bus registers and an explanation of their contents is given in Section 8.7.

During power-up, all I²C-bus registers are reset to their default value as indicated in Table 3.

Table 3: **I²C-bus address of TZA3054A**

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	1	0	1	0	0	1	X

8.6 Manual settings

In the default operating mode of the TZA3054A ACE is switched on. This means that the input bandwidth and output slew rate are adjusted automatically using the built-in performance monitors. This allows for an optimum performance over the temperature range at all bit rates in combination with very low power consumption.

As well as the fully automatic mode, two other modes are available:

- Semi-automatic mode: manual selection of bit rate range with automatic bandwidth and slew rate adjustment within this range
- Full manual mode: manual selection of bandwidth and slew rate values.

Control is done via two I^{2}C-bus registers: BW (15h) for the input stage and SLEW (14h) for the output stage. Each register contains two control parameters: performance monitor control (BW[4:0] and SLEW[4:0] respectively) and the octave selection (BWOCT[2:0] and SLEWOCT[2:0] respectively).

An overview of the possible modes and the I^{2}C-bus control values is given in Table 4. The typical behavior of the rise and fall time in the different modes is illustrated in Figure 13. A similar picture can be made for the input bandwidth.

Table 4: **The possible modes and the I^{2}C-bus control values**

Mode	SLEW[4:0] = BW[4:0] = variable	SLEW[4:0] = BW[4:0] = 00000
SLEWOCT[2:0] = BWOCT[2:0] = 111	fully automatic	not applicable
SLEWOCT[2:0] = BWOCT[2:0] = variable	semi-automatic	manual mode

8.6.1 Fully automatic mode: automatic bandwidth and slew rate adjustment over all bit rates

In the default and fully automatic mode SLEWOCT[2:0] and BWOCT[2:0] are equal to 111, which means that ACE is switched on.

By default, the performance monitor control values BW[4:0] and SLEW[4:0] are set to 01011. This leads to a bandwidth that is equal to approximately 70 % of the input data rate, and the slew rate is adjusted so that the rise and fall times are equal to approximately 0.1 UI.

This mode gives a good trade off between performance and power consumption and is the recommended setting.

Optimization of the relative bandwidth and relative slew rate is possible by changing the BW[4:0] and OCT[4:0] values.

A low value for the bits BW[4:0] means that the bandwidth is maximized but still adjusted according to the incoming bit rate. Increasing the value means that the bandwidth will be smaller. This allows for optimization of the input stage with respect to the used optical receiver, i.e. (A)PD + TIA; see Figure 11.

A similar approach is possible with the bits SLEW[4:0]. A low value give fast edges on the output stage while increasing the value minimizes the slew rate. This allows for optimization of the output stage with respect to EMI/EMC and power consumption; see Figure 12.
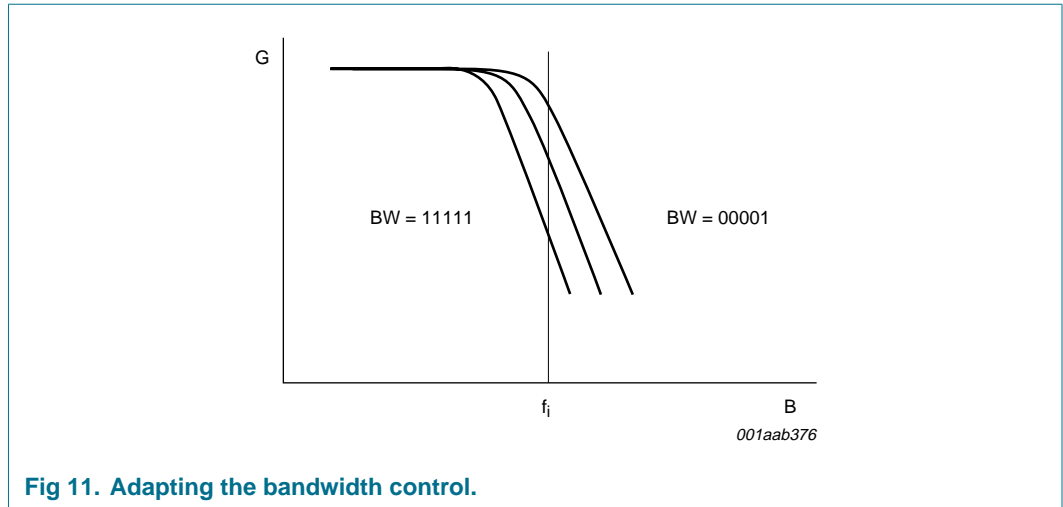
Fig 11. Adapting the bandwidth control.

(1) Slew = 00001.

(2) Slew = 11111.

The values are not based on measurements.
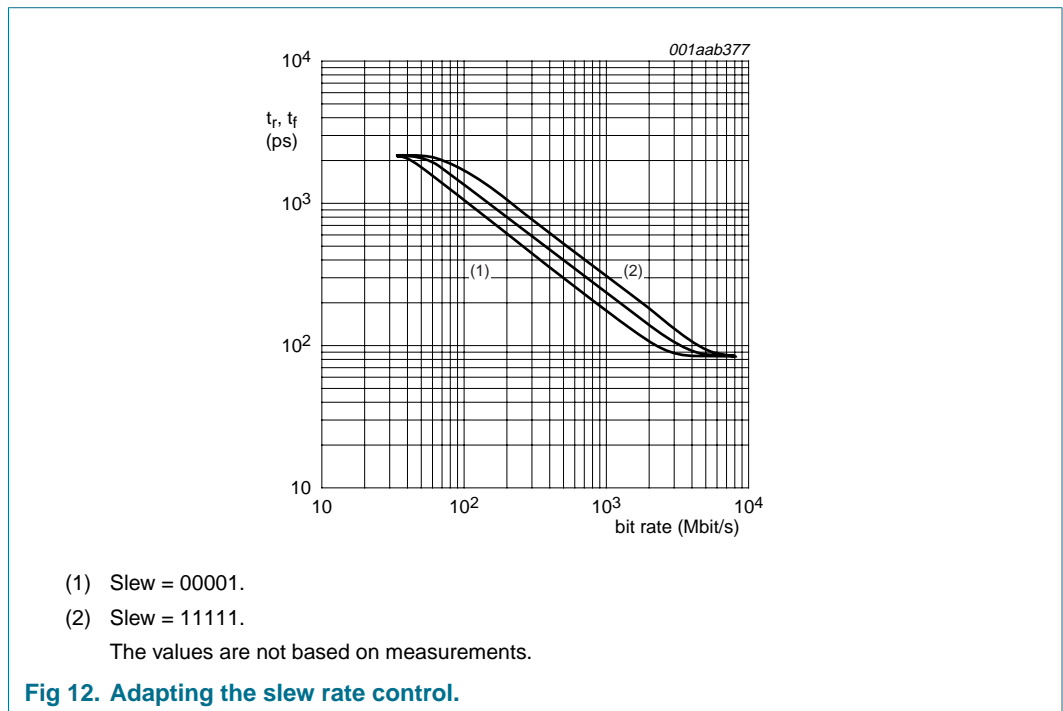
Fig 12. Adapting the slew rate control.

8.6.2 Semi-automatic mode: manual selection of bit rate range with automatic bandwidth and slew rate adjustment within this range

In this mode, the range of bit rates where the automatic selection of bandwidth and slew rate is operating is limited. However, within this range of bit rates, the optimum bandwidth and slew rate are automatically chosen.

This mode can be achieved by setting the SLEWOCT[2:0] and BWOCT[2:0] bits to the required range of bit rates. The ACE functionality is operating but limited to this range of bit rates.

Again, with the bits SLEW[4:0] and BW[4:0] further optimization of the relative bandwidth and relative slew rate is possible.

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Fig 13. Graphic overview of all modes for rise and fall time adjustment.

8.6.3 Full manual mode: manual selection of bandwidth and slew rate

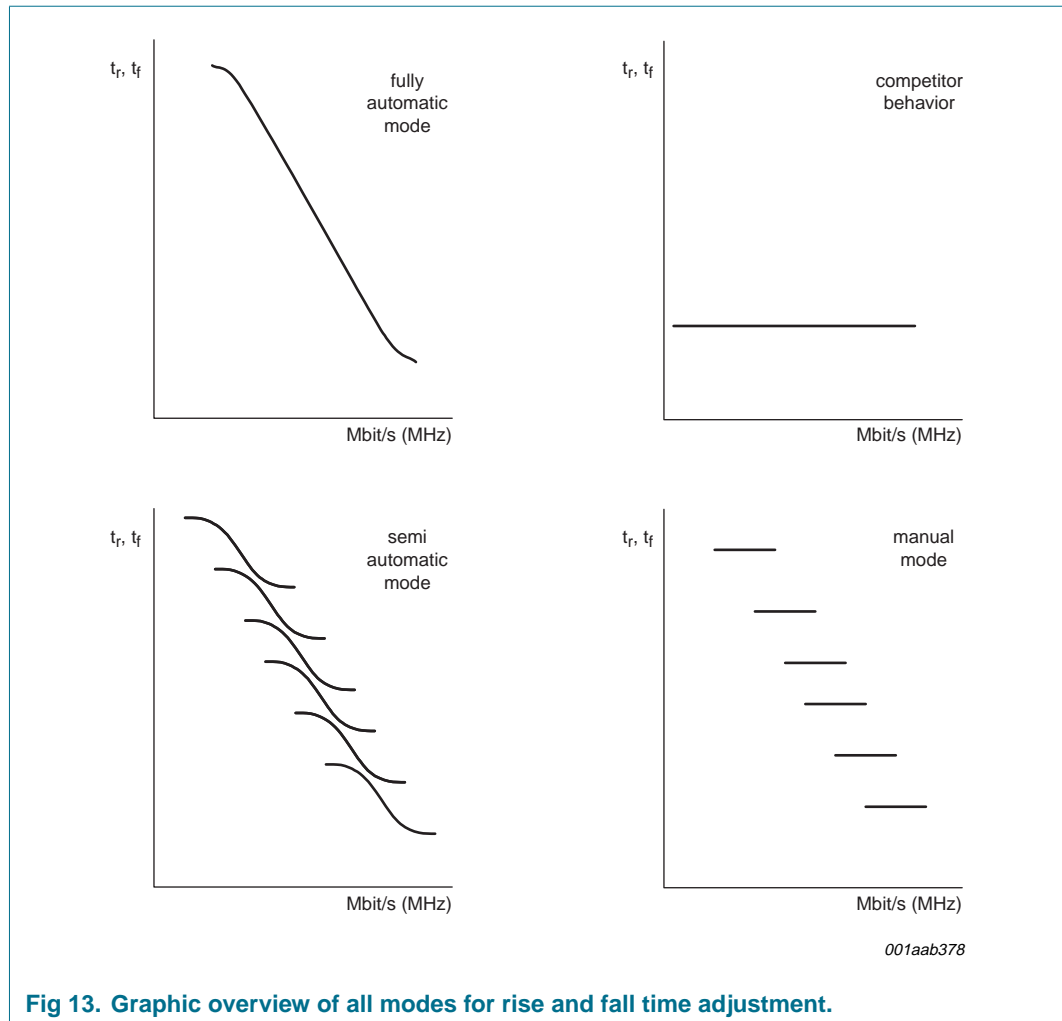By setting both BW[4:0] and SLEW[4:0] to 00000, the automatic bandwidth and the slew rate adjustment of the TZA3054A are completely switched off and the values for the bandwidth and slew rate can be controlled manually.

The bandwidth of the input stage and the slew rate of the output stage can be controlled with the bits BWOCT[2:0] in I^2C-bus register BW (15h) and the bits SLEWOCT[2:0] in I^2C-bus register SLEW (14h) respectively. By using the values given in Table 14 and Table 15 the right settings can be chosen.

In this mode the user gets 6 different limiting amplifiers, all optimized for their respective bandwidth range. The bandwidth spans from 1 kHz to the highest frequency of the chosen octave.

In the event that the DC cancellation loop is disabled as well, the lowest frequency is determined by the input coupling capacitor in combination with the input impedance. This enable burst mode operation.

8.7 I²C-bus

General characteristics of the I²C-bus can be found in "The I²C-bus specification", version 2.1, January 2000, available at "http://www.semiconductors.philips.com/buses/".

Table 5:   I²C-bus address (D2h)

A7	A6	A5	A4	A3	A2	A1	R/W
1	1	0	1	0	0	1	X

The TZA3054A contains both read only registers and read / write registers; see Table 6.

Table 6:   Address of all registers

Address	Name	Function	R/W	Default
00h	INTERRUPT	interrupt register	R	00h
01h	STATUS	status register	R	00h
08h	ADC_TJ	junction temperature ADC result register	R	00h
09h	ADC_VCC	supply voltage ADC result register	R	00h
0Ah	ADC_LLD	logarithmic level detect ADC result register	R	00h
0Bh	ADC_EXT	external voltage ADC result register	R	00h
0Ch	ADC_LOSTH	los threshold result register	R	00h
10h	LOSCNF	loss of signal detector configuration register	R/W	23h
11h	LOSTH	loss of signal threshold register	R/W	00h
12h	LIMCNF	limiter configuration register	R/W	B6h
13h	RFLVL	RF output configuration register	R/W	15h
14h	SLEW	RF output slew rate control register	R/W	08h
15h	BW	RF bandwidth control register	R/W	08h

8.7.1 Write protocol

During a write action, the I²C-bus controller in the TZA3054A allows one or more registers to be written to. Specifying the register address before writing the data is mandatory for each register; see Figure 14.
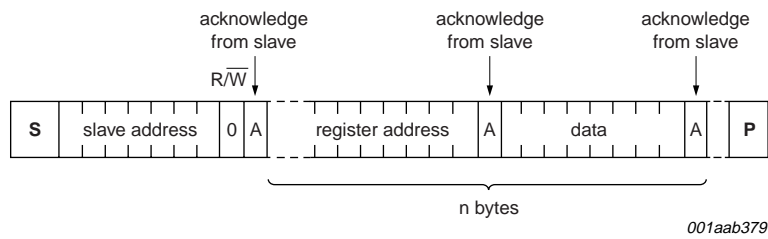
Fig 14. Write protocol.

8.7.2 Read protocol

During a read action, the I^{2}C-bus controller in the TZA3054A automatically increments the address pointer (auto-increment), allowing sequential registers to be read in a quick fashion; see Figure 15. Auto-increment reading is not possible when reading the ADC registers (08h, 09h, 0Ah, 0Bh and 0Ch); see Figure 16.
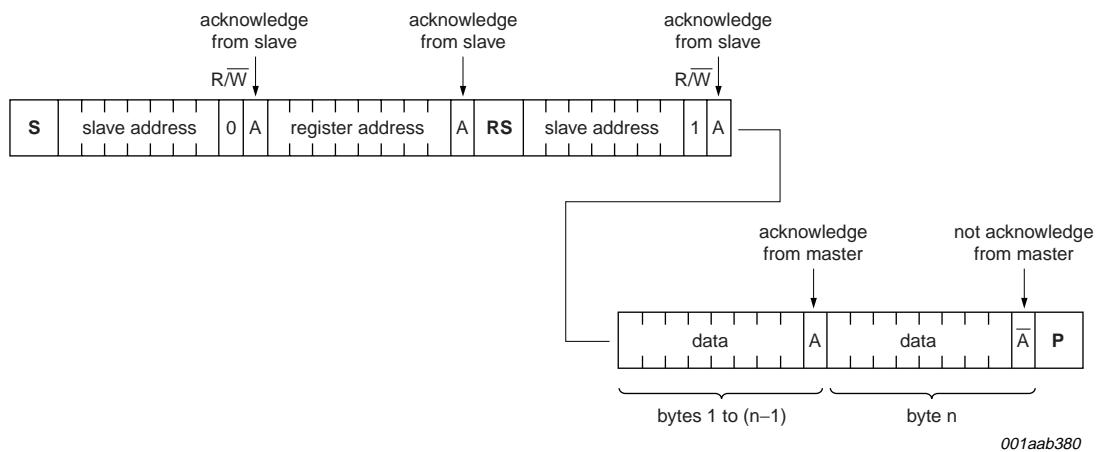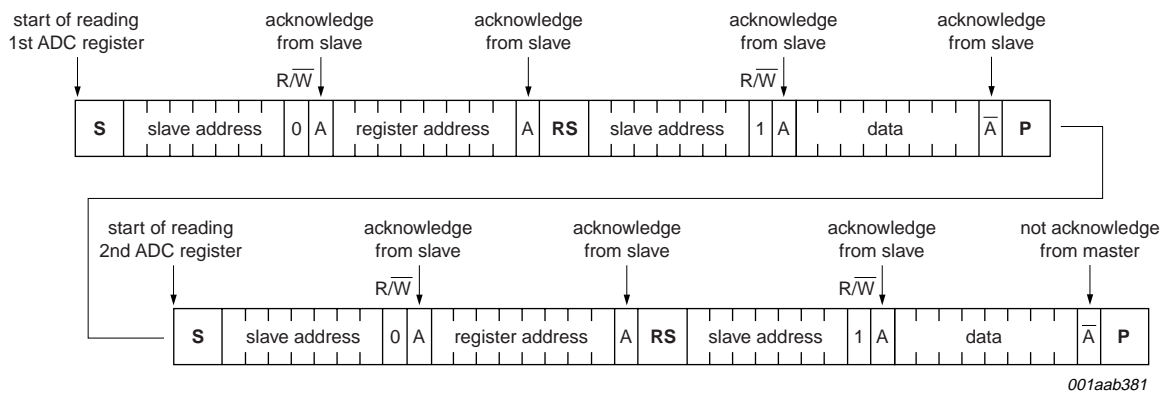

Fig 15. Auto-increment reading.

Fig 16. Example of reading two ADC registers.

Table 7: **INTERRUPT - I²C-bus register (address 00h) bit description**

Bit	Symbol	Description
7 to 3	-	reserved
2	LOS	Loss Of Signal
		1 = no signal present (loss of signal condition)
		0 = signal present (default value)
1	VCCALARM	supply voltage alarm
		1 = supply voltage < 3.0 V
		0 = supply voltage 3.0 V (default value)
0	TALARM	temperature alarm
		1 = junction temperature ≥ 125 °C
		0 = junction temperature < 125 °C (default value)

Table 8: **STATUS - I²C-bus register (address 01h) bit description**

Bit	Symbol	Description
7 to 3	-	reserved
2	LOS	Loss Of Signal
		1 = no signal present (loss of signal condition)
		0 = signal present (default value)
1	VCCALARM	supply voltage alarm
		1 = supply voltage < 3.0 V
		0 = supply voltage 3.0 V (default value)
0	TALARM	temperature alarm

Table 9: **ADC - I²C-bus register (address 08h. 09h, 0Ah, 0Bh and 0Ch) bit description**

Bit	Symbol	Description
7 to 0	ADC[7:0]	analog-to-digital conversion result [1]
		1 = maximum value
		0 = minimum value (default value)

[1]   For corresponding values, see Section 8.5.2.

Table 10: **LOSCNF - I²C-bus register (address 10h; default value = 23h) bit description**

Bit	Symbol	Description
7	-	reserved
6	LOSIOTYPE	loss of signal output polarity
		1 = CMOS
		0 = open-drain (default value)
5	LOSPOL	loss of signal output polarity
		1 = inverted (active LOW) (default value)
		0 = CMOS (active HIGH)
4	-	reserved

Table 10:   LOSCNF - I²C-bus register (address 10h; default value = 23h) bit description

Bit	Symbol	Description
3	I2CLOSTH	loss of signal detection
		1 = loss of signal detection set by I²C-bus
		0 = loss of signal detection set by pin LOSTH (default value)
2 to 0	HYST[2:0]	loss of signal detection hysteresis (default value = 011)
		000 = 0 dB
		001 = 1 dB
		010 = 2 dB
		011 = 3 dB
		100 = 4 dB
		101 = 5 dB
		110 = 6 dB
		111 = 7 dB

Table 11:   LOSTH - I²C-bus register (address 11h; default value = 00h) bit description

Bit	Symbol	Description
7 to 0	LOSTH[7:0]	loss of signal detection threshold
		1 = maximum LOS threshold, 1228 mV (p-p)
		0 = minimum LOS threshold, 0 mV (p-p) (default value)

Table 12:   LIMCNF - I²C-bus register (address 12h; default value = B6h) bit description

Bit	Symbol	Description
7 to 2	-	reserved
1	OFFSET	offset control
		1 = offset control on (default value)
		0 = offset control off
0	POLINV	limiter polarity
		1 = inverting
		0 = normal (default value)

Table 13:   RFLVL - I²C-bus register (address: 13h; default value = 15h) bit description

Bit	Symbol	Description
7	JAMI2C	jam function enabling [1]
		1 = JAM function enabled by I²C-bus
		0 = JAM function enabled by pin JAM (default value)
6	JAM	RF output jamming
		1 = output jammed with logic 0 on output
		0 = output not jammed (default value)
5	AUTOJAM	jam setting
		1 = automatic jamming in the event of LOS
		0 = no automatic jamming (default value)

Table 13:   RFLVL - I²C-bus register (address: 13h; default value = 15h) bit description

Bit	Symbol	Description
4	JAMPOL	jam input polarity
		1 = inverted (active LOW) (default value)
		0 = normal (active HIGH; CMOS)
3	I2CRFLVL	RF output signal level setting
		1 = I²C-bus setting enabled
		0 = pin LVL setting enabled (default value)
2 to 0	RFLVL[2:0]	RF output signal level (default value = 101)
		000 = RF output off, no dissipation in output stage
		001 = minimum RF output level, 500 mV (p-p) (differential)
		111 = maximum RF output level, 2000 mV (p-p) (differential)

[1]   Step size 250 mV (p-p) (differential).

Table 14:   SLEW - I²C-bus register (address: 14h; default value = E8h) bit description

Bit	Symbol	Description
7 to 5	SLEWOCT[7:5]	RF output slew rate octave selection
		000 = 3200 to 1800 Mbit/s
		001 = 1800 to 900 Mbit/s
		010 = 900 to 450 Mbit/s
		011 = 450 to 225 Mbit/s
		100 = 225 to 112 Mbit/s
		101 = 112 to 56 Mbit/s
		110 = reserved
		111 = fully automatic (default value)
4 to 0	SLEW[4:0]	RF output slew control (default value = 01011)
		00000 = automatic slew control off (selection with SLEWOCT)
		00001 = maximum slew rate (fastest edges)
		11111 = minimum slew rate (slowest edges)

Table 15:   BW - I²C-bus register (address: 15h; default value = E8h) bit description

Bit	Symbol	Description
7 to 5	BWOCT[7:5]	limiting amplifier bandwidth octave selection
		000 = 3200 to 1800 Mbit/s
		001 = 1800 to 900 Mbit/s
		010 = 900 to 450 Mbit/s
		011 = 450 to 225 Mbit/s
		100 = 225 to 112 Mbit/s
		101 = 112 to 56 Mbit/s
		110 = reserved
		111 = fully automatic (default value)

Table 15:   BW - I2C-bus register (address: 15h; default value = E8h) bit description

Bit	Symbol	Description
4 to 0	BW[4:0]	limiting amplifier bandwidth control (default value = 01011)
		00000 = automatic bandwidth control off (selection with BWOCT)
		00001 = highest bandwidth
		11111 = lowest bandwidth

9.   Limiting values

Table 16:   Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).; All voltages are referenced to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.3	+3.5	V
V_n	voltage on all input and output pins		−0.3	V_{CC} + 0.3	V
I_n	input current on pin		−1.0	+1.0	mA
T_{amb}	ambient temperature		−40	+85	°C
T_j	junction temperature		-	110	°C
T_{stg}	storage temperature		−65	+125	°C

10.   Thermal characteristics

Table 17:   Thermal characteristics
In compliance with JEDEC standards JESD51-5 and JESD51-7.

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	53	K/W

11. Characteristics

Table 18: Characteristics

$T_{amb} = -40\,^\circ C$ to $+85\,^\circ C$; $V_{CC} = 2.9\,V$ to $3.5\,V$; positive currents flow into the IC; all voltages are referenced to ground; all values apply to default configuration; ACE on, 2.5 Gbit/s; $V_o = 1500\,mV$ (p-p) (diff); LOS and LLD active; no jam; RF input values are listed as single-ended; RF output values are listed differential; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply: pins V$_{CCI}$ and V$_{CCO}$							
V$_{CC}$	supply voltage			2.9	3.3	3.5	V
I$_{CC(core)}$	core supply current	see Figure 17					
		OC48/STM-16; ACE on	[1]	10	20	26	mA
		OC48/STM-16; ACE off	[1]	9	17	21	mA
		GE; ACE off	[1]	5	12	15	mA
		OC3/STM-1; ACE off	[1]	5	9	10	mA
P$_{core}$	core power dissipation	OC48/STM-16, ACE on	[1]	35	67	90	mW
		OC48/STM-16, ACE off	[1]	33	57	74	mW
		GE, ACE off	[1]	20	41	54	mW
		OC3/STM-1, ACE off	[1]	19	30	38	mW
P$_{tot}$	total power dissipation	see Figure 17 and Figure 18					
		OC48/STM-16, ACE on	[1] [2] [3]	110	146	180	mW
		OC48/STM-16, ACE off	[1] [2] [3]	108	135	170	mW
		GE, ACE off	[1] [2] [3]	85	119	145	mW
		OC3/STM-1, ACE off	[1] [2] [3]	75	108	130	mW
RF input: pins IN and INQ							
V$_{i(p-p)}$	input voltage swing (peak-to-peak value)	limiting output		2.5	-	1200	mV
V$_{i(CM)}$	input common mode voltage		[4]	-	1.6	-	V
Z$_i$	input impedance	differential		80	100	120	Ω
f$_{-3dB}$	offset compensation low −3 dB cut-off frequency		[4]	-	1	-	kHz
DR	data rate			100	-	3200	Mbit/s
RF output; pins OUT and OUTQ							
V$_{o(p-p)}$	output voltage range (peak-to-peak value)	R$_{L(ext)}$ = 50 Ω (per pin)		400	-	2300	mV
	default output voltage (peak-to-peak value)	R$_{L(ext)}$ = 50 Ω (per pin)		1440	1570	1685	mV
Z$_o$	output impedance	single-ended to V$_{CC}$		60	75	90	Ω
t$_r$	rise time	20 % to 80 %; ACE OFF		-	40	-	ps
t$_f$	fall time	80 % to 20 %; ACE ON		-	0.1	-	UI
DJ$_{(p-p)}$	deterministic output jitter (peak-to-peak value)	R$_L$ = 50 Ω; V$_i$ = 100 mV; OC-48; K28.5 pattern		-	9	-	ps
RJ$_{(rms)}$	random output jitter (RMS value)	R$_L$ = 50 Ω; V$_i$ = 10 mV		-	2	-	ps

Table 18: **Characteristics** …continued

$T_{amb} = -40\,°C$ to $+85\,°C$; $V_{CC} = 2.9$ V to 3.5 V; positive currents flow into the IC; all voltages are referenced to ground; all values apply to default configuration; ACE on, 2.5 Gbit/s; $V_o = 1500$ mV (p-p) (diff); LOS and LLD active; no jam; RF input values are listed as single-ended; RF output values are listed differential; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Logarithmic level detect (LLD)						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)		1	-	1200	mV
S_{LLD}	LLD sensitivity	valid for input voltage above $V_i = 10$ mV (p-p) (SE)	14	17	20	mV/dB
V_{LLD}	LLD output voltage	$V_i = 10$ mV (p-p) (SE)	460	540	640	mV
Analog output; pin LLD						
Z_o	output impedance	[4]	-	2	10	Ω
$I_{O(source)}$	output source current		-	-	−1	mA
$I_{O(sink)}$	output sink current		-	-	1	mA
LOS detector						
hys	hysteresis	default value	-	3	-	dB
	hysteresis range		0	-	7	dB
t_a	assert time	$\Delta V_{i(p-p)} = 3$ dB	-	-	5	µs
t_d	de-assert time	$\Delta V_{i(p-p)} = 3$ dB	-	-	5	µs
Open-drain output; pin LOS (default)						
V_{OL}	LOW-level output voltage	$I_{OL} = 1$ mA	0	-	0.2	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC}$	-	-	10	µA
CMOS output; pin LOS (re-configured)						
V_{OL}	LOW-level output voltage	$I_{OL} = 1$ mA	0	-	0.2	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -1$ mA	$V_{CC} - 0.2$	-	V_{CC}	V
CMOS input; pin JAM and LVL						
V_{IL}	LOW-level input voltage		0	-	$0.33V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC}$	-	V_{CC}	V
I_{IL}	LOW-level input current	$V_{IL} = 0$ V	−200	-	-	µA
I_{IH}	HIGH-level input current	$V_{IH} = V_{CC}$	-	-	10	µA
Analog input; pin EXT						
V_I	input voltage		0	-	3.5	V
I_i	input current	[4]	-	-	10	µA
Z_i	input impedance	[4]	-	1	-	MΩ
Reference; pin RREF						
V_{ref}	reference voltage	10 kΩ resistor to GND	1.17	1.23	1.28	V

Table 18: **Characteristics** …*continued*

T_{amb} = −40 °C to +85 °C; V_{CC} = 2.9 V to 3.5 V; positive currents flow into the IC; all voltages are referenced to ground; all values apply to default configuration; ACE on, 2.5 Gbit/s; V_o = 1500 mV (p-p) (diff); LOS and LLD active; no jam; RF input values are listed as single-ended; RF output values are listed differential; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C-bus pins; SCL and SDA						
V_{IL}	LOW-level input voltage		0	-	$0.33V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC}$	-	V_{CC}	V
V_{hys}	hysteresis of Schmitt trigger inputs		$0.05V_{CC}$	-	-	V
V_{OL}	SDA LOW-level output voltage (open-drain)	I_{OL} = 3 mA	0	-	0.4	V
I_L	leakage current		-	-	-	µA
I_{IL}	LOW-level input current		−200	-	-	µA
I_{IH}	HIGH-level input current		-	-	10	µA
C_i	input capacitance		-	-	10	pF
I²C-bus timing						
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{LOW}	SCL LOW time		1.3	-	-	µs
$t_{HD;STA}$	hold time START condition		0.6	-	-	µs
t_{HIGH}	SCL HIGH time		0.6	-	-	µs
$t_{SU;STA}$	set-up time START condition		0.6	-	-	µs
$t_{HD;DAT}$	data hold time		0	-	0.9	µs
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{SU;STO}$	set-up time STOP condition		0.6	-	-	µs
t_r	SCL and SDA rise time		20	-	300	ns
t_f	SCL and SDA fall time		20	-	300	ns
t_{BUF}	bus free time between STOP and START		1.3	-	-	µs
C_b	capacitive load for each bus line		-	-	400	pF
t_{SP}	pulse width of allowable spikes		0	-	50	ns
V_{nL}	noise margin at LOW-level		$0.1V_{CC}$	-	-	V
V_{nH}	noise margin at HIGH-level		$0.2V_{CC}$	-	-	V

[1] Clarification of used abbreviations:

    a) OC3 and OC48 are SONET based standards, 155.52 Mbit/s and 2488.32 Mbit/s respectively.

    b) STM-1 and STM-16 are SDH based standards, 155.52 Mbit/s and 2488.32 Mbit/s respectively.

    c) GE is Gigabit Ethernet, 1250 Mbit/s.

[2] Adding both independent currents of Figure 17 and Figure 18 yields the total I_{CC}.

[3] Power listed is the power dissipated by the TZA3054A, excluding the power dissipated in the 50 Ω load.

[4] Guaranteed by design.
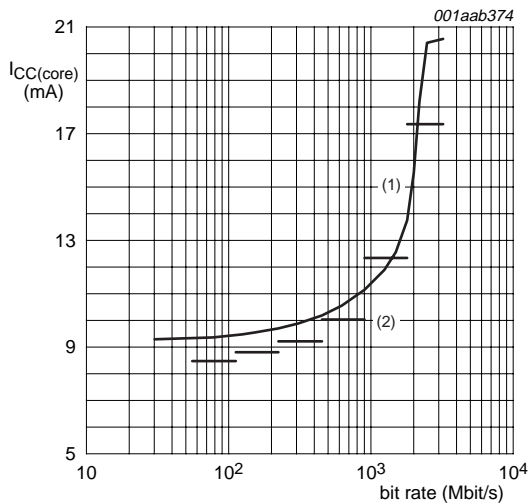
(1) ACE on.

(2) ACE off.

Fig 17. Core supply current as a function of bit rate.

Fig 18. RF output supply current as a function of output voltage swing.

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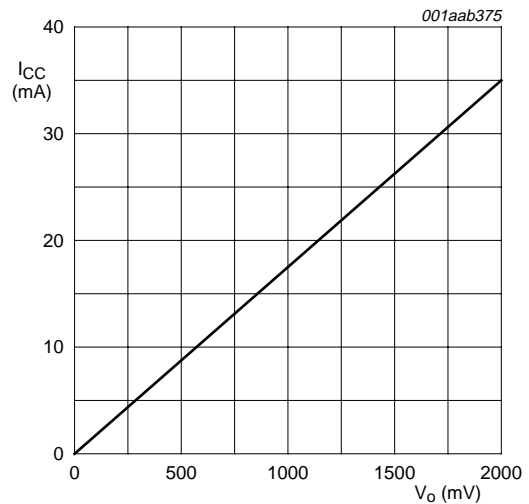
12. Package outline

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads;
20 terminals; body 4 x 3 x 0.85 mm

SOT797-1

DIMENSIONS (mm are the original dimensions)

UNIT	A[1] max.	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	3.1 2.9	1.75 1.45	0.5	2.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT797-1	- - -	- - -	- - -			03-03-19
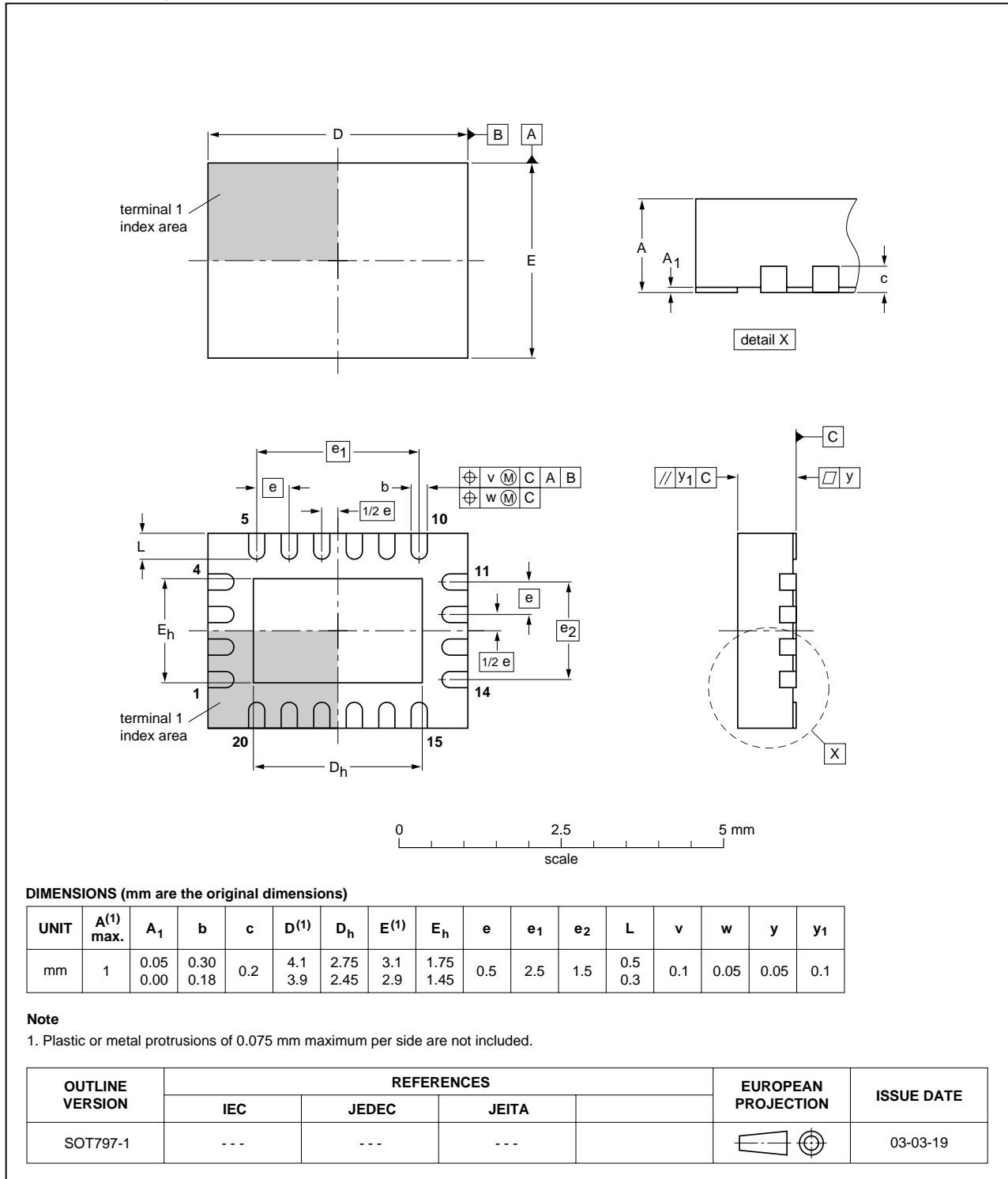
Fig 19. Package outline.

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness $\geq$ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume $\geq$ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

> – smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 19: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	**Reflow** [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

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[4]   These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5]   If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6]   Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7]   Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8]   Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9]   Hot bar soldering or manual soldering is suitable for PMFP packages.

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14. Revision history

Table 20: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
TZA3054A_1	20040812	Product data sheet	-	9397 750 13466	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1]   Please consult the most recently issued data sheet before initiating or completing a design.

[2]   The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3]   For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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18. Licenses

Purchase of Philips I²C-bus components

Purchase of Philips I²C-bus components conveys a license under the Philips' I²C-bus patent to use the components in the I²C-bus system provided the system conforms to the I²C-bus specification defined by Koninklijke Philips Electronics N.V. This specification can be ordered using the code 9398 393 40011.

19. Trademarks

A-rate — is a trademark of Koninklijke Philips Electronics N.V.

20. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

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