

TZA3046

Fiber Channel/Gigabit Ethernet transimpedance amplifier

Rev. 01 — 19 May 2006

Product data sheet

1. General description

The TZA3046 is a transimpedance amplifier with Automatic Gain Control (AGC), designed to be used in Fiber Channel/Gigabit Ethernet (FC/GE) fiber optic links. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage. It offers a current mirror of average photo current for RSSI monitoring to be used in SFF-8472 compliant modules.

The low noise characteristics makes it suitable for FC/GE applications, but also for FTTx applications.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

2. Features

- Low equivalent input noise current, typically 126 nA (RMS)
- Wide dynamic range, typically 2.5 μ A to 1.7 mA (p-p)
- Differential transimpedance of 7.5 k Ω (typical)
- Bandwidth from DC to 1050 MHz (typical)
- Differential outputs
- On-chip AGC with possibility of external control
- Single supply voltage 3.3 V, range 2.97 V to 3.6 V
- Bias voltage for PIN diode
- On-chip current mirror of average photo current for RSSI monitoring
- Identical ports available on both sides of die for easy bond layout and RF polarity selection

3. Applications

- Digital fiber optic receiver modules in telecommunications transmission systems, in high-speed data networks or in FTTx systems.

PHILIPS

4. Ordering information

Table 1: Ordering information

Type number	Package		Version
	Name	Description	
TZA3046U	-	bare die, dimensions approximately 0.82 mm × 1.3 mm	-

5. Block diagram

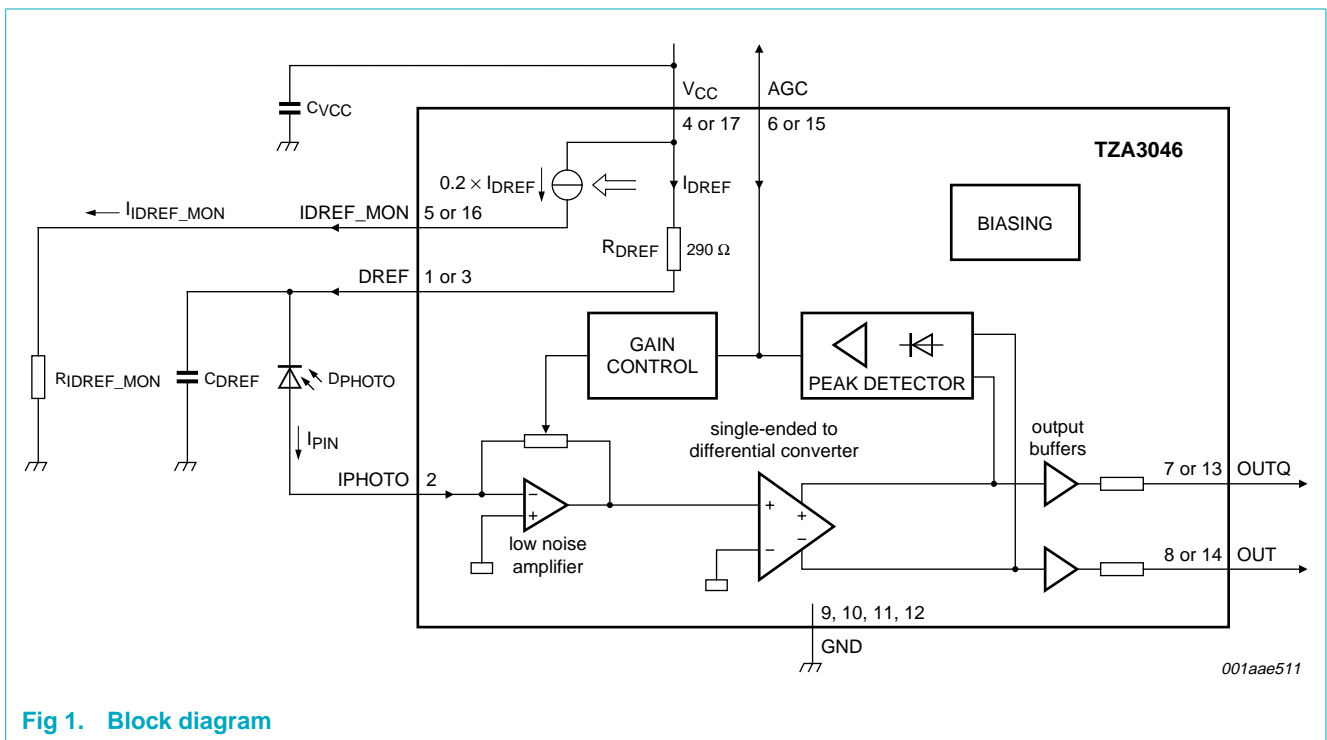


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

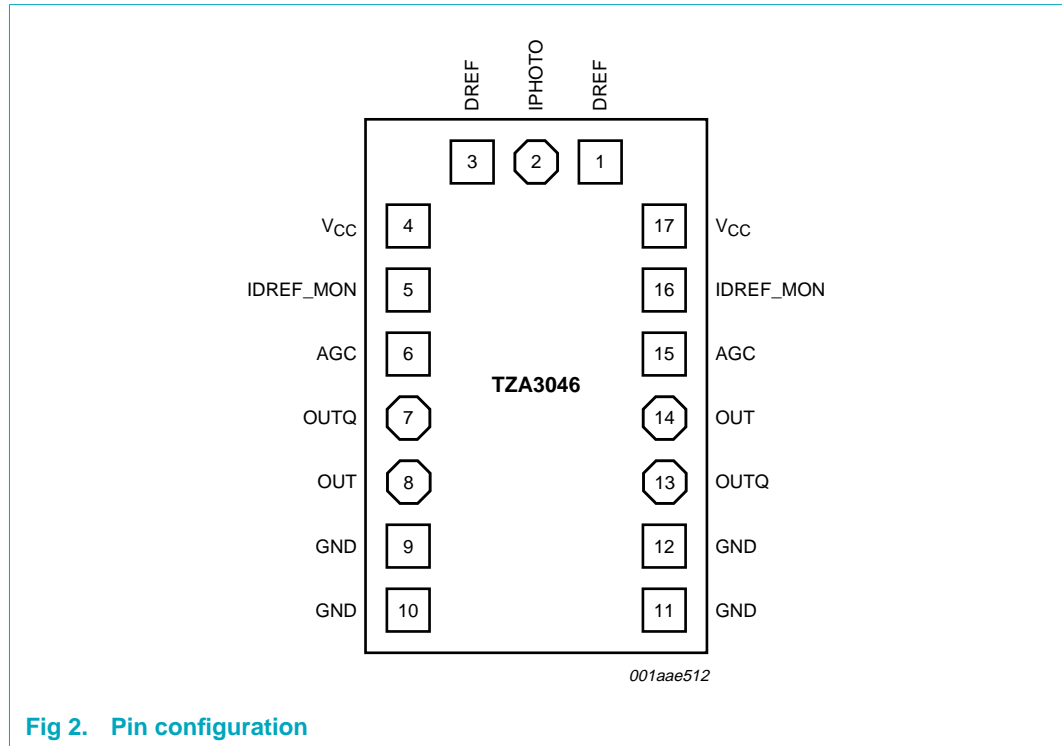


Fig 2. Pin configuration

6.2 Pin description

Table 2: Bonding pad description

Bonding pad locations with respect to the center of the die (see [Figure 10](#)); X and Y are in μm .

Symbol	Pad	X	Y	Type	Description
DREF	1	-493.6	140	output	bias voltage output for PIN diode; connect cathode of PIN diode to pad 1 or pad 3
IPHOTO	2	-493.6	0	input	current input; anode of PIN diode should be connected to this pad
DREF	3	-493.6	-140	output	bias voltage output for PIN diode; connect cathode of PIN diode to pad 1 or pad 3
V _{CC}	4	-353.6	-278.6	supply	supply voltage; connect supply voltage to pad 4 or pad 17
IDREF_MON	5	-213.6	-278.6	output	current output for RSSI measurements; connect a resistor to pad 5 or pad 16 and ground
AGC	6	-73.6	-278.6	input	AGC voltage; use pad 6 or pad 15
OUTQ	7	66.4	-278.6	output	data output; complement of pad OUT; use pad 7 or pad 13
OUT	8	206.4	-278.6	output	data output; use pad 8 or pad 14 [1]
GND	9	346.4	-278.6	ground	ground; connect together pads 9, 10, 11 and pad 12 as many as possible
GND	10	486.4	-278.6	ground	ground; connect together pads 9, 10, 11 and pad 12 as many as possible

Table 2: Bonding pad description ...continued

Bonding pad locations with respect to the center of the die (see [Figure 10](#)); X and Y are in μm .

Symbol	Pad	X	Y	Type	Description
GND	11	486.4	278.6	ground	ground; connect together pads 9, 10, 11 and pad 12 as many as possible
GND	12	346.4	278.6	ground	ground; connect together pads 9, 10, 11 and pad 12 as many as possible
OUTQ	13	206.4	278.6	output	data output; complement of pad OUT; use pad 7 or pad 13
OUT	14	66.4	278.6	output	data output; use pad 8 or pad 14 [1]
AGC	15	-73.6	278.6	input	AGC voltage; use pad 6 or pad 15
IDREF_MON	16	-213.6	278.6	output	current output for RSSI measurements; connect a resistor to pad 5 or pad 16 and ground
V _{CC}	17	-353.6	278.6	supply	supply voltage; connect supply voltage to pad 4 or pad 17

[1] These pads go HIGH when current flows into pad IPHOTO.

7. Functional description

The TZA3046 is a TransImpedance Amplifier (TIA) intended for use in fiber optic receivers for signal recovery in FC/GE or FTTx applications. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

The most important characteristics of the TZA3046 are high receiver sensitivity, wide dynamic range and large bandwidth. Excellent receiver sensitivity is achieved by minimizing transimpedance amplifier noise.

The TZA3046 has a wide dynamic range to handle the signal current generated by the PIN diode which can vary from 2.5 μA to 1.7 mA (p-p). This is implemented by an AGC loop which reduces the preamplifier feedback resistance so that the amplifier remains linear over the whole input range. The AGC loop hold capacitor is integrated on-chip, so an external capacitor is not required.

The bandwidth of TZA3046 is optimized for FC/GE application. It works from DC onward due to the absence of offset control loops. Therefore the amount of Consecutive Identical Digits (CID) will not effect the output waveform. A differential amplifier converts the output of the preamplifier to a differential voltage.

7.1 PIN diode connections

The performance of an optical receiver is largely determined by the combined effect of the transimpedance amplifier and the PIN diode. In particular, the method used to connect the PIN diode to the input (pad IPHOTO) and the layout around the input pad strongly influences the main parameters of a transimpedance amplifier, such as sensitivity, bandwidth, and PSRR.

Sensitivity is most affected by the value of the total capacitance at the input pad. Therefore, to obtain the highest possible sensitivity the total capacitance should be as low as possible.

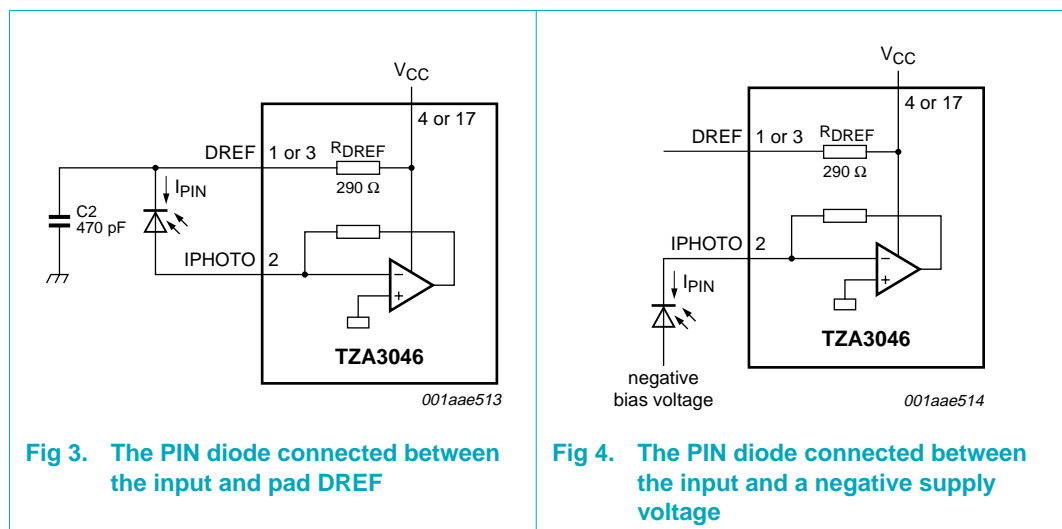
The parasitic capacitance can be minimized through:

1. Reducing the capacitance of the PIN diode. This is achieved by proper choice of PIN diode and typically a high reverse voltage.
2. Reducing the parasitics around the input pad. This is achieved by placing the PIN diode as close as possible to the TIA.

The PIN diode can be biased with a positive or a negative voltage. [Figure 3](#) shows the PIN diode biased positively, using the on-chip bias pad DREF. The voltage at DREF is derived from V_{CC} by a low-pass filter comprising internal resistor R_{DREF} and external capacitor $C2$ which decouples any supply voltage noise. The value of external capacitor $C2$ affects the value of PSRR and should have a minimum value of 470 pF. Increasing this value improves the value of PSRR. The current through R_{DREF} is measured and sourced at pad IDREF_MON, see [Section 7.3](#).

If the biasing for the PIN diode is done external to the IC, pad DREF can be left unconnected. If a negative bias voltage is used, the configuration shown in [Figure 4](#) can be used. In this configuration, the direction of the signal current is reversed to that shown in [Figure 3](#). It is essential that in these applications, the PIN diode bias voltage is filtered to achieve the best sensitivity.

For maximum freedom on bonding location, 2 outputs are available for DREF (pads 1 and 3). These are internally connected. Both outputs can be used if necessary. If only one is used, the other can be left open.



7.2 Automatic gain control

The TZA3046 transimpedance amplifier can handle input currents from 2.5 μA to 1.7 mA which is equivalent to a dynamic range of 56 dB (electrical equivalent with 28 dB optical). At low input currents, the transimpedance must be high to obtain enough output voltage, and the noise should be low enough to guarantee a minimum bit error rate. At high input currents however, the transimpedance should be low to prevent excessive distortion at the output stage. To achieve the dynamic range, the gain of the amplifier depends on the level of the input signal. This is achieved in the TZA3046 by an AGC loop.

The AGC loop comprises a peak detector and a gain control circuit. The peak detector detects the amplitude of the signal and stores it in a hold capacitor. The hold capacitor voltage is compared to a threshold voltage. The AGC is only active when the input signal level is larger than the threshold level and is inactive when the input signal is smaller than the threshold level.

When the AGC is inactive, the transimpedance is at its maximum. When the AGC is active, the feedback resistor value of the transimpedance amplifier is reduced, reducing its transimpedance, to keep the output voltage constant. [Figure 5](#) shows the transimpedance as function of the input current.

To reduce sensitivity to offsets and output loads, the AGC detector senses the output just before the output buffer. [Figure 6](#) shows the AGC voltage as function of the input current.

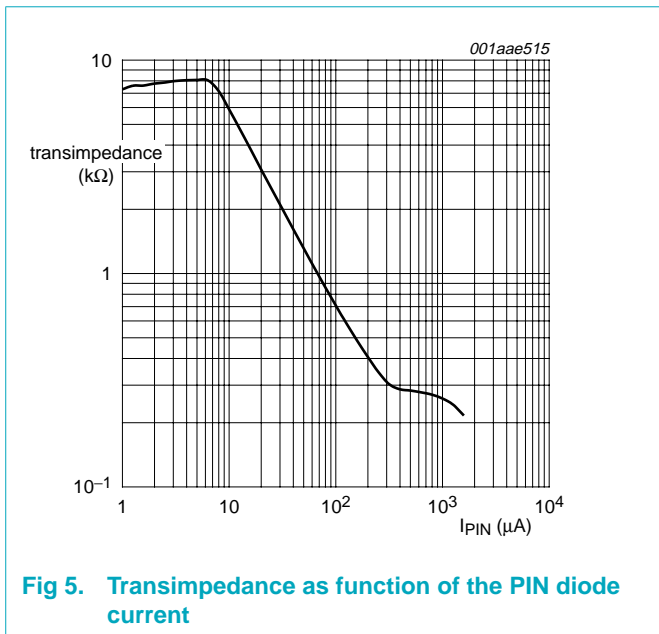


Fig 5. Transimpedance as function of the PIN diode current

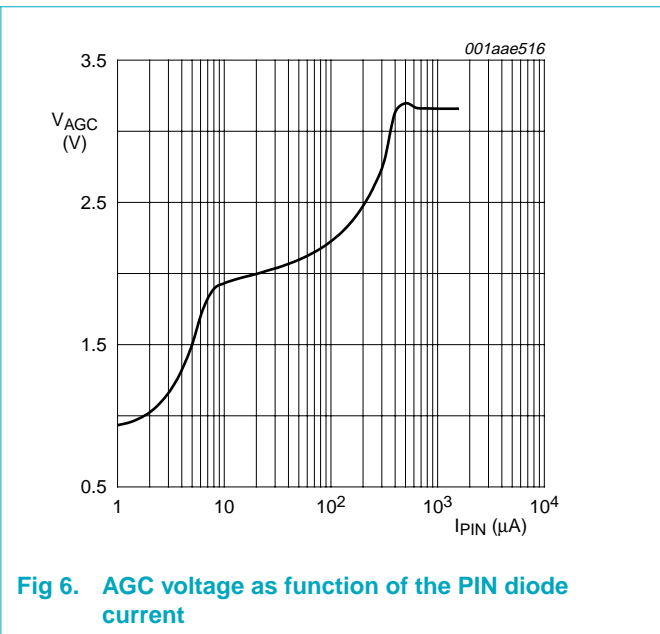
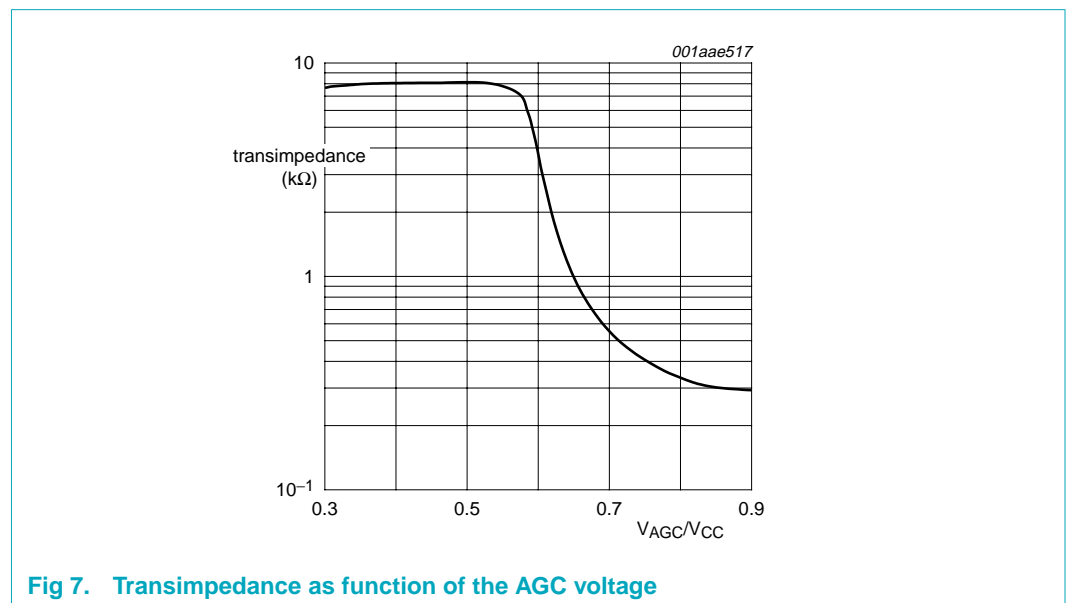


Fig 6. AGC voltage as function of the PIN diode current

For applications where the transimpedance is controlled by the TIA it is advised to leave the AGC pads unconnected to achieve fast attack and decay times.

The AGC function can be overruled by applying a voltage to pad AGC. In this configuration, connecting pad AGC to ground gives maximum transimpedance and connecting it to V_{CC} gives minimum transimpedance. This is depicted in [Figure 7](#). The AGC voltage should be derived from the V_{CC} for proper functioning.

For maximum freedom on bonding location, 2 pads are available for AGC (pads 6 and 15). These pads are internally connected. Both pads can be used if necessary.



7.3 Monitoring RSSI via IDREF_MON

To facilitate RSSI monitoring in modules (e.g. SFF-8472 compliant SFP modules), a current output is provided. This output gives a current which is 20 % of the average DREF current through the 290 Ω bias resistor. By connecting a resistor to the IDREF_MON output, a voltage proportional to the average input power can be obtained.

The RSSI monitoring is implemented by measuring the voltage over the 290 Ω bias resistor. This method is preferred over a simple current mirror because at small photo currents the voltage drop over the resistor is very small. This gives a higher bias voltage yielding better performance of the photodiode.

For maximum freedom on bonding location, 2 pads are available for IDREF_MON (pads 5 and 16). These pads are internally connected. Both pads can be used if necessary. If only one is used, the other can be left open.

8. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+3.8	V
V_n	voltage on any other pin	pad			
		IPHOTO	-0.5	+2.0	V
		OUT, OUTQ	-0.5	$V_{CC} + 0.5$	V
		AGC, IDREF_MON	-0.5	$V_{CC} + 0.5$	V
I_n	current on any other pin	pad			
		IPHOTO	-4.0	+4.0	mA
		OUT, OUTQ	-10	+10	mA
		AGC, IDREF_MON	-0.2	+0.2	mA
P_{tot}	total power dissipation		-	300	mW
T_{amb}	ambient temperature		-40	+85	°C
T_j	junction temperature		-	150	°C
T_{stg}	storage temperature		-65	+150	°C

9. Characteristics

Table 4: Characteristics

Typical values at $T_j = 25\text{ °C}$ and $V_{CC} = 3.3\text{ V}$; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages are measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.97	3.3	3.6	V
I_{CC}	supply current	AC-coupled; $R_{L(dif)} = 100\ \Omega$; excluding I_{DREF} and I_{IDREF_MON}	-	21	23	mA
P_{tot}	total power dissipation	$V_{CC} = 3.3\text{ V}$	-	70	76	mW
T_j	junction temperature		-40	-	+125	°C
T_{amb}	ambient temperature		-40	+25	+85	°C
R_{tr}	small-signal transresistance	measured differentially; AC-coupled, $R_{L(dif)} = 100\ \Omega$	5.5	7.5	10.5	k Ω
$f_{-3dB(h)}$	high frequency -3 dB point	$C_{PIN} = 0.5\text{ pF}$	800	1050	-	MHz
$I_{n(rms)(itg)(tot)}$	total integrated RMS noise current over bandwidth	referenced to input; $C_{PIN} = 0.5\text{ pF}$; $f_{-3dB(min)} = 875\text{ MHz}$	[1] -	126	164	nA

Automatic gain control loop: pad AGC

t_{att}	attack time	AGC pad unconnected	-	14	-	μs
t_{decay}	decay time	AGC pad unconnected	-	40	-	μs
$V_{th(AGC)(p-p)}$	peak-to-peak AGC threshold voltage	referenced to output; measured differentially	-	125	-	mV

Table 4: Characteristics ...continued

Typical values at $T_j = 25\text{ °C}$ and $V_{CC} = 3.3\text{ V}$; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages are measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bias voltage: pad DREF						
$R_{(DREF-VCC)}$	resistance between pin DREF and pin V_{CC}	tested at DC level; $T_{amb} = 25\text{ °C}$	260	290	320	Ω
TC_{RDREF}	temperature coefficient of R_{DREF}		-	0.33	-	$\Omega/^\circ\text{C}$
Input: pad IPHOTO						
$I_{IPHOTO(p-p)}$	peak-to-peak current on pad IPHOTO		[2][3] -1000	+1700	-	μA
$V_{bias(I)}$	input bias voltage		700	850	1000	mV
Monitor: pad IDREF_MON						
V_{mon}	monitor voltage		0	-	$V_{CC} - 0.4$	V
I_{IDREF_MON}/I_{DREF}	monitor current ratio	ratio I_{IDREF_MON} / I_{DREF}	19.5	20	20.5	%
$I_{offset(mon)}$	monitor offset current	$T_{amb} = 25\text{ °C}$	0	10	20	μA
$TC_{I(offset)mon}$	temperature coefficient of monitor offset current		-	30	-	$\text{nA}/^\circ\text{C}$
Data outputs: pads OUT and OUTQ						
$V_{O(cm)}$	common mode output voltage	AC-coupled; $R_{L(dif)} = 100\ \Omega$	-	$V_{CC} - 1.2$	-	V
$V_{O(dif)(p-p)}$	peak-to-peak differential output voltage	AC-coupled; $R_{L(dif)} = 100\ \Omega$				
		$I_{PIN} = 2.5\ \mu\text{A (p-p)} \times R_{tr}$	14	19	-	mV
		$I_{PIN} = 100\ \mu\text{A (p-p)}$	-	120	-	mV
		$I_{PIN} = 1500\ \mu\text{A (p-p)}$	[4] -	325	600	mV
$R_{O(dif)}$	differential output resistance	tested at DC level	-	100	-	Ω
t_r	rise time	20 % to 80 %; $I_{PIN} = 100\ \mu\text{A (p-p)}$	-	150	-	ps
t_f	fall time	80 % to 20 %; $I_{PIN} = 100\ \mu\text{A (p-p)}$	-	150	-	ps

[1] Guaranteed by design.

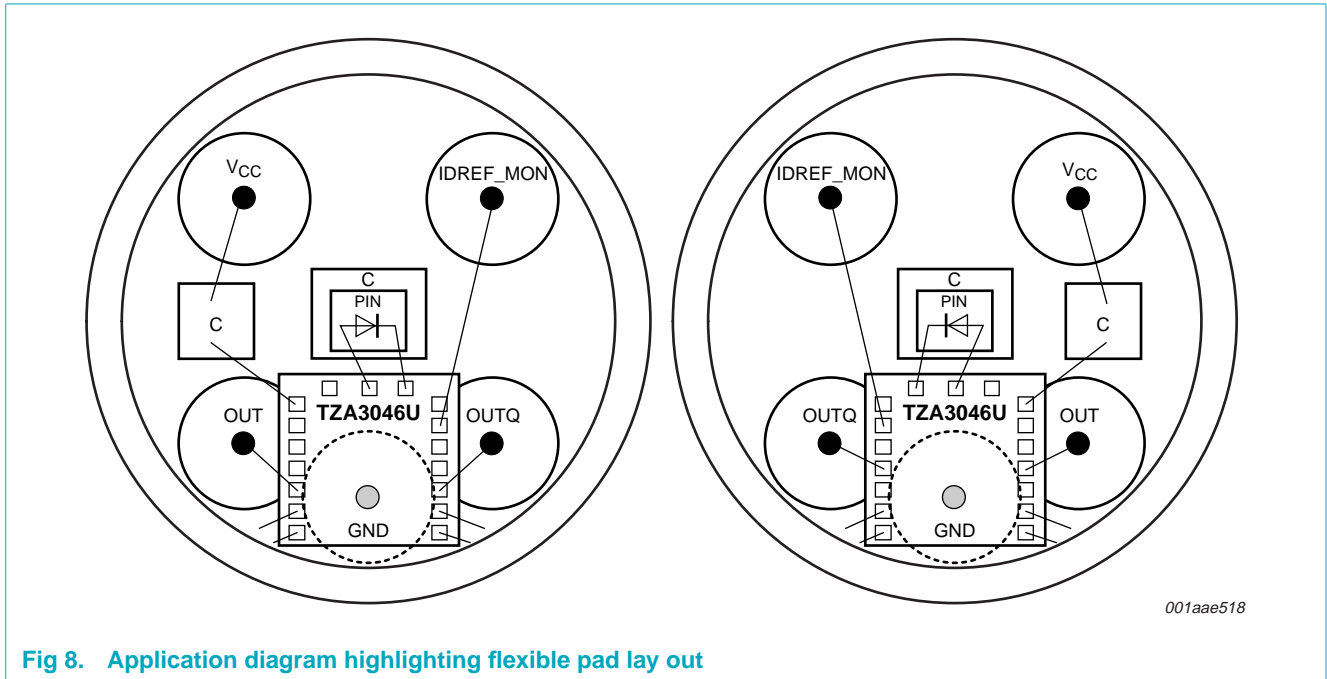
[2] Max input current is guaranteed for $BER < 10^{-10}$

[3] Max input current is guaranteed for $T_{amb} = 25^\circ$

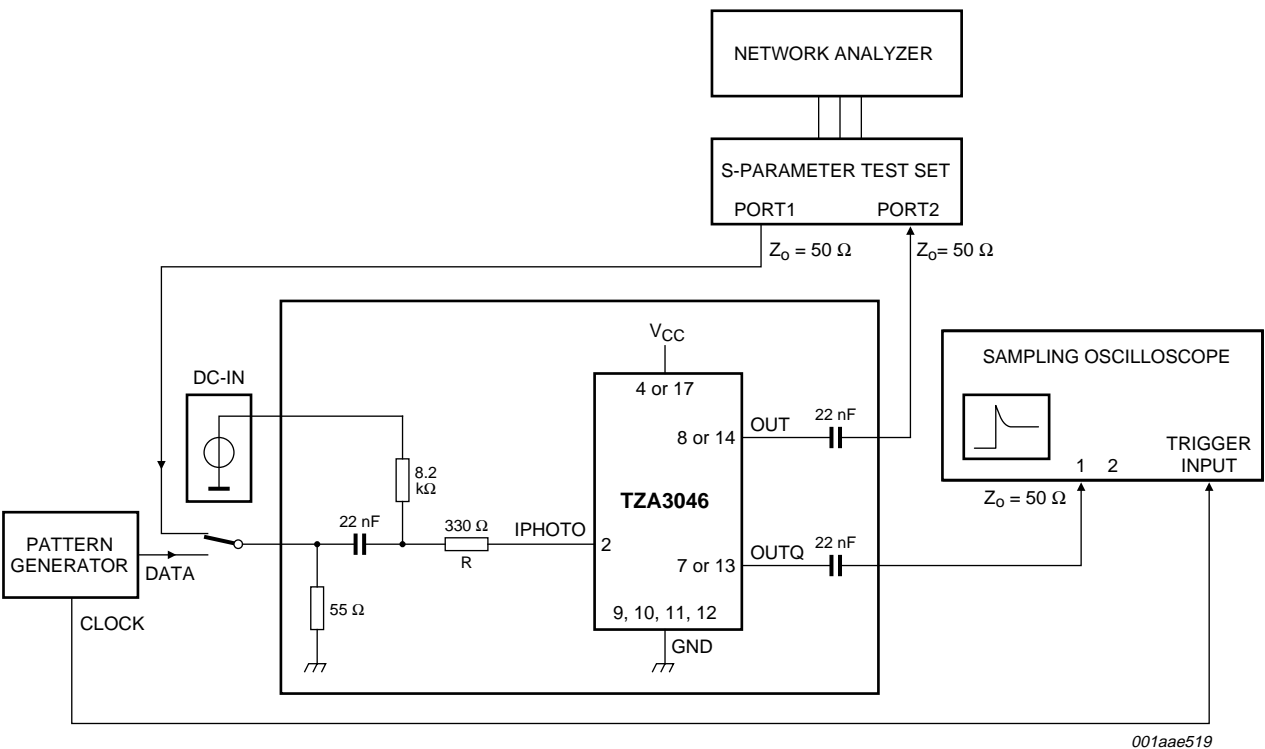
[4] Max value of 500 mV belongs to $I_{PIN} = 1250\ \mu\text{A (p-p)}$

10. Application information

For maximum freedom on bonding location, 2 outputs are available for OUT and OUTQ. The outputs should be used in pairs: pad 14 with pad 7 or pad 8 with pad 13. Pad 8 is internally connected with pad 14, pad 7 is internally connected with pad 13. The device is guaranteed with only one pair used. The other pair should be left open. Two examples of the bonding possibilities are shown in [Figure 8](#).



11. Test information



Total impedance of the test circuit ($Z_{tot(tc)}$) is calculated by the equation $Z_{tot(tc)} = s_{21} \times (R + Z_i) \times 2$, where s_{21} is the insertion loss of ports 1 and 2.
 Typical values: $R = 330 \Omega$, $Z_i = 30 \Omega$.

Fig 9. Test circuit

12. Bare die information

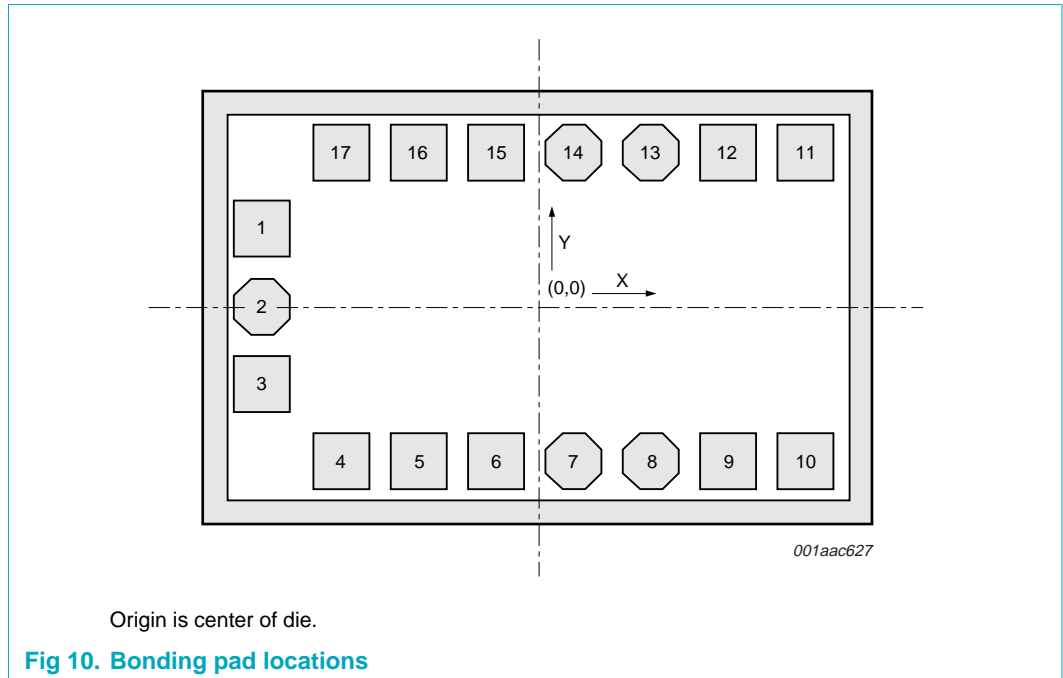


Table 5: Physical characteristics of the bare die

Parameter	Value
Glass passivation	0.3 μm PSG (PhosphoSilicate Glass) on top of 0.8 μm silicon nitride
Bonding pad dimension	minimum dimension of exposed metallization is 90 μm \times 90 μm (pad size = 100 μm \times 100 μm) except pads 2 and 3 which have exposed metallization of 80 μm \times 80 μm (pad size = 90 μm \times 90 μm)
Metallization	2.8 μm AlCu
Thickness	380 μm nominal
Die dimension	820 μm \times 1300 μm (\pm 20 μm^2)
Backing	silicon; electrically connected to GND potential through substrate contacts
Attach temperature	< 440 $^{\circ}\text{C}$; recommended die attach is glue
Attach time	< 15 s

13. Package outline

Not applicable.

14. Handling information

14.1 General

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

14.2 Additional information

Pad IPHOTO has limited protection to ensure good RF performance. This pad should be handled with extreme care.

15. Abbreviations

Table 6. Abbreviations

Acronym	Description
BER	Bit Error Rate
FTTx	Fiber To The "x"
OC3	Optical Carrier level 3 (155.52 Mbit/s)
PIN	Positive Intrinsic Negative
PSRR	Power Supply Rejection Ratio
RSSI	Received Signal Strength Indicator
SDH	Synchronous Digital Hierarchy
SFP	Small Form-factor Pluggable
SONET	Synchronous Optical NETwork
STM1	Synchronous Transport Module 1 (155.52 Mbit/s)

16. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TZA3046_1	20060519	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Philips Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Philips Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

17.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, Philips Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — Philips Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Philips Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a Philips Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Philips Semiconductors accepts no liability for inclusion and/or use of Philips Semiconductors products in such equipment or applications and therefore such inclusion and/or use is for the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — Philips Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.semiconductors.philips.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by Philips Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Bare die — All die are tested on compliance with all related technical specifications as stated in this data sheet up to the point of wafer sawing for a period of ninety (90) days from the date of delivery by Philips Semiconductors. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post-packing tests performed on individual die or wafers.

Philips Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

All die sales are conditioned upon and subject to the customer entering into a written die sale agreement with Philips Semiconductors through its legal department.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com

19. Contents

1	General description	1
2	Features	1
3	Applications	1
4	Ordering information	2
5	Block diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	4
7.1	PIN diode connections	4
7.2	Automatic gain control	6
7.3	Monitoring RSSI via IDREF_MON	7
8	Limiting values	8
9	Characteristics	8
10	Application information	10
11	Test information	11
12	Bare die information	12
13	Package outline	12
14	Handling information	13
14.1	General	13
14.2	Additional information	13
15	Abbreviations	13
16	Revision history	13
17	Legal information	14
17.1	Data sheet status	14
17.2	Definitions	14
17.3	Disclaimers	14
17.4	Trademarks	14
18	Contact information	14
19	Contents	15

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© Koninklijke Philips Electronics N.V. 2006. All rights reserved.

For more information, please visit: <http://www.semiconductors.philips.com>.

For sales office addresses, email to: sales.addresses@www.semiconductors.philips.com.

Date of release: 19 May 2006

Document identifier: TZA3046_1