DATA SHEET

TZA3017HW

30 Mbits/s up to 3.2 Gbits/s A-rate™ fibre optic transmitter

Product specification
Supersedes data of 2002 Jan 16

2003 May 14

Philips
Semiconductors

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30 Mbits/s up to 3.2 Gbits/s A-rate™ fibre optic transmitter

TZA3017HW

FEATURES

- Single 3.3 V power supply
- I²C-bus and pin programmable fibre optic transmitter.

Synthesizer features

- Supports SDH/SONET bit rates at 155.52, 622.08, 2488.32 and 2666.06 Mbits/s (STM16/OC48 + FEC)
- Supports Gigabit Ethernet at 1250 and 3125 Mbits/s
- Supports Fibre Channel at 1062.5 and 2125 Mbits/s
- Loss Of Lock (LOL) indicator
- ITU-T compliant jitter generation.

Multiplexer features

- 16:1, 10:1, 8:1 or 4:1 multiplexing ratio
- Rail-to-rail parallel inputs compliant with LVPECL, CML and LVDS
- 4-stage FIFO for wide tolerance to clock skew
- Supports co-directional and contra-directional clocking
- Programmable parity checking
- CML data and clock outputs, and loop mode inputs
- LVPECL outputs on parallel interface
- Line loop back input
- Diagnostic loop back output.

Additional features with the I²C-bus

- A-rate™(1) supports any bit rate from 30 Mbits/s to 3.2 Gbits/s with one reference frequency
- Programmable frequency resolution of 10 Hz
- Adjustable swings of data and clock outputs
- CML outputs on parallel interface
- Programmable polarity of all RF I/Os
- Exchangeable pin designations of RF clock with data for all I/Os for optimum connectivity
- Reversible pin designations of parallel data bus bits for optimum connectivity
- Four reference frequency ranges.

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APPLICATIONS

- Any optical transmission system with bit rates between 30 Mbits/s and 3.2 Gbits/s
- Physical interface IC in transmit channels
- Transponder applications
- Dense Wavelength Division Multiplexing (DWDM) systems.

GENERAL DESCRIPTION

The TZA3017HW is a fully integrated optical network transmitter, containing a clock synthesizer and a multiplexer with multiplexing ratios of 16:1, 10:1, 8:1 or 4:1.

The A-rate feature allows the IC to operate at any bit rate between 30 Mbits/s and 3.2 Gbits/s using a single reference frequency. The transmitter supports loop modes with serial clock and data inputs and outputs. All clock signals are generated using a fractional N synthesizer with 10 Hz resolution giving a true, continuous rate operation. For full configuration flexibility, the transmitter is programmable either by pin or via the I²C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3017HW	HTQFP100	plastic, heatsink thin quad flat package; 100 leads; body 14 × 14 × 1.0 mm	SOT638–1

BLOCK DIAGRAM

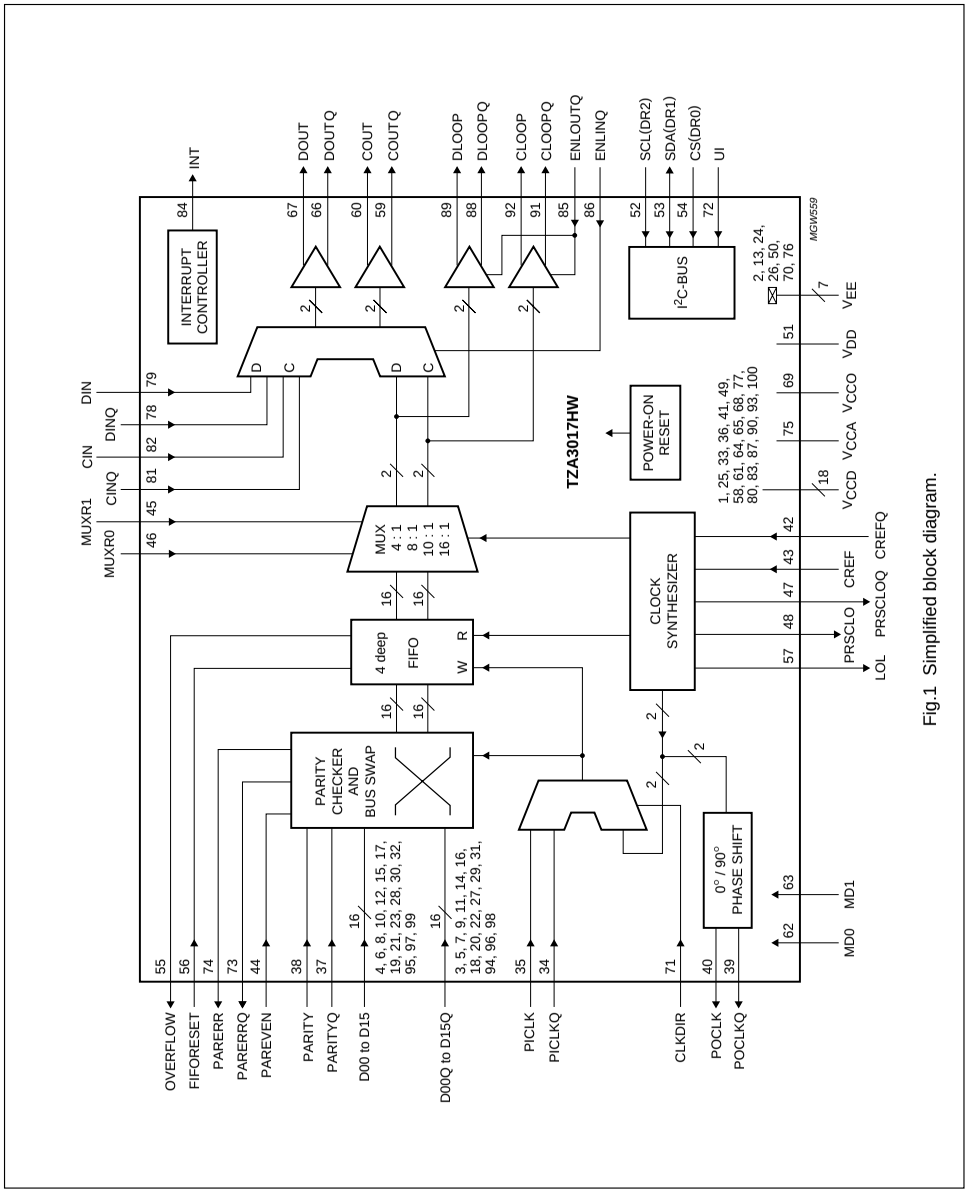


Fig.1 Simplified block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{EE}	die pad	common ground plane
V_{CCD}	1	supply voltage (digital part)
V_{EE}	2	ground
D12Q	3	parallel data input 12 inverted
D12	4	parallel data input 12
D11Q	5	parallel data input 11 inverted
D11	6	parallel data input 11
D10Q	7	parallel data input 10 inverted
D10	8	parallel data input 10
D09Q	9	parallel data input 09 inverted
D09	10	parallel data input 09
D08Q	11	parallel data input 08 inverted
D08	12	parallel data input 08
V_{EE}	13	ground
D07Q	14	parallel data input 07 inverted
D07	15	parallel data input 07
D06Q	16	parallel data input 06 inverted
D06	17	parallel data input 06
D05Q	18	parallel data input 05 inverted
D05	19	parallel data input 05
D04Q	20	parallel data input 04 inverted
D04	21	parallel data input 04
D03Q	22	parallel data input 03 inverted
D03	23	parallel data input 03
V_{EE}	24	ground
V_{CCD}	25	supply voltage (digital part)
V_{EE}	26	ground
D02Q	27	parallel data input 02 inverted
D02	28	parallel data input 02
D01Q	29	parallel data input 01 inverted
D01	30	parallel data input 01
D00Q	31	parallel data input 00 inverted
D00	32	parallel data input 00
V_{CCD}	33	supply voltage (digital part)
PICLKQ	34	parallel clock input inverted
PICLK	35	parallel clock input
V_{CCD}	36	supply voltage (digital part)
PARITYQ	37	parity input inverted
PARITY	38	parity input
POCLKQ	39	parallel clock output inverted
POCLK	40	parallel clock output
V_{CCD}	41	supply voltage (digital part)
CREFQ	42	reference clock input inverted
CREF	43	reference clock input
PAREVEN	44	parity select (odd or even)
MUXR1	45	multiplexing ratio select 1
MUXR0	46	multiplexing ratio select 0
PRSCLOQ	47	prescaler output signal inverted
PRSCLO	48	prescaler output signal
V_{CCD}	49	supply voltage (digital part)
V_{EE}	50	ground
V_{DD}	51	supply voltage (digital part)
SCL(DR2)	52	I^2C-bus serial clock (data rate select 2)
SDA(DR1)	53	I^2C-bus serial data (data rate select 1)
CS(DR0)	54	chip select (data rate select 0)
OVERFLOW	55	FIFO overflow alarm output
FIFORESET	56	FIFO reset input
LOL	57	loss of lock output
V_{CCD}	58	supply voltage (digital part)
COUTQ	59	serial clock output inverted
COUT	60	serial clock output
V_{CCD}	61	supply voltage (digital part)
MD0	62	parallel data input termination mode select 0
MD1	63	parallel data input termination mode select 1
V_{CCD}	64	supply voltage (digital part)
V_{CCD}	65	supply voltage (digital part)
DOUTQ	66	serial data output inverted
DOUT	67	serial data output
V_{CCD}	68	supply voltage (digital part)
V_{CCO}	69	supply voltage (clock generator)
V_{EE}	70	ground
CLKDIR	71	selection between co- and contra-directional clocking
UI	72	user interface select
PARERRQ	73	parity error output inverted
PARERR	74	parity error output
V_{CCA}	75	supply voltage (analog part)

SYMBOL	PIN	DESCRIPTION
V_{EE}	76	ground
V_{CCD}	77	supply voltage (digital part)
DINQ	78	loop mode data input inverted
DIN	79	loop mode data input
V_{CCD}	80	supply voltage (digital part)
CINQ	81	loop mode clock input inverted
CIN	82	loop mode clock input
V_{CCD}	83	supply voltage (digital part)
INT	84	interrupt output
ENLOUTQ	85	diagnostic loop back enable input (active LOW)
ENLINQ	86	line loop back enable input (active LOW)
V_{CCD}	87	supply voltage (digital part)
DLOOPQ	88	loop mode data output inverted
DLOOP	89	loop mode data output
V_{CCD}	90	supply voltage (digital part)

SYMBOL	PIN	DESCRIPTION
CLOOPQ	91	loop mode clock output inverted
CLOOP	92	loop mode clock output
V_{CCD}	93	supply voltage (digital part)
D15Q	94	parallel data input 15 inverted
D15	95	parallel data input 15
D14Q	96	parallel data input 14 inverted
D14	97	parallel data input 14
D13Q	98	parallel data input 13 inverted
D13	99	parallel data input 13
V_{CCD}	100	supply voltage (digital part)

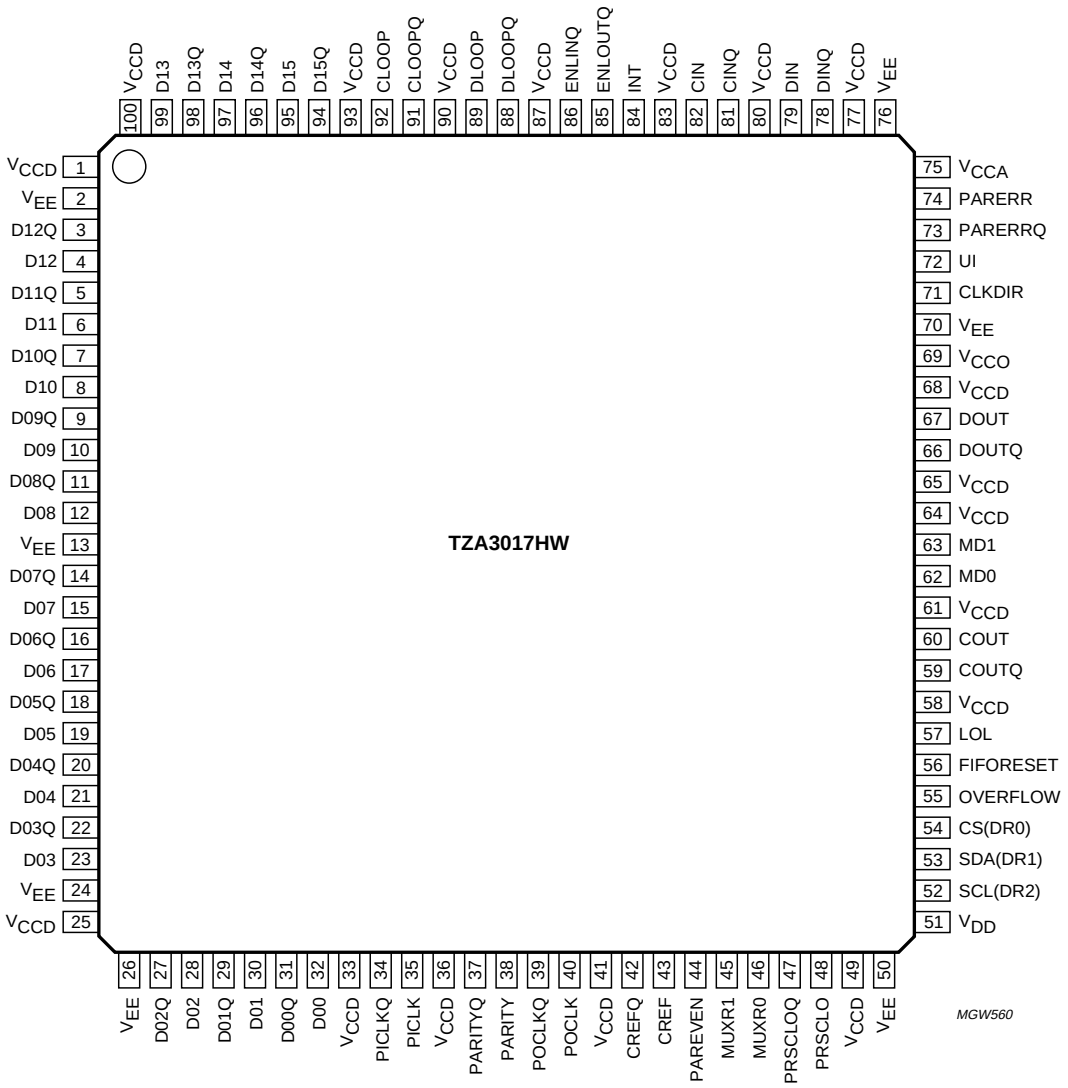


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TZA3017HW converts parallel input data into serial output data having a bit rate from 30 Mbits/s up to 3.2 Gbits/s. An internal clock synthesizer synchronizes the internal oscillator to an external reference frequency. The parallel input data is multiplexed at ratios of 16:1, 10:1, 8:1 or 4:1.

Choice of user interface control

The TZA3017HW can be controlled either via the I²C-bus or using programming pins DR0 to DR2. Pin UI selects the user interface required. I²C-bus control and A-rate functionality are enabled when pin UI is either open circuit or connected to V_{CC}. Pre-programmed mode is enabled when pin UI is connected to V_{EE}; see Table 1.

Table 1 Truth table for pin UI

UI	MODE	PIN 54	PIN 53	PIN 52
LOW	pre-programmed	DR0	DR1	DR2
HIGH	I²C-bus control	CS	SDA	SCL

In I²C-bus control mode, the chip is configured using I²C-bus pins SDA and SCL. During I²C-bus read or write actions, pin CS must be HIGH. When pin CS is LOW, the programmed configuration remains active, but pins SDA and SCL are ignored. This allows several TZA3017HWs in the application with the same I²C-bus address to be selected separately. The I²C-bus address of the TZA3017HW is shown in Table 2.

Table 2 I²C-bus address of the TZA3017HW

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	1	0	1	0	0	X

The function and content of the I²C-bus registers are described in Section “I²C-bus registers”. Some functions in the TZA3017HW can be controlled either by the I²C-bus or a designated pin. The method required is specified by an extra bit named I2C<pin name> in the corresponding I²C-bus register, for example, bit I2CPARITY in register MUXCNF2. The default is enable by pin.

If the application has no I²C-bus control, the IC has to operate with reduced functionality in pre-programmed mode. In pre-programmed mode, pins DR0 to DR2 are standard CMOS inputs that allow the selection of up to eight pre-programmed bit rates using an external reference clock frequency of 19.44 MHz; see Table 3.

Table 3 Truth table for selecting bit rate in pre-programmed mode (pin UI = V_{EE})

DR2	DR1	DR0	PROTOCOL	BIT RATE (Mbits/s)
LOW	LOW	LOW	STM1/OC3	155.52
LOW	LOW	HIGH	STM4/OC12	622.08
LOW	HIGH	LOW	STM16/OC48	2488.32
LOW	HIGH	HIGH	STM16 + FEC	2666.06
HIGH	LOW	LOW	GE	1250.00
HIGH	LOW	HIGH	10GE	3125.00
HIGH	HIGH	LOW	Fibre Channel	1062.50
HIGH	HIGH	HIGH	Fibre Channel	2125.00

After power-up, the TZA3017HW initiates a Power-On Reset (POR) sequence to restore the default settings of the I²C-bus registers, irrespective of the level on pin UI. The default settings are shown in Table 10.

Clock synthesizer

Refer to Fig.3. The clock synthesizer is a fractional N-type synthesizer which provides the A-rate™ functionality. It consists of a Voltage Controlled Oscillator (VCO), octave divider M, main divider N, fractional divider K, reference divider R, Phase Frequency Detector (PFD), integrated loop filter, Loss Of Lock (LOL) detection circuit, and a prescaler output buffer. The internal VCO is phase-locked to a reference clock signal of typically 19.44 MHz applied to pins CREF and CREFQ.

The clock synthesizer has a 22-bit fractional N capability which allows any combination of bit rate and reference frequency between 18 x R and 21 x R MHz, where R is the reference division factor. The LSB (bit k[0]) of the fractional divider, should be set to logic 1 to avoid limit cycles. These are cycles of less than maximum length that generate spurs in the frequency spectrum. This leaves 21 bits (k[21:1]) available for programming the fraction, allowing a resolution frequency of approximately 10 Hz at a fixed reference frequency.

The clock synthesizer does not require any external components, allowing easier application use.

To comply with most transmission standards, the reference frequency must be very accurate with minimum phase noise in order to synthesize a pure RF clock signal that complies with the strictest requirements for jitter generation; see Section “Jitter performance”.

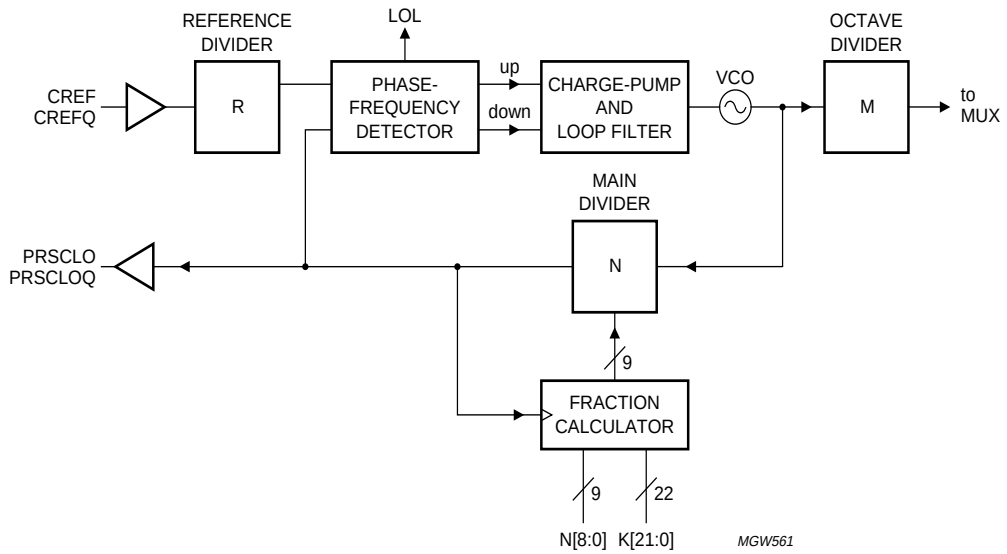


Fig.3 Block diagram of the clock synthesizer.

Programming the reference clock

Pre-programmed operation requires a reference clock frequency of between 18 and 21 MHz connected to pins CREF and CREFQ. However, to obtain the bit rates in Table 3, the reference clock frequency must be 19.44 MHz. For SDH/SONET applications, a reference clock frequency of 19.44 × R MHz is preferred.

I²C-bus control operation allows any one of four possible reference clock frequency ranges to be selected by programming reference divider R using bits REFDIV in I²C-bus register SYNTHCNF (address B6H).
The REFDIV bit settings, reference clock frequency ranges, and division factor are shown in Table 4.
The reference frequency is always divided internally to the lowest range of 18 to 21 MHz.

Table 4 Truth table for bits REFDIV in I²C-bus register SYNTHCNF

REFDIV	R DIVISION FACTOR	SDH/SONET REFERENCE FREQUENCY (MHz)	REFERENCE FREQUENCY RANGE (MHz)
00	1	19.44	18 to 21
01	2	38.88	36 to 42
10	4	77.76	72 to 84
11	8	155.52	144 to 168

Programming the clock synthesizer

The following dividers are used to program the clock synthesizer: the main divider N, the fractional divider K and the octave divider M.

The division factor for M is obtained by first determining in which octave the desired bit rate belongs as shown in Figure 4 and Tables 5 and 6.

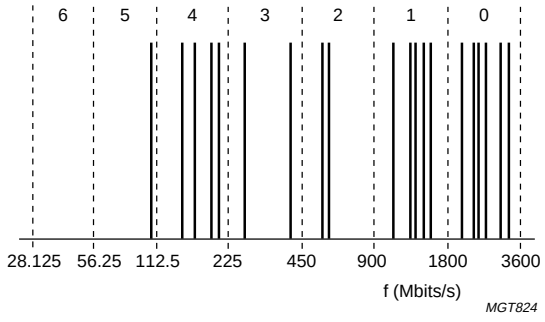


Fig.4 Allocation of octaves for common bit rates shown on a logarithmic scale.

Table 5 Octave designation and M division factor

LOWEST BIT RATE (Mbits/s)	HIGHEST BIT RATE (Mbits/s)	OCTAVE	M DIVISION FACTOR
1800	3200	0	1
900	1800	1	2
450	900	2	4
225	450	3	8
112.5	225	4	16
56.25	112.5	5	32
28.125	56.25	6	64

Table 6 Common optical transmission protocols and corresponding octaves

PROTOCOL	BIT RATE (Mbits/s)	OCTAVE
10GE	3125.00	0
2xHDTV	2970.00	0
STM16/OC48 + FEC	2666.06	0
STM16/OC48	2488.32	0
DV-6000	2380.00	0
Fibre Channel	2125.00	0
HDTV	1485.00	1
D-1 Video	1380.00	1
DV-6010	1300.00	1
Gigabit Ethernet (GE)	1250.00	1
Fibre Channel	1062.50	1
OptiConnect	1062.50	1
ISC	1062.50	1
STM4/OC12	622.08	2
DV-6400	595.00	2
Fibre Channel	425.00	3
OptiConnect	265.63	3
Fibre Channel	212.50	4
ESCON/SBCON	200.00	4
STM1/OC3	155.52	4
FDDI	125.00	4
Fast Ethernet	125.00	4
Fibre Channel	106.25	5
OC1	51.84	6

Once the octave and M division factor are known, the division factors for N and K can be calculated for a given reference frequency using the Flowchart in Fig.5.

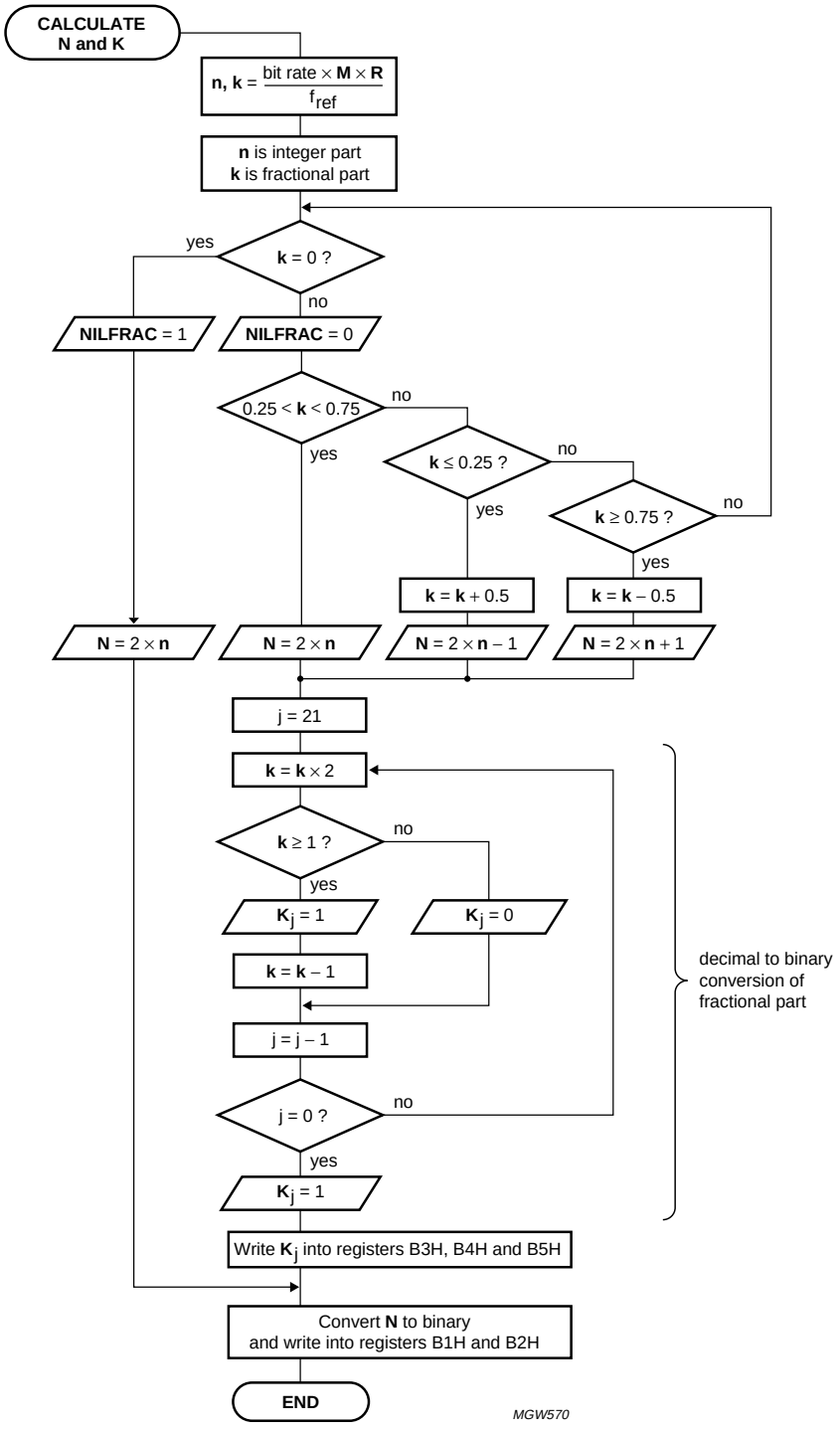


Fig.5 Flowchart for calculating N and K for the required bit rate.

The following examples refer to the flowchart in Fig.5.

Example 1: An SDH or SONET link has a bit rate of 2488.32 Mbits/s (STM16/OC48) that corresponds to octave 0 and an M division factor of 1. If the reference frequency f_{ref} at pins CREF and CREFQ is 77.76 MHz, the division factor R is required to be 4. The initial values for integer n and fractional part k are calculated using the equation:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2488.32\ \text{Mbits} \times 1 \times 4}{77.76\ \text{MHz}} = 128$$

In this example, n = 128 and k = 0. Since k is 0, fractional functionality is not required, so bit NILFRAC in I²C-bus register FRACN2 should be set to logic 1; see Table 19. $N = n \times 2 = 256$ with no further correction required. The resulting values of R = 4, M = 1 and N = 256 are set by I²C-bus registers SYNTHCNF (Table 22), DIVCNF (Table 16), MAINDIV1 (Table 17) and MAINDIV0 (Table 18).

Example 2: An SDH or SONET link has a bit rate of 2666.057143 Mbits/s ($15/14 \times 2488.32$ Mbits/s) (STM16/OC48 link with FEC) that corresponds to octave 0 and an M division factor of 1. If f_{ref} at pins CREF and CREFQ is 38.88 MHz, the division factor R is required to be 2. The values for n and k are calculated as follows:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2666.05714283\ \text{Mbits} \times 1 \times 2}{38.88\ \text{MHz}} = 137.1428571$$

In this example, n = 137 and k = 0.1428571. Fractional functionality is required, so bit NILFRAC in I²C-bus register FRACN2 should be set to logic 0. Since k is less than 0.25, k is corrected to $k = k + 0.5 = 0.6428571$, and N is corrected to $N = n \times 2 - 1 = 273$. The resulting values of R = 2, M = 1, N = 273 and K = 10 1001 0010 0100 1001 0011 are set by I²C-bus registers SYNTHCNF (Table 22), DIVCNF (Table 16), MAINDIV1 (Table 17), MAINDIV0 (Table 18), FRACN2 (Table 19), FRACN1 (Table 20) and FRACN0 (Table 21). The FEC bit rate is usually rounded up to 2666.06 Mbits/s, which actually gives a different value for k than in this example.

Example 3: A Fibre Channel link has a bit rate of 1062.50 Mbits/s that corresponds to octave 1 and an M division factor of 2. If f_{ref} at pins CREF and CREFQ is 19.44 MHz, the division factor R is required to be 1. The values for n and k are calculated as follows: $n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{1062.50\ \text{Mbits} \times 2 \times 1}{19.44\ \text{MHz}} = 109.3106996$

In this example, n = 109 and k = 0.3107. Fractional functionality is required, so bit NILFRAC in I²C-bus register FRACN2 should be set to logic 0. Since k is greater than 0.25 and less than 0.75, k does not need to be corrected. N is corrected to $N = n \times 2 = 218$. The resulting values of R = 1, M = 2, N = 218 and K = 01 0011 1110 0010 1000 0001 are set by I²C-bus registers SYNTHCNF (Table 22), DIVCNF (Table 16), MAINDIV1 (Table 17), MAINDIV0 (Table 18), FRACN2 (Table 19), FRACN1 (Table 20) and FRACN0 (Table 21).

Example 4: A non standard transmission link has a bit rate of 3012 Mbits/s that corresponds to octave 0 and an M division factor of 1. If f_{ref} at pins CREF and CREFQ is 20.50 MHz, the division factor R is required to be 1. The values for n and k are calculated as follows: $n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{3012\ \text{Mbits} \times 1 \times 1}{20.50\ \text{MHz}} = 146.9268293$

In this example, n = 146 and k = 0.9268293. Fractional functionality is required, so bit NILFRAC in I²C-bus register FRACN2 should be set to logic 0. Since k is greater than 0.75, k is corrected to $k = k - 0.5 = 0.4268293$, and N is corrected to $N = n \times 2 + 1 = 293$. The resulting values of R = 1, M = 1, N = 293 and K = 01 1011 0101 0001 0010 1011 are set by I²C-bus registers SYNTHCNF (Table 22), DIVCNF (Table 16), MAINDIV1 (Table 17), MAINDIV0 (Table 18), FRACN2 (Table 19), FRACN1 (Table 20) and FRACN0 (Table 21).

If the I²C-bus is not used, the clock synthesizer can be set up for the eight pre-programmed bit rates shown in Table 3, by pins DR0, DR1 and DR2 using an external reference clock frequency of 19.44 MHz.

Prescaler outputs

The frequency of prescaler outputs PRSCLO and PRSCLOQ is the VCO frequency divided by a ratio of N.K. If the synthesizer is in-lock, the frequency of the prescaler output is equal to the reference frequency at CREF and CREFQ divided by R. This provides an accurate reference that can be used by other phase locked loops in the application. If required, the polarity of the prescaler outputs can be inverted by setting bit PRSCLOINV in I^2C-bus register IOCNF2. If no prescaler information is required, its output can be disabled by setting bit PRSCLOEN to logic 0 in the same register. In addition, the prescaler output can be set for type of output, termination mode and signal amplitude. These parameter settings also apply to the parallel clock outputs POCLK and POCLKQ and parity error outputs PARERR and PARERRQ. For programming details; see Section “Configuring the parallel interface”.

Loss of Lock (LOL)

During normal operation, pin LOL should be LOW to indicate that the clock synthesizer is in-lock and that the output frequency corresponds to the programmed value. If pin LOL goes HIGH, phase and/or frequency lock is lost, and the output frequency may deviate from the programmed value. The LOL function is also available using I^2C-bus registers INTERRUPT and STATUS; see Sections “Interrupt register” and “Status register”.
If bit LOL in register INTERRUPT is not masked, a loss of lock condition will generate an interrupt signal at pin INT. Bit LOL is masked by default; see Section “Interrupt generation”.

Jitter performance

The clock synthesizer is optimized for minimum jitter generation. For all SDH/SONET bit rates, the generated jitter complies with ITU-T standard G.958 using a pure reference clock. To ensure negligible loss of performance, the reference signal should have a single sideband phase noise of better than −140 dBc/Hz, at frequencies of more than 12 kHz from the carrier. If reference divider R is used, this negative value is allowed to increase at approximately $20 \times \log (R)$.

Reference input

For optimum jitter performance and Power Supply Rejection Ratio (PSRR), the sensitive reference input should be driven differentially. If the reference frequency source (f_{ref}) is single-ended, the unused CREF or CREFQ input should be terminated with an impedance which matches the source impedance R_{source}; see Fig.6.
The PSRR can be improved by AC coupling the reference frequency source to inputs CREF and CREFQ. Any low frequency noise injected from the f_{ref} power supply will be attenuated by the resulting high-pass filter. The low cut-off frequency of the AC coupling must be lower than the reference frequency, otherwise the reference signal will be attenuated and the signal to noise ratio will be made worse. The value of coupling capacitor C is calculated using the formula: $C > \frac{1}{2\pi R_{source} f_{ref}}$

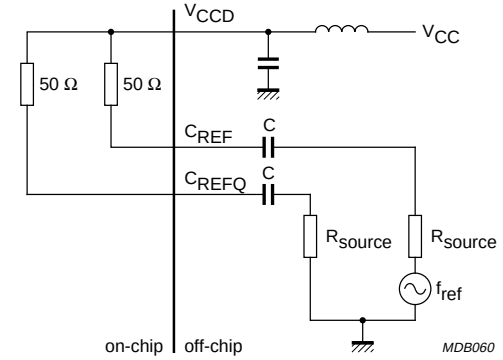


Fig.6 Reference input with single-ended clock source.

Multiplexer

The multiplexer comprises a high-speed input register, a 4-bit deep First In First Out (FIFO) elastic buffer, a parity check circuit and a multiplexing tree.

Parallel data bus clocking schemes

The TZA3017HW supports both co-directional and contra-directional clocking schemes for the parallel data bus; see Figs 7 and 8. The clocking scheme is selected by pin CLKDIR or I^2C-bus bit CLKDIR in I^2C-bus register MUXCNF1 (address A1H). Co-directional clocking is the default setting, and is selected when pin CLKDIR is HIGH or when I^2C-bus bit CLKDIR is set to logic 1.
With co-directional clocking selected, the incoming clock is applied to pins PICLK and PICLKQ and the input data is applied to pins D00 and D00Q to D15 and D15Q.
A parallel output clock is also available, if required, at pins POCLK and POCLKQ, and can be disabled by bit POCLKEN in I^2C-bus register MUXCNF1.

When contra-directional clocking is selected, any incoming clock at pins PICLK and PICLKQ is not used.
In contra-directional clocking mode, the incoming data on the parallel data bus is sampled by the internally generated parallel output clock. In this mode, the parallel data source must be clocked using the parallel output clock signal at pins POCLK and POCLKQ. To avoid timing problems, the clock signal at pins POCLK and POCLKQ can be phase shifted with respect to the internal clock in four 90 degree steps, controlled by bits POCLKINV and POPHASE in I²C-bus register MUXCNF1 (address A1H); see Table 7.

Table 7 Truth table for bits POCLKINV and POPHASE in I²C-bus register MUXCNF1

POCLKINV	POPHASE	PHASE SHIFT
0	0	0°
0	1	90°
1	0	180°
1	1	270°

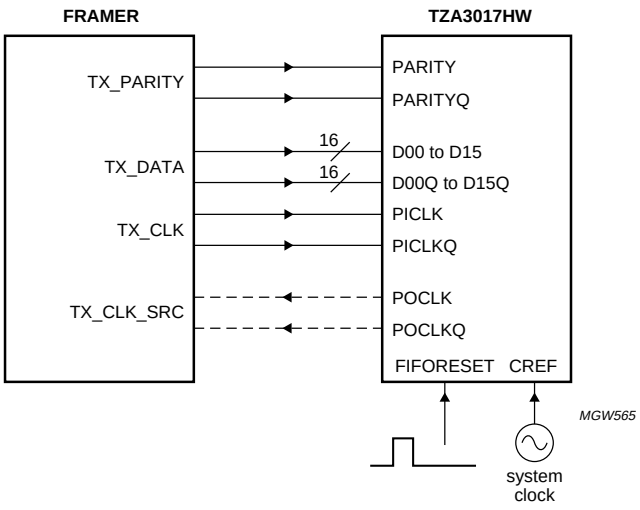


Fig.7 Co-directional clocking.

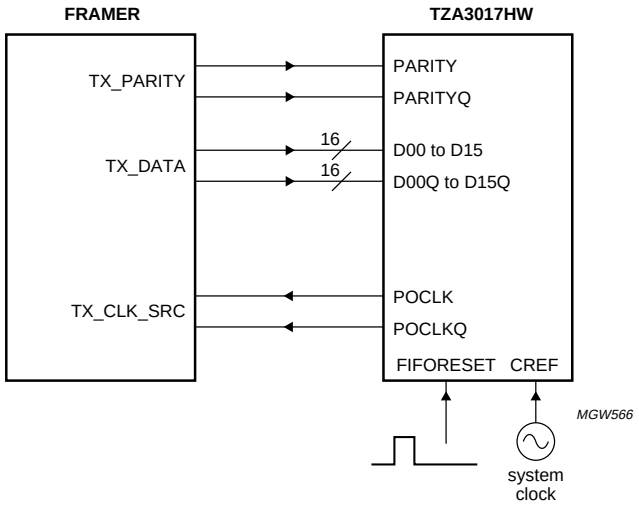


Fig.8 Contra-directional clocking.

FIFO

In the co-directional clocking scheme, the FIFO input register samples the incoming parallel data on the rising edge of the clock signal at pins PICLK and PICLKQ. Data is retrieved from the FIFO by an internal clock, derived from the multiplexing tree clock generator. This provides a high tolerance to jitter, or clock skew, at inputs on the parallel interface; the FIFO can compensate for brief phase deviations, or clock skew, of up to plus or minus 1 unit interval. Large phase deviations will most likely cause the FIFO to either overflow or underflow, and is indicated by bit OVERFLOW in both I^{2}C-bus registers INTERRUPT and STATUS; see Sections “Interrupt register” and “Status register”. A FIFO overflow is also indicated by a HIGH level at pin OVERFLOW. If bit OVERFLOW in register INTERRUPT is not masked, a FIFO overflow or underflow condition will generate an interrupt signal at pin INT; see Section “Interrupt generation”.

The overflow interrupt exists until the FIFO is reset by a HIGH level on pin FIFORESET or by setting bits FIFORESET and I2CFIFORESET in I^{2}C-bus register MUXCNF0 (address A2H). FIFORESET also initializes the FIFO. For optimum performance, the FIFO should be reset whenever there has been a Loss Of Lock condition, or whenever the bit rate is changed.

The FIFORESET signal is re-timed by the internal clock generator signal. The FIFO will initialize two clock cycles after FIFORESET goes HIGH and is operational two clock cycles after FIFORESET goes LOW. The FIFO can be initialized automatically when an overflow occurs by connecting pin OVERFLOW to pin FIFORESET.

Adjustable multiplexing ratio

For optimum layout connectivity, the physical positions of parallel data bus pins D00 and D00Q to D15 and D15Q on the chip are located either side of pin V_{EE} (pin 13). The number of parallel data bus inputs that are used depends on the multiplexing ratio selected by pins MUXR0 and MUXR1 or by bits MUXR in I^{2}C-bus register MUXCNF1 (address A1H). Any unused parallel data bus inputs are disabled. The configuration settings and active inputs for each multiplexing ratio are shown in Table 8.

In I^{2}C-bus control mode, the default multiplexing ratio is 16:1. For multiplexing ratios 16:1, 8:1 and 4:1, the MSB is transmitted first. For multiplexing ratio 10:1, the LSB is transmitted first.

To allow optimum layout connectivity, the pin designations of the parallel data bus bits can be reversed so that the default designated pin for the MSB is exchanged with the default designated pin for the LSB. This is implemented by bit BUSSWAP in I^2C-bus register MUXCNF2 (address A0H).

The highest supported speed for the parallel data bus is 400 Mbits/s. Therefore a multiplexing ratio of 4:1 will support bit rates of up to 1.6 Gbits/s.

Table 8 Setting multiplexing ratio

PIN MUXR1	PIN MUXR0	BITS MUX (REG. MUXCNF1)	MULTIPLEXING RATIO	ACTIVE INPUTS LSB to MSB
LOW	LOW	00	4:1	D06 to D09
LOW	HIGH	01	8:1	D04 to D11
HIGH	LOW	10	10:1	D03 to D12
HIGH	HIGH	11	16:1	D00 to D15

Parity checking

The parity checking function verifies the integrity of the incoming data on the parallel data bus. The calculated parity is compared to the parity expected at pins PARITY and PARITYQ. If these levels do not match, a parity error has occurred and pin PARERR goes HIGH during the next parallel clock period at pins PICLK and PICLKQ; (see Fig.9).

The calculated parity can be configured to be either odd or even by pin PAREVEN or by bit PARITY in I^2C-bus register MUXCNF2 (address A0H). Odd parity is configured by either a LOW level at pin PAREVEN or setting bit PARITY. The default setting for bit PARITY is even parity (logic 0).

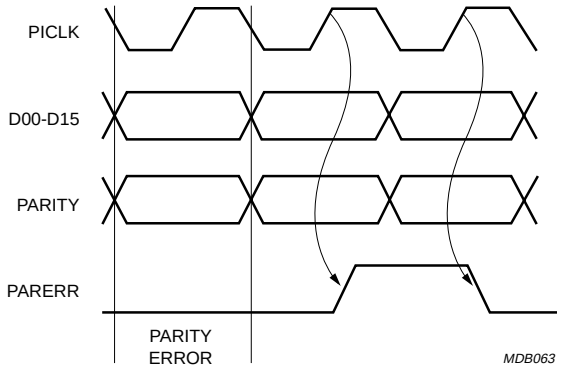


Fig.9 Parity timing.

Configuring the parallel interface

There are several options for configuring the parallel interface which comprises the parallel data bus and associated inputs and outputs. The options for parallel clock outputs POCLK and POCLKQ, parity error outputs PARERR and PARERRQ and prescaler outputs PRSCLO and PRSCLOQ are: output driver type, termination mode and output amplitude. I²C-bus register IOCNF2, bit MFOUTMODE selects either the CML or LVPECL output driver. The default is LVPECL. Bit MFOUTTERM sets the output termination mode to either standard LVPECL or floating termination, or in CML mode, to either DC or AC-coupled. In all cases, bits MFS adjust the amplitude. The default output amplitude is 850 mV (p-p), single-ended.

The signal polarity and selective enabling or disabling of POCLK, POCLKQ, PRSCLO and PRSCLOQ can also be configured. These options are set in I²C-bus registers MUXCNF1 (address A1H) and IOCNF2 (address C8H).

In I²C-bus register MUXCNF2 (address A0H), setting bit PDINV inverts the polarity of the parallel data. Setting bit PICLKINV inverts the co-directional input clock on pins PICLK and PICLKQ so that the clock edge is shifted by half a clock cycle, changing the rising edge to a falling edge. This function can be used to resolve a parallel data bus timing problem.

Rail-to-rail parallel data and clock inputs

The differential parallel data, parity and clock inputs, D00 to D15, D00Q to D15Q, PARITY, PARITYQ, PICLK, and PICLKQ can handle input swings from 100 mV, single-ended, to a maximum of 1000 mV. These rail-to-rail inputs can also accept any absolute value between V_{EE} and V_{CC}.

To keep the number of external components required to a minimum, most of the common standards: LVPECL, CML and LVDS are terminated internally; see Fig.10.

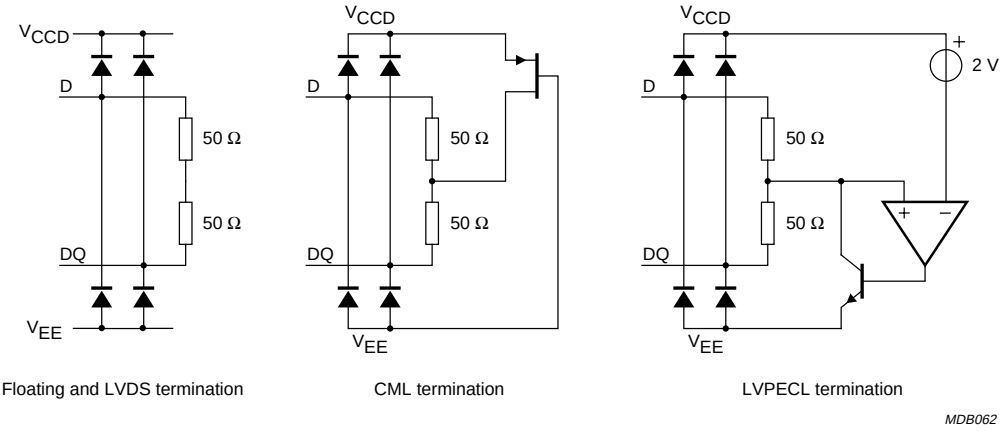


Fig.10 Rail-to-rail input termination configurations.

The termination mode is determined by pins MD0 and MD1; see Table 9.

Table 9 Input termination mode selection

PIN MD1	PIN MD0	INPUT MODE	TERMINATION
0	0	floating	100 Ω differential
0	1	LVDS	100 Ω differential (hysteresis on)
1	0	CML	50 Ω to V_{CC}
1	1	LVPECL	50 Ω to V_{CC} − 2 V

The LVDS mode has a differential hysteresis of 30 mV implemented by default. Setting bit PIHYST in I²C-bus register MUXCNF0 (address A2H) activates hysteresis for all input modes.

Loop mode I/Os

In line loopback mode, the internal data and clock routing switch selects serial data and clock signals from inputs DIN, DINQ, CIN, and CINQ instead of from the output of the multiplexer. Line loopback mode is activated by a LOW level on pin ENLINQ. Line loopback mode is also selected by setting bit ENLIN in I²C-bus register MUXCNF2 (address A0H).

In diagnostic loopback mode, the synthesized serial data and clock signals are available at loop mode output pins DLOOP and DLOOPQ, and CLOOP and CLOOPQ and at output pins DOUT and DOUTQ and COUT and COUTQ. Diagnostic loopback mode is activated by making pin ENLOUTQ LOW. Diagnostic loopback mode is also selected by setting bit ENLOUT in I²C-bus register MUXCNF2 (address A0H).

Configuring the RF I/Os

The polarity of specific RF serial data and clock I/O signals can be inverted using I²C-bus registers IOCNF0 (address CBH) and IOCNF1 (address CAH).

To allow easier connection to other ICs, the pin designations for input data can be exchanged with the pin designations for input clock. The pin designations for output data and output clock can also be exchanged.

The default pin designations for loop mode input data and clock are exchanged by setting bit CDINSWAP in I²C-bus register IOCNF1 so that signals at pins CIN and CINQ are treated as data and signals at pins DIN and DINQ are treated as clock.

The default pin designations for RF output data and clock are exchanged by setting bit CDOUTSWAP in I²C-bus register IOCNF1 so that signals at pins COUT and COUTQ are treated as data and signals at pins DOUT and DOUTQ are treated as clock.

The default pin designations for Loop mode output data and clock are exchanged by setting bit CDLOOPSWAP in I²C-bus register IOCNF0 (address CBH) so that loop mode output data is present at pins CLOOP and CLOOPQ and loop mode clock output is present at pins DLOOP and DLOOPQ.

Outputs DOUT and DOUTQ and COUT and COUTQ can be independently disabled by bits DOUTENA and COUTENA in I²C-bus register IOCNF1 (address CAH).

The amplitude of the RF serial output signals in CML drive mode, is adjustable (in 16 steps) between 70 mV (p-p) and 1100 mV (p-p), single-ended, controlled by bits RFS in I²C-bus register IOCNF0 (address CBH). The default amplitude is 280 mV (p-p), single-ended. The RF serial outputs can be either DC or AC-coupled, terminated by bit RFOUTTERM in I²C-bus register IOCNF0 (address CBH). The default termination is DC-coupled.

CMOS control inputs

CMOS control inputs UI, MUXR0, MUXR1, PAREVEN, CLKDIR, ENLOUTQ, ENLINQ, MD0, MD1, FIFORESET and CS(DR0) have an internal pull-up resistor so that these pins go HIGH when open circuit, and only go LOW when deliberately forced. This is also true for pins DR1 and DR2 in pre-programmed mode (pin UI is LOW). In I²C-bus control mode (pin UI is HIGH), pins SCL and SDA comply with the I²C-bus interface standard.

Power supply connections

Four separate supply domains (V_{DD}, V_{CCD}, V_{CCO} and V_{CCA}) provide isolation between the various functional blocks. Each supply domain should be connected to a common V_{CC} using a separate filter. **All supply pins, including the exposed die pad, must be connected**. The die pad connection to ground must have the lowest possible inductance. Since the die pad is also used as the main ground return of the chip, this connection must also have a low DC impedance. The voltage supply levels should be in accordance with the values specified in Chapters “Characteristics” and “Limiting values”.

All external components should be surface mounted, with a preferable size of 0603 or smaller. The components must be mounted as close to the IC as possible.

Interrupt register

The following events are recorded by setting the appropriate bit(s) in I²C-bus register INTERRUPT (address 00H):

- Loss of lock
- High junction temperature
- FIFO overflow or underflow.

When register INTERRUPT is polled by an I²C-bus read action, any set bits are reset. If a condition is still active, the corresponding bit remains set.

Status register

The current status of the conditions that are recorded by register INTERRUPT are indicated by setting the appropriate bit(s) in I²C-bus register STATUS (address 01H). A bit is set only for the period that the condition is active and resets when the condition clears. Register STATUS is polled by an I²C-bus read action.

Interrupt generation

An interrupt is generated if an interrupt condition sets a bit in I²C-bus register INTERRUPT (address 00H) and if the bit is not masked by I²C-bus register INTMASK (address CCH). Only the high junction temperature interrupt bit is not masked by default. A generated interrupt is indicated by an active logic level at pin INT.

The active output level used is set by bit INTPOL in I²C-bus register INTMASK. The default is an active LOW level. Bit INTOUT sets the output mode at pin INT to either open-drain or to standard CMOS. The default is open-drain. An active LOW output in open-drain mode allows several receivers to be connected together, and requires only one 3.3 kΩ pull-up resistor.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

Refer to Fig.11. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

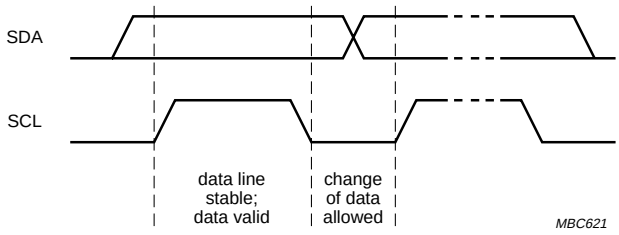


Fig.11 Bit transfer.

Start and stop conditions

Refer to Fig.12. Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

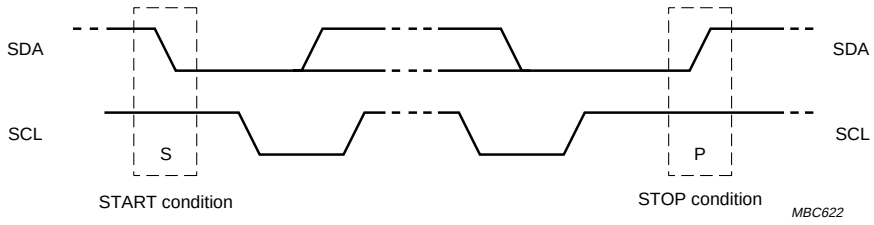


Fig.12 Definition of start and stop conditions.

System configuration

Refer to Fig.13. A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

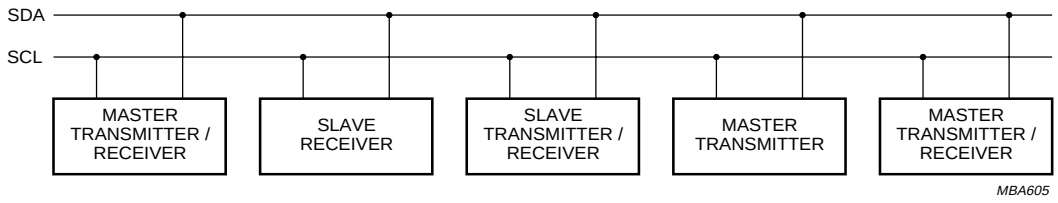


Fig.13 System configuration.

Acknowledge

Refer to Fig.14. Only one data byte is transferred between the start and stop conditions during a write from the transmitter to the receiver. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition; see Fig.17.

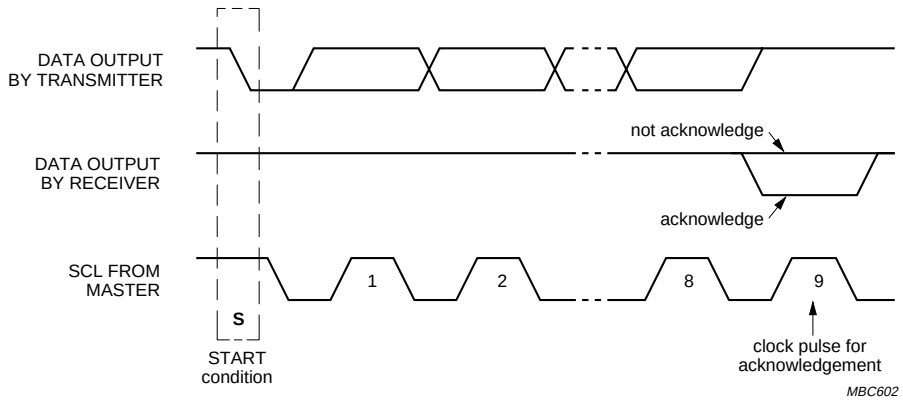


Fig.14 Acknowledgment on the I²C-bus.

I²C-BUS PROTOCOL

Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The address byte is sent after the start condition.

The master transmitter/receiver either reads from the read-registers or writes to the write-registers. It is not possible to read from and write to the same register. Figure 15 shows how the slave and register address bytes are defined.

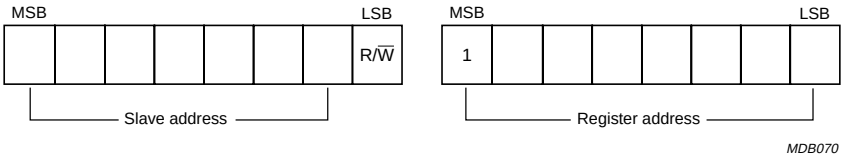


Fig.15 Slave and register addresses.

Read/Write protocols

The protocol for writing to a single register is shown in Fig.16. The transmitter sends the address of the slave device, waits for an acknowledge from the slave, sends register address, waits for an acknowledge from the slave, sends data byte, waits for an acknowledge from the slave, followed by a stop condition.

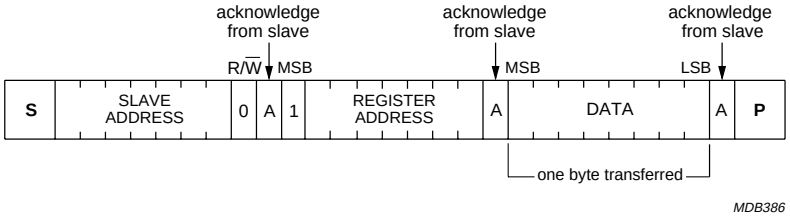
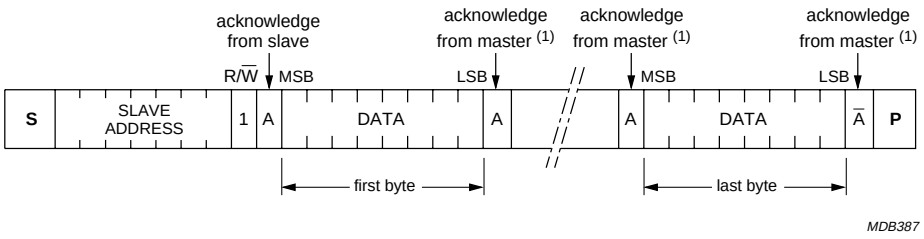


Fig.16 Write protocol.

The protocol for reading one or more registers is shown in Fig.17. The receiver sends the address of the slave device, waits for an acknowledge from the slave, receives data byte(s) from slave (the TZA3017AHW starts sending data after asserting an acknowledge), after receiving the data, the receiver sends an acknowledge or, if finished, a not-acknowledge, followed by a stop condition.



(1) The master receiver must signal an end of data to the slave transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave.

Fig.17 Read protocol.

I²C-bus registers

The I²C-bus registers are accessed in I²C-bus control mode by setting pin UI HIGH or leaving pin UI open circuit. Address and read/write data are transferred serially via pin SDA and clocked via pin SCL when pin CS (chip select) is HIGH. The I²C-bus registers are listed in Table 10.

Table 10 I²C-bus registers

ADDRESS (HEX)(1)	NAME	FUNCTION	DEFAULT VALUE	READ/ WRITE
00	INTERRUPT	Interrupt register; see Table 11	–	R
01	STATUS	Status register; see Table 12	–	R
A0	MUXCNF2	Multiplexer configuration register 2; see Table 13	0000 0000	W
A1	MUXCNF1	Multiplexer configuration register 1; see Table 14	0110 1001	W
A2	MUXCNF0	Multiplexer configuration register 0; see Table 15	0001 1000	W
B0	DIVCNF	Octave and loop mode configuration register; see Table 16	0000 0000	W
B1	MAINDIV1	Main divider division factor N; most significant byte; range 128 to 511; see Table 17	0000 0001	W
B2	MAINDIV0	Main divider division factor N; least significant byte; see Table 18	0000 0000	W
B3	FRACN2	Fractional divider division factor K; see Table 19	1000 0000	W
B4	FRACN1	Fractional divider division factor K; see Table 20	0000 0000	W
B5	FRACN0	Fractional divider division factor K; see Table 21	0000 0000	W
B6	SYNTHCNF	Clock synthesizer configuration register; see Table 22	0000 0000	W
C8	IOCNF2	Parallel interface output configuration register 2; see Table 23	0010 1100	W
CA	IOCNF1	RF serial I/O configuration register 1; see Table 24	1100 0000	W
CB	IOCNF0	RF serial output configuration register 0; see Table 25	0000 0011	W
CC	INTMASK	Interrupt masking register; see Table 26	0101 0000	W
FD	MUXTIMING	Multiplexer timing register; see Table 27	0000 1000	W

Note

1. Addresses not shown must not be accessed.

Table 11 Register INTERRUPT (address 00H)

BIT								PARAMETER	
7	6	5	4	3	2	1	0	DESCRIPTION	NAME
								clock synthesizer Loss of Lock (LOL)	LOL
							1	out of lock (loss of lock condition)	
							0	in lock	
				X	X	X		reserved	
								high junction temperature	TALARM
			1					junction temperature ≥ 130 °C	
			0					junction temperature < 130 °C	
								FIFO overflow or underflow	OVERFLOW
		1						overflow or underflow	
		0						normal operation	
0	0							reserved	

Table 12 Register STATUS (address 01H)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								clock synthesizer Loss of Lock (LOL)	LOL
							1	out of lock (loss of lock condition)	
							0	in lock	
				X	X	X		reserved	
								high junction temperature	TALARM
			1					junction temperature ≥ 130 °C	
			0					junction temperature < 130 °C	
								FIFO overflow or underflow	OVERFLOW
		1						overflow or underflow	
		0						normal operation	
0	0							reserved	

Table 13 Register MUXCNF2 (address A0H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								parallel data bus bit designations	BUSSWAP
							1	D00 = MSB, D15 = LSB (reversed)	
							0	D15 = MSB, D00 = LSB (normal)	
								parity checking	PARITY
						1		odd parity	
						0		even parity	
								parity programming	I2CPARITY
					1			via I^2C-bus interface	
					0			via pin PAREVEN	
								parallel clock input polarity	PICLKINV
				1				inverted	
				0				normal	
								parallel data input polarity	PDINV
			1					inverted	
			0					normal	
								enable/disable loop mode inputs	ENLIN
		1						enabled	
		0						disabled	
								enable/disable loop mode outputs	ENLOUT
	1							enabled	
	0							disabled	
								loop mode control	I2CLOOPMODE
1								via I^2C-bus interface	
0								via pins ENLINQ and/or ENLOUTQ	
0	0	0	0	0	0	0	0	default value	

Table 14 Register MUXCNF1 (address A1H); default value 69H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								parallel clock output enable	POCLKEN
							1	enabled	
							0	disabled	
								parallel clock output phase	POPHASE
						1		90° phase shift	
						0		0° phase shift	
								parallel clock output polarity	POCLKINV
					1			inverted	
					0			normal	
								parallel clock direction	CLKDIR
				1				co-directional	
				0				contra-directional	
								parallel clock direction programming	I2CLKDIR
			1					via I²C-bus interface	
			0					via pin CLKDIR	
								multiplexing ratio	MUXR
	1	1						16:1	
	1	0						10:1	
	0	1						8:1	
	0	0						4:1	
								multiplexing ratio programming	I2CMUXR
1								via I²C-bus interface	
0								via pins MUXR0 and MUXR1	
0	1	1	0	1	0	0	1	default value	

Table 15 Register MUXCNF0 (address A2H); default value 18H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								FIFO reset	FIFORESET
							1	reset	
							0	normal mode	
								FIFO reset programming	I2CFIFORESET
						1		via I^2C-bus interface	
						0		via pin FIFORESET	
								parallel input hysteresis	PIHYST
					1			all input modes	
					0			LVDS mode only	
0	0	0	1	1				reserved	
0	0	0	1	1	0	0	0	default value	

Table 16 Register DIVCNF (address B0H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								octave divider division factor M, octave selection	DIV_M
					0	0	0	M = 1, octave number 0	
					0	0	1	M = 2, octave number 1	
					0	1	0	M = 4, octave number 2	
					0	1	1	M = 8, octave number 3	
					1	0	0	M = 16, octave number 4	
					1	0	1	M = 32, octave number 5	
					1	1	0	M = 64, octave number 6	
0	0	0	0	0				reserved	
0	0	0	0	0	0	0	0	default value	

Table 17 Register MAINDIV1 (address B1H); default value 01H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
0	0	0	0	0	0	0	N8	main divider division factor N; N8 = MSB	DIV_N
0	0	0	0	0	0	0	1	default value	

Table 18 Register MAINDIV0 (address B2H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
N7	N6	N5	N4	N3	N2	N1	N0	main divider division factor N; N0 = LSB	DIV_N
0	0	0	0	0	0	0	0	default value	

Table 19 Register FRACN2 (address B3H); default value 80H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
	X	K21	K20	K19	K18	K17	K16	fractional divider division value K; K21 = MSB	DIV_K
								NILFRAC control bit	NILFRAC
1								no fractional N functionality	
0								fractional N functionality	
1	0	0	0	0	0	0	0	default value	

Table 20 Register FRACN1 (address B4H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
K15	K14	K13	K12	K11	K10	K9	K8	fractional divider division value K	DIV_K
0	0	0	0	0	0	0	0	default value	

Table 21 Register FRACN0 (address B5H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
K7	K6	K5	K4	K3	K2	K1	K0	fractional divider division value K; K0 = LSB	DIV_K
0	0	0	0	0	0	0	0	default value	

Table 22 Register SYNTHCNF (address B6H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
			0	0	0	0	0	reserved	
								clock synthesizer manual initialization	INITSYNTH
		1						toggle to initialize synthesizer	
		0						normal operation; auto initialize	
								reference divider division factor R; reference frequency	REFDIV
1	1							R = 8; 155.52 MHz	
1	0							R = 4; 77.76 MHz	
0	1							R = 2; 38.88 MHz	
0	0							R = 1; 19.44 MHz	
0	0	0	0	0	0	0	0	default value	

Table 23 Register IOCNF2 (address C8H); default value 2CH

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								parallel output signal amplitude	MFS
				0	0	0	0	minimum: 60 mV (p-p)	
				1	1	0	0	default: 850 mV (p-p)	
				1	1	1	1	maximum: 1000 mV (p-p)	
								prescaler output polarity	PRSCLOINV
			1					inverted	
			0					normal	
								prescaler output enable	PRSCLOEN
		1						enabled	
		0						disabled	
								parallel output termination	MFOUTTERM
	1							LVPECL mode: floating; CML mode: AC-coupled	
	0							LVPECL mode: standard; CML mode: DC-coupled	
								parallel output mode	MFOUTMODE
1								Current Mode Logic (CML)	
0								Low Voltage Positive Emitter Coupled Logic (LVPECL)	
0	0	1	0	1	1	0	0	default value	

Table 24 Register IOCNF1 (address CAH); default value C0H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loop mode clock input polarity	CININV
							1	inverted	
							0	normal	
								loop mode data input polarity	DININV
						1		inverted	
						0		normal	
								loop mode clock and data inputs swap	CDINSWAP
					1			clock and data input pairs swapped	
					0			normal	
								clock output polarity	COUTINV
				1				inverted	
				0				normal	
								data output polarity	DOUTINV
			1					inverted	
			0					normal	
								clock and data outputs swap	CDOUTSWAP
		1						clock and data output pairs swapped	
		0						normal	
								serial clock output enable	COUTENA
	1							enabled	
	0							disabled	
								serial data output enable	DOUTENA
1								enabled	
0								disabled	
1	1	0	0	0	0	0	0	default value	

Table 25 Register IOCNF0 (address CBH); default value 03H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
				0 0 1	0 0 1	0 1 1	0 1 1	RF serial output signal amplitude minimum: 70 mV (p-p) default: 280 mV (p-p) maximum: 1100 mV (p-p)	RFS
			1 0					loop mode clock output polarity inverted normal	CLOOPINV
		1 0						loop mode data output polarity inverted normal	DLOOPINV
	1 0							RF serial output termination AC-coupled DC-coupled	RFOUTTERM
1 0								loop mode clock and data outputs swap clock and data output pairs swapped normal	CDLOOPSWAP
0	0	0	0	0	0	1	1	default value	

Table 26 Register INTMASK (address CCH); default value 50H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
							1 0	mask LOL interrupt bit not masked masked; note 1	MLOL
				0	0	0		reserved	
			1 0					mask high junction temperature interrupt bit not masked masked; note 1	MTALARM
		1 0						mask OVERFLOW interrupt bit not masked masked; note 1	MOVERFLOW
	1 0							pin INT output polarity inverted; active LOW output normal; active HIGH output	INTPOL
1 0								pin INT output mode standard CMOS output open-drain output	INTOUT
0	1	0	1	0	0	0	0	default value	

Note

1. Signal is not processed by interrupt controller.

Table 27 Register MUXTIMING (address FDH); default value 80H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								multiplexing ratio 10:1 maximum bit rate	MUX_TIMING
0	0	0	0	0	1	0	0	up to 3.2 Gbits/s	
0	0	0	0	1	0	0	0	up to 2.7 Gbits/s	
0	0	0	0	1	0	0	0	default value	

TZA3017HW FEATURES IN PRE-PROGRAMMED MODE

Although the TZA3017HW is primarily intended to be programmed via the I^2C-bus, many of the TZA3017HW functions can be accessed either via the I^2C-bus in I^2C-bus control mode (pin UI HIGH), or via the external chip pins in pre-programmed mode (pin UI LOW). The TZA3017HW functions that are accessible in pre-programmed mode and their control pins are as follows:

- Choice of four pre-programmed SDH/SONET bit rates: STM1/OC3, STM4/OC12, STM16/OC48, STM16/OC48 + FEC; pins DR0 to DR2
- Choice of four pre-programmed bit rates: Fibre Channel, double Fibre Channel, Gigabit Ethernet, 10-Gigabit Ethernet; pins DR0 to DR2
- Choice of four multiplexing ratios: 16:1, 10:1, 8:1 or 4:1: pins MUXR1 and MUXR0
- Co-directional or contra-directional clocking scheme: pin CLKDIR
- Loop mode serial input and output configuration: pins ENLINQ and ENLOUTQ
- Even/odd parity checking: pin PAREVEN
- LVPECL outputs on parallel interface with 800 mV (p-p), single-ended signal, (DC-coupled termination to V_{CC} – 2 V)
- CML serial RF outputs with typical 280 mV (p-p), single-ended signal, (DC-coupled load)
- Loss Of Lock indication (LOL)
- FIFO overflow indication
- FIFO reset
- High junction temperature indication (pin INT; open-drain)
- 18 to 21 MHz reference frequency supported.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCD}, V_{CCA}, V_{CCO}, V_{DD}	supply voltages	–0.5	+3.6	V
V_n	DC voltage on pins			
	D00 to D15, D00Q to D15Q, PICLK, PICLKQ, PARITY, and PARITYQ	V_{CC} – 0.5	V_{CC} + 0.5	V
	POCLK, POCLKQ, PARERR, PARERRQ, PRSCLO, and PRSCLOQ	V_{CC} – 2.5	V_{CC} + 0.5	V
	UI, CS, SDA, SCL, MUXR0, MUXR1, CLKDIR, PAREVEN, FIFORESET, MD0, MD1, ENLOUTQ and ENLINQ	–0.5	V_{CC} + 0.5	V
	LOL and OVERFLOW	–0.5	V_{CC} + 0.5	V
	INT	–0.5	V_{CC} + 0.5	V
I_n	input current on pins			
	D00 to D15, D00Q to D15Q, PICLK, PICLKQ, PARITY, and PARITYQ	–25	+25	mA
	CREF, CREFQ, CIN, CINQ, DIN and DINQ	–20	+20	mA
	INT	–2	+2	mA
T_{amb}	ambient temperature	–40	+85	°C
T_j	junction temperature		+125	°C
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	notes 1 and 2	16	K/W

Notes

1. In compliance with JEDEC standards JESD51-5 and JESD51-7.
2. Four-layer Printed-Circuit Board (PCB) in still air with 36 plated vias connected with the heatsink and the second and fourth layer in the PCB.

CHARACTERISTICS

V_{CC} = 3.14 to 3.47 V; T_{amb} = –40 to +85 °C; $R_{th(j-a)} \leq 16$ K/W; all characteristics are specified for the default settings (note 1); all voltages are referenced to ground; positive currents flow into the device unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
I_{CCA}	analog supply current		0.5	1.2	2.4	mA
I_{CCD}	digital supply current	notes 1 and 2	170	215	270	mA
		notes 2 and 3	285	345	430	mA
I_{DD}	digital supply current		0	2	4	mA
I_{CCO}	oscillator supply current		20	31	41	mA
$I_{CC(tot)}$	total supply current	notes 1 and 2	190	250	318	mA
		notes 2 and 3	305	380	478	mA
P_{tot}	total power dissipation	notes 1 and 2	0.6	0.82	1.1	W
		notes 2 and 3	0.96	1.25	1.66	W
CMOS input; pins UI, DR0, DR1, DR2, MUXR0, MUXR1, MD0, MD1, ENLINQ, ENLOUTQ, FIFORESET, PAREVEN and CLKDIR						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{CC}$	–	–	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–200	–	–	µA
I_{IH}	HIGH-level input current	$V_{IH} = V_{CC}$	–	–	10	µA
CMOS output; pins OVERFLOW, LOL and INT						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.5 mA	$V_{CC} – 0.2$	–	V_{CC}	V
Open-drain output; pin INT						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC}$	–	–	10	µA
Serial output; pins COUT, COUTQ, DOUT, DOUTQ, CLOOP, CLOOPQ, DLOOP, and DLOOPQ						
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	single-ended with 50 Ω external load; note 4	220	280	340	mV
Z_o	output impedance	single-ended to V_{CC}	40	50	60	Ω
t_r	rise time	20% to 80%	–	60	90	ps
t_f	fall time	80% to 20%	–	60	90	ps
t_{D-C}	data-to-clock delay	between differential crossovers	–50	–	50	ps
δ	duty cycle COUT and COUTQ	between differential crossovers	40	50	60	%
f_{SBR}	serial bit rate	MUX 16:1, 8:1, 4:1	30	–	3200	Mbits/s
		MUX 10:1; note 5	30	–	3200	Mbits/s
Serial input; pins DIN, DINQ, CIN and CINQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_i	input voltage range		$V_{CC} – 1$	–	$V_{CC} + 0.25$	V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
Parallel input (rail-to-rail); pins D00 to D15, D00Q to D15Q, PARITY, PARITYQ, PICLK, and PICLKQ						
V_i	input voltage range		V_{EE} – 0.25	–	V_{CC} + 0.25	V
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended	100	–	1000	mV
V_{hys}	input differential hysteresis	MD1 = LOW; MD0 = HIGH	–	30	–	mV
$Z_{i(diff)}$	differential input impedance	MD1 = LOW	80	100	120	Ω
$Z_{i(se)}$	single-ended input impedance	MD1 = HIGH	40	50	60	Ω
$V_{T(CML)}$	input termination voltage in CML mode	MD1 = HIGH; MD0 = LOW	–	V_{CC}	–	V
$V_{T(LVPECL)}$	input termination voltage in LVPECL mode	MD1 = HIGH; MD0 = HIGH	V_{CC} – 2.3	V_{CC} – 2	V_{CC} – 1.7	V
$t_{su(co)}$	set-up time	co-directional clocking	0	–	–	ps
$t_{h(co)}$	hold time	co-directional clocking	1000	–	–	ps
$t_{su(contra)}$	set-up time	contra-directional clocking	1300	–	–	ps
$t_{h(contra)}$	hold time	contra-directional clocking	–300	–	–	ps
δ	duty cycle PICLK and PICLKQ	between differential crossovers	40	50	60	%
f_{PBR}	parallel bit rate		–	–	400	Mbits/s
CML mode output; pins POCLK, POCLKQ, PARERR, PARERRQ, PRSCLO, and PRSCLOQ						
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	single-ended with 50 Ω external load, DC-coupled; note 6	600	850	1100	mV
Z_o	output impedance	single-ended to V_{CC}	80	95	110	Ω
t_r	rise time	20% to 80%	200	250	350	ps
t_f	fall time	80% to 20%	200	250	350	ps
LVPECL mode output; pins POCLK, POCLKQ, PARERR, PARERRQ, PRSCLO, and PRSCLOQ						
V_{OH}	HIGH-level output voltage	50 Ω termination to V_{CC} – 2V	V_{CC} – 1.2	V_{CC} – 1.0	V_{CC} – 0.9	V
V_{OL}	LOW-level output voltage	50 Ω termination to V_{CC} – 2V	V_{CC} – 2.0	V_{CC} – 1.9	V_{CC} – 1.7	V
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	LVPECL floating; single-ended with 50 Ω external load	700	900	1150	mV
t_r	rise time	20% to 80%	300	350	400	ps
t_f	fall time	80% to 20%	300	350	400	ps
Reference frequency input; pins CREF, and CREFQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_i	input voltage range		V_{CC} – 1	–	V_{CC} + 0.25	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Δf_{CREF}	reference clock frequency accuracy	SDH/SONET requirement	–20	–	+20	ppm
f_{CREF}	reference clock frequency	see Table 4; R = 1, 2, 4, or 8	18 × R	19.44 × R	21 × R	MHz
I²C-bus; pins SCL and SDA						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{CC}$	–	–	V
V_{hys}	hysteresis of Schmitt trigger inputs		$0.05V_{CC}$	–	–	V
V_{OL}	SDA LOW-level output voltage (open-drain)	I_{OL} = 3 mA	0	–	0.4	V
I_L	input leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
I²C-bus timing						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{HD;STA}$	hold time START condition		0.6	–	–	µs
$t_{SU;STA}$	set-up time START condition		0.6	–	–	µs
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	µs
t_r	SCL and SDA rise time		20	–	300	ns
t_f	SCL and SDA fall time		20	–	300	ns
t_{BUF}	bus free time between STOP and START		1.3	–	–	µs
C_b	capacitive load on each bus line		–	–	400	pF
t_{SP}	pulse width of allowable spikes		0	–	50	ns
V_{nL}	noise margin at LOW-level		$0.1V_{CC}$	–	–	V
V_{nH}	noise margin at HIGH-level		$0.2V_{CC}$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Jitter generation						
$J_{gen(p-p)}$	jitter generation (peak-to-peak value)	STM1/OC3 mode; notes 7 and 8				
		f = 500 Hz to 1.3 MHz	–	–	16	mUI
		f = 12 kHz to 1.3 MHz	–	–	4	mUI
		f = 65 kHz to 1.3 MHz	–	–	4	mUI
		STM4/OC12 mode; notes 7 and 8				
		f = 1 kHz to 5 MHz	–	–	63	mUI
		f = 12 kHz to 5 MHz	–	–	13	mUI
		f = 250 kHz to 5 MHz	–	–	13	mUI
		STM16/OC48 mode; notes 7 and 8				
		f = 5 kHz to 20 MHz	–	35	250	mUI
		f = 12 kHz to 20 MHz	–	32	50	mUI
		f = 1 MHz to 20 MHz	–	7	50	mUI

Notes

1. Default settings: UI = LOW (pre-programmed mode; see Table 1); DR0 = LOW, DR1 = HIGH, DR2 = LOW (STM16/OC48); PAREVEN = HIGH (even parity); MUXR0 = HIGH, MUXR1 = HIGH (multiplexing ratio is 16:1); FIFORESET = LOW; MD0 = LOW, MD1 = LOW (100Ω differential); CLKDIR = HIGH (co-directional clocking); ENLOUTQ = HIGH (DLOOP, DLOOPQ, CLOOP and CLOOPQ disabled); ENLINQ = HIGH (DIN, DINQ, CIN and CINQ disabled); CREF and CREFQ = 19.44MHz; COUT, COUTQ, DOUT, DOUTQ, POCLK, POCLKQ, PARERR, PARERRQ, PRSCLO and PRSCLOQ are not connected.
2. The total supply current and power dissipation is dependent on the I^2C settings such as output swing, loop modes, multiplexing ratio and input and output termination conditions. For dependency on output termination and output swing; see Figs 18 and 20.
3. ENLOUTQ = LOW (DLOOP, CLOOP enabled); ENLINQ = LOW (DIN, CIN enabled) and maximum output swing; COUT, COUTQ, DOUT, DOUTQ, POCLK, POCLKQ, PARERR, PARERRQ, PRSCLO, PRSCLOQ, DLOOP, DLOOPQ, CLOOP and CLOOPQ are not connected.
4. The output swing is adjustable in 16 steps controlled by bits RFS in the I^2C-bus register IOCNF0 (address CBH).
5. For multiplexing ratio 10:1, the I^2C-bus register MUXTIMING (address FDH) should be programmed with 0000.0100 (04H) for supporting 3.2 Gbits/s. The highest supported bit rate for multiplexing ratio 10:1 in a pin programmed application is 2.7 Gbits/s.
6. The output swing is adjustable in 16 steps controlled by bits MFS in the I^2C-bus register IOCNF2 (address C8H).
7. Reference frequency of 19.44 MHz, with a phase-noise of less than −140 dBc for frequencies of more than 12 kHz from the carrier. Measured for 60 seconds within the appropriate bandwidth.
8. For bit rates lower than 1.8 Gbits/s, the jitter decreases with the octave division ratio.

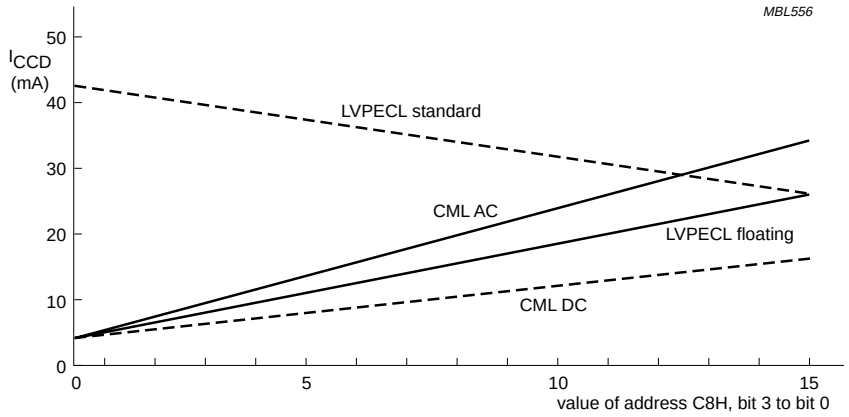


Fig.18 Supply current per parallel output.

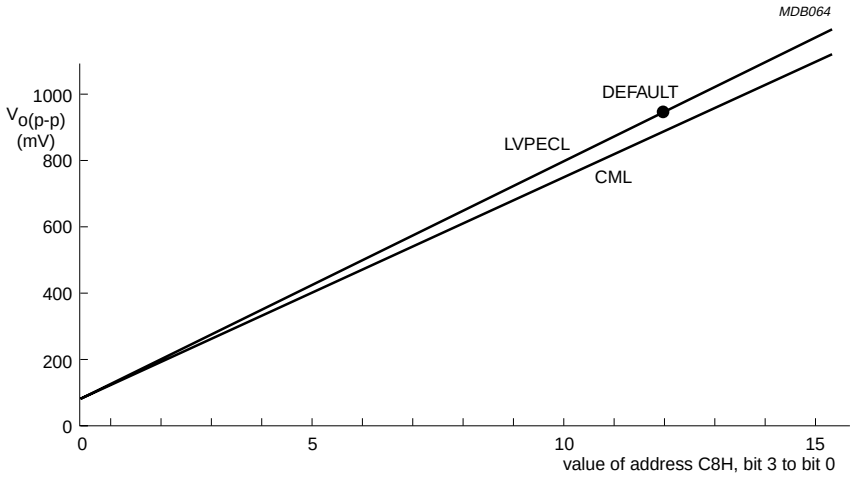


Fig.19 Output voltage swing of parallel output.

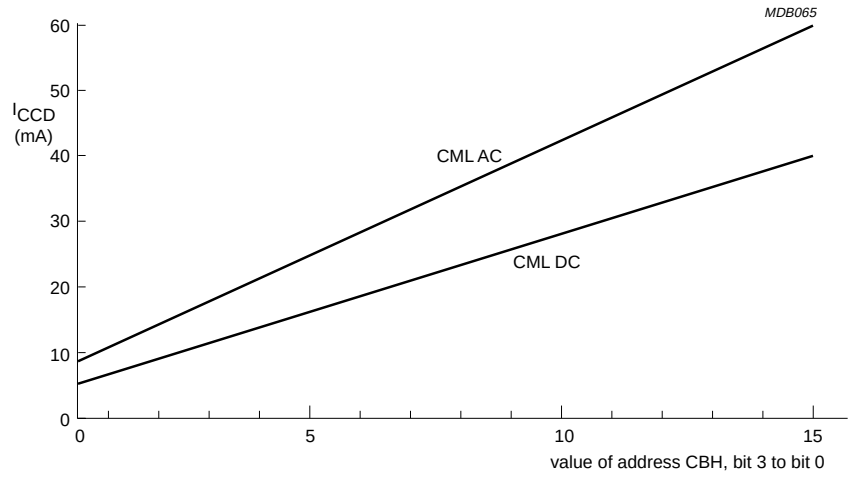


Fig.20 Supply current per serial output.

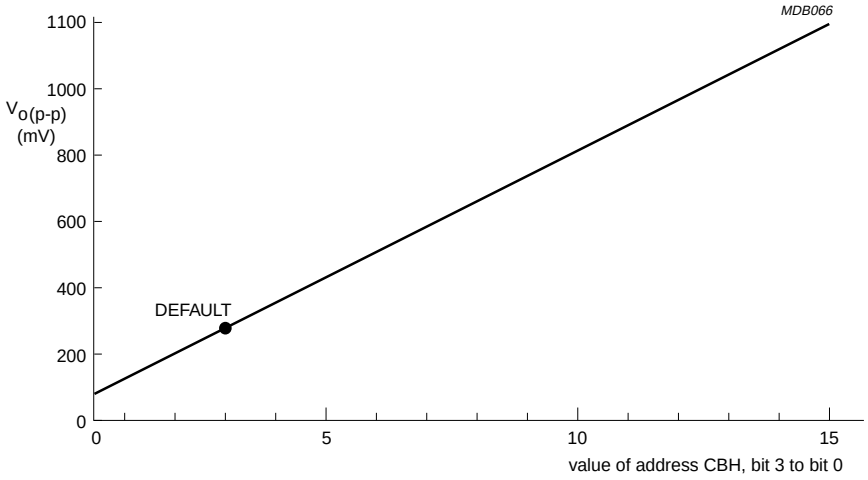


Fig.21 Output voltage swing of serial output.

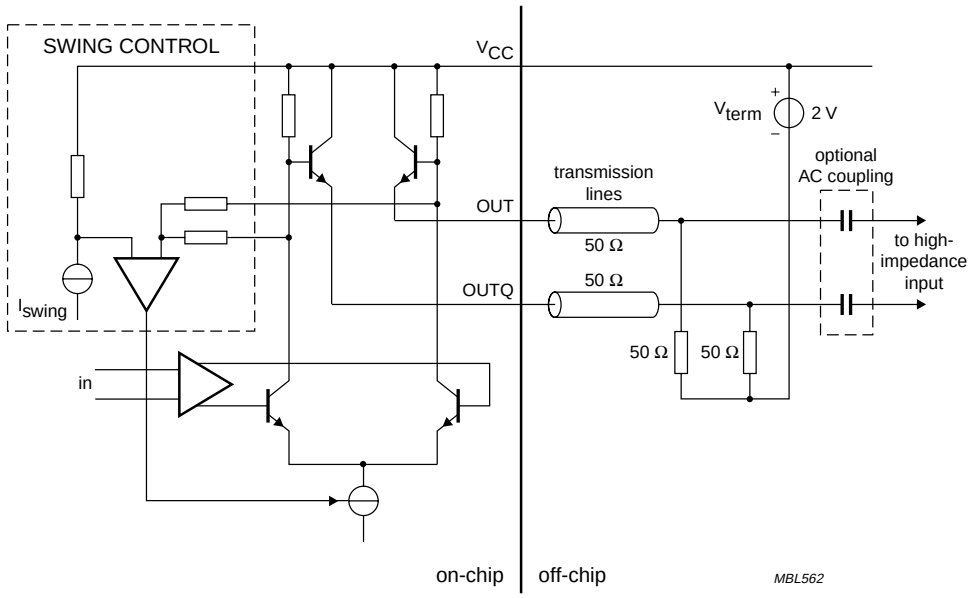


Fig.22 Parallel output standard LVPECL mode.

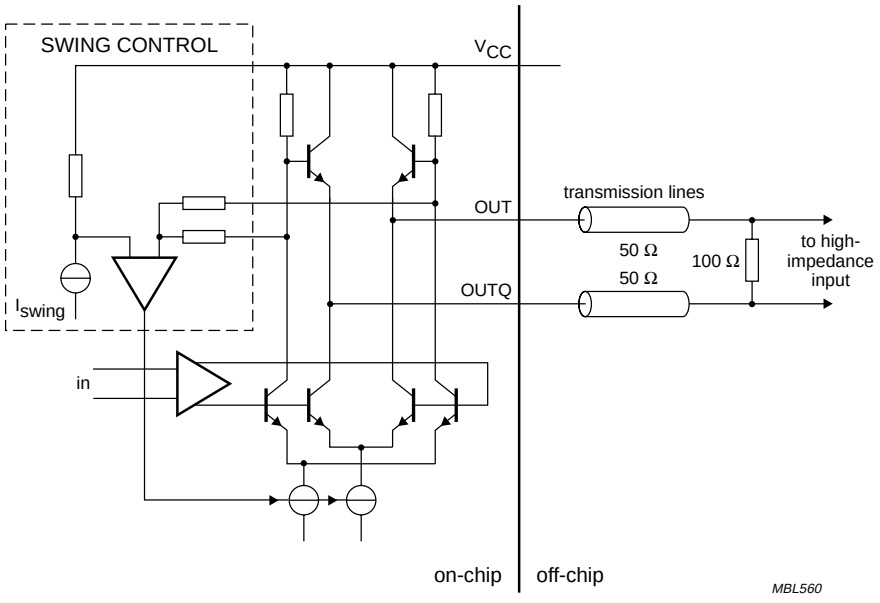


Fig.23 Parallel output floating LVPECL mode (DC-coupled).

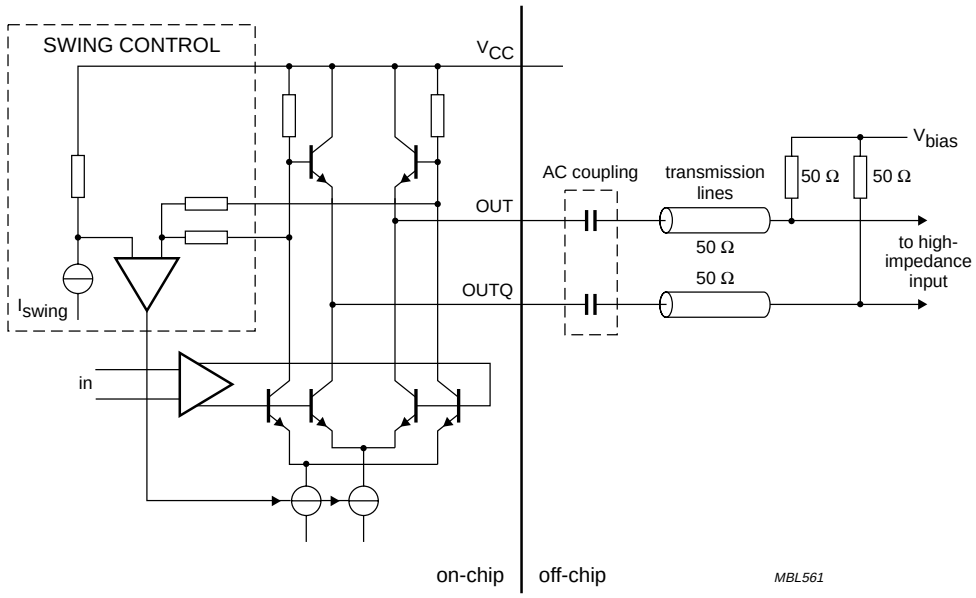


Fig.24 Parallel output floating LVPECL mode (AC-coupled).

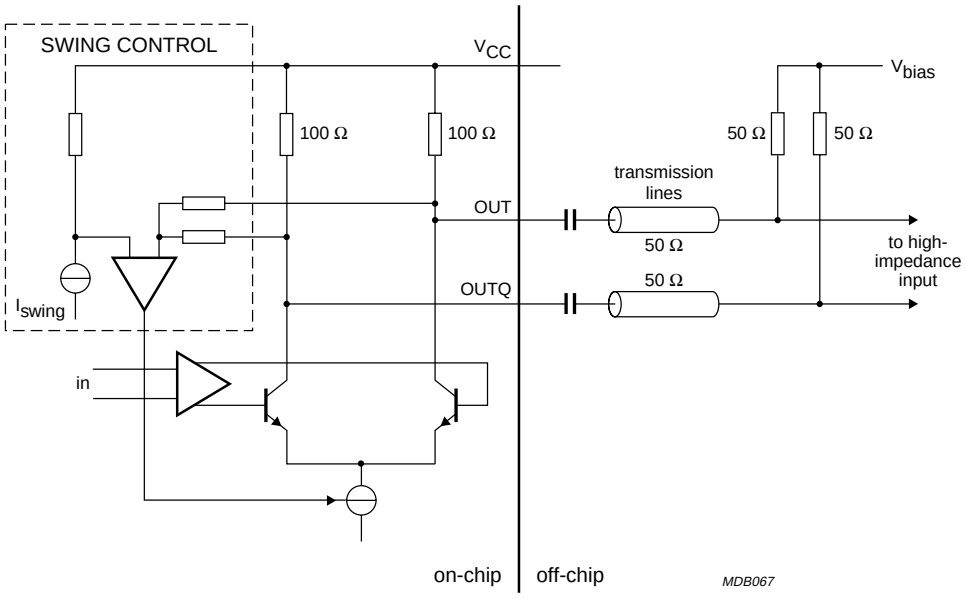


Fig.25 Parallel output CML mode (AC-coupled).

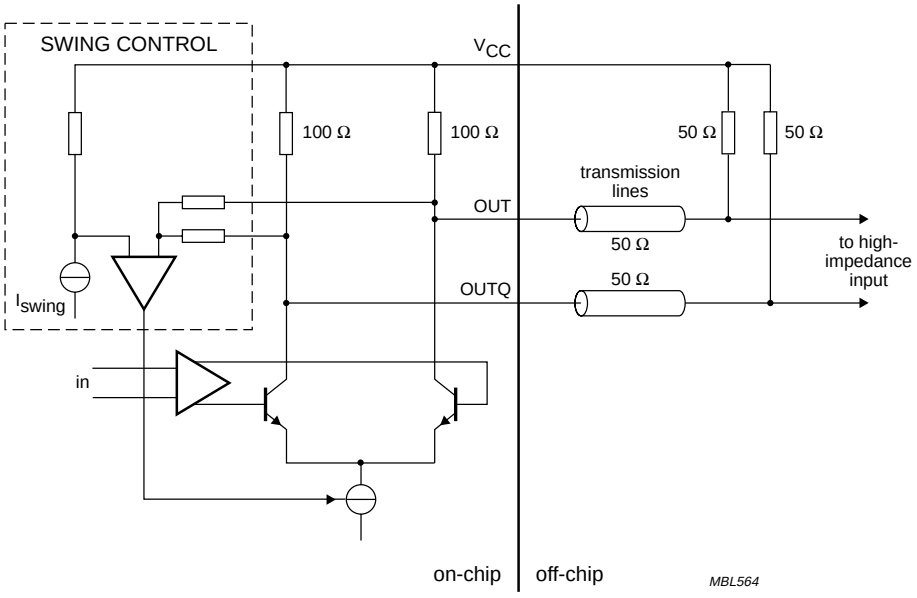


Fig.26 Parallel output CML mode (DC-coupled).

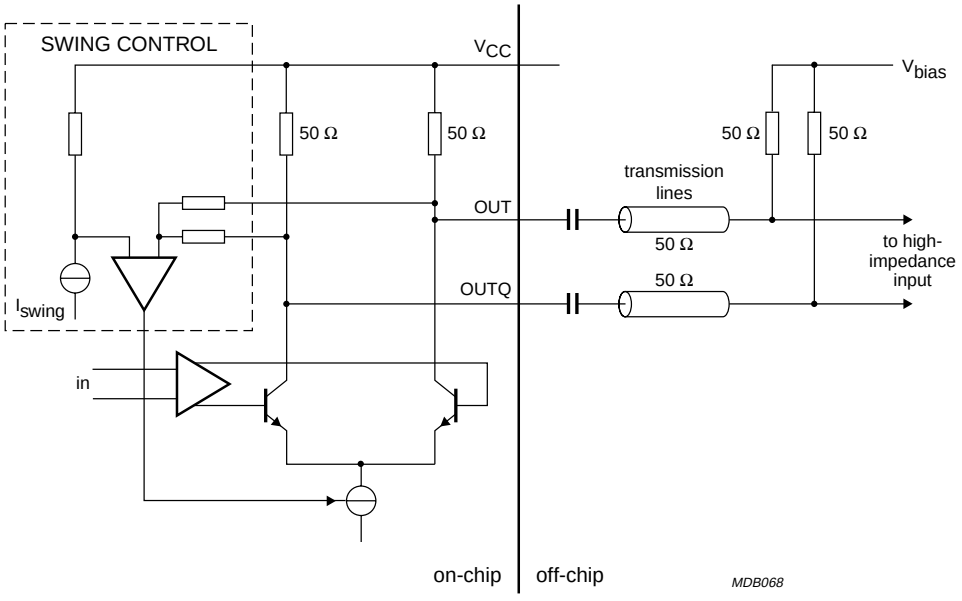


Fig.27 Serial output CML mode (AC-coupled).

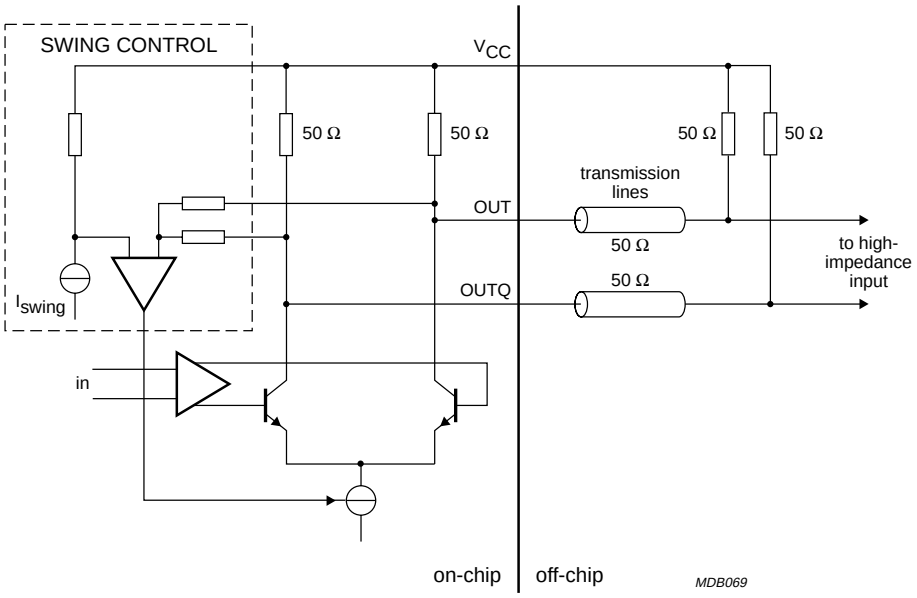
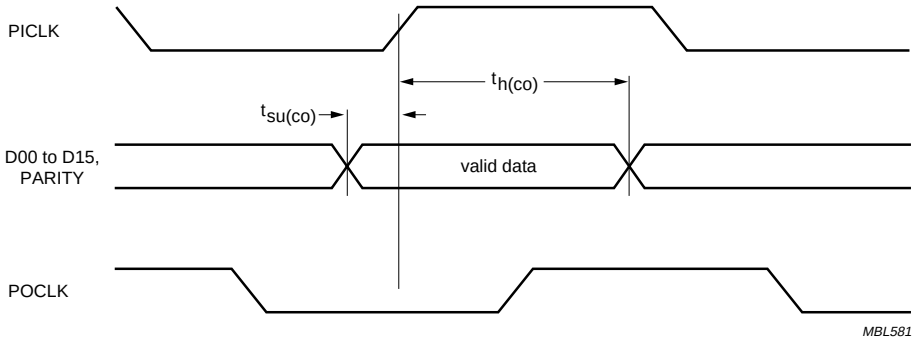
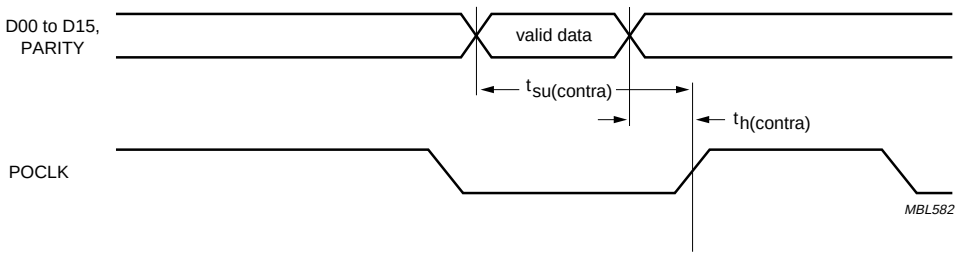


Fig.28 Serial output CML mode (DC-coupled).



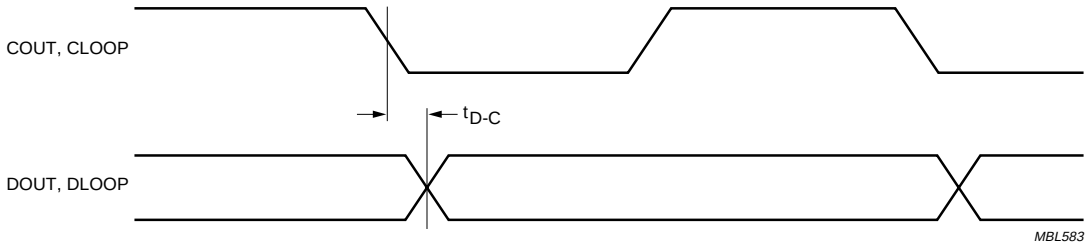
The timing is measured from the crossover point of the reference signal to the crossover point of the input.

Fig.29 Parallel bus co-directional timing.



The timing is measured from the crossover point of the reference signal to the crossover point of the input.

Fig.30 Parallel bus contra-directional timing.

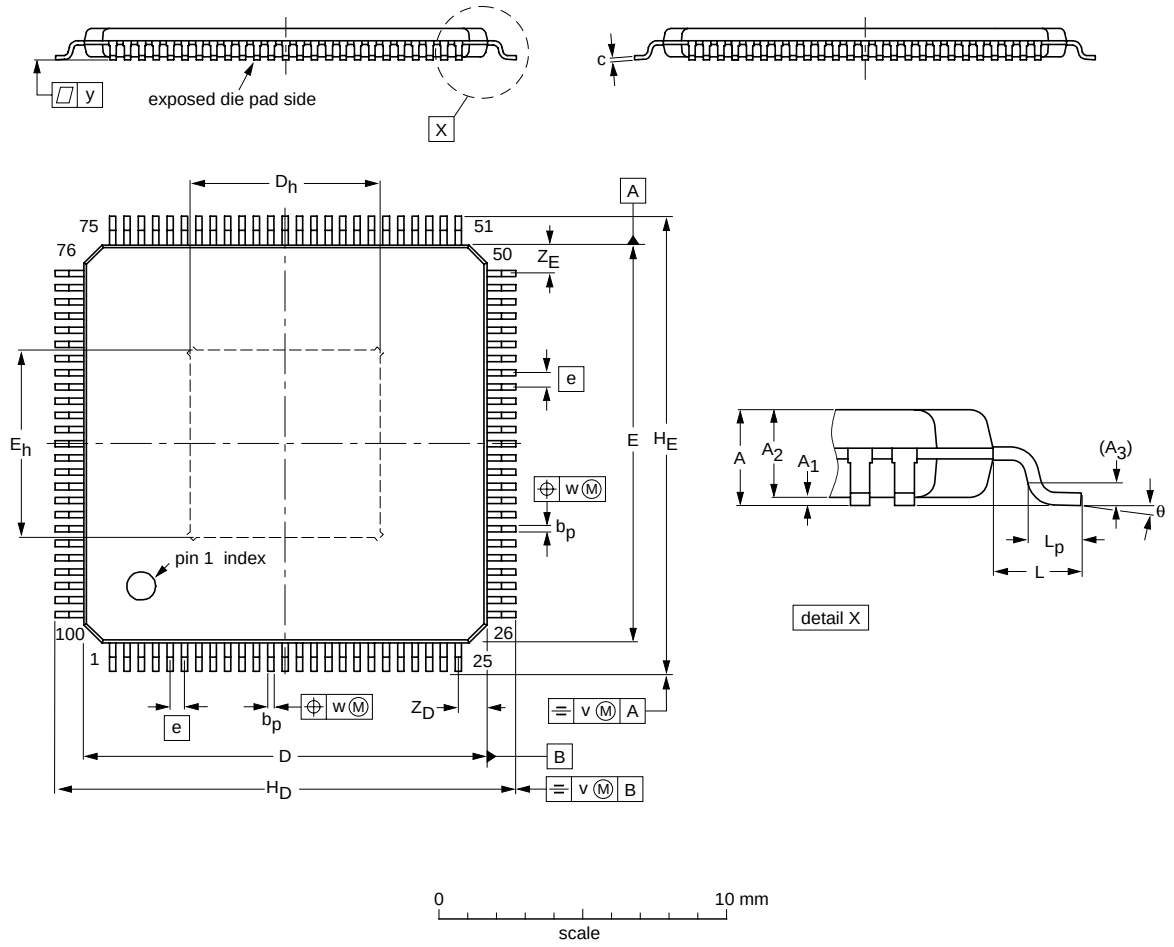


The timing is measured from the crossover point of the reference signal to the crossover point of the output.

Fig.31 RF output timing.

PACKAGE OUTLINE

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed die pad **SOT638-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-1						~~01-03-30~~ 03-04-07

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

SCA75

Printed in The Netherlands 403510/02/pp52 Date of release: 2003 May 14 Document order number: 9397 750 10574

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