DATA SHEET

TZA3012AHW

30 Mbits/s up to 3.2 Gbits/s
A-rate™ fibre optic receiver

Product specification
Supersedes data of 2002 Sep 10

2003 May 21

Philips
Semiconductors

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30 Mbits/s up to 3.2 Gbits/s A-rate™ fibre optic receiver

TZA3012AHW

FEATURES

- Single 3.3 V power supply
- I²C-bus and pin programmable fibre optic receiver.

Dual limiter features

- Dual limiting input with 12 mV sensitivity
- Received Signal Strength Indicator (RSSI)
- Loss Of Signal (LOS) indicator with threshold adjust
- Differential overvoltage protection.

Data and clock recovery features

- Supports SHD/SONET bit rates at 155.52, 622.08, 2488.32 and 2666.06 Mbits/s (STM16/OC48 + FEC)
- Supports Gigabit Ethernet at 1250 and 3125 Mbits/s
- Supports Fibre Channel at 1062.5 and 2125 Mbits/s
- ITU-T compliant jitter tolerance
- Frequency lock indicator
- Stable clock signal when input data absent
- Outputs for recovered data and clock loop mode.

Demultiplexer features

- 1:16, 1:10, 1:8 or 1:4 demultiplexing ratio
- LVPECL or CML demultiplexer outputs
- Frame detection for SDH/SONET and GE frames
- Parity bit generation
- Loop mode inputs to demultiplexer.

Additional features with the I2C-bus

- A-rate™(1) supports any bit rate from 30 Mbits/s to 3.2 Gbits/s with one reference frequency
- Programmable frequency resolution of 10 Hz
- Four reference frequency ranges
- Adjustable swing of data, clock and parallel outputs
- Programmable polarity of all RF I/Os
- Exchangeable pin designations of RF clock with data for all I/Os for optimum connectivity
- Reversible pin designations of parallel data bus bits for optimum connectivity
- Slice level adjustment to improve Bit Error Rate (BER)
- Mute function for a forced logic 0 output state
- Programmable parity
- Programmable 32-bit frame detection.

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APPLICATIONS

- Any optical transmission system with bit rates between 30 Mbits/s and 3.2 Gbits/s
- Physical interface IC in receive channels
- Transponder applications
- Dense Wavelength Division Multiplexing (DWDM) systems.

GENERAL DESCRIPTION

The TZA3012AHW is a fully integrated optical network receiver containing a dual limiter, Data and Clock Recovery (DCR) and a demultiplexer with demultiplexing ratios 1:16, 1:10, 1:8 or 1:4.

The A-rate feature allows the IC to operate at any bit rate between 30 Mbits/s and 3.2 Gbits/s using a single reference frequency. The receiver supports loop modes with serial clock and data inputs and outputs. All clock signals are generated using a fractional N synthesizer with 10 Hz resolution giving a true, continuous rate operation. For full configuration flexibility, the receiver is programmable by pin or via the I²C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3012AHW	HTQFP100	plastic thermal enhanced thin quad flat package; 100 leads; body 14 × 14 × 1 mm; exposed die pad	SOT638–1

BLOCK DIAGRAM

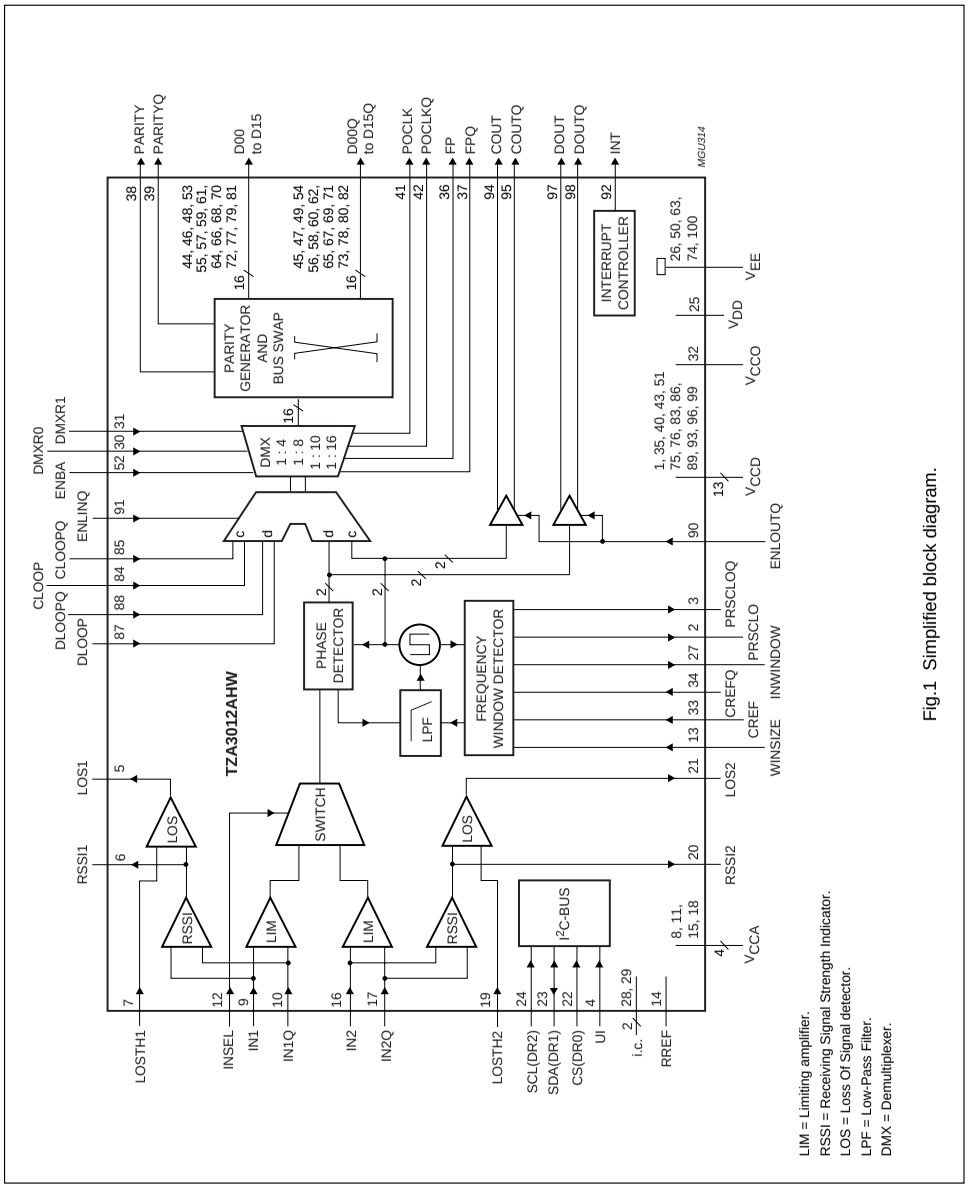


Fig.1 Simplified block diagram.

LIM = Limiting amplifier.
RSSI = Receiving Signal Strength Indicator.
LOS = Loss Of Signal detector.
LPF = Low-Pass Filter.
DMX = Demultiplexer.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{EE}	die pad	common ground plane
V_{CCD}	1	supply voltage (digital part)
PRSCLO	2	prescaler output
PRSCLOQ	3	prescaler inverted output
UI	4	user interface select
LOS1	5	first input channel loss of signal output
RSSI1	6	first input channel received signal strength indicator output
LOSTH1	7	first input channel loss of signal threshold input
V_{CCA}	8	supply voltage (analog part)
IN1	9	first channel input
IN1Q	10	first channel inverted input
V_{CCA}	11	supply voltage (analog part)
INSEL	12	input selector
WINSIZE	13	wide and narrow frequency detect window select
RREF	14	reference resistor input
V_{CCA}	15	supply voltage (analog part)
IN2	16	second channel input
IN2Q	17	second channel inverted input
V_{CCA}	18	supply voltage (analog part)
LOSTH2	19	second input channel loss of signal threshold input
RSSI2	20	second input channel received signal strength indicator output
LOS2	21	LOS output of second input channel
CS(DR0)	22	chip select (data rate select 0)
SDA(DR1)	23	I^2C-bus serial data (data rate select 1)
SCL(DR2)	24	I^2C-bus serial clock (data rate select 2)
V_{DD}	25	supply voltage (digital part)
V_{EE}	26	ground
INWINDOW	27	frequency window detector output
i.c.	28	internally connected
i.c.	29	internally connected
DMXR0	30	demultiplexing ratio select 0
DMXR1	31	demultiplexing ratio select 1

SYMBOL	PIN	DESCRIPTION
V_{CCO}	32	supply voltage (clock generator)
CREF	33	reference clock input
CREFQ	34	reference clock inverted input
V_{CCD}	35	supply voltage (digital part)
FP	36	frame pulse output
FPQ	37	frame pulse inverted output
PARITY	38	parity output
PARITYQ	39	parity inverted output
V_{CCD}	40	supply voltage (digital part)
POCLK	41	parallel clock output
POCLKQ	42	parallel clock inverted output
V_{CCD}	43	supply voltage (digital part)
D00	44	parallel data 00 output
D00Q	45	parallel data 00 inverted output
D01	46	parallel data 01 output
D01Q	47	parallel data 01 inverted output
D02	48	parallel data 02 output
D02Q	49	parallel data 02 inverted output
V_{EE}	50	ground
V_{CCD}	51	supply voltage (digital part)
ENBA	52	byte alignment enable input
D03	53	parallel data 03 output
D03Q	54	parallel data 03 inverted output
D04	55	parallel data 04 output
D04Q	56	parallel data 04 inverted output
D05	57	parallel data 05 output
D05Q	58	parallel data 05 inverted output
D06	59	parallel data 06 output
D06Q	60	parallel data 06 inverted output
D07	61	parallel data 07 output
D07Q	62	parallel data 07 inverted output
V_{EE}	63	ground
D08	64	parallel data 08 output
D08Q	65	parallel data 08 inverted output
D09	66	parallel data 09 output
D09Q	67	parallel data 09 inverted output
D10	68	parallel data 10 output
D10Q	69	parallel data 10 inverted output
D11	70	parallel data 11 output
D11Q	71	parallel data 11 inverted output
D12	72	parallel data 12 output

SYMBOL	PIN	DESCRIPTION
D12Q	73	parallel data 12 inverted output
V_{EE}	74	ground
V_{CCD}	75	supply voltage (digital part)
V_{CCD}	76	supply voltage (digital part)
D13	77	parallel data 13 output
D13Q	78	parallel data 13 inverted output
D14	79	parallel data 14 output
D14Q	80	parallel data 14 inverted output
D15	81	parallel data 15 output
D15Q	82	parallel data 15 inverted output
V_{CCD}	83	supply voltage (digital part)
CLOOP	84	loop mode clock input
CLOOPQ	85	loop mode clock inverted input
V_{CCD}	86	supply voltage (digital part)
DLOOP	87	loop mode data input
DLOOPQ	88	loop mode data inverted input
V_{CCD}	89	supply voltage (digital part)

SYMBOL	PIN	DESCRIPTION
ENLOUTQ	90	line loop back enable input (active LOW)
ENLINQ	91	diagnostic loop back enable input (active LOW)
INT	92	interrupt output
V_{CCD}	93	supply voltage (digital part)
COUT	94	recovered clock output
COUTQ	95	recovered clock inverted output
V_{CCD}	96	supply voltage (digital part)
DOUT	97	recovered data output
DOUTQ	98	recovered data inverted output
V_{CCD}	99	supply voltage (digital part)
V_{EE}	100	ground

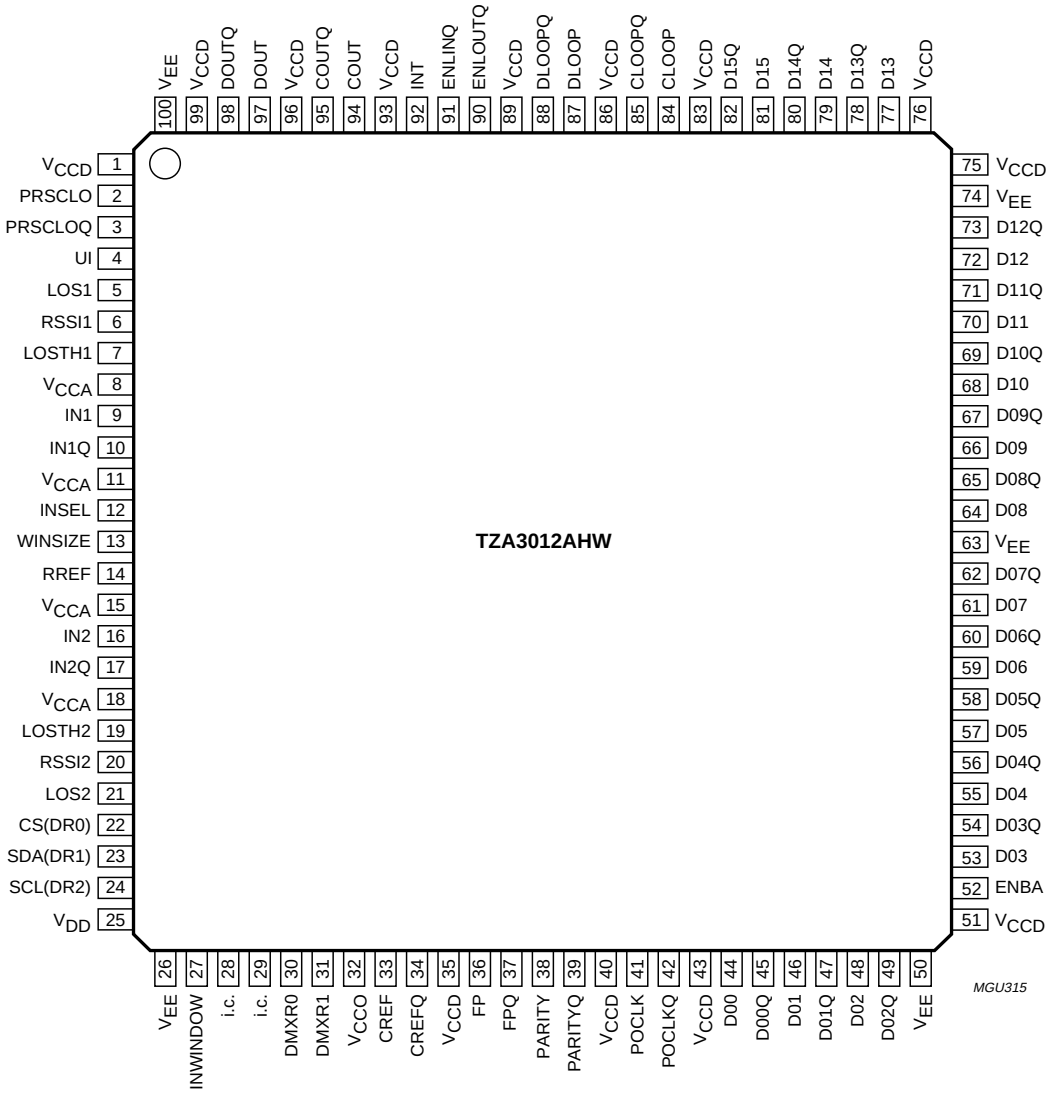


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TZA3012AHW receives data from an incoming bit stream having a bit rate from 30 Mbits/s up to 3.2 Gbits/s. Two line inputs with limiting amplifiers are available. An internal DCR synchronizes the internal clock generator to the incoming data. The recovered serial data and clock are demultiplexed at ratios of 1:16, 1:10, 1:8 or 1:4.

Choice of user interface

The TZA3012AHW can be controlled either via the I²C-bus or using programming pins DR0 to DR2. Pin UI selects the user interface required. I²C-bus control and A-rate functionality are enabled when pin UI is either open circuit or connected to V_{CC}. Pre-programmed mode is enabled when pin UI is connected to V_{EE}; see Table 1.

Table 1 Truth table for pin UI

UI	MODE	PIN 22	PIN 23	PIN 24
LOW	pre-programmed	DR0	DR1	DR2
HIGH	I²C-bus control	CS	SDA	SCL

In I²C-bus control mode, the chip is configured using the I²C-bus pins SDA and SCL. During I²C-bus read or write actions, pin CS must be HIGH. When pin CS is LOW, the programmed configuration remains active but signals SDA and SCL are ignored. This allows several TZA3012AHWs in the application with the same I²C-bus address to be selected separately. The I²C-bus address of the TZA3012AHW is shown in Table 2.

Table 2 I²C-bus address of the TZA3012AHW

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	1	0	0	0	0	X

The function and content of the I²C-bus registers are described in Section “I²C-bus registers”. Some functions in the TZA3012AHW can be controlled either by the I²C-bus or a designated pin. The method required is specified by an extra bit named I2C<pin name> in the corresponding I²C-bus register, for example, bit I2CDMXR in register DMXCNF. The default is enable by pin.

If the application has no I²C-bus control, the IC must operate with reduced functionality in pre-programmed mode. In pre-programmed mode, pins DR0 to DR2 are standard CMOS inputs that allow the selection of up to eight pre-programmed bit rates using an external reference clock frequency of typically 19.44 MHz; see Table 3.

Table 3 Truth table for selecting bit rate in pre-programmed mode (pin UI = V_{EE})

DR2	DR1	DR0	PROTOCOL	BIT RATE (Mbits/s)
LOW	LOW	LOW	STM1/OC3	155.52
LOW	LOW	HIGH	STM4/OC12	622.08
LOW	HIGH	LOW	STM16/OC48	2488.32
LOW	HIGH	HIGH	STM16 + FEC	2666.06
HIGH	LOW	LOW	GE	1250.00
HIGH	LOW	HIGH	10GE	3125.00
HIGH	HIGH	LOW	Fibre Channel	1062.50
HIGH	HIGH	HIGH	Fibre Channel	2125.00

After power-up, the TZA3012AHW initiates a Power-On Reset (POR) sequence to restore the default settings of the I²C-bus registers, irrespective of the level on pin UI. The default settings are shown in Table 12.

Limiting amplifiers

The TZA3012AHW has two switchable RF line inputs. Each input has a limiting amplifier (limiter) which provides optimum receiver sensitivity at any bit rate. The bandwidth of each limiter is automatically adjusted in accordance with the input bit rate. This ensures that wideband noise present in the optical front-end (photo-detector and transimpedance amplifier) is reduced at low input bit rates. The maximum bandwidth is selected by default at power-up. The bandwidth can be set independently of input bit rate using bits AMPOCT in I²C-bus register LIMCNF (address C2H).

Normally, only one limiter is activated at any one time so that only the RF signal applied to the active channel is routed to the DCR. The unused limiter automatically enters a sleep mode to reduce power dissipation. A limiter is selected by pin INSEL as shown in Table 4.

Table 4 Truth table for pin INSEL

PIN INSEL	SELECTED CHANNEL	SELECTED INPUTS
HIGH	channel 1; limiter 1 active	IN1 and IN1Q
LOW	channel 2; limiter 2 active	IN2 and IN2Q

A limiter can also be selected by setting bit I2CINSEL in I²C-bus register LIMCNF, and specifying bit INSEL as shown in Table 5.

Table 5 Channel selection

I^2C BIT		PIN INSEL	SELECTED CHANNEL
I2CINSEL	INSEL		
0	X	LOW	channel 2; limiter 2 active
0	X	HIGH	channel 1; limiter 1 active
1	0	X	channel 2; limiter 2 active
1	1	X	channel 1; limiter 1 active

Both limiters can be made active by setting bit BOTHON in I^2C-bus register LIMCNF. This allows 'hot switching', where the second channel can be selected quickly if the first channel loses its signal. Note that even when both limiters are active, only one channel is selected at any time; see Table 6.

When only one limiter is active, the time taken to deactivate its limiter and activate the limiter in the other channel takes 4 µs typical.

Table 6 Channel and limiter selection with bit BOTHON

I^2C BIT BOTHON	PIN INSEL	SELECTED CHANNEL	SELECTED INPUTS
0	HIGH	channel 1; limiter 1 active	IN1 and IN1Q
1	HIGH	channel 1; limiters 1 and 2 active	IN1 and IN1Q
0	LOW	channel 2; limiter 2 active	IN2 and IN2Q
1	LOW	channel 2; limiters 1 and 2 active	IN2 and IN2Q

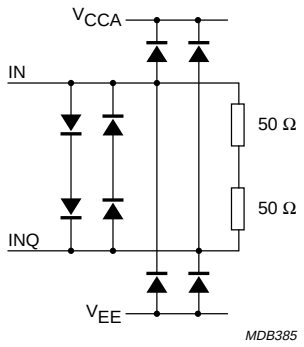


Fig.3 Limiter input termination configuration.

Received Signal Strength Indicator (RSSI)

The strength of signal present at each RF input is measured by a logarithmic detector and represented by an analog voltage at pins RSSI1 and RSSI2 for channels 1 and 2, respectively. The RSSI has a sensitivity of 17 mV/dB typical for an input voltage swing $V_{i(p-p)}$ range of 5 mV to 500 mV; see Fig.4. RSSI output voltage V_{RSSI} can be calculated using the following formula:

$$V_{RSSI} = V_{RSSI(32\ mV)} + S_{RSSI} \times 20\log\frac{V_{i(p-p)}}{32\ mV}$$

Both logarithmic detectors are always active to allow the input with the strongest signal to be selected.

Loss Of Signal (LOS) indicator

In addition to the analog RSSI output, the TZA3012AHW also provides a digital LOS indication output on pins LOS1 and LOS2. The RSSI level is internally compared with a LOS threshold voltage level, which can be set either by an external resistor connected to pins LOSTH1 and LOSTH2, or by using an internal D/A converter. The method used is determined by bit I2CREFLVL1 in I^2C-bus register LIMLOS1CNF (address BDH) for channel 1, or bit I2CREFLVL2 in I^2C-bus register LIMLOS2CNF (address BFH) for channel 2. Using the internal D/A converter requires a value representing the threshold voltage to be programmed into I^2C-bus registers LIMLOS1TH (address BCH) or LIMLOS2TH (address BEH). This allows separate LOS threshold levels to be specified per channel.

If the received signal strength is **below** the default hysteresis value of 3 dB, the corresponding LOS pin will be HIGH. Alternative hysteresis values from 0 to 7 dB in steps of 1 dB can be specified using bits HYS1 and HYS2 in I^2C-bus registers LIMLOS1CNF and LIMLOS2CNF respectively. If required, the polarity of the LOS indicator outputs can be inverted by setting bits LOS1POL and LOS2POL in the same registers. The LOS function can be disabled by setting bit LOS1 or LOS2 to logic 0 for channel 1 or channel 2 respectively.

The LOS function is also available using I^2C-bus registers INTERRUPT and STATUS; see Sections "Interrupt register" and "Status register". If bit LOS1 or LOS2 in register INTERRUPT is not masked, a loss of signal condition will generate an interrupt signal at pin LOS1 or pin LOS2. Bits LOS1 and LOS2 are masked by default; see Section "Interrupt generation".

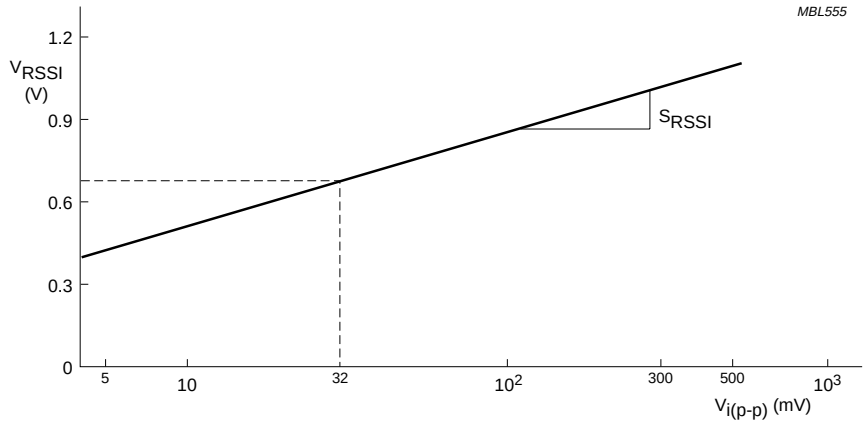


Fig.4 V_{RSSI} as a function of $V_{i(p-p)}$.

Setting LOSTH reference level by external resistor

If the internal D/A converter is not used, the reference voltage level on pin LOSTH1 (or LOSTH2) can be set by connecting an external resistor (R2) from the relevant pin to ground. The voltage on the pin is determined by the ratio between R2 and R1; see Fig.5. For resistor R1 a value of 10 to 20 kΩ is recommended, giving a current of 120 to 60 μA.

The LOSTH voltage equals $\frac{R2}{R1} \times V_{ref}$

Voltage V_{ref} represents a temperature stabilized and accurate reference voltage of 1.2 V. The minimum threshold level corresponds to 0 V and the maximum to 1.2 V. Hence, the value of R2 may not be higher than R1. The accuracy of the LOSTH voltage depends mainly on carefully choosing the values of the two external resistors.

Instead of using resistors (R1 and R2) to set the LOS threshold, an accurate external voltage source can also be used.

If no resistor is connected to LOSTH1 (or LOSTH2), or an external voltage higher than $\frac{2}{3} \times V_{CC}$ is applied to the pin, the LOS detection circuit (including the RSSI reading for that channel) is automatically switched off to reduce power dissipation. This 'auto power off' only works if UI = V_{EE}, i.e. manual control of the TZA3012AHW. In I^2C-bus mode, several I^2C-bus bits allow flexible configuration.

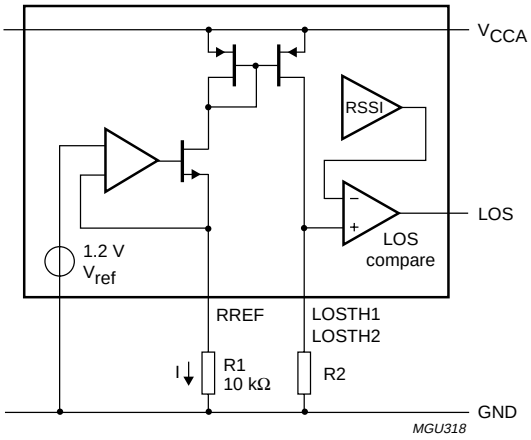


Fig.5 Setting the LOSTH reference level by external resistors.

Slice level adjustment

The TZA3012AHW uses a slice level circuit to counter the affects of asymmetrical noise that can occur in some optical transmission systems. The slice level circuit improves pre-detection signal-to-noise ratio by adding a DC offset to the input signal. The offset required will depend on the characteristics of the photo detector in the optical front-end and the amplitude of the received signal. The slice level is adjustable between −50 mV and +50 mV in 512 steps of 0.2 mV.

The slice level function is enabled by setting bits SL1 and SL2 in I^2C-bus registers LIMLOS1CNF (address BDH) and LIMLOS2CNF (address BFH) for channel 1 and channel 2 respectively. The slice level is set by sign and magnitude convention. The sign, either positive or negative (polarity), is set by I^2C-bus bits SL1SGN and SL2SGN. The magnitude, 0 to 50 mV in 256 steps, is set by an 8-bit D/A converter via I^2C-bus register LIMSLICE1 (address C0H) and LIMSLICE2 (C1H) for channel 1 and channel 2 respectively.

The introduced offset is not present at inputs IN and INQ to prevent the logarithmic RSSI detector from detecting the offset as a valid input signal.

Data and Clock Recovery (DCR)

The TZA3012AHW recovers the clock and data contents from the incoming bit stream; see Fig.6. The DCR uses a combined frequency and phase locking scheme, providing reliable and quick data acquisition at any bit rate between 30 Mbits/s and 3.2 Gbits/s. The DCR contains a Voltage Controlled Oscillator (VCO), Frequency Window Detector (FWD), octave divider M, main divider N, fractional divider K, reference divider R, and a phase detector. The internal VCO is phase-locked to a reference clock signal of typically 19.44 MHz applied to pins CREF and CREFQ.

The FWD is a conventional frequency locked PLL, which, at power-up, initially applies a coarse adjustment to the free running VCO frequency. The FWD checks the VCO frequency, which has to be within a 1000 ppm (parts per million) window around the desired frequency. The FWD then compares the divided VCO frequency (also available on pins PRSCLO and PRSCLOQ) with the reference frequency, usually 19.44 MHz, on pins CREF and CREFQ. If the VCO frequency is found to be outside this window, the FWD disables the Data Phase Detector (DPD) and forces the VCO to a frequency within the window. As soon as the ‘in window’ condition occurs, which is visible on pin INWINDOW, the DPD starts acquiring lock on the incoming bit stream. Since the VCO frequency is very close to the expected bit rate, the phase acquisition will be almost instantaneous, resulting in quick phase lock to the incoming data stream.

Although the VCO is now locked to the incoming bit stream, the FWD is still supervising the VCO frequency and takes over control if the VCO drifts outside the predefined frequency window. This might occur during a ‘loss of signal’ situation. Due to the FWD, the VCO frequency is always close to the required bit rate, enabling rapid phase acquisition if the lost input signal returns.

The default frequency window of 1000 ppm means that the reference frequency does not need to be highly accurate or stable. Any crystal-based oscillator that generates a reasonably accurate frequency, such as 100 ppm, is suitable.

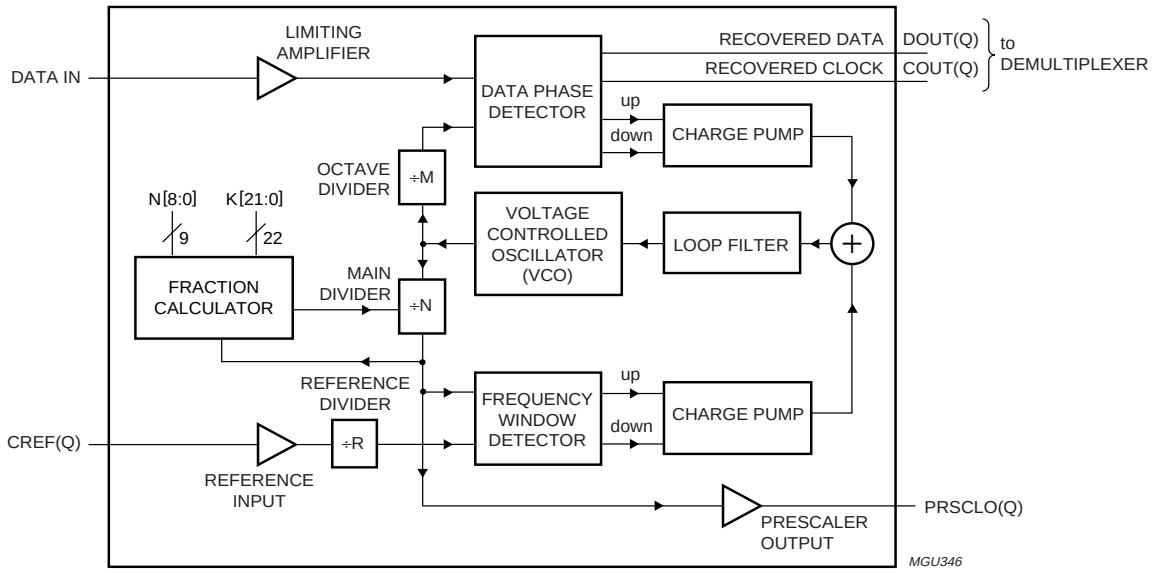


Fig.6 Block diagram of data and clock recovery.

Fractional N synthesizer

The DCR uses a fractional N-type synthesizer to provide the A-rate functionality that allows the DCR to synchronize to incoming data, regardless of its bit rate.

The DCR has a 22-bit fractional N capability which allows any combination of bit rate and reference frequency between 18 × R and 21 × R MHz, where R is the reference division factor. The LSB (bit k[0]) of the fractional divider, should be set to logic 1 to avoid limit cycles. These are cycles of less than maximum length that generate spurs in the frequency spectrum. This leaves 21 bits (k[21:1]) available for programming the fraction, allowing a resolution frequency of approximately 10 Hz at a fixed reference frequency.

Programming the reference clock

Pre-programmed operation requires a reference clock frequency of between 18 and 21 MHz connected to pins CREF and CREFQ. However, to obtain the bit rates in Table 3, the reference clock frequency must be 19.44 MHz. For SDH/SONET applications, a reference clock frequency of 19.44 × R MHz is preferred.

I²C-bus control operation allows any one of four possible reference clock frequency ranges to be selected by programming reference divider R using bits REFDIV in I²C-bus register DCRCNF (address B6 H).
The REFDIV bit settings, reference clock frequency ranges, and division factor are shown in Table 7.
The reference frequency is always divided internally to the lowest range of 18 to 21 MHz.

Table 7 Truth table for bits REFDIV in I²C-bus register DCRCNF

REFDIV	R DIVISION FACTOR	SDH/SONET REFERENCE FREQUENCY (MHz)	REFERENCE FREQUENCY RANGE (MHz)
00	1	19.44	18 to 21
01	2	38.88	36 to 42
10	4	77.76	72 to 84
11	8	155.52	144 to 168

Programming the DCR

The following dividers are used to program the clock synthesizer: the main divider N, the fractional divider K and the octave divider M.

The division factor for M is obtained by first determining in which octave the desired bit rate belongs as shown in Figure 7 and Tables 8 and 9.

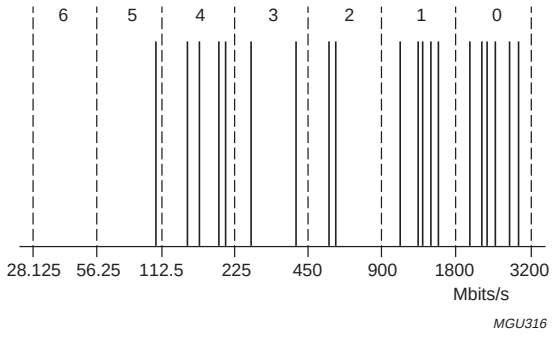


Fig.7 Allocation of octaves for common bit rates shown on a logarithmic scale.

Table 8 Octave designation and M division factor

LOWEST BIT RATE (Mbits/s)	HIGHEST BIT RATE (Mbits/s)	OCTAVE	M DIVISION FACTOR
1800	3200	0	1
900	1800	1	2
450	900	2	4
225	450	3	8
112.5	225	4	16
56.25	112.5	5	32
28.125	56.25	6	64

Table 9 Common optical transmission protocols and corresponding octaves

PROTOCOL	BIT RATE (Mbits/s)	OCTAVE
10GE	3125.00	0
2xHDTV	2970.00	0
STM16/OC48 + FEC	2666.06	0
STM16/OC48	2488.32	0
DV-6000	2380.00	0
Fibre Channel	2125.00	0
HDTV	1485.00	1
D-1 Video	1380.00	1
DV-6010	1300.00	1
Gigabit Ethernet (GE)	1250.00	1
Fibre Channel	1062.50	1
OptiConnect	1062.50	1
ISC	1062.50	1
STM4/OC12	622.08	2
DV-6400	595.00	2
Fibre Channel	425.00	3
OptiConnect	265.63	3
Fibre Channel	212.50	4
ESCON/SBCON	200.00	4
STM1/OC3	155.52	4
FDDI	125.00	4
Fast Ethernet	125.00	4
Fibre Channel	106.25	5
OC1	51.84	6

Once the octave and M division factor are known, the division factors for N and K can be calculated for a given reference frequency using the Flowchart in Fig.8.

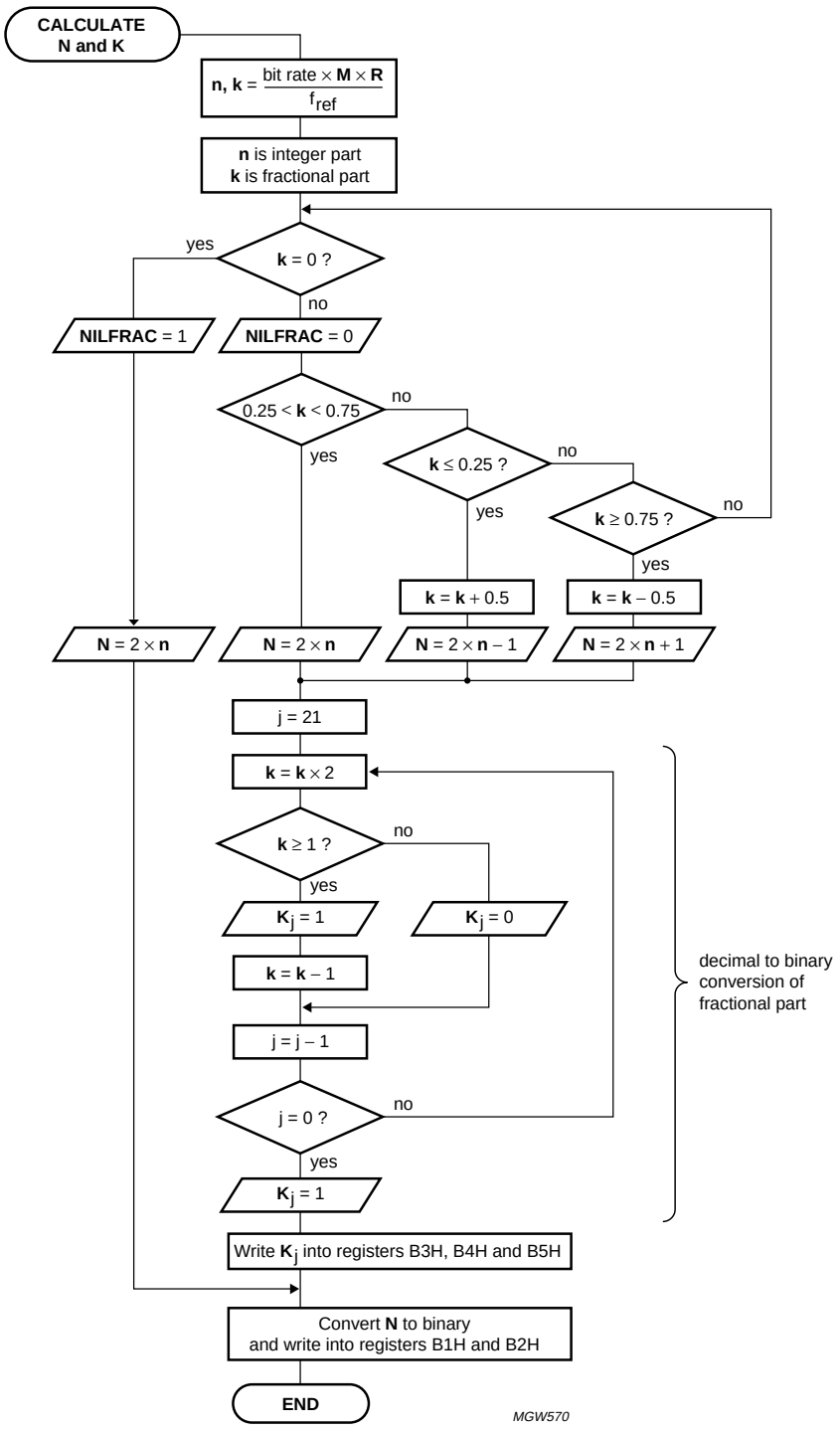


Fig.8 Flowchart for calculating N and K for the required bit rate.

The following examples refer to the flowchart in Fig.8.

Example 1: An SDH or SONET link has a bit rate of 2488.32 Mbits/s (STM16/OC48) that corresponds to octave 0 and an M division factor of 1. If the reference frequency f_{ref} at pins CREF and CREFQ is 77.76 MHz, the division factor R is required to be 4. The initial values for integer n and fractional part k are calculated using the equation:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2488.32\ \text{Mbits} \times 1 \times 4}{77.76\ \text{MHz}} = 128$$

In this example, n = 128 and k = 0. Since k is 0, fractional functionality is not required, so bit NILFRAC in I²C-bus register FRACN2 should be set to logic 1; see Table 19. $N = n \times 2 = 256$ with no further correction required. The resulting values of R = 4, M = 1 and N = 256 are set by I²C-bus registers DCRCNF (Table 22), DIVCNF (Table 16), MAINDIV1 (Table 17) and MAINDIV0 (Table 18).

Example 2: An SDH or SONET link has a bit rate of 2666.057143 Mbits/s (15/14 × 2488.32 Mbits/s) (STM16/OC48 link with FEC) that corresponds to octave 0 and an M division factor of 1. If f_{ref} at pins CREF and CREFQ is 38.88 MHz, the division factor R is required to be 2. The values for n and k are calculated as follows:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2666.05714283\ \text{Mbits} \times 1 \times 2}{38.88\ \text{MHz}} = 137.1428571$$

In this example, n = 137 and k = 0.1428571. Fractional functionality is required, so bit NILFRAC in I²C-bus register FRACN2 should be set to logic 0. Since k is less than 0.25, k is corrected to $k = k + 0.5 = 0.6428571$, and N is corrected to $N = n \times 2 - 1 = 273$. The resulting values of R = 2, M = 1, N = 273 and K = 10 1001 0010 0100 1001 0011 are set by I²C-bus registers DCRCNF (Table 22), DIVCNF (Table 16), MAINDIV1 (Table 17), MAINDIV0 (Table 18), FRACN2 (Table 19), FRACN1 (Table 20) and FRACN0 (Table 21). The FEC bit rate is usually rounded up to 2666.06 Mbits/s, which actually gives a different value for k than in this example.

Example 3: A Fibre Channel link has a bit rate of 1062.50 Mbits/s that corresponds to octave 1 and an M division factor of 2. If f_{ref} at pins CREF and CREFQ is 19.44 MHz, the division factor R is required to be 1. The values for n and k are calculated as follows: $n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{1062.50\ \text{Mbits} \times 2 \times 1}{19.44\ \text{MHz}} = 109.3106996$

In this example, n = 109 and k = 0.3107. Fractional functionality is required, so bit NILFRAC in I²C-bus register FRACN2 should be set to logic 0. Since k is greater than 0.25 and less than 0.75, k does not need to be corrected. N is corrected to $N = n \times 2 = 218$. The resulting values of R = 1, M = 2, N = 218 and K = 01 0011 1110 0010 1000 0001 are set by I²C-bus registers DCRCNF (Table 22), DIVCNF (Table 16), MAINDIV1 (Table 17), MAINDIV0 (Table 18), FRACN2 (Table 19), FRACN1 (Table 20) and FRACN0 (Table 21).

Example 4: A non standard transmission link has a bit rate of 3012 Mbits/s that corresponds to octave 0 and an M division factor of 1. If f_{ref} at pins CREF and CREFQ is 20.50 MHz, the division factor R is required to be 1. The values for n and k are calculated as follows: $n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{3012\ \text{Mbits} \times 1 \times 1}{20.50\ \text{MHz}} = 146.9268293$

In this example, n = 146 and k = 0.9268293. Fractional functionality is required, so bit NILFRAC in I²C-bus register FRACN2 should be set to logic 0. Since k is greater than 0.75, k is corrected to $k = k - 0.5 = 0.4268293$, and N is corrected to $N = n \times 2 + 1 = 293$. The resulting values of R = 1, M = 1, N = 293 and K = 01 1011 0101 0001 0010 1011 are set by I²C-bus registers DCRCNF (Table 22), DIVCNF (Table 16), MAINDIV1 (Table 17), MAINDIV0 (Table 18), FRACN2 (Table 19), FRACN1 (Table 20) and FRACN0 (Table 21).

If the I²C-bus is not used, the clock synthesizer can be set up for the eight pre-programmed bit rates shown in Table 3, by pins DR0, DR1 and DR2 using an external reference clock frequency of 19.44 MHz.

Prescaler outputs

The frequency of prescaler outputs PRSCLO and PRSCLOQ is the VCO frequency divided by a ratio of N.K. If the synthesizer is in-lock, the frequency of the prescaler output is equal to the reference frequency at CREF and CREFQ divided by R which also corresponds to the recovered data rate. This provides an accurate reference that can be used by other phase locked loops in the application. If required, the polarity of the prescaler outputs can be inverted by setting bit PRSCLOINV in I^{2}C-bus register IOCNF0 (address CBH) to logic 1. If no prescaler information is required, its output can be disabled by setting bit PRSCLOEN in the same register to logic 0. In addition, the prescaler output can be set for type of output, termination mode and signal amplitude. These parameter settings also apply to the parallel output clock POCLK and POCLKQ and parity error output PARERR and PARERRQ. For programming details, These parameter settings also apply to the parallel demultiplexer outputs. For programming details; see Section “Configuring the parallel interface”.

Programming the FWD

The default window for frequency acquisition is 1000 ppm around the desired bit rate. The size of window determines the amount of variation in the frequency of the applied reference clock, and VCO, that is tolerated by the FWD. The window size can be set to other predefined values between 250 and 2000 ppm by bits WINDOWSIZE in I^{2}C-bus register DCRCNF (address B6H).

An additional feature allows the size of the frequency acquisition window to be set to 0 ppm, which effectively removes the ‘dead zone’ from the FWD, converting it to a classical PLL. The VCO will then be directly phase-locked to the reference signal instead of the incoming bit stream. This is implemented by either applying a LOW level to pin WINSIZE, or by setting bit WINSIZE to logic 0 and bit I2CWINSIZE to logic 1 in I^{2}C-bus register DCRCNF; see Table 10.

Table 10 Truth table for pin WINSIZE

WINSIZE	WINDOW SIZE (ppm)
LOW	0
HIGH	1000

Accurate clock generation during loss of signal

During a loss of signal, there is no data present for clock recovery to use. A frequency acquisition window size of zero will make the recovered clock frequency equal to the reference frequency, including its tolerance.

Setting bit AUTOWIN in I^{2}C-bus register DCRCNF makes the window size dependent on the LOS status of the active limiter channel. If the optical input signal is lost, the FWD automatically selects the 0 ppm window size, so that the VCO is directly phase-locked to the reference signal. This ensures that the output clock signal remains stable during loss of signal, and automatically reverts to normal DCR operation when the input signal returns.

Note that the accuracy of the reference frequency must be better than 20 ppm for the application to comply with ITU-T recommendations.

INWINDOW signal

The status of the FWD circuit is indicated by the level on pin INWINDOW. A HIGH level indicates that the VCO is within the defined frequency acquisition window size, and a LOW level indicates that the VCO is outside the defined window size. The status of the FWD circuit is also indicated by bit INWINDOW in I^{2}C-bus registers INTERRUPT and STATUS.

Jitter performance

The clock synthesizer is optimized for minimum jitter generation. For all SDH/SONET bit rates, the generated jitter complies with ITU-T standard G.958 using a pure reference clock. To ensure negligible loss of performance when a reference clock is used, the reference signal should have a single sideband phase noise of better than −140 dBc/Hz, at frequencies of more than 12 kHz from the carrier. If reference divider R is used, this negative value is allowed to increase at approximately 20 $\times$ log (R).

Demultiplexer

The demultiplexer converts the serial input bit stream to parallel formats of 1:16, 1:10, 1:8, and 1:4. The output data is available on a scalable bus, of which the output driver type can be either LVPECL or CML. In addition to the deserializing function, the demultiplexer comprises a parity calculator and a frame header detection circuit.
A calculated parity of EVEN is output at pins PARITY and PARITYQ. A detected frame header pattern in the data stream results in a 1 clock cycle wide pulse on outputs FP and FPQ.

Making pin ENBA HIGH automatically aligns the parallel output into logical bytes or words. The same function is implemented by setting bit ENBA in I²C-bus register DMXCNF (address A8H).

To support most commonly used transmission systems and protocols, the demultiplexing ratio can be set to 1:16, 1:10, 1:8, and 1:4, and the frame header pattern programmed to any 32 or 10-bit pattern; see Section “Frame detection”.

If required, the demultiplexer output can be forced into a fixed logic 0 state by bit DMXMUTE in I²C-bus register DMXCNF.

Adjustable demultiplexing ratio

For optimum layout connectivity, the physical positions of parallel data bus pins D00 to D15 and D00Q to D15Q on the chip are located either side of pin V_{EE} (pin 63). The number of parallel data bus outputs that are used depends on the demultiplexing ratio selected by pins DMXR0 and DMXR1 or by bits DMXR in I²C-bus register DMXCNF (address A8 H). Any unused parallel data bus outputs are disabled. The configuration settings and active outputs for each demultiplexing ratio are shown in Table 11.

In I²C-bus control mode, the default demultiplexing ratio is 16:1.

To allow optimum layout connectivity, the pin designations of the parallel data bus bits can be reversed so that the default designated pin for D15 (MSB) is exchanged with the default designated pin for D0 (LSB). This is implemented by bit BUSSWAP in I²C-bus register DMXCNF (address A8H).

The highest supported speed for the parallel data bus is 400 Mbits/s. Therefore a demultiplexing ratio of 4:1 will support bit rates of up to 1.6 Gbits/s.

Table 11 Setting demultiplexing ratio

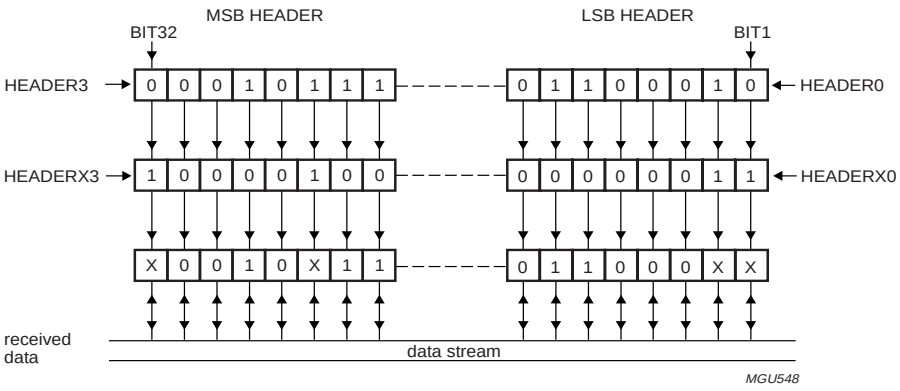
PIN DMXR1	PIN DMXR0	BITS DMXR (REG DMXCNF)	DEMULTIPLEXING RATIO	ACTIVE OUTPUTS LSB to MSB
LOW	LOW	00	1:4	D06 to D09
LOW	HIGH	01	1:8	D04 to D11
HIGH	LOW	10	1:10	D03 to D12
HIGH	HIGH	11	1:16	D00 to D15

Frame detection

Byte alignment is enabled if the Enable Byte Alignment input (pin ENBA) is HIGH, or if bit I2CENBA and bit ENBA are both logic 1 in I²C-bus register DMXCNF (address A8H). Whenever the incoming data has a 32-bit or 10-bit sequence that matches the programmed frame header pattern, the data is formatted into logical bytes or words, and a frame pulse is generated on differential outputs FP and FPQ. Any frame header pattern can be programmed in I²C-bus registers HEADER0 to HEADER3.

Any bit position can be programmed with a ‘don’t care’ to give a frame header pattern that is either much shorter than 32 or 10 bits, or has gaps. The “don’t care” bits are produced by programming a pattern into I²C-bus registers HEADERX0 to HEADERX3 which is used to mask the programmed frame header pattern as shown in the example Fig.9.

The default frame header pattern is F6F62828H, corresponding to the middle section of the standard SDH/SONET frame header (the last two A1 bytes plus the first two A2 bytes).



'X' = "don't care"
'MSB' = Most Significant Byte.

Fig.9 Example of programming the frame header pattern.

If ENBA is LOW, no active alignment takes place. However, if the frame header pattern occurs in the formatted data, a frame pulse will still be output on pins FP and FPQ.

For 10-bit oriented protocols, such as Gigabit Ethernet, the frame header detection operates on a 10-bit pattern sequence. These 10 bits should be programmed into I^2C-bus registers HEADER3 and the two MSBs of HEADER2; the remaining 22 bits are ignored. A 'don't care' pattern overlay can be programmed in I^2C-bus register HEADERX3 and the two MSBs of HEADERX2.

Since some 10-bit oriented protocols use a DC balancing code, the detection pattern could appear in complementary form in the data stream. By setting bit CMPL in I^2C-bus register DMXCNF (address A8H), the header detection scans the data stream for both the programmed pattern and its complement simultaneously. Either occurrence produces a 'byte' alignment and a corresponding frame pulse on pins FP and FPQ.

The default pattern (after power-up) is '0011111010' or K28.5 character plus alternating 010. This is the only pattern containing five consecutive bits of the same sign.

Receiver framing in SDH/SONET applications

Figure 10 shows a typical SDH/SONET reframe sequence involving byte alignment. Frame and byte boundary detection is enabled on the rising edge of ENBA and remains enabled while ENBA is HIGH. Boundaries are recognized on receipt of the second A2 byte and FP goes HIGH for one POCLK cycle.

In 1:16 mode, the first two A2 bytes in the frame header are the first data word to be reported with the correct alignment on the outgoing data bus (D00 to D15). In 1:8 mode the first A2 byte is the first aligned data byte (D04 to D11), while in 1:4 mode the most significant nibble of the first A2 byte is the first aligned data (D06 to D09).

When interfacing with a section terminating device, ENBA must remain HIGH for a full frame after the initial frame pulse. This is to allow the section terminating device to verify internally that frame and byte alignment are correct; see Fig.11. Byte boundary detection is disabled on the first FP pulse after ENBA has gone LOW.

Figure 12 shows frame and byte boundary detection activated on the rising edge of ENBA, and deactivated by the first FP pulse after ENBA has gone LOW.

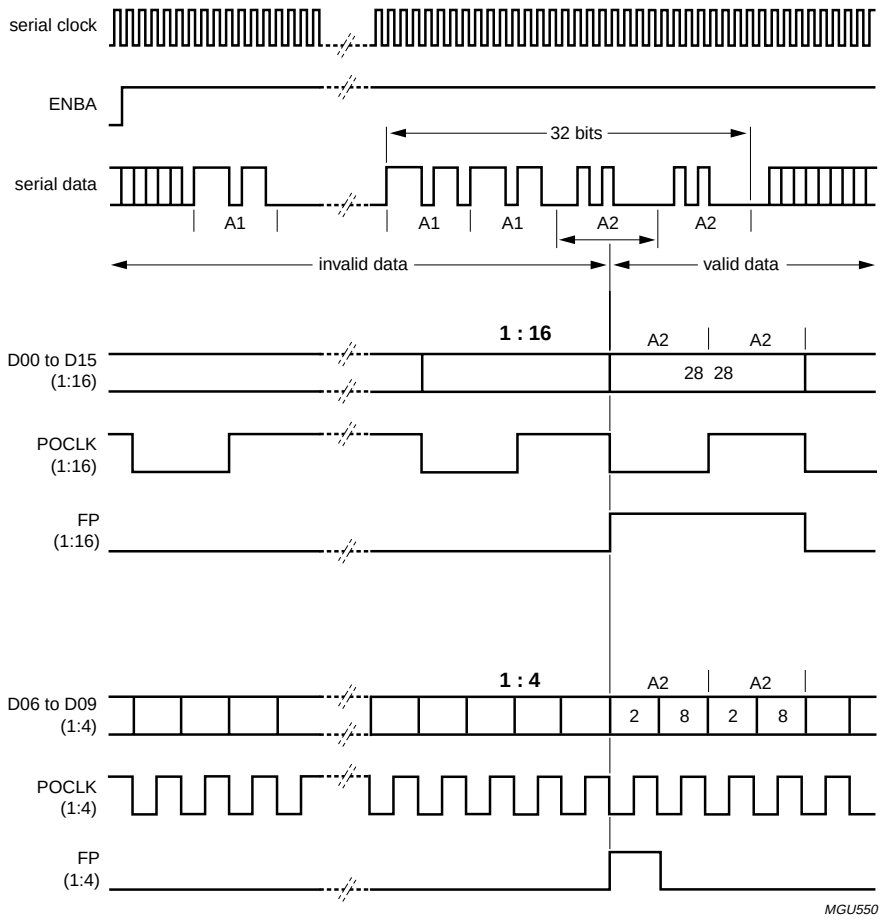


Fig.10 Frame and byte detection in SDH/SONET application.

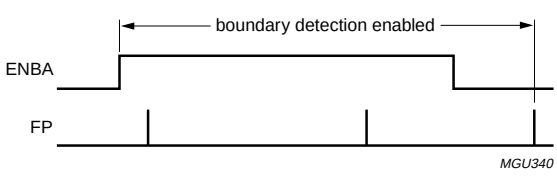


Fig.11 ENBA timing with section terminating device.

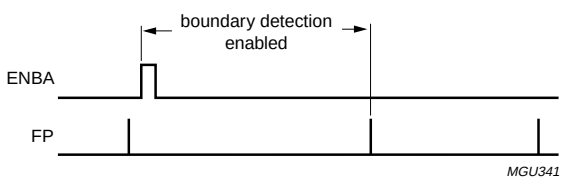


Fig.12 Alternate ENBA timing.

Parity generation

Outputs PARITY and PARITYQ provide the even parity of the byte/word that is currently available on the parallel bus. Odd parity can be output by setting bit PARINV to logic 1 in I²C-bus register IOCNF2 (address C9H). If no parity output is required, and/or to reduce output power, set bit PAREN, in the same register, to logic 0.

Configuring the parallel interface

There are several options for configuring the parallel interface which comprises the parallel data bus and associated outputs. The options for parallel data output D00 to D15 and D00Q to D15Q, parallel clock output POCLK and POCLKQ, parity output PARITY and PARITYQ, frame pulse output FP and FPQ, and prescaler output PRSCLO and PRSCLOQ are: output driver type, termination mode, output amplitude, signal polarity, and selective enabling or disabling. The parallel data bus pin designations can also be reversed and/or muted. These options are set in I²C-bus registers IOCNF3 (address C8H) and IOCNF2 (address C9H), IOCNF0 (address CBH) and DMXCNF (address A8H).

I²C-bus register IOCNF3, bit MFOUTMODE selects either the CML or LVPECL output driver. The default is LVPECL. Bit MFOUTTERM sets the output termination mode to either standard LVPECL or floating termination, or in CML mode, to either DC or AC-coupled. In all cases, bits MFS adjust the amplitude. The default output amplitude is 800 mV (p-p) single-ended.

In I²C-bus register IOCNF2, setting bit PDEN to logic 0 disables the parallel interface output driver. This is not the same effect as setting bit DMXMUTE in I²C-bus register DMXCNF (address A8H), which forces the outputs to a logic 0 state. Setting bit PDINV to logic 1 in I²C-bus register IOCNF2 (address C9H) inverts the polarity of the parallel data. Setting bit POCLKINV to logic 1 in the same register inverts the clock output so that the clock edge is shifted by half a clock cycle, changing the rising edge to a falling edge. This function can be used to resolve a parallel data bus timing problem. The parallel bus clock is disabled by setting bit POCLKEN to logic 0 in the same register. Control bits in the same register and in register IOCNF0 (address CBH) also apply the same options to the parity, frame pulse and prescaler outputs.

Loop mode I/Os

In line loopback mode, the internal data and clock routing switch routes the received serial data and recovered clock to outputs DOUT, DOUTQ COUT and COUTQ instead of to the demultiplexer. Line loopback mode is activated by a LOW level on pin ENLOUTQ. Line loopback mode is also selected by setting bit ENLOOPOUT and bit I2CLOOPMODE in I²C-bus register DIVCNF (address B0H).

In diagnostic loopback mode, the demultiplexer selects the serial data and clock signals at loop mode input pins DLOOP, DLOOPQ and CLOOP, CLOOPQ instead of from the DCR. Diagnostic loopback mode is activated by a LOW level on pin ENLINQ. Diagnostic loopback mode is also selected by setting bit ENLOOPIN and bit I2CLOOPMODE in I²C-bus register DIVCNF (address B0H).

Configuring the RF I/Os

The polarity of specific RF serial data and clock I/O signals can be inverted using I²C-bus register IOCNF1 (address CAH).

To allow easier connection to other ICs, the pin designations for input data can be exchanged with the pin designations for input clock. The pin designations for output data and output clock can also be exchanged.

The default pin designations for Loop mode input data and clock are exchanged by setting bit CDINSWAP in I²C-bus register IOCNF1 so that signals at pins CLOOP and CLOOPQ are treated as data and signals at pins DLOOP and DLOOPQ are treated as clock.

The default pin designations for Loop mode output data and clock are exchanged by setting bit CDOUTSWAP in I²C-bus register IOCNF1 so that signals at pins COUT and COUTQ are treated as data and signals at pins DOUT and DOUTQ are treated as clock.

The amplitude of the RF serial output signals in CML drive mode, is adjustable (in 16 steps) between 60 mV (p-p) and 1000 mV (p-p), single-ended, controlled by bits RFS and RFSWING in I²C-bus register IOCNF0 (address CBH). The default amplitude is 80 mV (p-p), single-ended. The RF serial outputs are AC-coupled.

CMOS control inputs

CMOS control inputs UI, INSEL, WINSIZE, DMXR0, DMXR1, ENBA, ENLOUTQ, ENLINQ and CS(DR0) have an internal pull-up resistor so that these pins go HIGH when open circuit, and only go LOW when deliberately forced. This is also true for pins DR1 and DR2 in pre-programmed mode (pin UI is LOW). In I^2C-bus control mode (pin UI is HIGH), pins SCL and SDA comply with the I^2C-bus interface standard.

Power supply connections

Four separate supply domains (V_{DD}, V_{CCD}, V_{CCO} and V_{CCA}) provide isolation between the various functional blocks. Each supply domain should be connected to a common V_{CC} using a separate filter. **All supply pins, including the exposed die pad, must be connected**. The die pad connection to ground must have the lowest possible inductance. Since the die pad is also used as the main ground return of the chip, this connection must also have a low DC impedance. The voltage supply levels should be in accordance with the values specified in Chapters “Characteristics” and “Limiting values”.

All external components should be surface mounted, with a preferable size of 0603 or smaller. The components must be mounted as close to the IC as possible.

Interrupt register

The following events are recorded by setting the appropriate bit(s) in I^2C-bus register INTERRUPT (address 00 H):

- Loss of signal on channel 1
- Loss of signal on channel 2
- DCR frequency locked or unlocked
- Limiter channel switching enabled or disabled
- High junction temperature.

When register INTERRUPT is polled by an I^2C-bus read action, any set bits are reset. If a condition is still active, the corresponding bit remains set.

Status register

The current status of the conditions that are recorded by register INTERRUPT are indicated by setting the appropriate bit(s) in I^2C-bus register STATUS (address 01H). A bit is set only for the period that the condition is active and resets when the condition clears. Register STATUS is polled by an I^2C-bus read action.

Interrupt generation

An interrupt is generated if an interrupt condition sets a bit in I^2C-bus register INTERRUPT (address 00H) and if the bit is not masked by I^2C-bus register INTMASK (address CCH). Only the high junction temperature interrupt bit is not masked by default. A generated interrupt is indicated by an active logic level at pin INT. The active output level used is set by bit INTPOL in I^2C-bus register INTMASK. The default is an active LOW level. Bit INTOUT sets the output mode at pin INT to either open-drain or to standard CMOS. The default is open-drain. An active LOW output in open-drain mode allows several receivers to be connected together, and requires only one 3.3 kΩ pull-up resistor.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

Refer to Fig.13. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

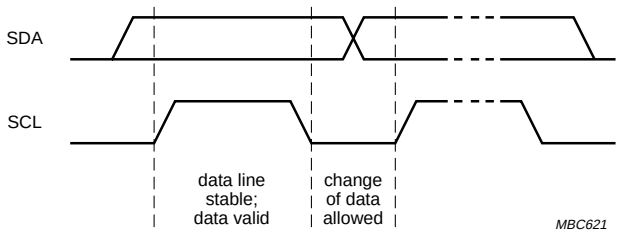


Fig.13 Bit transfer.

Start and stop conditions

Refer to Fig.14. Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

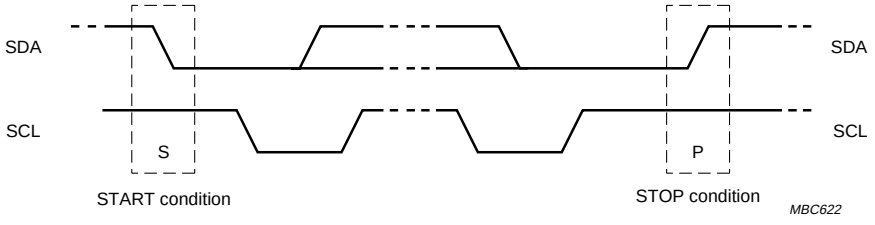


Fig.14 Definition of start and stop conditions.

System configuration

Refer to Fig.15. A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

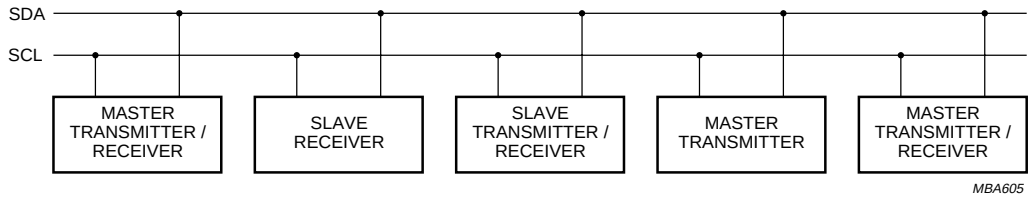


Fig.15 System configuration.

Acknowledge

Refer to Fig.16. Only one data byte is transferred between the start and stop conditions during a write from the transmitter to the receiver. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition; see Fig.19.

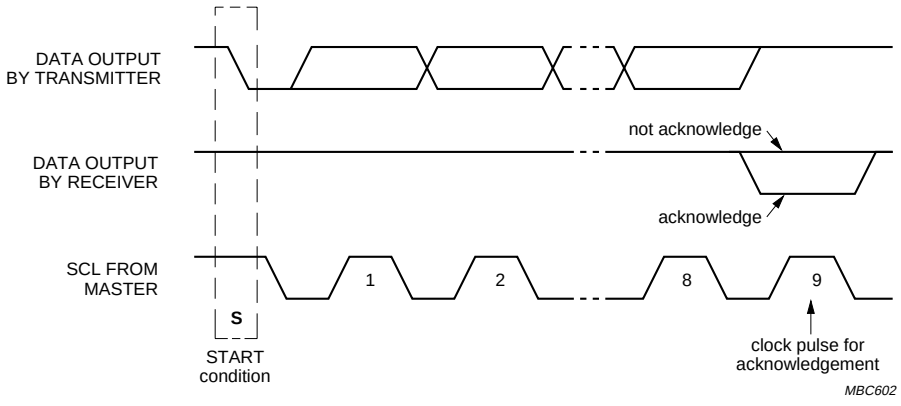


Fig.16 Acknowledgment on the I^2C-bus.

I²C-BUS PROTOCOL

Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The address byte is sent after the start condition.

The master transmitter/receiver either reads from the read-registers or writes to the write-registers. It is not possible to read from and write to the same register. Figure 17 shows how the slave and register address bytes are defined.

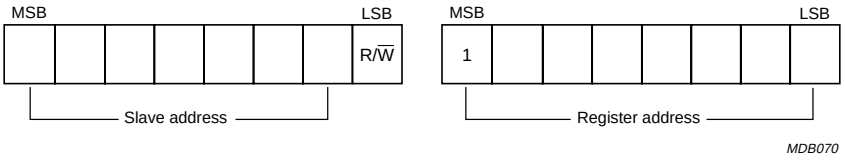


Fig.17 Slave and register addresses.

Read/Write protocols

The protocol for writing to a single register is shown in Fig.18. The transmitter sends the address of the slave device, waits for an acknowledge from the slave, sends register address, waits for an acknowledge from the slave, sends data byte, waits for an acknowledge from the slave, followed by a stop condition.

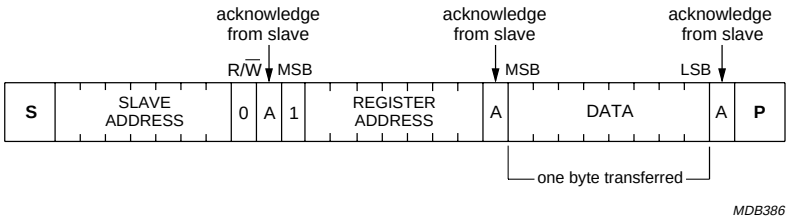
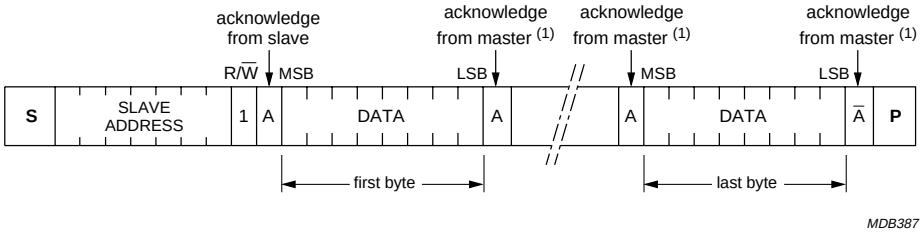


Fig.18 Write protocol.

The protocol for reading one or more registers is shown in Fig.19. The receiver sends the address of the slave device, waits for an acknowledge from the slave, receives data byte(s) from the slave (the TZA3012AHW starts sending data after asserting an acknowledge), after receiving the data, the receiver sends an acknowledge or, if finished, a not-acknowledge, followed by a stop condition.



(1) The master receiver must signal an end of data to the slave transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave.

Fig.19 Read protocol.

I²C-bus registers

The I²C-bus registers are accessed in I²C-bus control mode by setting pin UI HIGH or leaving pin UI open circuit. Address and read/write data are transferred serially via pin SDA and clocked via pin SCL when pin CS (chip select) is HIGH. The I²C-bus registers are listed in Table 12.

Table 12 I²C-bus registers

ADDRESS (HEX)(1)	NAME	FUNCTION	DEFAULT VALUE	READ/ WRITE
00	INTERRUPT	Interrupt register; see Table 13	–	R
01	STATUS	Status register; see Table 14	–	R
A0	HEADER3	Programmable header, most significant byte 1:10 ratio	1111 0110 0011 1110	W
A1	HEADER2	Programmable header 1:10 ratio	1111 0110 10X XXXX	W
A2	HEADER1	Programmable header	0010 1000	W
A3	HEADER0	Programmable header, least significant byte	0010 1000	W
A4	HEADERX3	Programmable header, don't care, most significant byte 1:10 ratio	0000 0000 0000 0000	W
A5	HEADERX2	Programmable header, don't care 1:10 ratio	0000 0000 00XX XXXX	W
A6	HEADERX1	Programmable header, don't care	0000 0000	W
A7	HEADERX0	Programmable header, don't care, least significant byte	0000 0000	W
A8	DMXCNF	Demultiplexer configuration register; see Table 15	0000 1011	W
B0	DIVCNF	Octave and loop mode configuration register; see Table 16	0000 0000	W
B1	MAINDIV1	Main divider division factor N; most significant byte; range 128 to 511; see Table 17	0000 0001	W
B2	MAINDIV0	Main divider division factor N; least significant byte; see Table 18	0000 0000	W
B3	FRACN2	Fractional divider division factor K; see Table 19	1000 0000	W
B4	FRACN1	Fractional divider division factor K; see Table 20	0000 0000	W
B5	FRACN0	Fractional divider division factor K; see Table 21	0000 0000	W
B6	DCRCNF	DCR configuration register; see Table 22	0000 1100	W
BC	LIMLOS1TH	Limiter 1 loss of signal threshold register; range 0 to 255	0000 0000	W
BD	LIMLOS1CNF	Limiter 1 loss of signal configuration register; see Table 23	0000 1101	W
BE	LIMLOS2TH	Limiter 2 loss of signal threshold register; range 0 to 255	0000 0000	W
BF	LIMLOS2CNF	Limiter 2 loss of signal configuration register; see Table 24	0000 1101	W
C0	LIMSLICE1	Limiter 1 slice level register; range 0 to 255	0000 0000	W
C1	LIMSLICE2	Limiter 2 slice level register; range 0 to 255	0000 0000	W
C2	LIMCNF	Limiter configuration register; see Table 25	0000 1000	W
C8	IOCNF3	Parallel interface output configuration register 3; see Table 26	0000 1100	W
C9	IOCNF2	Parallel interface output configuration register 2; see Table 27	1010 1010	W
CA	IOCNF1	RF serial I/O configuration register 1; see Table 28	0000 0000	W
CB	IOCNF0	RF serial output configuration register 0; see Table 29	0010 0011	W
CC	INTMASK	Interrupt masking register; see Table 30	0101 0000	W

Notes

1. Addresses not shown must not be accessed.
2. X = don't care.

Table 13 Register INTERRUPT (address 00H)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loss of signal on channel 1	LOS1
							1	no signal present (loss of signal condition)	
							0	signal present	
								loss of signal on channel 2	LOS2
						1		no signal present (loss of signal condition)	
						0		signal present	
								DCR frequency indication	INWINDOW
					1			frequency outside predefined window (unlocked)	
					0			frequency inside predefined window (locked)	
								auto-switching between channels	LIMSW
				1				enabled (active limiter indicated in Status register)	
				0				disabled (no auto-switching between channels)	
								high junction temperature	TALARM
			1					junction temperature ≥130 °C	
			0					junction temperature <130 °C	
0	0	0						reserved	

Table 14 Register STATUS (address 01H)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loss of signal on channel 1	LOS1
							1	no signal present (loss of signal condition)	
							0	signal present	
								loss of signal on channel 2	LOS2
						1		no signal present (loss of signal condition)	
						0		signal present	
								DCR frequency indication	INWINDOW
					1			frequency inside predefined window (locked)	
					0			frequency outside predefined window (unlocked)	
								active limiter indication	LIMSEL
				1				limiter 1 active	
				0				limiter 2 active	
								high junction temperature	TALARM
			1					junction temperature ≥130 °C	
			0					junction temperature <130 °C	
0	0	0						reserved	

Table 15 Register DMXCNF (address A8H); default value 0BH

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								demultiplexing ratio	DMXR
						1	1	1:16	
						1	0	1:10	
						0	1	1:8	
						0	0	1:4	
								demultiplexing ratio programming	I2CDMXR
					1			via I^2C-bus interface	
					0			via pins DMXR0 and DMXR1	
								frame header detection in 1:10 Gigabit Ethernet mode	CMPL
				1				simultaneously check for complementary header	
				0				check programmed header only	
								parallel data bus bit designations	BUSSWAP
			1					D00 = MSB, D15 = LSB (reversed)	
			0					D15 = MSB, D00 = LSB (normal)	
								demultiplexer mute parallel interface outputs	DMXMUTE
		1						mute; parallel interface outputs forced to logic 0	
		0						no mute	
								enable/disable byte alignment	ENBA
	1							enabled	
	0							disabled	
								ENBA control	I2CENBA
1								via I^2C-bus interface	
0								via pin ENBA	
0	0	0	0	1	0	1	1	default value	

Table 16 Register DIVCNF (address B0H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								octave divider division factor M, octave selection	DIV_M
					0	0	0	M = 1, octave number 0	
					0	0	1	M = 2, octave number 1	
					0	1	0	M = 4, octave number 2	
					0	1	1	M = 8, octave number 3	
					1	0	0	M = 16, octave number 4	
					1	0	1	M = 32, octave number 5	
					1	1	0	M = 64, octave number 6	
			0	0				reserved	
								enable/disable loop mode inputs	ENLOOPIN
		1						enabled	
		0						disabled	
								enable/disable loop mode outputs	ENLOOPOUT
	1							enabled	
	0							disabled	
								loop mode control	I2CLOOPMODE
1								via I^2C-bus interface	
0								via pin ENLINQ and/or pin ENLOUTQ	
0	0	0	0	0	0	0	0	default value	

Table 17 Register MAINDIV1 (address B1H); default value 01H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
–	–	–	–	–	–	–	N8	main divider division factor N; N8 = MSB	DIV_N
0	0	0	0	0	0	0	1	default value	

Table 18 Register MAINDIV0 (address B2H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
N7	N6	N5	N4	N3	N2	N1	N0	main divider division factor N; N0 = LSB	DIV_N
0	0	0	0	0	0	0	0	default value	

Table 19 Register FRACN2 (address B3H); default value 80H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
NF	X	K21	K20	K19	K18	K17	K16	fractional divider division value K; K21 = MSB	DIV_K
1 0								NILFRAC control bit no fractional N functionality fractional N functionality	NILFRAC
1	0	0	0	0	0	0	0	default value	

Note

1. X = don't care.

Table 20 Register FRACN1 (address B4H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
K15	K14	K13	K12	K11	K10	K9	K8	fractional divider division value K	DIV_K
0	0	0	0	0	0	0	0	default value	

Table 21 Register FRACN0 (address B5H); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
K7	K6	K5	K4	K3	K2	K1	K0	fractional divider division value K; K0 = LSB	DIV_K
0	0	0	0	0	0	0	0	default value	

Table 22 Register DCRCNF (address B6H); default value 0CH

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								FWD window size; relative to bit rate	WINDOWSIZE
					0	1	1	2000 ppm	
					1	0	0	1000 ppm	
					1	0	1	500 ppm	
					1	1	0	250 ppm	
								FWD window size select; WINDOWSIZE value or zero	WINSIZE
				1				window size specified by 'WINDOWSIZE'; PLL frequency allowed to vary around the reference frequency	
				0				window size = 0 ppm; PLL frequency directly synthesized from reference frequency	
								WINSIZE control bit	I2CWINSIZE
			1					via I^2C-bus interface	
			0					via pin WINSIZE	
								automatic window size select	AUTOWIN
		1						enabled	
		0						disabled	
								reference divider division factor R; reference frequency	REFDIV
1	1							R = 8; 155.52 MHz	
1	0							R = 4; 77.76 MHz	
0	1							R = 2; 38.88 MHz	
0	0							R = 1; 19.44 MHz	
0	0	0	0	1	1	0	0	default value	

Table 23 Register LIMLOS1CNF (address BDH); default value 0DH

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loss of signal detection on channel 1	LOS1
							1	enabled	
							0	disabled	
								loss of signal threshold level control bit on channel 1	I2CREFLVL1
						1		via I^2C-bus interface by internal DAC; register LIMLOS1TH	
						0		via analog voltage on pin LOSTH1	
								loss of signal detection hysteresis on channel 1	HYS1
			0	0	0			0 dB	
			0	0	1			1 dB	
			0	1	0			2 dB	
			0	1	1			3 dB	
			1	0	0			4 dB	
			1	0	1			5 dB	
			1	1	0			6 dB	
			1	1	1			7 dB	
								slice level on channel 1	SL1
		1						enabled	
		0						disabled	
								slice level sign on channel 1	SL1SGN
	1							positive	
	0							negative	
								polarity of LOS on channel 1	LOS1POL
1								inverted	
0								normal	
0	0	0	0	1	1	0	1	default value	

Table 24 Register LIMLOS2CNF (address BFH); default value 0DH

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loss of signal detection on channel 2	LOS2
							1	enabled	
							0	disabled	
								loss of signal threshold level control bit on channel 2	I2CREFLVL2
						1		via I^2C-bus interface by internal DAC; register LIMLOS2TH	
						0		via analog voltage on pin LOSTH2	
								loss of signal detection hysteresis on channel 2	HYS2
			0	0	0			0 dB	
			0	0	1			1 dB	
			0	1	0			2 dB	
			0	1	1			3 dB	
			1	0	0			4 dB	
			1	0	1			5 dB	
			1	1	0			6 dB	
			1	1	1			7 dB	
								slice level on channel 2	SL2
		1						enabled	
		0						disabled	
								slice level sign on channel 2	SL2SGN
	1							positive	
	0							negative	
								polarity of LOS on channel 2	LOS2POL
1								inverted	
0								normal	
0	0	0	0	1	1	0	1	default value	

Table 25 Register LIMCNF (address C2H); default value 08H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								amplifier octave selection	AMPOCT
					0	0	0	octave number 0; 1800 to 3200 Mbits/s	
					0	0	1	octave number 1; 900 to 1800 Mbits/s	
					0	1	0	octave number 2; 450 to 900 Mbits/s	
					0	1	1	octave number 3; 225 to 450 Mbits/s	
					1	X	X	octave number 4; 30 to 225 Mbits/s	
								channel selection	INSEL
				1				channel 1 selected; limiter 1 active	
				0				channel 2 selected; limiter 2 active	
								channel selection control bit	I2CINSEL
			1					via I^2C-bus interface; bit INSEL	
			0					via pin INSEL	
								single/dual limiter selection	BOTHON
		1						both limiters active	
		0						single limiter active, specified by bit INSEL	
0	0							reserved	
0	0	0	0	1	0	0	0	default value	

Note

1. X = don’t care.

Table 26 Register IOCNF3 (address C8H); default value 0CH

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								parallel output signal amplitude	MFS
				0	0	0	0	60 mV (p-p)	
				0	0	0	1	minimum; 120 mV (p-p)	
				1	1	0	0	default; 800 mV (p-p)	
				1	1	1	1	maximum; 1000 mV (p-p)	
		0	0					reserved	
								parallel output termination	MFOUTTERM
	1							LVPECL mode: floating; CML mode: AC-coupled	
	0							LVPECL mode: standard; CML mode: DC-coupled	
								parallel output mode	MFOUTMODE
1								Current Mode Logic (CML)	
0								Low Voltage Positive Emitter Coupled Logic (LVPECL)	
0	0	0	0	1	1	0	0	default value	

Table 27 Register IOCNF2 (address C9H); default value AAH

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								parallel data output polarity	PDINV
							1	inverted	
							0	normal	
								parallel data output enable	PDEN
						1		enabled	
						0		disabled	
								parallel clock output polarity	POCLKINV
					1			inverted	
					0			normal	
								parallel clock output enable	POCLKEN
				1				enabled	
				0				disabled	
								parity output polarity	PARINV
			1					inverted	
			0					normal	
								parity output enable	PAREN
		1						enabled	
		0						disabled	
								frame pulse output polarity	FPINV
	1							inverted	
	0							normal	
								frame pulse output enable	FPEN
1								enabled	
0								disabled	
1	0	1	0	1	0	1	0	default value	

Table 28 Register IOCNF1 (address CAH); default value 00H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loop mode clock input polarity	CININV
							1	inverted	
							0	normal	
								loop mode data input polarity	DININV
						1		inverted	
						0		normal	
								loop mode clock and data inputs swap	CDINSWAP
					1			clock and data input pairs swapped	
					0			normal	
								loop mode clock output polarity	COUTINV
				1				inverted	
				0				normal	
								loop mode data output polarity	DOUTINV
			1					inverted	
			0					normal	
								loop mode clock and data outputs swap	CDOUTSWAP
		1						clock and data output pairs swapped	
		0						normal	
0	0							reserved	
0	0	0	0	0	0	0	0	default value	

Table 29 Register IOCNF0 (address CBH); default value 23H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								RF serial output signal amplitude	RFS
				0	0	0	0	minimum: 20mV (p-p); 60 mV (p-p) high swing	
				0	0	1	1	default: 80mV (p-p); 250 mV (p-p) high swing	
				1	1	1	1	maximum: 300mV (p-p); 1000 mV (p-p) high swing	
								prescaler output polarity	PRSCLOINV
			1					inverted	
			0					normal	
								prescaler output enable	PRSCLOEN
		1						enabled	
		0						disabled	
								RF serial output swing	RFSWING
	1							high swing	
	0							low swing	
0								reserved	
0	0	1	0	0	0	1	1	default value	

Table 30 Register INTMASK (address CCH); default value A0H

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								mask LOS1 signal	MLOS1
							1	not masked	
							0	masked; note 1	
								mask LOS2 signal	MLOS2
						1		not masked	
						0		masked; note 1	
								mask INWINDOW signal	MINWINDOW
					1			not masked	
					0			masked; note 1	
								mask LIMSEL signal	MLIMSEL
				1				not masked	
				0				masked; note 1	
								mask high junction temperature	MTALARM
			1					not masked	
			0					masked; note 1	
		0						reserved	
								pin INT polarity mode	INTPOL
	1							inverted; active LOW output	
	0							normal; active HIGH output	
								pin INT output mode	INTOUT
1								standard CMOS output	
0								open-drain output	
0	1	0	1	0	0	0	0	default value	

Note

1. Signal is not processed by the interrupt controller.

TZA3012AHW FEATURES IN PRE-PROGRAMMED MODE

Although the TZA3012AHW is primarily intended to be programmed via the I^2C-bus (pin UI HIGH), many of the TZA3012AHW functions can be accessed via the external chip pins in pre-programmed mode (pin UI LOW) as follows:

- Choice of four pre-programmed SDH/SONET bit rates: STM1/OC3, STM4/OC12, STM16/OC48, STM16/OC48 + FEC; pins DR0 to DR2
- Choice of four pre-programmed bit rates; Fibre Channel, double Fibre Channel, Gigabit Ethernet, 10-Gigabit Ethernet; pins DR0 to DR2
- Choice of four demultiplexing ratios; 1:16, 1:10, 1:8 or 1:4 pins DMUXR1 and DMUXR0
- Input channel selection (INSEL)
- Received signal strength indicator, independently for channels 1 and 2
- Loss of signal detection threshold for each input channel individually (LOSTH1 and LOSTH2)
- Automatic disable of unused logarithmic detector (LOSTH1 and LOSTH2)
- Loop mode serial input and output configuration: pins ENLINQ and ENLOUTQ
- Automatic byte alignment for SDH/SONET or Gigabit Ethernet (ENBA)
- Frame detection for SDH/SONET (pattern is A1A1A2A2) or Gigabit Ethernet
- EVEN parity generation
- LVPECL outputs on parallel interface with 800 mV (p-p), single-ended signal, (DC-coupled termination to V_{CC} – 2 V)
- CML serial RF outputs with typical 80 mV (p-p), single-ended signal, (AC-coupled load)
- In window detection (INWINDOW)
- FWD window size select, WINDOWSIZE value ppm or 0 ppm (WINSIZE)
- High junction temperature indication (pin INT; open-drain)
- 18 to 21 MHz reference frequency supported.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}, V_{CCD}, V_{CCO}, V_{DD}	supply voltages	–0.5	+3.6	V
V_n	DC voltage on pins			
	D00 to D15, D00Q to D15Q, POCLK, POCLKQ, FP, FPQ, PARITY, PARITYQ, PRSCLO and PRSCLOQ	V_{CC} – 2.5	V_{CC} + 0.5	V
	LOSTH1, LOSTH2 and RREF	–0.5	V_{CC} + 0.5	V
	RSSI1 and RSSI2	–0.5	V_{CC} + 0.5	V
	UI, INSEL, WINSIZE, CS, SDA, SCL, DMXR0, DMXR1, ENBA, ENLOUTQ and ENLINQ	–0.5	V_{CC} + 0.5	V
	LOS1, LOS2 and INWINDOW	–0.5	V_{CC} + 0.5	V
	INT	–0.5	V_{CC} + 0.5	V
I_n	input current on pins			
	IN1, IN1Q, IN2 and IN2Q	–30	+30	mA
	CREF, CREFQ, CLOOP, CLOOPQ, DLOOP and DLOOPQ	–20	+20	mA
	INT	–2	+2	mA
T_{amb}	ambient temperature	–40	+85	°C
T_j	junction temperature	–	+125	°C
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	notes 1 and 2	16	K/W

Notes

1. In compliance with JEDEC standards JESD51-5 and JESD51-7.
2. Four-layer Printed-Circuit Board (PCB) in still air with 36 plated vias connected with the heatsink and the second and fourth layer in the PCB.

CHARACTERISTICS

V_{CC} = 3.14 to 3.47 V; T_{amb} = –40 to +85 °C; $R_{th(j-a)} \leq 16$ K/W; all characteristics are specified for the default settings (note 1); all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
I_{CCA}	analog supply current		15	20	27	mA
I_{CCD}	digital supply current	see Figs 20 and 22	270	350	450	mA
I_{CCO}	oscillator supply current		20	25	33	mA
I_{DD}	digital supply current		0	0	1	mA
$I_{CC(tot)}$	total supply current	note 2	305	395	511	mA
P_{tot}	total power dissipation	note 2	0.96	1.3	1.77	W
CMOS input: pins UI, DR0, DR1, DR2, INSEL, WINSIZE, DMXR0, DMXR1, ENBA, ENLOUTQ and ENLINQ						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{CC}$	–	–	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–200	–	–	µA
I_{IH}	HIGH-level input current	$V_{IH} = V_{CC}$	–	–	10	µA
CMOS output: pins LOS1, LOS2, INWINDOW and INT						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.5 mA	V_{CC} – 0.2	–	V_{CC}	V
Open-drain output: pin INT						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC}$	–	–	10	µA
Serial output: pins COUT, COUTQ, DOUT and DOUTQ						
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	single-ended with 50 Ω external load; ENLOUTQ = LOW; see Figs 23 and 27; note 3	50	80	110	mV
Z_o	output impedance	single-ended to V_{CC}	80	100	120	Ω
t_r	rise time	20% to 80%	–	100	–	ps
t_f	fall time	80% to 20%	–	100	–	ps

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{D-C}	data-to-clock delay	(COUT, COUTQ and DOUT, DOUTQ) between differential crossovers; see Fig.29	80	140	200	ps
δ	duty cycle COUT and COUTQ	between differential crossovers	40	50	60	%
Serial input: pins CLOOP, CLOOPQ, DLOOP and DLOOPQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_i	DC input voltage		$V_{CC} - 1$	–	$V_{CC} + 0.25$	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
t_d	clock delay	see Fig.30	260	340	400	ps
t_{su}	set-up time	see Fig.30	15	30	60	ps
t_h	hold time	see Fig.30	15	30	60	ps
δ	duty cycle signals CLOOP and CLOOPQ	between differential crossovers	40	50	60	%
CML mode parallel output: pins D00 to D15, D00Q to D15Q, FP, FPQ, PARITY, PARITYQ, POCLK, POCLKQ, PRSCLO and PRSCLOQ						
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	single-ended with 50 Ω external load to V_{CC}; AC-coupled; see Fig.27 or DC-coupled; see Fig.28; note 4	650	800	1000	mV
Z_o	output impedance	single-ended to V_{CC}	70	95	110	Ω
t_r	rise time	20% to 80%	200	250	350	ps
t_f	fall time	80% to 20%	200	250	350	ps
f_{PBR}	parallel bit rate		–	–	400	Mbits/s
LVPECL mode parallel output: pins D00 to D15, D00Q to D15Q, FP, FPQ, PARITY, PARITYQ, POCLK, POCLKQ, PRSCLO and PRSCLOQ						
V_{OH}	HIGH-level output voltage	50 Ω termination to $V_{CC} - 2V$; see Fig.24	$V_{CC} - 1.2$	$V_{CC} - 1.0$	$V_{CC} - 0.9$	V
V_{OL}	LOW-level output voltage	50 Ω termination to $V_{CC} - 2V$; see Fig.24	$V_{CC} - 2.0$	$V_{CC} - 1.9$	$V_{CC} - 1.7$	V
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	LVPECL floating; Fig.21; single-ended with 50 Ω external load to V_{CC}; AC-coupled; see Fig.26 or DC-coupled; see Fig.25; note 4	700	900	1150	mV
t_r	rise time	20% to 80%	300	350	400	ps
t_f	fall time	80% to 20%	300	350	400	ps
f_{par}	parallel bit rate		–	–	400	Mbits/s

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Parallel timing output: pins D00 to D15, D00Q to D15Q, FP, FPQ, PARITY, PARITYQ, POCLK, POCLKQ, PRSCLO and PRSCLOQ						
t_{D-C}	data-to-clock delay D00 to D15/POCLK	DMX 1:16, 1:10, 1:8; see Fig.31; note 5	–100	100	250	ps
t_{D-C}	data-to-clock delay D06 to D09/POCLK	DMX 1:4; see Fig.31; note 5	150	180	250	ps
δ	duty cycle POCLK		40	50	60	%
skew	channel to channel skew D00 and Dn (between channels)	DMX 1:16, 1:10, 1:8; note 5	–	–	200	ps
skew	channel to channel skew D06 and D09 (between channels)	DMX 1:4; note 5	–	–	50	ps
Reference: pin RREF						
V_{ref}	reference voltage	10 to 20 kΩ resistor to V_{EE}	1.17	1.21	1.26	V
I²C-bus pins SCL and SDA						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{CC}$	–	–	V
V_{hys}	hysteresis of Schmitt trigger inputs		$0.05V_{CC}$	–	–	V
V_{OL}	SDA LOW-level output voltage (open-drain)	I_{OL} = 3 mA	0	–	0.4	V
I_L	leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
I²C-bus timing						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{LOW}	SCL LOW time		1.3	–	–	µs
$t_{HD;STA}$	hold time START condition		0.6	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{SU;STA}$	set-up time START condition		0.6	–	–	µs
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	µs
t_r	SCL and SDA rise time		20	–	300	ns
t_f	SCL and SDA fall time		20	–	300	ns
t_{BUF}	bus free time between STOP and START		1.3	–	–	µs
C_b	capacitive load on each bus line		–	–	400	pF
t_{SP}	pulse width of allowable spikes		0	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{nL}	noise margin at LOW-level		$0.1V_{CC}$	–	–	V
V_{nH}	noise margin at HIGH-level		$0.2V_{CC}$	–	–	V
RF input: pins IN1, INQ1, IN2 and IN2Q						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended; note 6	12	–	500	mV
V_{sl}	typical slice level range	note 7	–50	–	+50	mV
Z_i	input impedance	differential	80	100	120	Ω
α_{iso}	between channel isolation		–	60	–	dB
Received Signal Strength Indicator (RSSI)						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended	5	–	500	mV
S_{RSSI}	RSSI sensitivity	see Fig.4	15	17	20	mV/dB
V_{RSSI}	output voltage	$V_{i(p-p)}$ = 32 mV (p-p); PRBS (2^{31}–1)	580	680	780	mV
$\Delta V_{o(RSSI)}$	output voltage variation	input 30 to 3200 Mbits/s; PRBS (2^{31}–1); V_{CC} = 3.14 to 3.47 V; ΔT = 120 °C	–50	–	+50	mV
Output: pins RSSI1 and RSSI2						
Z_o	output impedance		–	1	10	Ω
$I_{O(source)}$	output source current		–	–	1	mA
$I_{O(sink)}$	output sink current		–	–	0.4	mA
LOS detector						
hys	hysteresis	note 8	–	3	–	dB
t_a	assert time	$\Delta V_{i(p-p)}$ = 3 dB	–	–	5	µs
t_d	de-assert time	$\Delta V_{i(p-p)}$ = 3 dB	–	–	5	µs
Reference frequency input: pins CREF and CREFQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_i	DC input voltage		V_{CC} – 1	–	V_{CC} + 0.25	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
Δf_{CREF}	reference clock frequency accuracy	SDH/SONET requirement	–20	–	+20	ppm
f_{CREF}	reference clock frequency	see Table 7; R = 1, 2, 4 or 8	18 × R	19.44 × R	21 × R	MHz
PLL characteristics						
t_{acq}	acquisition time	30 Mbits/s	–	–	200	µs
$t_{acq(pc)}$	acquisition time at power cycle	30 Mbits/s	–	–	10	ms
$t_{acq(o)}$	acquisition time octave change	30 Mbits/s	–	–	10	µs
TDR	transitionless data run	30 Mbits/s	–	1000	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Jitter tolerance						
$J_{tol(p-p)}$	jitter tolerance (peak-to-peak value)	STM1/OC3 mode (ITU-T G.958); PRBS (2^{31}–1); note 9				
		f = 6.5 kHz	3	10	–	UI
		f = 65 kHz	0.3	1	–	UI
		f = 1 MHz	0.3	0.5	–	UI
		STM4/OC12 mode (ITU-T G.958); PRBS (2^{31}–1); note 10				
		f = 25 kHz	3	10	–	UI
		f = 250 kHz	0.3	1	–	UI
		f = 5 MHz	0.3	0.5	–	UI
		STM16/OC48 mode (ITU-T G.958); PRBS (2^{31}–1); note 11				
		f = 100 kHz	3	10	–	UI
		f = 1 MHz	0.3	1	–	UI
		f = 20 MHz	0.3	0.5	–	UI

Notes

1. Default settings: UI = LOW (pre-programmed mode; see Table 1); DR0 = LOW, DR1 = HIGH, DR2 = LOW (STM16/OC48); INSEL = HIGH (limiter 1 active); WINSIZE = HIGH (1000 ppm); ENBA = HIGH (automatic byte alignment); ENLOUTQ = HIGH (DOUT, COUT disabled); ENLINQ = HIGH (DLOOP, CLOOP disabled); DMXR0 = HIGH, DMXR1 = HIGH (DMX ratio 1:16); CREF and CREFQ = 19.44 MHz; LOSTH2 not connected (LOS2 switched off); D00 to D15 and D00Q to D15Q, FP, FPQ, PARITY, PARITYQ, POCLK, POCLKQ, PRSCLO and PRSCLOQ not connected.
2. The total supply current and power dissipation is dependent on the IC setups such as swing and loop modes and termination conditions.
3. The output swing is adjustable in 16 steps controlled by bits RFS in I^2C-bus register CBH.
4. The output swing is adjustable in 16 steps controlled by bits MFS in I^2C-bus register IOCNF3 (address C8H). In standard LVPECL mode only swing = 12 (default) should be used.
5. With 50% duty cycle.
6. The RF input is protected against a differential overvoltage; the maximum input current is 30 mA. It is assumed that both inputs carry a complementary signal of the specified peak-to-peak value.
7. The slice level is adjustable in 256 steps controlled by I^2C-bus registers LIMSLICE1 (address C0H) and LIMSLICE2 (address C1H).
8. The hysteresis is adjustable in 8 steps controlled by bits HYS1 and HYS2 in I^2C-bus registers LIMLOS1CNF (address BDH) and LIMLOS2CNF (address BFH).
9. The $J_{tol(p-p)}$ min. value is 0.25UI for T_{amb} = –40 °C to 0 °C at f = 65 kHz and 1 MHz.
10. The $J_{tol(p-p)}$ min. value is 0.25UI for T_{amb} = –40 °C to 0 °C at f = 250 kHz and 5 MHz.
11. The $J_{tol(p-p)}$ min. value is 0.25UI for T_{amb} = –40 °C to 0 °C at f = 1 MHz and 20 MHz.

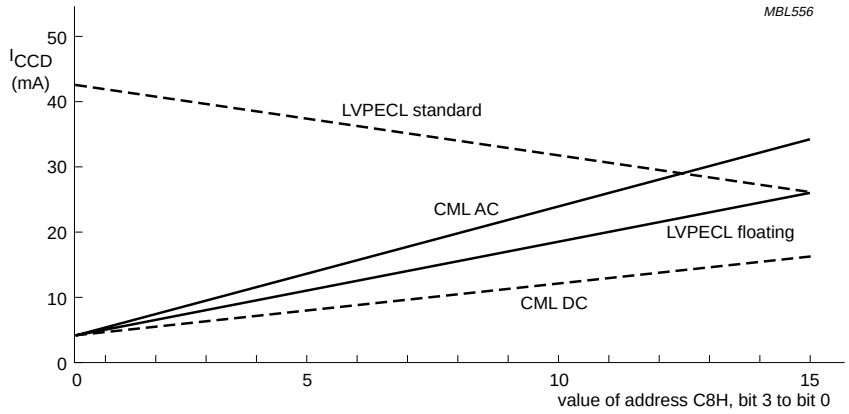


Fig.20 Supply current per parallel output.

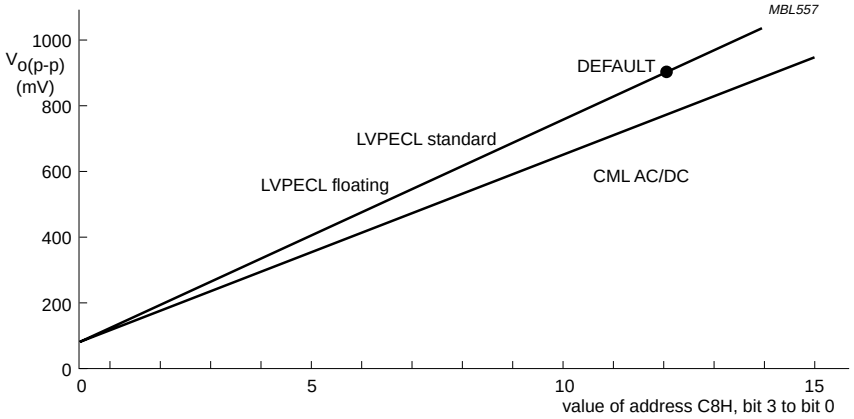
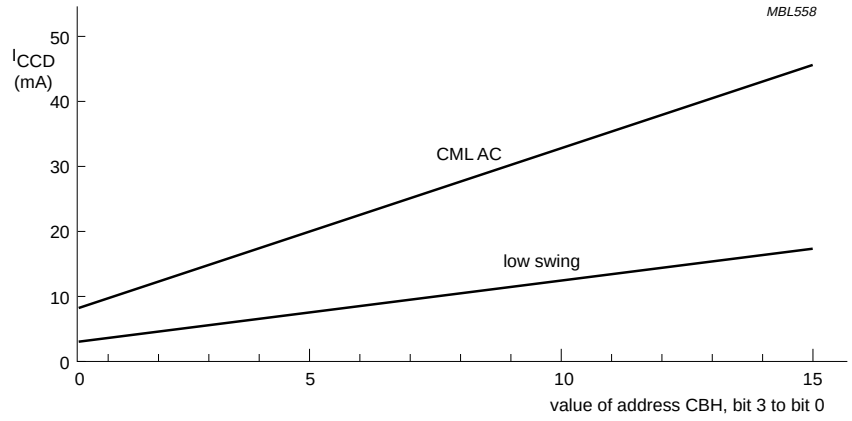


Fig.21 Output voltage swing of parallel output.



Serial outputs are off (default).

Fig.22 Supply current per serial output.

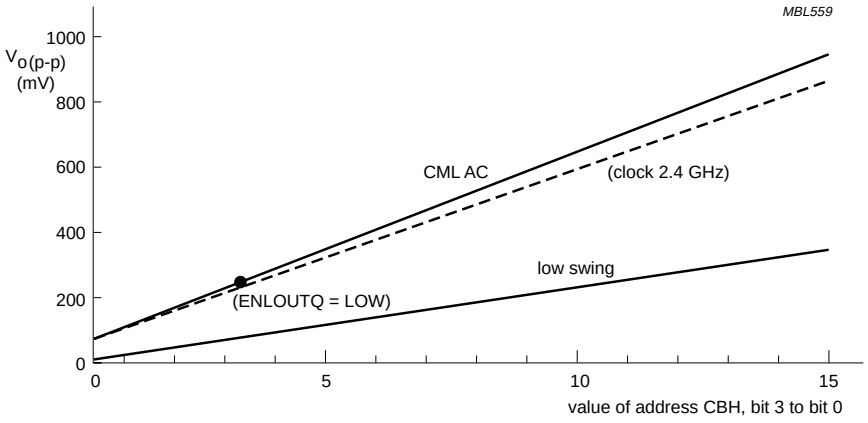


Fig.23 Output voltage swing of serial output.

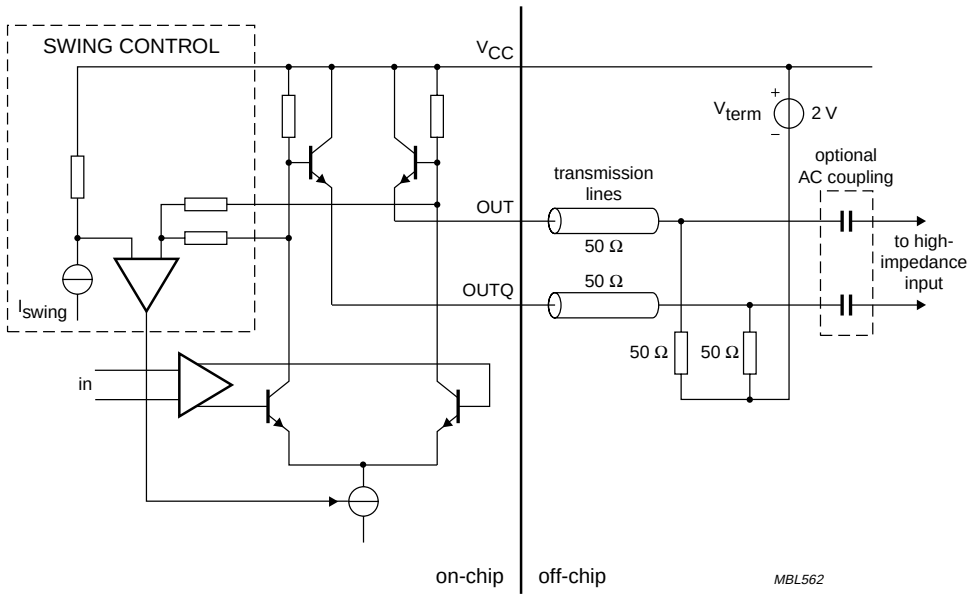


Fig.24 Standard PECL mode.

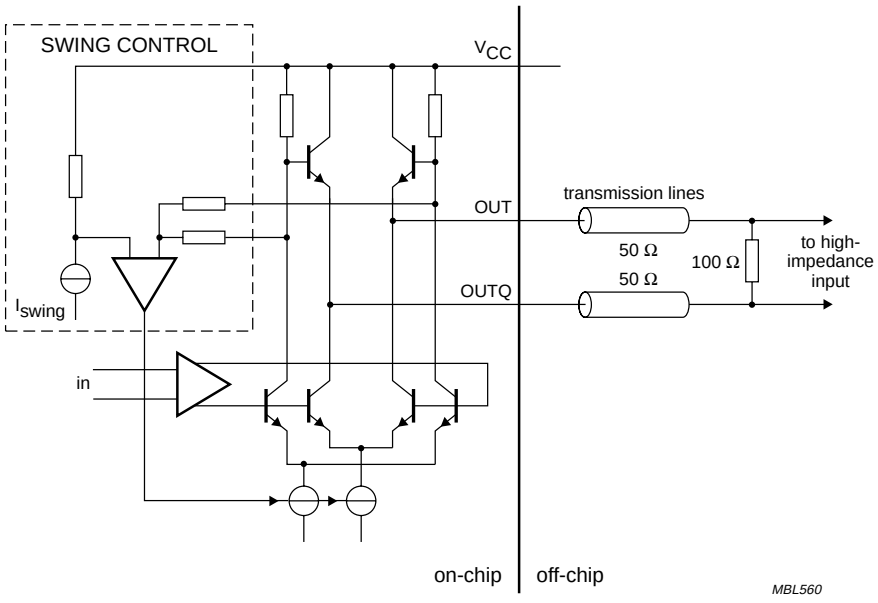


Fig.25 Floating PECL mode (DC-coupled).

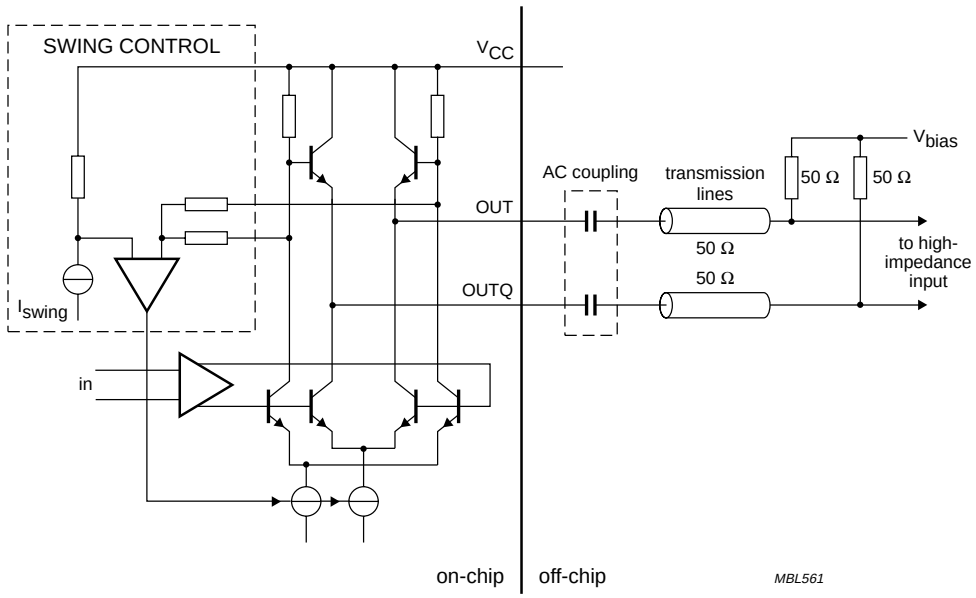


Fig.26 Floating LVPECL mode (AC-coupled).

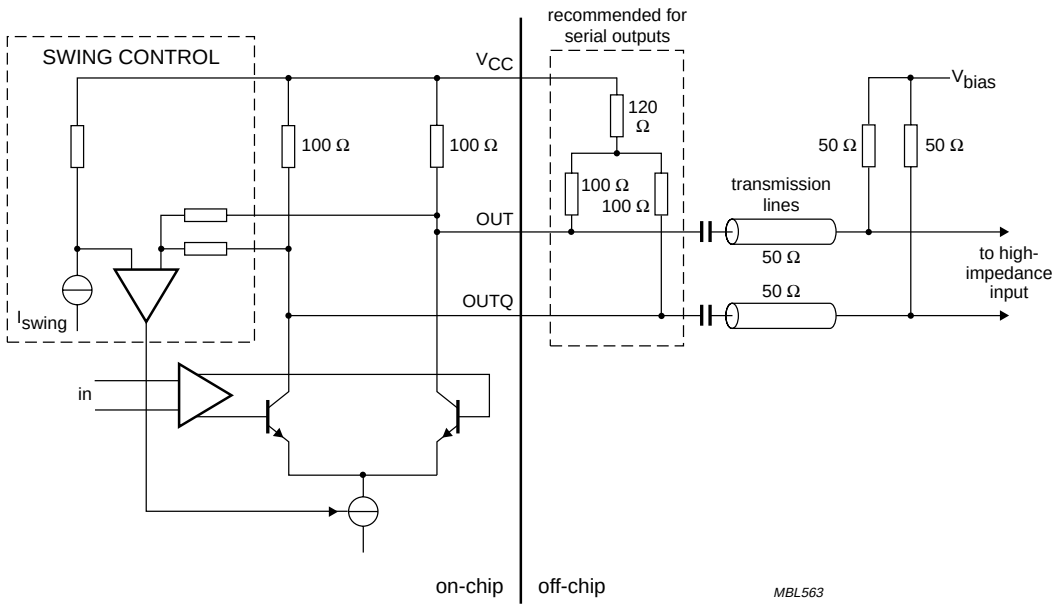


Fig.27 CML mode (AC-coupled).

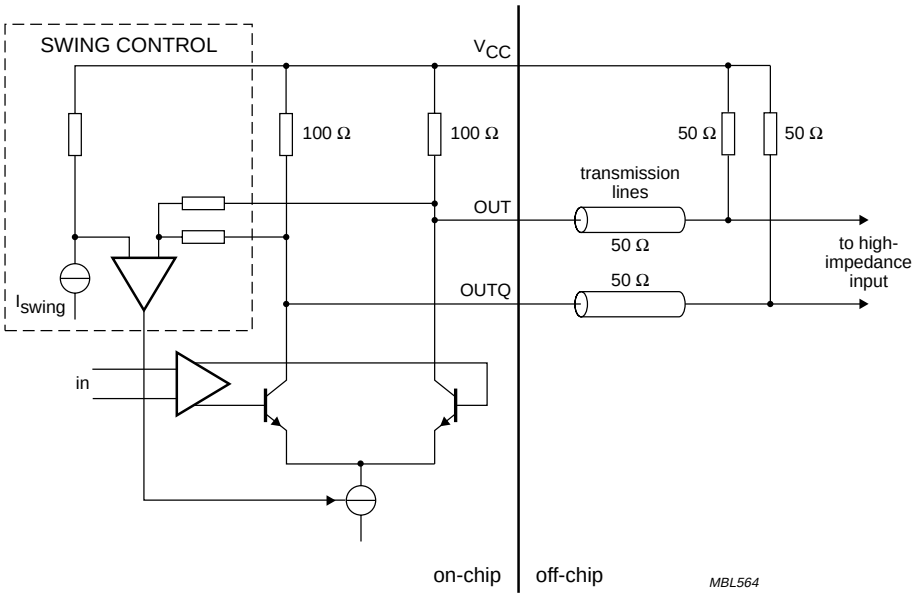
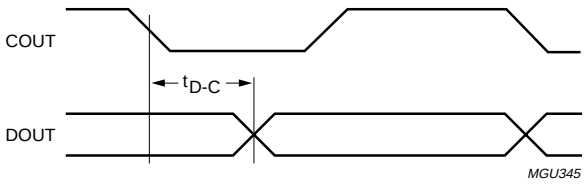
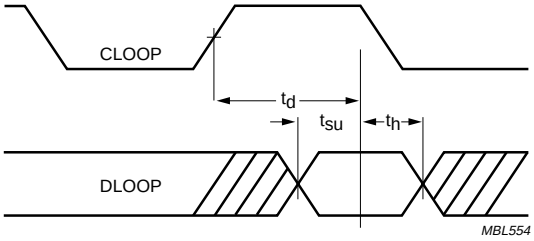


Fig.28 CML mode (DC-coupled).



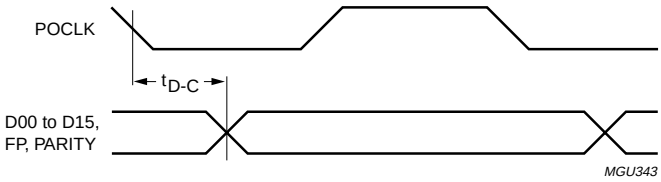
The timing is measured from the crossover point of the clock output signal to the crossover point of the data output (all signals are differential).

Fig.29 Loop mode output timing.



The timing is measured from the crossover point of the clock input signal to the crossover point of the data input.

Fig.30 Loop mode input timing.

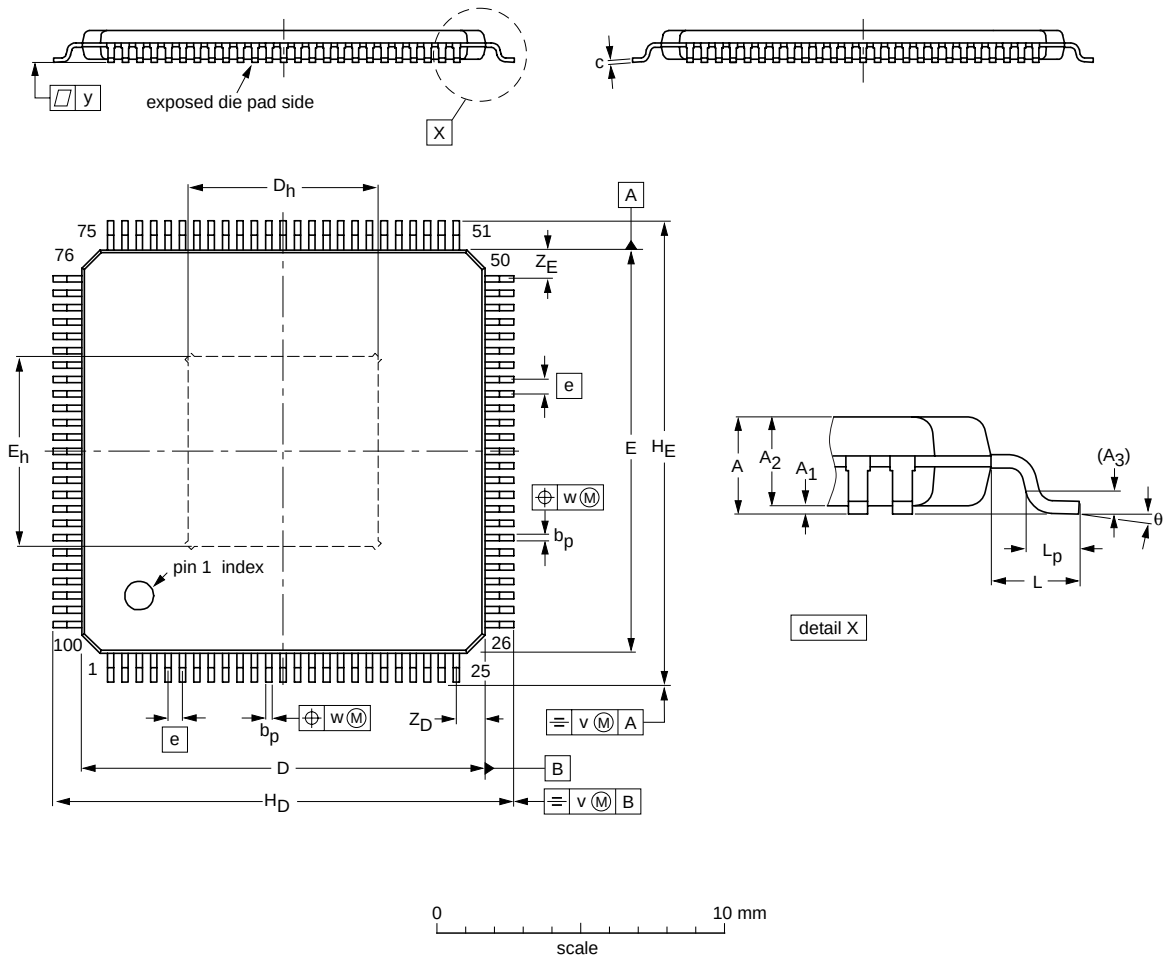


The timing is measured from the crossover point of the clock output signal to the crossover point of the data output (all signals are differential).

Fig.31 Parallel bus output timing.

PACKAGE OUTLINE

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed die pad **SOT638-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-1						~~01-03-30~~ 03-04-07

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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