SC4215
Very Low Input /Very Low Dropout 2 Amp Regulator With Enable

POWER MANAGEMENT

Description

The SC4215 is a high performance positive voltage regulator designed for use in applications requiring very low Input voltage and very low dropout voltage at up to 2 amperes. It operates with a Vin as low as 1.6V, with output voltage programmable as low as 0.8V. The SC4215 features ultra low dropout, ideal for applications where Vout is very close to Vin. Additionally, the SC4215 has an enable pin to further reduce power dissipation while shut down. The SC4215 provides excellent regulation over variations in line, load and temperature.

The SC4215 is available in the SOIC-8-EDP (Exposed Die Pad) package. The output voltage can be set via an external divider or to fixed settings of 0.8V and 2.5V depending on how the ADJ pin is configured.

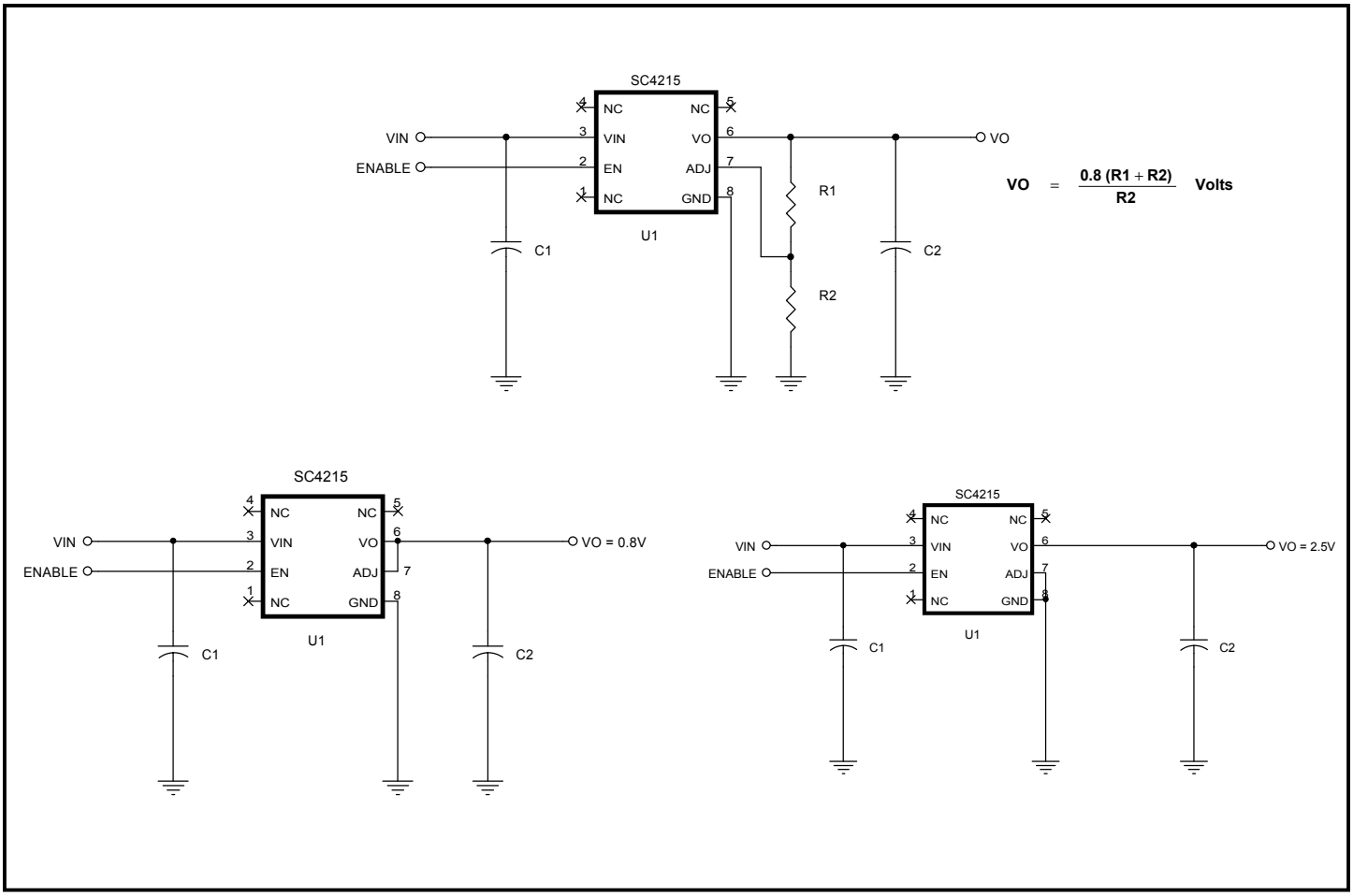
Features

- Input Voltage as low as 1.6V
- 500mV dropout @ 2A
- Adjustable output from 0.8V
- Over current and over temperature protection
- Enable pin
- 10µA quiescent current in shutdown
- Full industrial temperature range
- Available in SOIC-8-EDP Lead- free package, fully WEEE and RoHS compliant

Applications

- Telecom/Networking cards
- Motherboards/Peripheral cards
- Industrial Applications
- Wireless infrastructure
- Set top boxes
- Medical equipment
- Notebook computers
- Battery powered systems

Typical Application Circuits



$$VO = \frac{0.8\,(R1 + R2)}{R2} \text{ Volts}$$

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Max	Units
Vin, EN, Vo, ADJ to GND		7	V
Power Dissipation	P_D	Internally Limited	W
Thermal Resistance Junction to Ambient (1)	θ_{JA}	36	°C/W
Thermal Resistance Junction to Case (1)	θ_{JC}	5.5	°C/W
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Peak IR Reflow Temperature (10s to 30s)	T_P	260	°C
ESD Rating (Human Body Model) (2)	V_{ESD}	2	kV

Notes:
(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards,
(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless specified: $V_{EN} = V_{IN}$. V_{IN} = 1.6V to 5.5V, I_O = 10µA to 2A.
Values in **bold** apply over the full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VIN						
Supply Voltage Range	V_{IN}		**1.6**		**5.5**	V
Quiescent Current	I_Q	V_{IN} = 3.3V		0.75	**1.75**	mA
		V_{IN} = 5.5V, V_{EN} = 0V		10	**50**	µA
VO						
Output Voltage(1)	V_O	$V_{IN} = V_O$ + 0.5V, I_O = 10mA	-2%	V_O	+2%	V
(Fixed Voltage, V_{ADJ} = 0)		1.60V ≤ V_{IN} ≤ 5.5V, I_O = 10mA	**-3%**		**+3%**	
Line Regulation(1)	$REG_{(LINE)}$	I_O = 10mA		0.2	**0.4**	%/V
Load Regulation(1)	$REG_{(LOAD)}$	I_O = 10mA to 2A		0.5	**1.0**	%
Dropout Voltage(1)(2)	V_{DO}	I_O = 1A		90	300	mV
					400	
		I_O = 1.5A		200	400	mV
					500	

Electrical Characteristics (Cont.)

Unless specified: $V_{EN} = V_{IN}$. V_{IN} = 1.6V to 5.5V, I_O = 10µA to 2A.
Values in **bold** apply over the full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VO (Cont.)						
Dropout Voltage[1][2]	V_{DO}	I_O = 2A, $V_{IN} = V_O$ + 0.5V		300	500	mV
		I_O = 2A, $V_{IN} = V_O$ + 0.6V			**600**	
Minimum Load Current[3]	I_O	$V_{IN} = V_O$ + 0.5V		1	**10**	µA
Current Limit	I_{CL}		**2.2**	3	**4.5**	A
ADJ						
Reference Voltage[1]	V_{REF}	V_{IN} = 3.3V, $V_{ADJ} = V_{OUT}$, I_O = 10mA	0.792	0.8	0.808	V
			0.784		**0.816**	
Adjust Pin Current[4]	I_{ADJ}	$V_{ADJ} = V_{REF}$		80	**200**	nA
Adjust Pin Threshold[5]	$V_{TH(ADJ)}$		**0.05**	0.16	**0.40**	V
EN						
Enable Pin Current	I_{EN}	V_{EN} = 0V, V_{IN} = 3.3V		1.5	**10**	µA
Enable Pin Threshold	V_{IH}	V_{IN} = 3.3V	**1.6**			V
	V_{IL}	V_{IN} = 3.3V			**0.4**	
Over Temperature Protection						
High Trip level	T_{HI}			160		°C
Hysteresis	T_{HYST}			10		°C

Notes:
(1) Low duty cycle pulse testing with Kelvin connections required.
(2) $V_{DO} = V_{IN} - V_O$ when V_O decreases by 1.5% of its nominal output voltage with $V_{IN} = V_O$ +0.8V
(3) Required to maintain regulation. Voltage set resistors R1 and R2 are usually utilized to meet this requirement. Adjustable versions only.
(4) Guaranteed by design.
(5) When V_{ADJ} exceeds this threshold, the “Sense Select” switch disconnects the internal feedback chain from the error amplifier and connects V_{ADJ} instead.

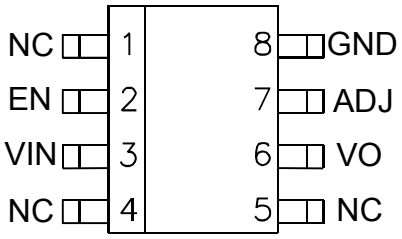
Ordering Information

Part Number	Package	Temp. Range (T_J)
SC4215ISTR(1)	SOIC-8-EDP-2	-40 to +125°C
SC4215ISTRT(1)(2)		
SC4215EVB	Evaluation Board	

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead-free product. This product is fully WEEE and RoHS compliant.

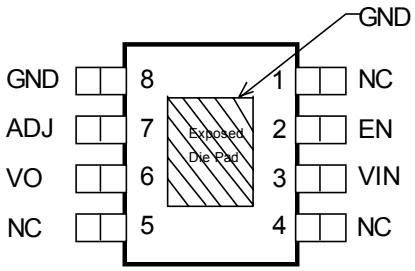
Pin Configuration

Top View



SOIC-8-EDP-2

Bottom View

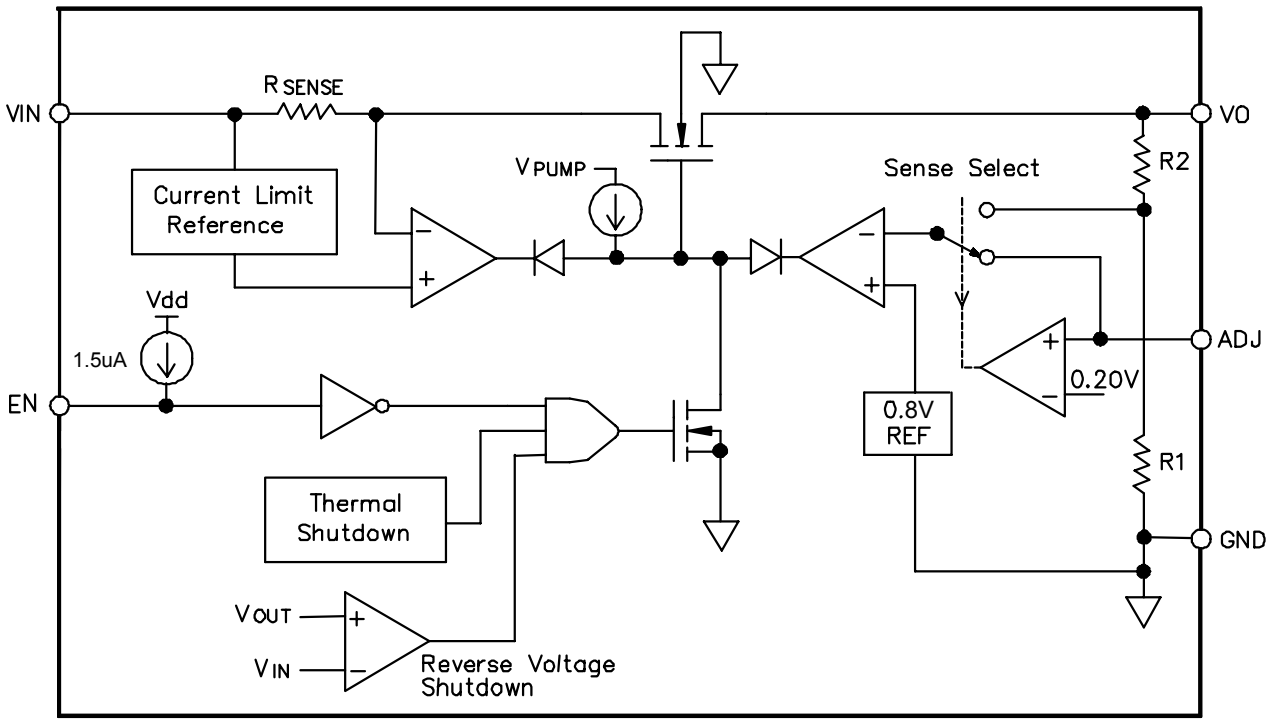


SOIC-8-EDP-2

Pin Descriptions

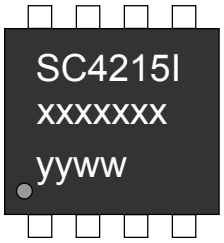
Pin #	Pin Name	Pin Desciption
2	EN	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open. Connect to VIN if not being used.
3	VIN	Input voltage. For regulation at full load, the input to this pin must be between (VO+ 0.5V) and 5.5V. Minimum VIN = 1.6V. A large bulk capacitance should be placed closely to this pin to ensure that the input supply does not sag below 1.6V. Also a minimum of 4.7uF ceramic capacitor should be placed directly at this pin.
6	VO	The pin is the power output of the device. A minimum of 10uF capacitor should be placed directly at this pin.
7	ADJ	When this pin is grounded, an internal resistor divider sets the output voltage to 2.5V. If connected to the Vo pin, the output voltage will be set at 0.8V. If external feedback resistors are used, the output voltage will be (See Application Circuits on page 1): $VO = \frac{0.8\ (R1 + R2)}{R2}$ Volts
8	GND	Reference ground. The GND pin and the exposed die pad must be connected together at the IC pin.
1,4,5	NC	No Connection.
	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not electrically connected internally.

Block Diagram



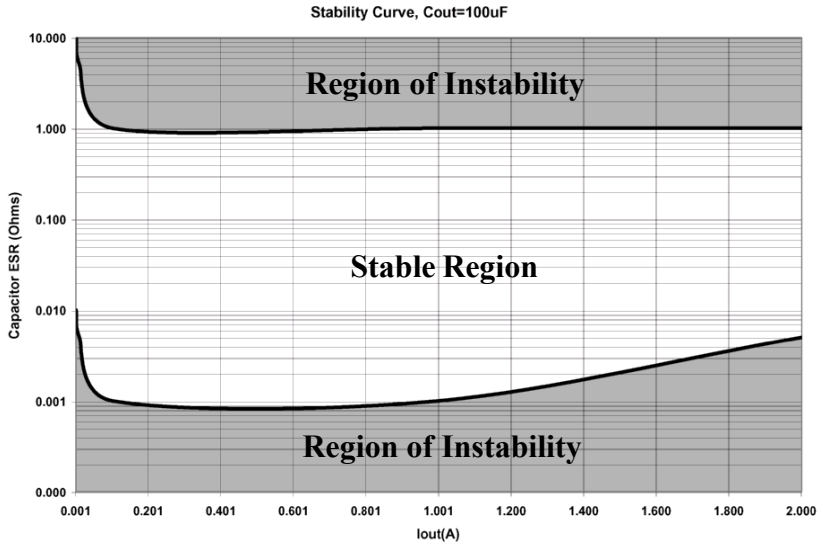
Marking Information

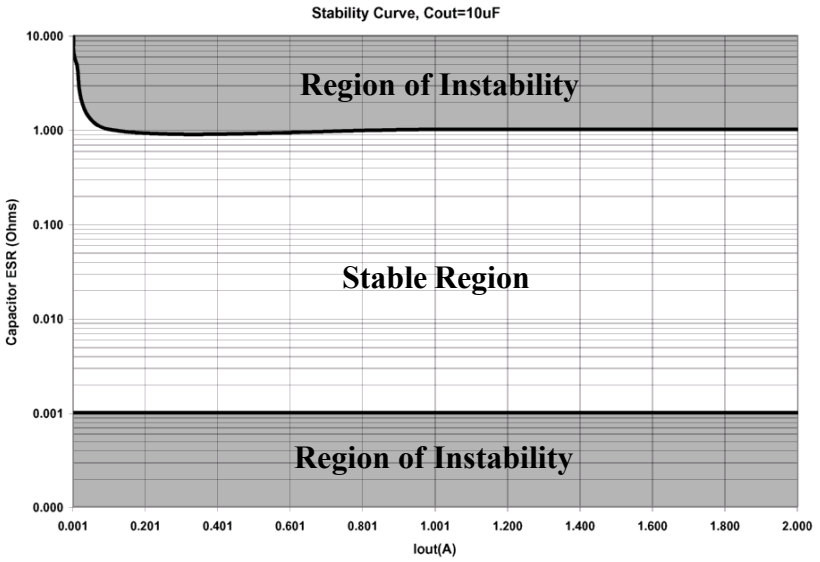
Top View



yyww = Datecode (Example: 0015)
xxxxxxx = Semtech Lot No. (Example: 00101)

Typical Characteristics





Applications Information

Introduction

The SC4215 is intended for applications where high current capability and very low dropout voltage are required. It provides a very simple, low cost solution that uses very little pcb real estate. Additional features include an enable pin to allow for a very low power consumption standby mode, and a fully adjustable output.

Component Selection

Input capacitor: A minimum of 4.7µF ceramic capacitor is recommended to be placed directly next to the Vin pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, bulk capacitance of about ≥ 10µF/A (output load) may be added closely to the input supply pin of the SC4215 to ensure that Vin does not sag, improving load transient response.

Output capacitor: A minimum bulk capacitance of ≥ 10µF/A (output load), along with a 0.1µF ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the SC4215 is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

Noise immunity: In very electrically noisy environments, it is recommended that 0.1µF ceramic capacitors be placed from IN to GND and OUT to GND as close to the device pins as possible.

Internal voltage selection: By connecting the ADJ pin to GND, an internal resistor divider will regulate the output voltage to 2.5V. If the ADJ pin is connected directly to the VO pin, the output voltage will be regulated to the 0.8V internal reference.

External voltage selection resistors: The use of 1% resistors, and designing for a current flow ≥ 10µA is recommended to ensure a well regulated output (thus R2 ≤ 50kΩ).

Enable: Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. A pull up resistor up to 400kOhms should be connected from this pin to the VIN pin in application where supply voltages of Vin < 1.9V are required. For applications with higher voltages than 1.9V, EN pin could be left open or connected to VIN.

Thermal Considerations

The power dissipation in the SC4215 is approximately equal to the product of the output current and the input to output voltage differential:

$$P_D \approx (VIN - VOUT) \bullet I_O$$

The absolute worst-case dissipation is given by:

$$P_{D(MAX)} = (VIN_{(MAX)} - VOUT_{(MIN)}) \bullet I_{O(MAX)} + VIN_{(MAX)} \bullet I_{Q(MAX)}$$

For a typical scenario, V_{IN} = 3.3V ± 5%, V_{OUT} = 2.8V and I_O = 1.5A, therefore:

$V_{IN(MAX)}$ = 3.465V, $V_{OUT(MIN)}$ = 2.744V and $I_{Q(MAX)}$ = 1.75mA,

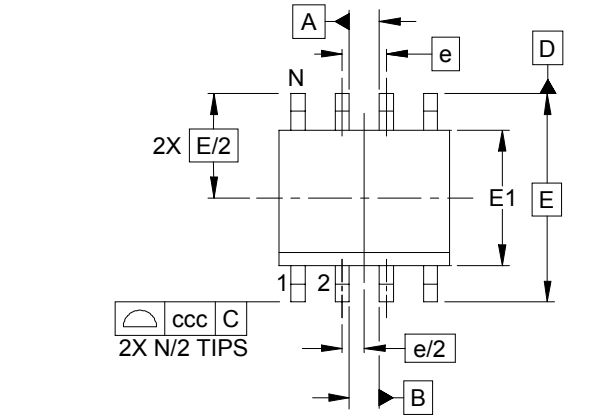
Thus $P_{D(MAX)}$ = 1.09W.

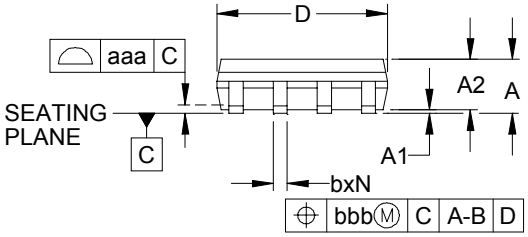
Using this figure, and assuming $T_{A(MAX)}$ = 70°C, we can calculate the maximum thermal impedance allowable to maintain $T_J \leq 150°C$:

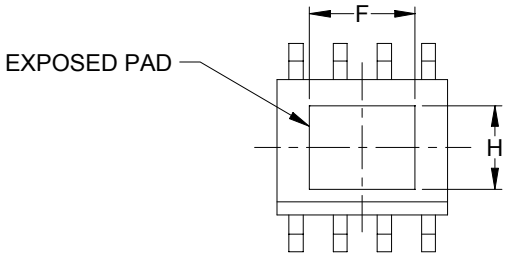
$$R_{TH(J-A)(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{P_{D(MAX)}} = \frac{(150 - 70)}{1.09} = 73.4°C / W$$

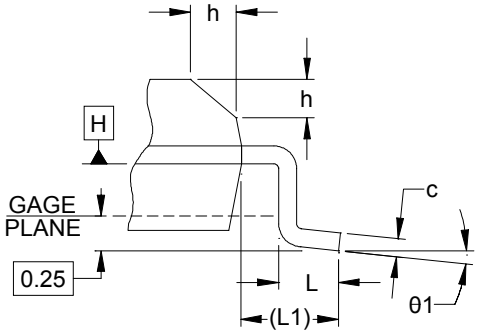
This should be achievable for the SOIC-8EDP package using pcb copper area to aid in conducting the heat away, such as one square inch of copper connected to the exposed die pad of the device. Internal ground/power planes and air flow will also assist in removing heat. For higher ambient temperatures it may be necessary to use additional copper area.

Outline Drawing - SOIC-8-EDP-2

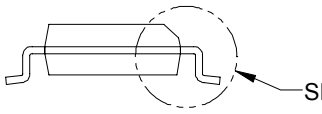








DETAIL A



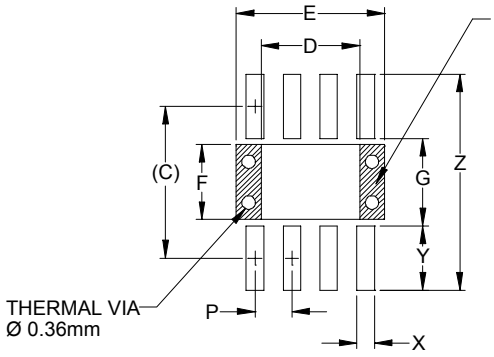
SIDE VIEW

DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.000	-	.005	0.00	-	0.13
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.116	.120	.130	2.95	3.05	3.30
H	.085	.095	.099	2.15	2.41	2.51
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.05)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION BA.

Land Pattern - SOIC-8-EDP-2



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
D	.134	3.40
E	.201	5.10
F	.101	2.56
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804