

NCP5252

2.0 A, 1.0 MHz Integrated Synchronous Buck Regulator with Light Load Efficiency

NCP5252 is a synchronous buck regulator with integrated high-side and low-side MOSFETs. The device is capable of operating from a 5 V or 12 V supply and can output a voltage down to 0.6 V. The switching frequency is adjustable from 333 kHz up to 1.0 MHz and has the ability to provide skip mode for light load efficiency. NCP5252 protection features include Under Voltage Lock Out (UVLO), Over Voltage Protection (OVP), Cycle-by-Cycle Current Protection (OCP) and Thermal Shutdown. The parts are packaged in a 3x3mm QFN-16.

Features

- 1% Accuracy 0.6 V Reference
- V_{CC} Voltage 4.5 V to 13.2 V
- Adjustable Output Voltage Range: 0.6 V to 5.0 V V_{out}
- Transient Response Enhancement (TRE) Feature.
- Lossless Low Side Sense Current Control
- Input Voltage Feed Forward Control
- Internal Digital Soft-Start
- Integrated Output Discharge (Soft-Stop)
- Cycle-by-Cycle Current Limit
- PGOOD Indication
- Overvoltage and Undervoltage Protection
- Thermal Shutdown Protection
- Power Saving Mode at Light Load
- Integrated Boost Diode
- QFN-16 (3 mm x 3 mm)
- These Devices are Pb-Free and are RoHS Compliant

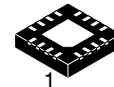
Typical Applications

- Desktop Application
- System Power
- XDSL, Modems, DC-DC Modules
- Set Top Box
- HD Driver
- LED Driver, DVD Recorders



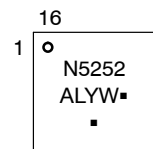
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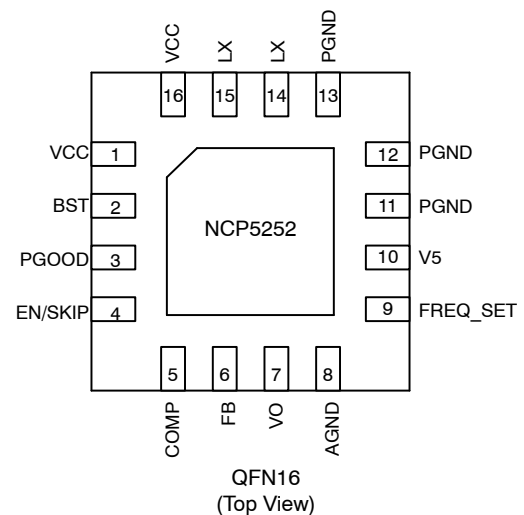
QFN16
CASE 485G

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)



ORDERING INFORMATION

Device	Package	Shipping†
NCP5252MNTXG	QFN16 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP5252

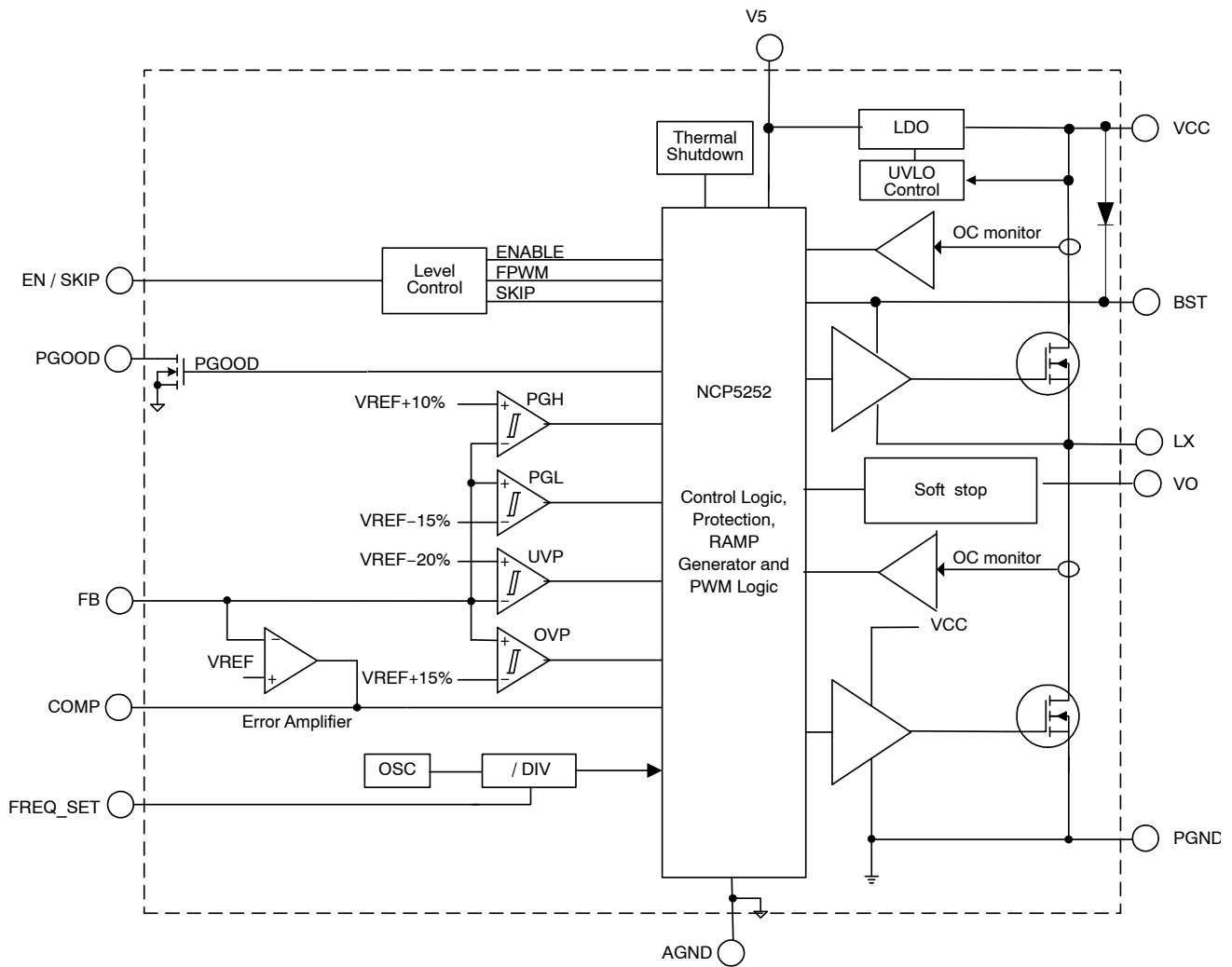


Figure 1. NCP5252 Typical Block Diagram

NCP5252

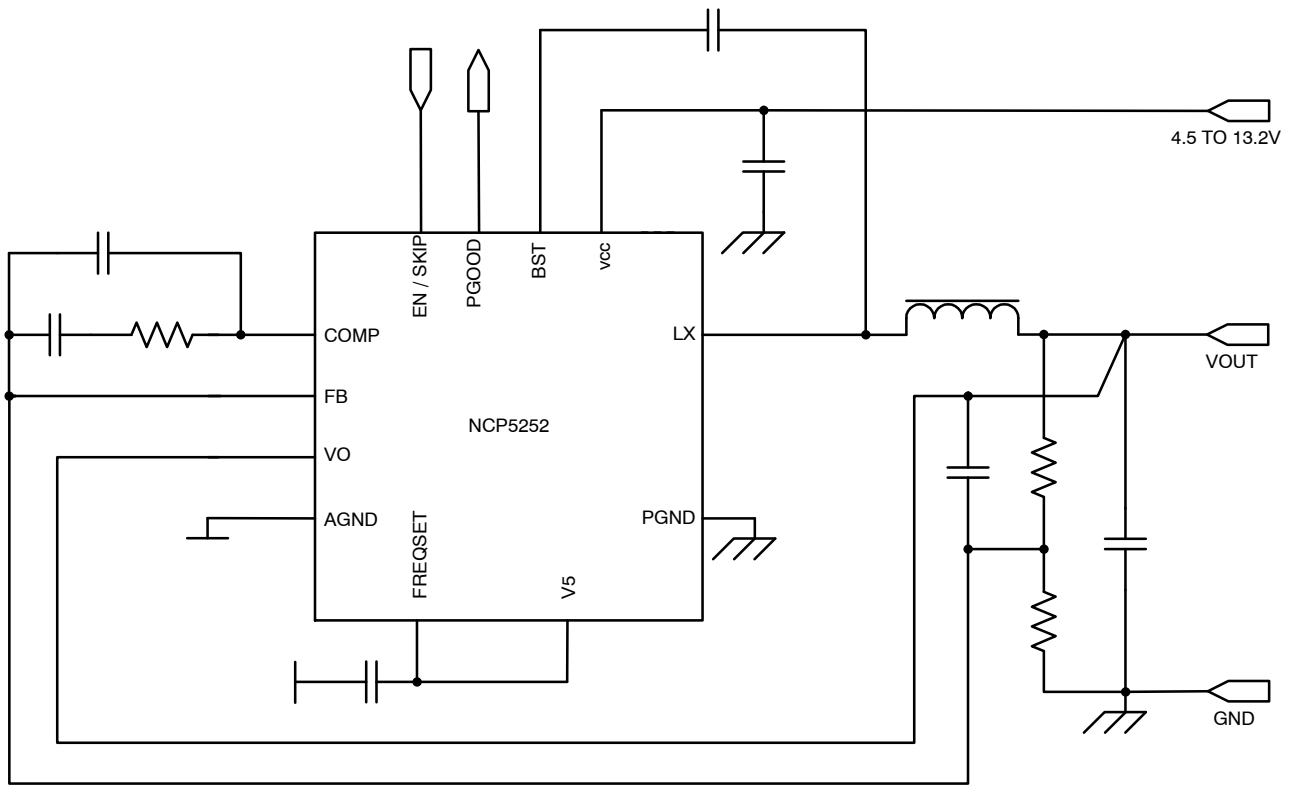


Figure 2. NCP5252 Typical Application Circuits

PIN FUNCTION DESCRIPTION

Pin No	Symbol	Description
1	V _{CC}	Internal LDO power supply
2	BST	Top MOSFET driver input supply, a bootstrap capacitor connection between LX and this pin.
3	PGOOD	Power good indicator of the output voltage. High impedance (open drain) if power good (in regulation). Low impedance if power not good.
4	EN/SKIP	This pin serves as two functions. Enable: Logic control for enabling the switcher. SKIP: Power saving mode (Skip and Force PWM) programmable pin.
5	COMP	Output of the error amplifier.
6	FB	Output voltage feed back.
7	VO	Output voltage.
8	AGND	Analog ground.
9	FREQ_SET	Frequency selection pin, 0 V = 333k, No connect = 500 kHz, 5 V = 1.0 MHz
10	V5	Power supply for analog circuit.
11–13	PGND	Ground reference and high-current return path for the bottom power MOSFET.
14–15	LX	Switch node between the top MOSFET and bottom MOSFET.
16	V _{CC}	Internal Main FET power supply
17	EPAD	Connect to PGND for thermal enhancement. Exposed pad is not electrically connected.

NCP5252

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V _{CC} Power Supply Voltage to AGND	V _{CC}	-0.3, 15	V
EN / SKIP to AGND	V _{EN}	-0.3, 15	V
Bootstrap Supply Voltage: BST to LX	V _{BST} - V _{LX}	-0.3, 15	V
LDO regulator: V5 to AGND	V5 - V _{AGND}	-0.3, 6	V
Input / Output Pins to AGND	V _{IO}	-0.3, 6	V
Switch Node to PGND	V _{LX}	15 -1 (DC) -5 (200 ns)	V
PGND	V _{PGND}	-0.3, 0.3	V
Thermal Resistance Junction-to-Ambient (0 lfpm)	R _{θJA}	90	°C/W
Thermal Resistance Junction-to-Case (0 lfpm)	R _{θJC}	15	°C/W
Operating Ambient Temperature Range	T _A	-40 to + 85	°C
Operating Junction Temperature Range	T _J	-40 to + 150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1.4	W
Moisture Sensitivity Level	MSL	1	-

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

V_{CC} UNDERVOLTAGE

Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CC} UVLO Rise Threshold		4.1	4.3	4.5	V
V _{CC} UVLO Hysteresis		300	400	500	mV

NCP5252

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.5$ to 13.2 V, $T_A = -40^\circ\text{C}$ to 85°C , unless other noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
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SUPPLY VOLTAGE

Input Voltage	V_{CC}		4.5		13.2	V
POR Threshold for Internal Reset Logic	V_{CC_POR}			3.0	3.7	V

SUPPLY CURRENT

V_{CC} Quiescent Supply Current	I_{CC_FPWM}	EN/SKIP = 5 V, $V_{FB} = 1$ V (No switching), $V_{CC} = 4.5$ V to 13.2 V		1.0	2.5	mA
V_{CC} Shutdown Current	I_{VCC_SD}	EN/SKIP = 0 V			10	μA
BST Quiescent Supply Current	I_{BST_FPWM}	EN/SKIP = H, $V_{FB} = 1$ V, $V_{BST} = 5$ V			0.3	mA
BST Shut Down Current	I_{BST_SD}	EN/SKIP = L, $V_{FB} = 1$ V, $V_{BST} = 5$ V			10	μA
V_{CC} Input Current	I_{VCC}	FREQ_SET = AGND. FREQ = 333 kHz		18		mA

LDO REGULATOR

V5 Regulator Voltage	V5	$V_{CC} > 6$ V, $I_{V5} = 5$ mA	4.85	5.0	5.15	V
V5 Rise Threshold	$V5_th+$	Wake Up	4.1	4.3	4.45	V
V5 UVLO Hysteresis	$V5_{HYS}$		300	400	500	mV
V5 Loading	$V5_{LOAD}$				3.0	mA
V5 Current Limit	I_{LIMIT_V5}		20			mA
Drop-out Voltage ($V_{CC} - V5$)	V_{DR}	$I_o = 5$ mA, $T_A = 25^\circ\text{C}$, $V_{CC} = 4.5$ V, $FB = 1$ V			200	mV

POWER GOOD

Power Good High Threshold	VPGH	PGOOD in from higher V_o (PGOOD goes high)	100	110	120	%
Power Good High Hysteresis	VPGH_HYS	PGOOD high hysteresis (PGOOD goes low)		5		%
Power Good Low Threshold	VPGL	PGOOD in from lower V_o (PGOOD goes high)	75	85	95	%
Power Good Low Hysteresis	VPGL_HYS	PGOOD low hysteresis (PGOOD goes low)		-5		%
Power Good High Delay	T_d_PGH			150		μs
Power Good Low Delay	T_d_PGL			1.5		μs
Output Overvoltage Rising Threshold	OVPth+	$OVPth+ = VPGH + VPGH_SYS$	105	115	125	%
Over voltage Fault Propagation Delay	OVPTblk	FB Forced 2% above trip threshold		1.5		μs
Output Undervoltage Trip Threshold	UVPth	$UVPth = VPGL + VPGL_HYS$	70	80	90	%
Output Undervoltage Protection Blanking Time	UVPTblk			8.0		μs

REFERENCE OUTPUT

Internal Reference Voltage	V_{REF}	25°C -40°C to 85°C	0.594 0.591	0.6 0.6	0.606 0.609	V
Output Voltage Accuracy (Note 1)		$V_{IN} = 12$ V, $I_o = 0$ A to 2 A	-1	0	+1	%
Line Regulation (Note 1)		$V_{IN} = 5$ to 12 V, $I_{OUT} = 500$ mA		0.1		%/V

OSCILLATOR

Operation Frequency	F_{SW}	FREQ_SET = V5	900	1000	1100	kHz
		FREQ_SET = NC	450	500	550	kHz
		FREQ_SET = AGND	300	333	366	kHz

INTERNAL SOFT-START

Soft-Start Time	t_{SS}	Digital Soft-Start (V_{OUT} from 10% to 90%)		800		μs
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1. Guaranteed by design, not tested in production.
2. Test mode disables the T_{on}/T_{off} min.

NCP5252

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.5$ to 13.2 V, $T_A = -40^{\circ}\text{C}$ to 85°C , unless other noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
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SWITCHING MODULATOR

Minimum T_{on}	T_{on_min}	(Note 1)	40	50	60	ns
Minimum T_{off}	T_{off_min}	(Note 1)	200	225	250	ns
PWM Comparator Offset		(Note 1)		5.0	10	mV
Propagation Delay of PWM Comparator	TD_PWM	(Note 1)			20	ns

VOLTAGE ERROR AMPLIFIER

DC Gain	GAIN_VEA	(Note 1)	80	88		dB
Open-Loop Phase Margin	PH_EA	(Note 1)	50			Deg
Unity Gain Bandwidth	BW_VEA	(Note 1)	15	20		MHz
Slew Rate	SR_VEA	COMP PIN TO GND = 100 pF (Note 1)	5.0			V/ μ s
FB Bias Current	I_{bias_FB}				0.1	μ A
Output Voltage Swing	V_{max_EA}	$I_{source_EA} = 2\text{mA}$	3.3	3.5		V
	V_{min_EA}	$I_{sink_EA} = 2\text{mA}$		0.15	0.3	V

OVERCURRENT PROTECTION LIMIT

High Side Peak Current Limit (Cycle-by-Cycle)	HSOC	T_{on} Minimum > 100 ns (Notes 1 & 2)	3.4	4.0	4.6	A
Low Side Valley Current Limit, Short-Circuit (4 μ s)	LSOC_S	(Notes 1 & 2)	3.0	3.75	4.5	A
Low Side Valley Current Limit (Current Limit, 16 μ s)	LSOC_L	(Notes 1 & 2)	2.0	2.5	3.4	A

POWER OUTPUT SECTION

Internal Main FET ON-Resistance	$R_{DS(on)_M}$	($I_{LX} = 100\text{mA}$, $V_{BST-LX} = 5\text{V}$, $FB = 0$, $T_A = 25^{\circ}\text{C}$) (Note 1)		150	225	$\text{m}\Omega$
Internal Sync FET ON-Resistance	$R_{DS(on)_F}$	($I_{LX} = 100\text{mA}$, $FB = 1\text{V}$, $T_A = 25^{\circ}\text{C}$) (Note 1)		100	150	$\text{m}\Omega$
LX Leakage Current	LX_LK	$V_{EN} = 0\text{V}$, $LX = 0$, $V_{CC} = 13.2\text{V}$			+5.0	μ A
		$LX = 13.2$, $V_{CC} = 13.2\text{V}$			-5.0	μ A

CONTROL SECTION

EN / SKIP Logic Input Voltage for Disable	$V_{EN_DISABLE}$	Set as Disable	0.7	1.0	1.3	V
	V_{EN_HYS}	Hysteresis		300		mV
EN / SKIP Logic Input Voltage for FPWM	V_{EN_FPWM}	Set as FCCM mode	1.7	1.95	2.10	V
EN / SKIP Logic Input Voltage for Skip Mode	V_{EN_SKIP}	Set as SKIP Mode	2.25	2.45	2.65	V
	V_{EN_HYS}	Hysteresis		250		mV
EN / SKIP Source Current	I_{EN_SOURCE}	$V_{EN_SKIP} = 0\text{V}$			0.1	μ A
EN / SKIP Sink Current	I_{EN_SINK}	$V_{EN_SKIP} = 5\text{V}$			0.1	μ A
EN_SKIP Logic Input Delay		Change mode delay active		3		Clk
PGOOD Pin ON Resistance	PGOOD_R	$I_{PGOOD} = 5\text{mA}$		75		Ω
PGOOD Pin OFF Current	PGOOD_LK	PGOOD = 5 V			1	μ A

OUTPUT DISCHARGE MODE

Output Discharge On-Resistance	$R_{discharge}$	EN = 0 V		20	35	Ω
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THERMAL SHUTDOWN

Thermal Shutdown	T_{sd}	(Note 1)		150		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	T_{sdhys}	(Note 1)		25		$^{\circ}\text{C}$

1. Guaranteed by design, not tested in production.
2. Test mode disables the T_{on}/T_{off} min.

TYPICAL OPERATING CHARACTERISTICS

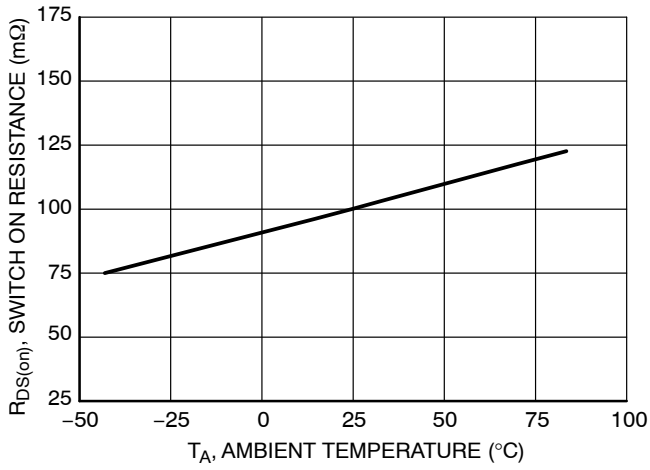


Figure 3. Sync FET ON Resistance vs. Temperature

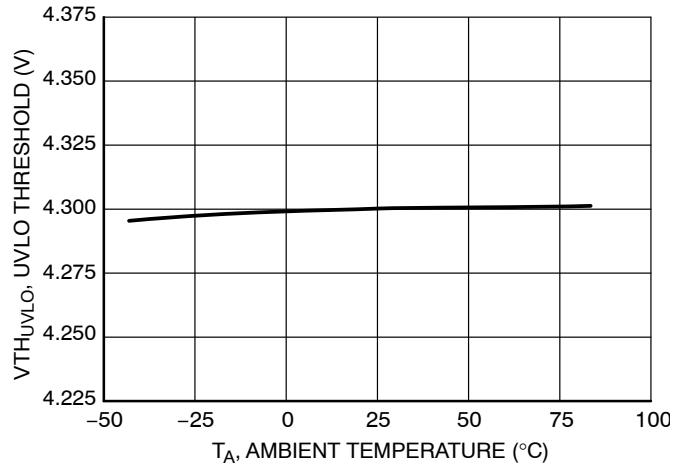


Figure 4. UVLO Threshold vs. Temperature

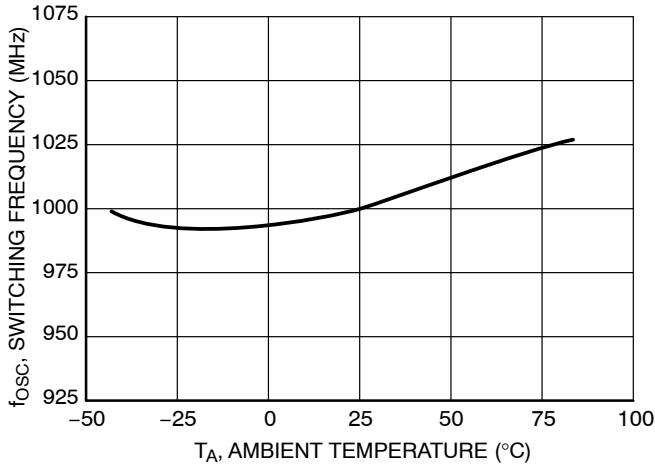


Figure 5. Switching Frequency vs. Temperature

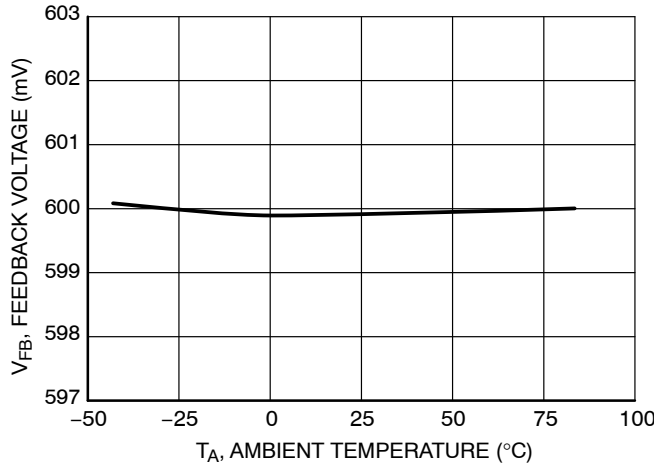


Figure 6. Feedback Input Threshold vs. Temperature

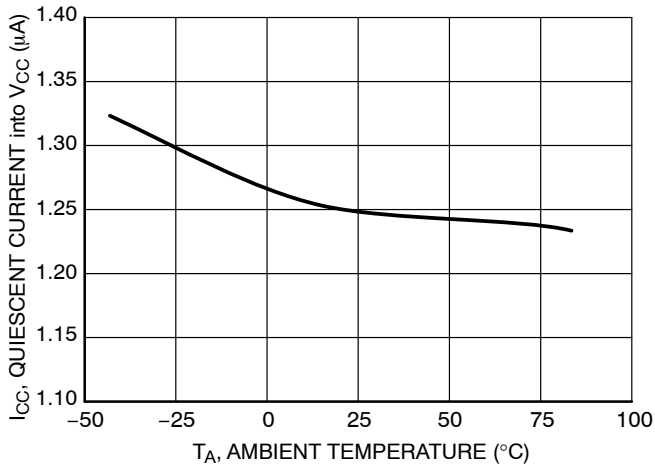


Figure 7. Quiescent Current into V_{CC} vs. Temperature

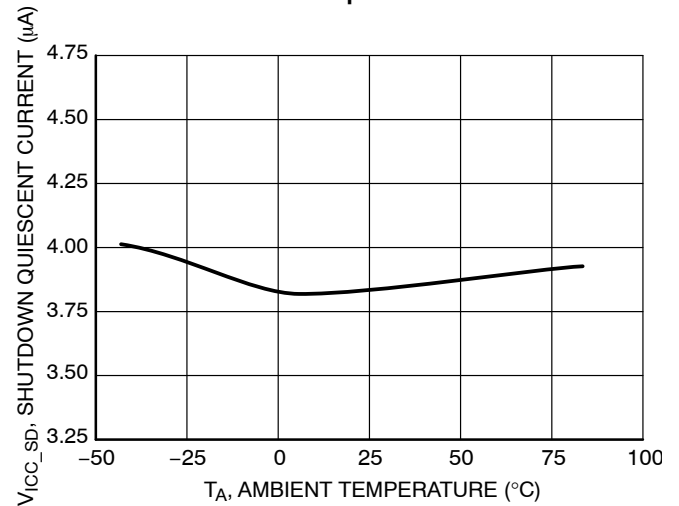


Figure 8. Shutdown Quiescent Current vs. Temperature

TYPICAL OPERATING CHARACTERISTICS

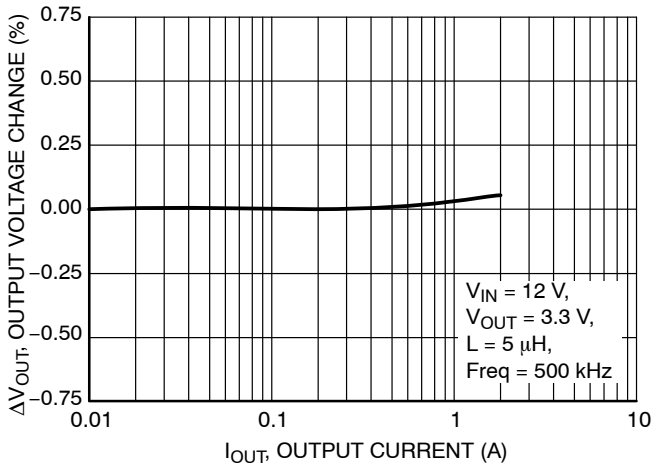


Figure 9. Output Voltage Change vs. Output Current

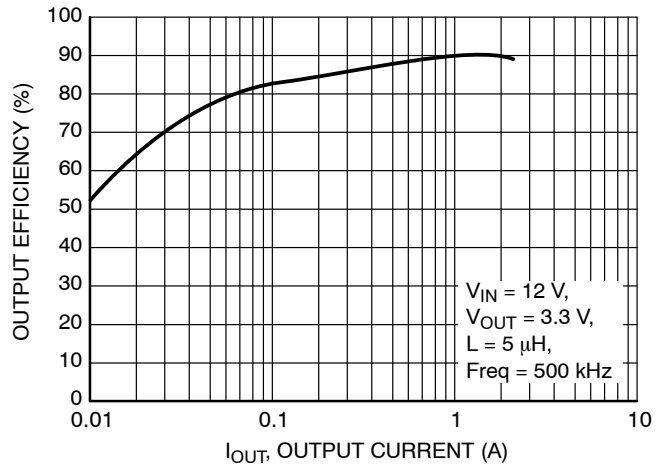


Figure 10. Efficiency vs. Output Current

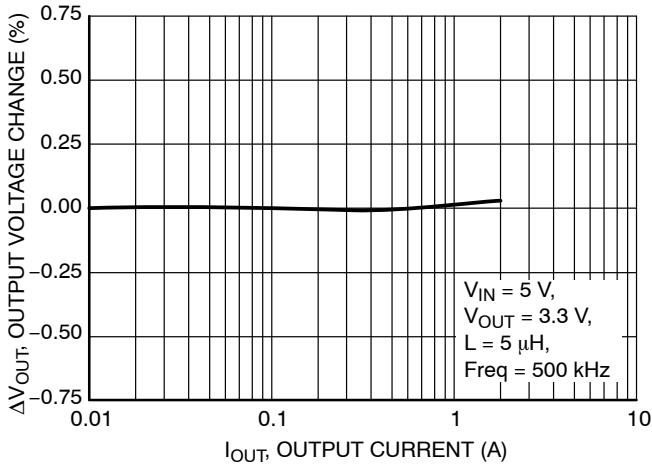


Figure 11. Output Voltage Change vs. Output Current

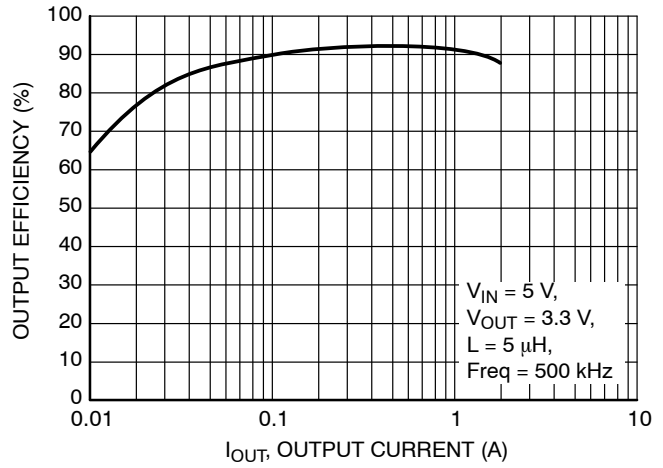


Figure 12. Efficiency vs. Output Current

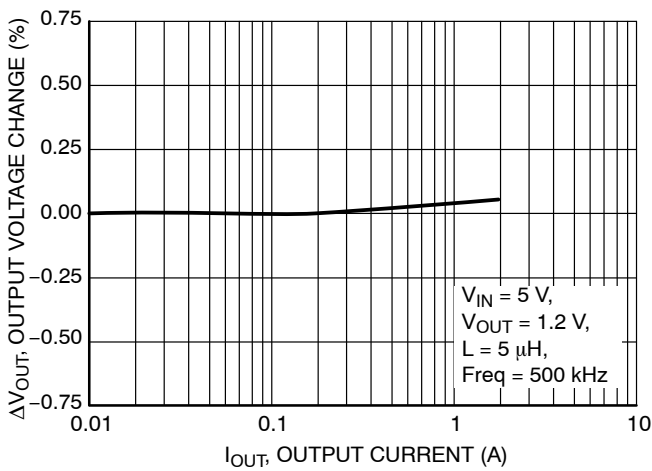


Figure 13. Output Voltage Change vs. Output Current

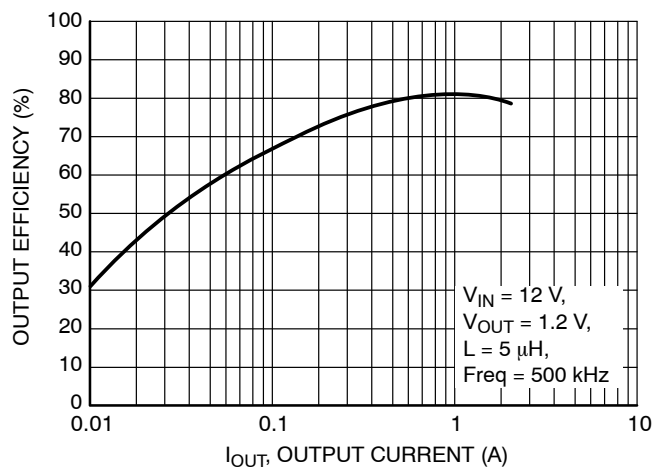
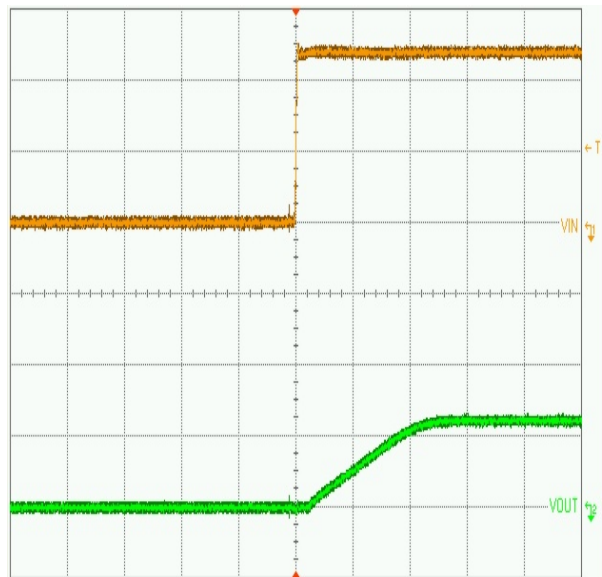


Figure 14. Efficiency vs. Output Current



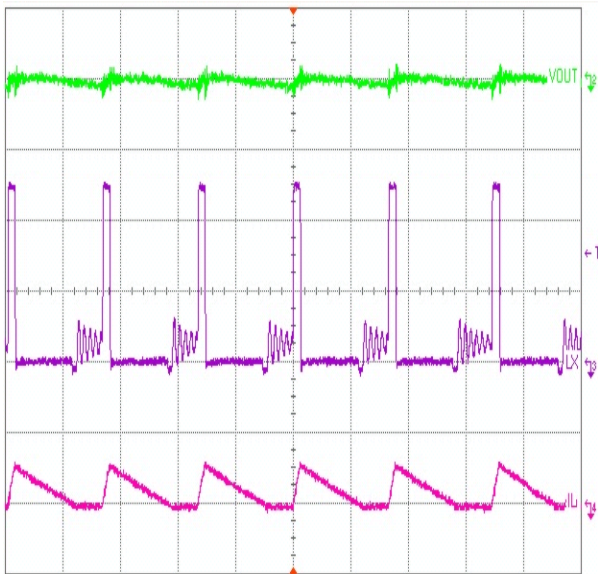
($V_{in} = 12\text{ V}$, $I_{LOAD} = 10\text{ mA}$,
 $L = 5\text{ }\mu\text{H}$, $C_{OUT} = 100\text{ }\mu\text{F}$)
 Upper trace: Input voltage, 5 V/div
 Lower trace: Output voltage, 1 V/div
 Time base: 500 $\mu\text{s}/\text{div}$

Figure 15. Soft-Start Waveforms for $V_{out} = 3.3\text{ V}$



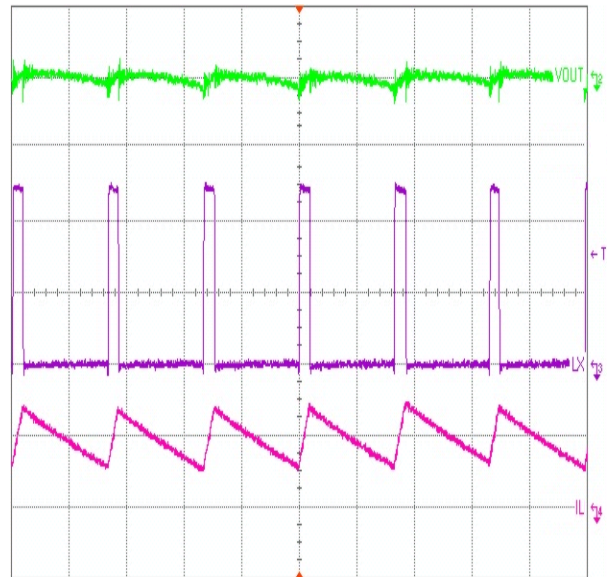
($V_{in} = 12\text{ V}$, $I_{LOAD} = 10\text{ mA}$,
 $L = 5\text{ }\mu\text{H}$, $C_{OUT} = 100\text{ }\mu\text{F}$)
 Upper trace: Input voltage, 5 V/div
 Lower trace: Output voltage, 1 V/div
 Time base: 500 $\mu\text{s}/\text{div}$

Figure 16. Soft-Start Waveforms for $V_{out} = 1.2\text{ V}$



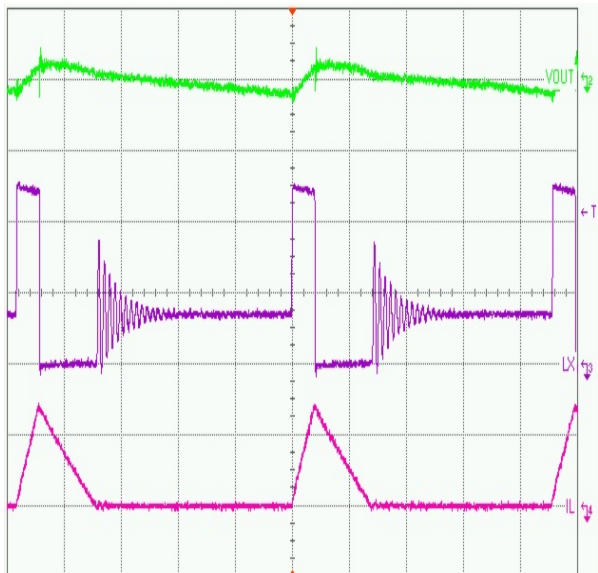
($V_{in} = 12\text{ V}$, $I_{LOAD} = 200\text{ mA}$, $L = 5\text{ }\mu\text{H}$, $C_{OUT} = 100\text{ }\mu\text{F}$)
 Upper trace: Output ripple voltage, 50 mV/div
 Middle trace: Lx pin switching waveform, 5 V/div
 Lower trace: Inductor current waveforms, 1 A/div
 Time base: 2 $\mu\text{s}/\text{div}$

Figure 17. DCM Switching Waveforms for $V_{out} = 1.2\text{ V}$



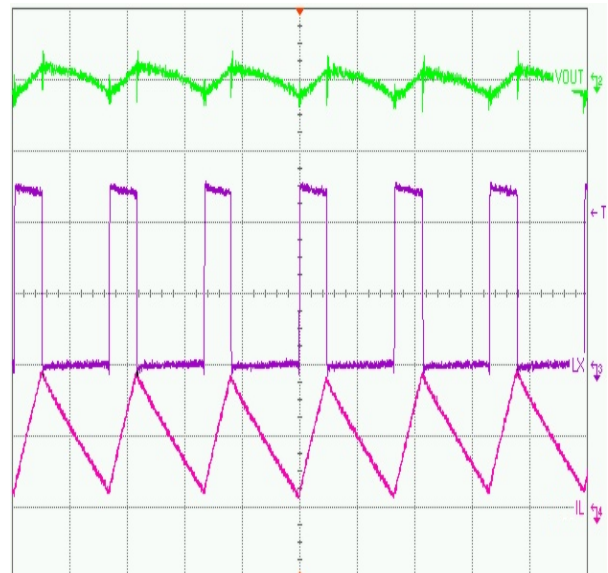
($V_{in} = 12\text{ V}$, $I_{LOAD} = 1\text{ A}$, $L = 5\text{ }\mu\text{H}$, $C_{OUT} = 100\text{ }\mu\text{F}$)
 Upper trace: Output ripple voltage, 50 mV/div
 Middle trace: Lx pin switching waveform, 5 V/div
 Lower trace: Inductor current waveforms, 1 A/div
 Time base: 2 $\mu\text{s}/\text{div}$

Figure 18. CCM Switching Waveforms for $V_{out} = 1.2\text{ V}$



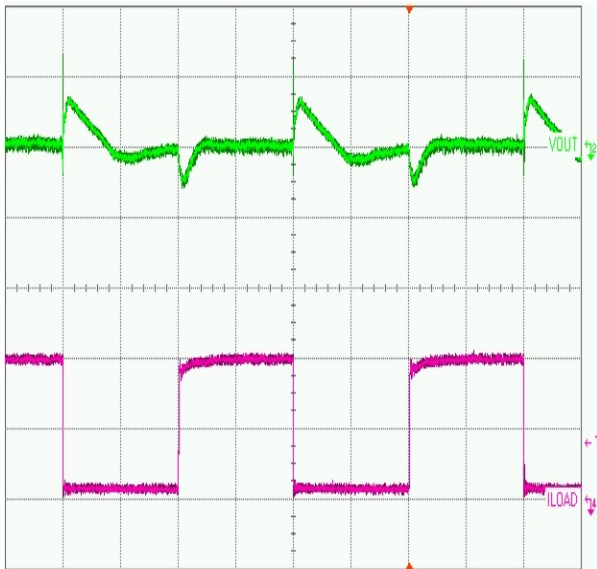
($V_{in} = 12\text{ V}$, $I_{LOAD} = 200\text{ mA}$, $L = 5\text{ }\mu\text{H}$, $C_{OUT} = 100\text{ }\mu\text{F}$)
 Upper trace: Output ripple voltage, 50 mV/div
 Middle trace: Lx pin switching waveform, 5 V/div
 Lower trace: Inductor current waveforms, 500 mA/div
 Time base: 2 $\mu\text{s}/\text{div}$

Figure 19. DCM Switching Waveforms for $V_{out} = 3.3\text{ V}$



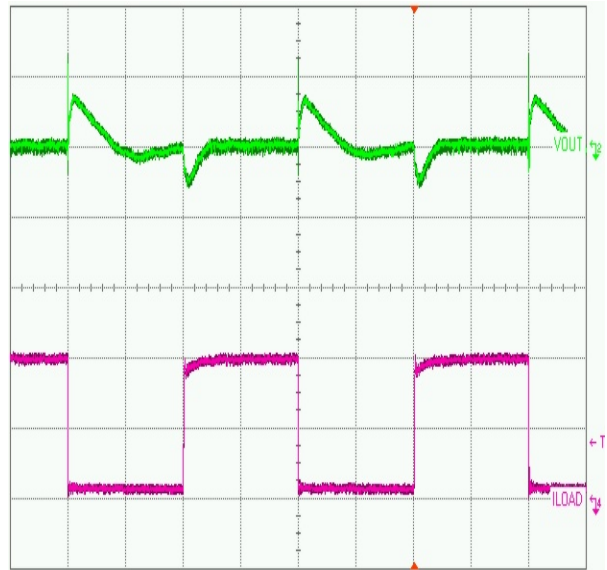
($V_{in} = 12\text{ V}$, $I_{LOAD} = 500\text{ mA}$, $L = 5\text{ }\mu\text{H}$, $C_{OUT} = 100\text{ }\mu\text{F}$)
 Upper trace: Output ripple voltage, 50 mV/div
 Middle trace: Lx pin switching waveform, 5 V/div
 Lower trace: Inductor current waveforms, 500 mA/div
 Time base: 2 $\mu\text{s}/\text{div}$

Figure 20. CCM Switching Waveforms for $V_{out} = 3.3\text{ V}$



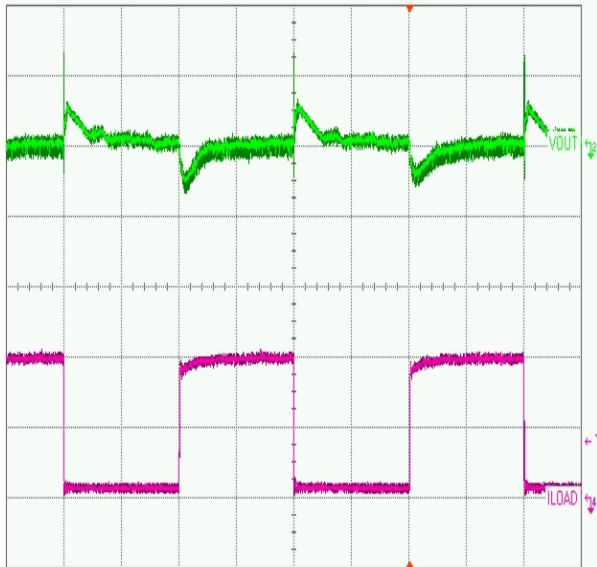
($V_{in} = 12\text{ V}$, $L = 5\ \mu\text{H}$, $C_{OUT} = 100\ \mu\text{F}$, $\text{Freq} = 500\ \text{kHz}$)
 Upper trace: Output dynamic voltage, 100 mV/div
 Lower trace: Output current, 1 A/div
 Time base : 50 $\mu\text{s}/\text{div}$

Figure 21. Load Transient Response for $V_{out} = 1.2\text{ V}$



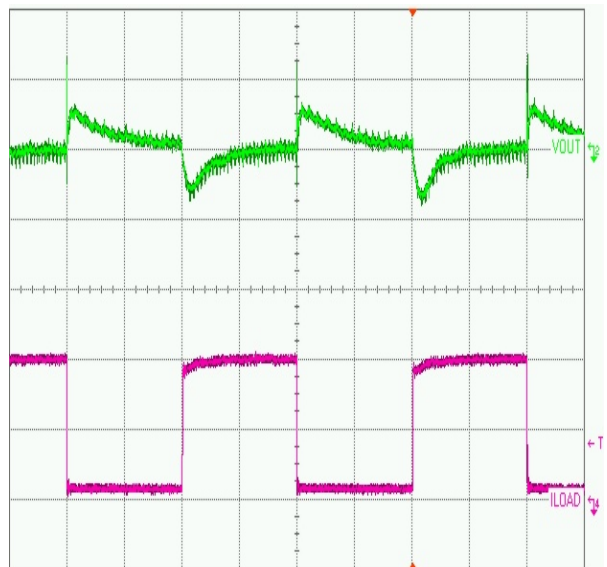
($V_{in} = 5\text{ V}$, $L = 5\ \mu\text{H}$, $C_{OUT} = 100\ \mu\text{F}$, $\text{Freq} = 1\ \text{MHz}$)
 Upper trace: Output dynamic voltage, 100 mV/div
 Lower trace: Output current, 1 A/div
 Time base : 50 $\mu\text{s}/\text{div}$

Figure 22. Load Transient Response for $V_{out} = 1.2\text{ V}$



($V_{in} = 12\text{ V}$, $L = 5\ \mu\text{H}$, $C_{OUT} = 100\ \mu\text{F}$, $\text{Freq} = 1\ \text{MHz}$)
 Upper trace: Output dynamic voltage, 100 mV/div
 Lower trace: Output current, 1 A/div
 Time base : 50 $\mu\text{s}/\text{div}$

Figure 23. Load Transient Response for $V_{out} = 3.3\text{ V}$



($V_{in} = 5\text{ V}$, $L = 5\ \mu\text{H}$, $C_{OUT} = 100\ \mu\text{F}$, $\text{Freq} = 333\ \text{kHz}$)
 Upper trace: Output dynamic voltage, 100 mV/div
 Lower trace: Output current, 1 A/div
 Time base : 50 $\mu\text{s}/\text{div}$

Figure 24. Load Transient Response for $V_{out} = 3.3\text{ V}$

DETAILED OPERATING DESCRIPTION

General

The NCP5252 is a PWM regulator intended for DC–DC conversion from 5 V & 12 V buses and supplies up to a 2 A load. The NCP5252 is a step down synchronous–rectifier buck topology regulator with integrated high–side and a low–side NMOS switch. The output voltage of the converter can be precisely regulated down to 600 mV $\pm 1.0\%$ when the V_{FB} pin is tied to V_{OUT} . The switching frequency can be adjusted to 333 kHz, 500 kHz or 1 MHz. A skip mode can be enabled to provide light load efficiency.

The NCP5252 includes features like power good monitor, internal soft–start, cycle–by–cycle current limit, short circuit protection, output undervoltage/overvoltage protection and thermal shutdown.

Control Logic

The internal control logic is powered by an internal LDO. The device is controlled by EN/SKIP pin. The EN/SKIP serves two functions. When voltage of EN/SKIP is below $V_{EN_DISABLE}$, the converter will shut down. If the voltage of EN/SKIP is set between V_{EN_FPWM} and V_{EN_SKIP} , the device will force to PWM mode operation. When voltage level of EN/SKIP is above V_{EN_SKIP} , the device will operate in PFM power saving mode. During start–up, the internal LDO is activated and power–on reset occurs which resets the logic and all protection faults. Once V_{REF} reaches its regulation voltage, an internal signal will wake up the supply undervoltage monitor which will assert a “GOOD” condition. In addition, the NCP5252 continuously monitors V_{CC} level with an undervoltage lockout (UVLO) function.

Forced PWM Operation (FPWM Mode)

The device is operating in the force PWM mode if an EN/SKIP pin voltage is set between V_{EN_FPWM} and V_{EN_SKIP} threshold. The low–side Power MOSFET is forced to be the complement of high–side Power MOSFET. This allows reverse inductor current. During the soft–start operation, the NCP5252 will automatically run as FPWM mode until output voltage is higher than internal soft–start ramp.

Pulse Skipping Operation (Skip Mode/PFM)

The device operates as skip mode if EN/SKIP pin voltage is higher than 2.9 V. Skip mode can reduce the switching loss at light load condition.

When the converter inductor current is higher than zero, the converter will run in continuous–conduction–mode (CCM) which behaves exactly the same as FPWM mode. In a light load condition, the regulator will automatically transition to skip mode.

Transient Response Enhancement (TRE)

For the conventional PWM controller in CCM, the fastest response time is one switching cycle in the worst case. To further improve transient response in CCM, a transient

response enhancement circuitry is implemented inside the NCP5252.

In CCM operation, the controller is continuously monitoring the COMP pin output voltage of the error amplifier and detecting the load transient events. The functional block diagram of TRE is shown as follows:

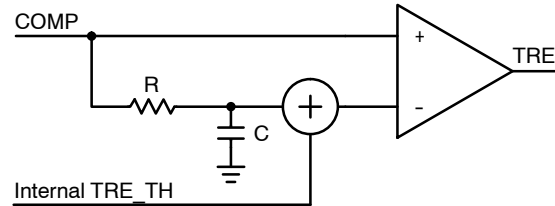


Figure 25. Block Diagram of TRE Circuit

Once the large transient occurs, the COMP signal may be large enough to exceed the threshold and then TRE “flag” signal will be asserted in a short period which is typically around one normal switching cycle.

In this short period, the controller will be running at high frequency and hence has faster response. After that the controller comes back to normal switching frequency operation.

Overcurrent Protection (OCP)

The NCP5252 will protect the system if an overcurrent event occurs. The regulator will continuously monitor the output current through the internal MOSFETs. If the main MOSFET current exceeds the internal current limit threshold, it will be turned off. If a repetitive overcurrent event occurs, both MOSFETs will be turned off and the device will hold for 3 normal soft–start periods before re–starting. A discharge resistor is turned on to discharge V_o before re–starting.

Overvoltage Protection (OVP)

When the SMPS output voltage is above 115% (typ) of the preset nominal regulation voltage for over 1.5 μs , an OV fault is set. The high side MOSFET will turn off and the bottom side MOSFET will be turned on to discharge the output until V_o drops below the default threshold (105%). Then the device will recover to normal regulation.

Undervoltage Protection (UVP)

A UVP circuit monitors the output voltage to detect an undervoltage event. The undervoltage limit is 80% (typ) of the nominal output voltage level. If the output voltage is below this threshold for over 4 clock cycles, an UVP fault is set and the device will hold for 3 soft–start periods and then restart the regulator through the soft–start cycle. Before the soft–start time, a discharge resistor is turned on to discharge V_o before re–starting.

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LDO Regulator

The internal LDO regulator (V5) can provide up to 20 mA typically for internal use. Connect a capacitor to pin V5 for proper regulation.

Undervoltage Logout

The UVLO circuit will activate when the V_{CC} voltage is below 3.5 V (typ). At that time both MOSFETs will turn off.

When the V_{CC} voltage is higher than 4.0 V, the UVLO flag will be cleared and the soft-start function will activate.

Thermal Shutdown

The IC will shutdown if the die temperature exceeds 150°C. The IC will restart with soft-start operation only after the junction temperature drops below 125°C.

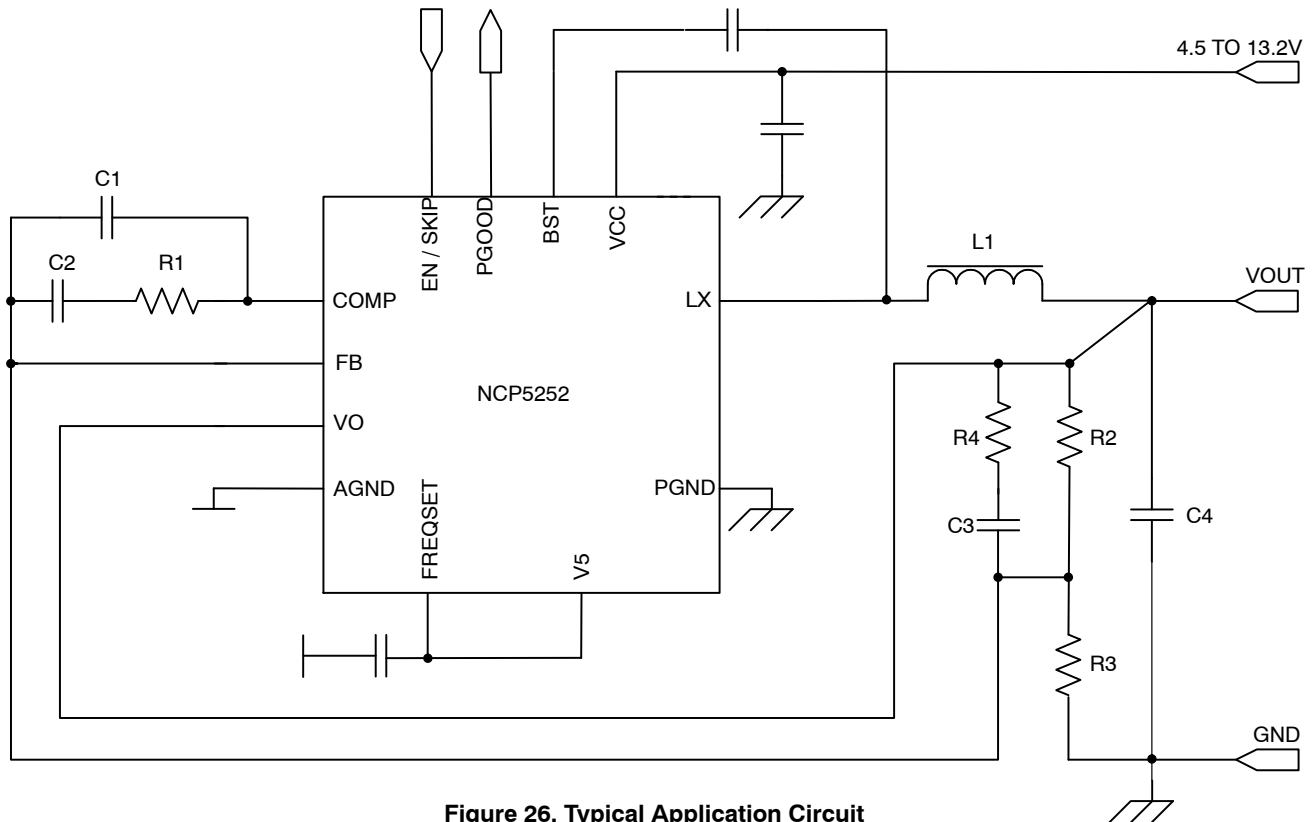


Figure 26. Typical Application Circuit

NCP5252

Table 1. Typical Design Value

For Vcc = 12 V Application											
Vin (V)	Vout (V)	Fsw (kHz)	C1 (pF)	C2 (nF)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (Ω)	C3 (pF)	C4 (μF)	L1 (μH)
12	5	Any	10	2.0	23	10	1.4	200	800	Ceramic 22 μF x 2	5.0
12	3.3	Any	10	2.0	23	10	2.2	200	800	Ceramic 22 μF x 2	5.0
12	1.2	Any	10	2.0	23	10	10	200	800	Ceramic 22 μF x 2	5.0
12	5	Any	10	2.0	54	10	1.4	200	800	SP 100 μF / 12 mΩ	5.0
12	3.3	Any	10	2.0	54	10	2.2	200	800	SP 100 μF / 12 mΩ	5.0
12	1.2	Any	10	2.0	54	10	10	200	800	SP 100 μF / 12 mΩ	5.0
12	5	Any	10	1.0	30	10	1.4	NC	NC	Electrolytic 470 μF/160 mΩ	5.0
12	3.3	Any	10	1.0	30	10	2.2	NC	NC	Electrolytic 470 μF/160 mΩ	5.0
12	1.2	Any	10	1.0	30	10	10	NC	NC	Electrolytic 470 μF/160 mΩ	5.0
For Vcc = 5 V Application											
Vin (V)	Vout (V)	Fsw (kHz)	C1 (pF)	C2 (nF)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (Ω)	C3 (pF)	C4 (μF)	L1 (μH)
5	3.3	Any	10	2.0	56	10	2.2	200	800	Ceramic 22 μF x 2, ESR = 4 mΩ	5.0
5	1.2	Any	10	2.0	56	10	10	200	800	Ceramic 22 μF x 2, ESR = 4 mΩ	5.0
5	3.3	Any	10	2.0	100	10	2.2	200	800	SP 100 μF / ESR = 12 mΩ	5.0
5	1.2	Any	10	2.0	100	10	10	200	800	SP 100 μF / ESR = 12 mΩ	5.0
5	3.3	Any	10	1.0	60	10	2.2	NC	NC	Electrolytic 470 μF/ESR = 160 mΩ	5.0
5	1.2	Any	10	1.0	60	10	10	NC	NC	Electrolytic 470 μF/ESR = 160 mΩ	5.0

NCP5252

TIMING DIAGRAMS

Timing 1 (SMPS Enable and Disable by EN_SKIP)

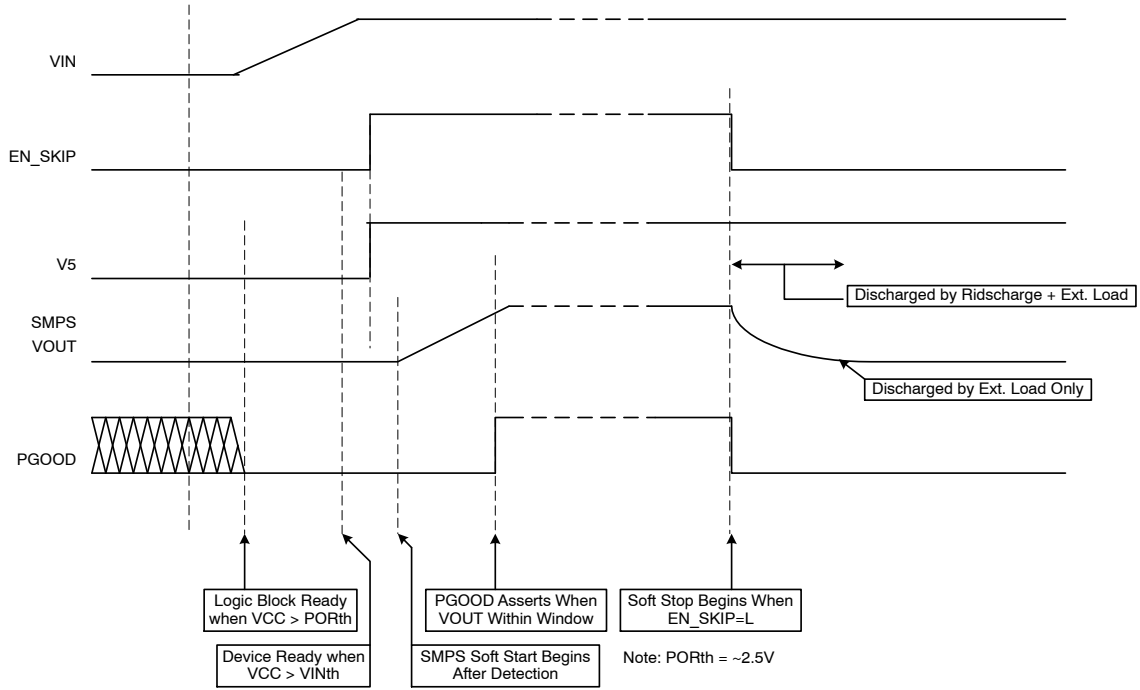


Figure 27.

Timing 2 (SMPS OVP & UVP Operation)

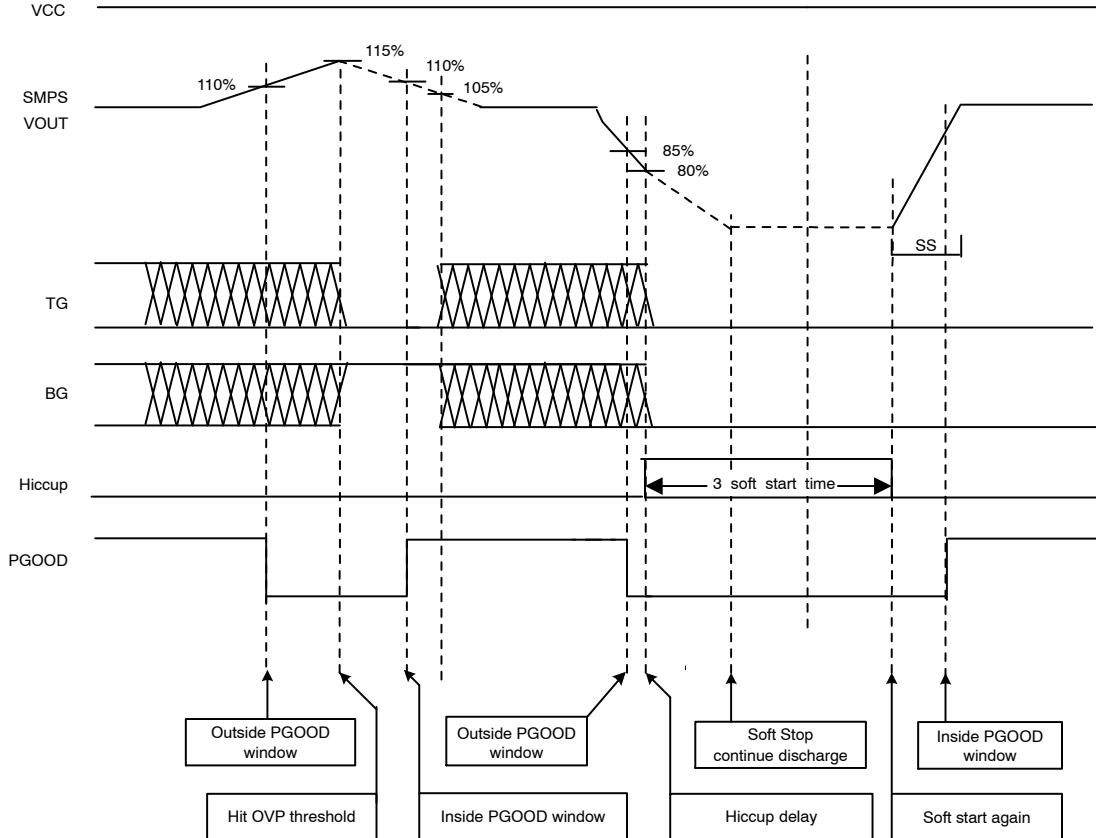
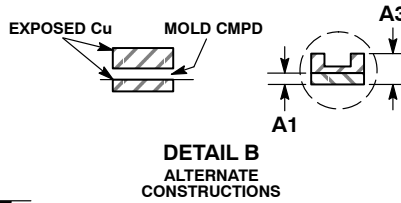
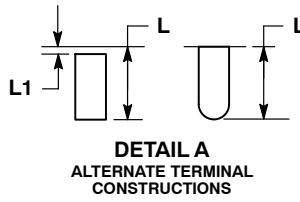
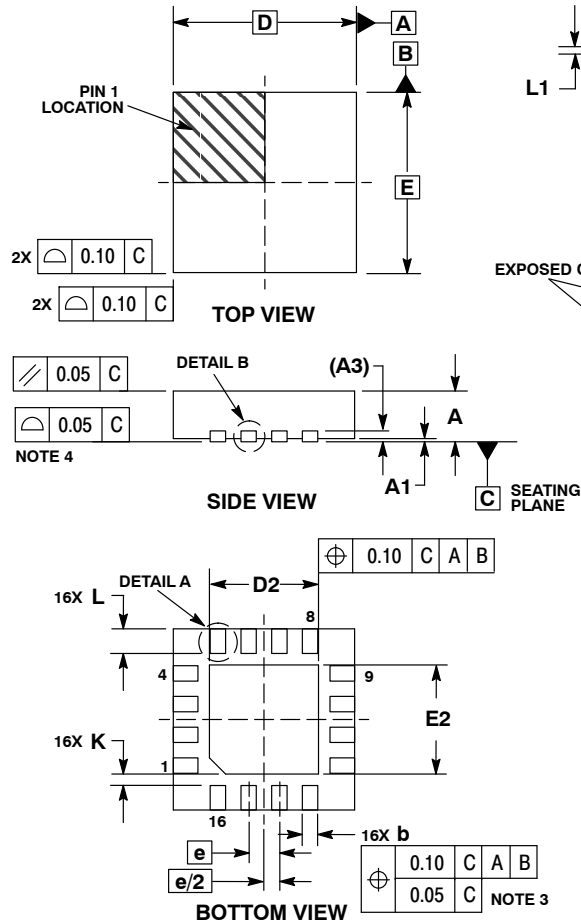


Figure 28.

NCP5252

PACKAGE DIMENSIONS

QFN16, 3x3, 0.5P
CASE 485G-01
ISSUE E

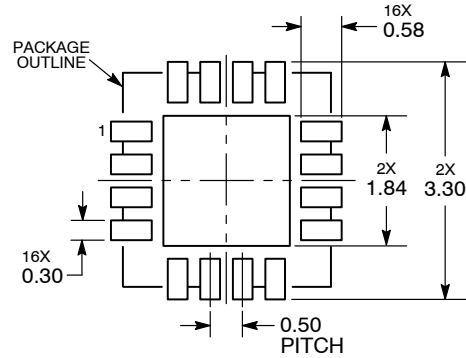


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	1.65	1.85
E	3.00	BSC
E2	1.65	1.85
e	0.50	BSC
K	0.18	TYP
L	0.30	0.50
L1	0.00	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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