# NCP5220A

# 3-in-1 PWM Dual Buck and Linear Power Controller

The NCP5220A 3−in−1 PWM Dual Buck and Linear Power Controller, is a complete power solution for MCH and DDR memory. This IC combines the efficiency of PWM controllers for the VDDQ supply and the MCH core supply voltage with the simplicity of linear regulator for the VTT termination voltage.

This IC contains two synchronous PWM buck controllers for driving four external N−Ch FETs to form the DDR memory supply voltage (VDDQ) and the MCH regulator. The DDR memory termination regulator (VTT) is designed to track at half of the reference voltage with sourcing and sinking current.

Protective features include, soft−start circuitry, undervoltage monitoring of 5VDUAL, BOOT voltage and thermal shutdown. The device is housed in a thermal enhanced space−saving DFN−20 package.

### Features

- Incorporates Synchronous PWM Buck Controllers for VDDQ and VMCH
- Integrated Power FETs with VTT Regulator Source/Sink up to 2.0 A
- All External Power MOSFETs are N−Channel
- Adjustable VDDQ and VMCH by External Dividers
- VTT Tracks at Half the Reference Voltage
- Fixed Switching Frequency of 250 kHz for VDDQ and VMCH
- Doubled Switching Frequency of 500 kHz for VDDQ Controller in Standby Mode to Optimize Inductor Current Ripple and Efficiency
- Soft−Start Protection for All Controllers
- Undervoltage Monitor of Supply Voltages
- Overcurrent Protections for DDQ and VTT Regulators
- VTT Regulators Soft−Start Current Protection
- Fully Complies with ACPI Power Sequencing Specifications
- Short Circuit Protection Prevents Damage to Power Supply Due to Reverse DIMM Insertion
- Thermal Shutdown
- 5x6 DFN−20 Package
- Pb−Free Package is Available*

### Typical Applications

- DDR I and DDR II Memory and MCH Power Supply

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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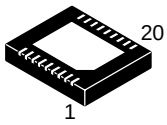
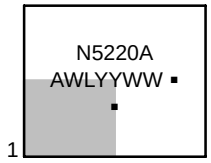



**DFN−20**
**MN SUFFIX**
**CASE 505AB**

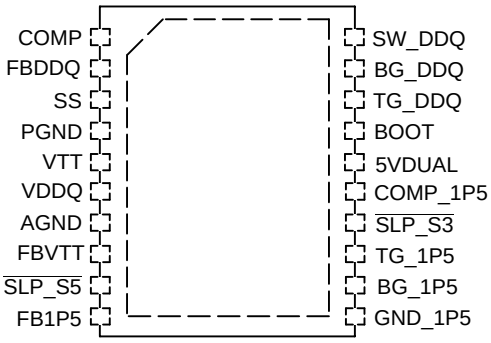
### MARKING DIAGRAM




| | |
|---|---|
| N5220A | = Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### PIN CONNECTIONS




NOTE: Pin 21 is the thermal pad on the bottom of the device.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCP5220AMNR2 | DFN−20 | 2500/Tape & Reel |
| NCP5220AMNR2G | DFN−20 (Pb−Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

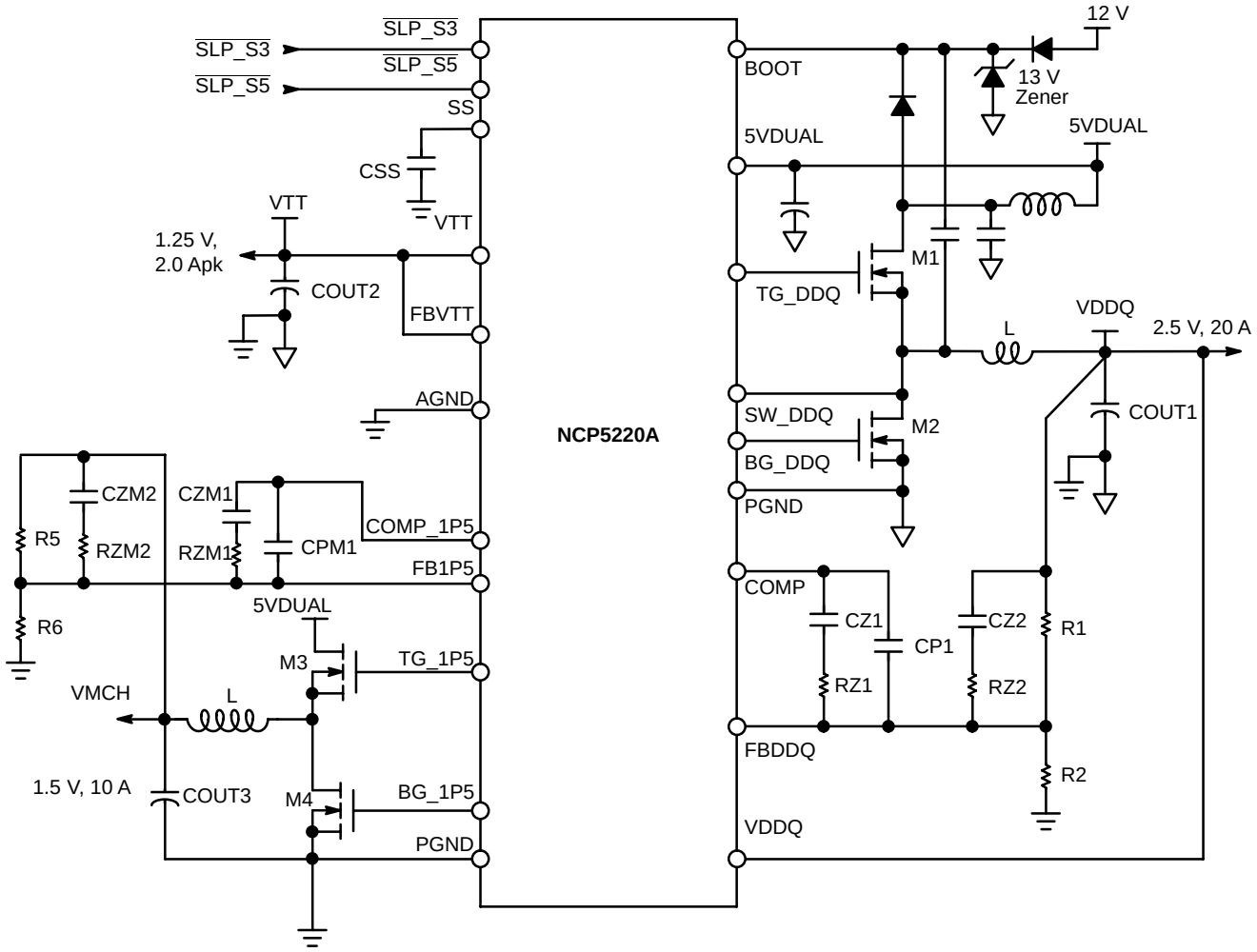



**Figure 1. Application Diagram**

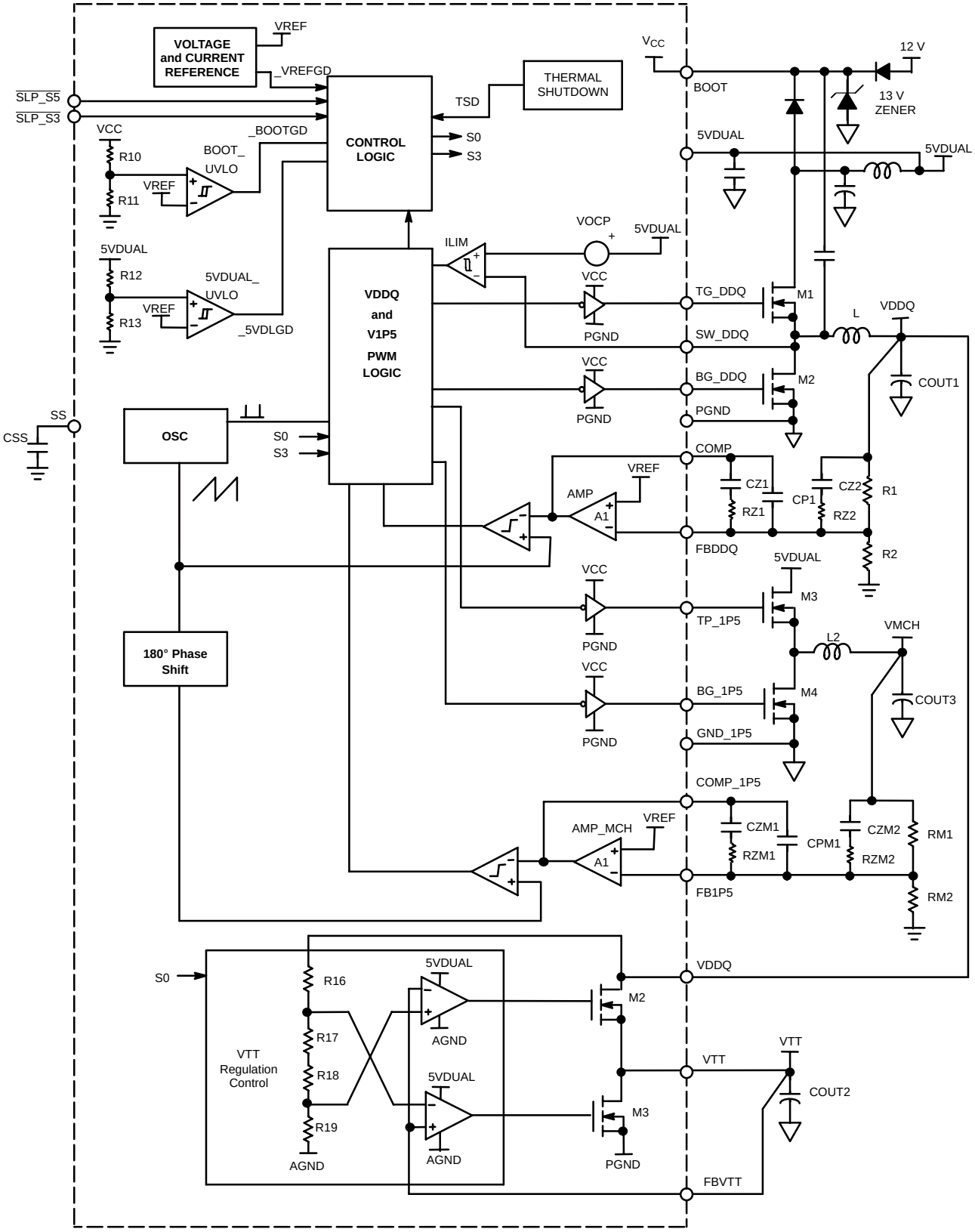



**Figure 2. Internal Block Diagram**

## PIN DESCRIPTION

| Pin | Symbol | Description |
|---|---|---|
| 1 | COMP | VDDQ error amplifier compensation node. |
| 2 | FBDDQ | DDQ regulator feedback pin. |
| 3 | SS | Soft−start pin of DDQ and MCH. |
| 4 | PGND | Power ground. |
| 5 | VTT | VTT regulator output. |
| 6 | VDDQ | Power input for VTT linear regulator. |
| 7 | AGND | Analog ground connection and remote ground sense. |
| 8 | FBVTT | VTT regulator pin for closed loop regulation. |
| 9 | $\overline{\text{SLP\_S5}}$ | Active LOW control signal to activate S5 Power OFF State. |
| 10 | FB1P5 | V1P5 switching regulator feedback pin. |
| 11 | GND_1P5 | Power ground for V1P5 regulator. |
| 12 | BG_1P5 | Gate driver output for V1P5 regulator low side N−Channel Power FET. |
| 13 | TG_1P5 | Gate driver output for V1P5 regulator high side N−Channel Power FET. |
| 14 | $\overline{\text{SLP\_S3}}$ | Active LOW control signal to activate S3 sleep state. |
| 15 | COMP_1P5 | V1P5 error amplifier compensation node. |
| 16 | 5VDUAL | 5.0 V dual supply input, which is monitored by undervoltage lock out circuitry. |
| 17 | BOOT | Gate driver input supply, which is monitored by undervoltage lock out circuitry, and a boost capacitor connection between SWDDQ and this pin. |
| 18 | TG_DDQ | Gate driver output for DDQ regulator high side N−Channel Power FET. |
| 19 | BG_DDQ | Gate driver output for DDQ regulator low side N−Channel Power FET. |
| 20 | SW_DDQ | DDQ regulator switch node and current limit sense input. |
| 21 | TH_PAD | Copper pad on bottom of IC used for heatsinking. This pin should be connected to the ground plane under the IC. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage (Pin 16) to AGND (Pin 7) | 5VDUAL | −0.3, 6.0 | V |
| BOOT (Pin 17) to AGND (Pin 7) | BOOT | −0.3, 14 | V |
| Gate Drive (Pins 12, 13, 18, 19) to AGND (Pin 7) | Vg | −0.3 DC,<br>−4.0 for $<$100 ns; 14 | V |
| Input / Output Pins to AGND (Pin 7)<br>Pins 1−3, 5, 6, 8−10, 14−15, 20 | $V_{IO}$ | −0.3, 6.0 | V |
| PGND (Pin 4), GND_1P5 (Pin 11) to AGND (Pin 7) | $V_{GND}$ | −0.3, 0.3 | V |
| Thermal Characteristics<br>DFN−20 Plastic Package<br>Thermal Resistance, Junction−to−Air | $R_{\theta JA}$ | 35 | °C/W |
| Operating Junction Temperature Range | $T_J$ | 0 to +150 | °C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Moisture Sensitivity Level | MSL | 2.0 | |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests: Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22–A114. Machine Model (MM) ±200 V per JEDEC standard: JESD22–A115.
2. Latchup Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.

**ELECTRICAL CHARACTERISTICS** (5VDUAL = 5.0 V, BOOT = 12 V, $T_A$ = 0°C to 70°C, L = 1.7 μH, COUT1 = 3770 μF, COUT2 = 470 μF, COUT3 = NA, CSS = 33 nF, R1 = 2.166 kΩ, R2 = 2.0 kΩ, RZ1 = 20 kΩ, RZ2 = 8.0 Ω, CP1 = 10 nF, CZ1 = 6.8 nF, CZ2 = 100 nF, RM1 = 2.166 kΩ, RM2 = 2.0 kΩ, RZM1 = 20 kΩ, RZM2 = 8.0 Ω, CPM1 = 10 nF, CZM1 = 6.8 nF, CZM2 = 100 nf for min/max values unless otherwise noted). Duplicate component values of MCH regulator from DDQ.

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | | |
| 5VDUAL Supplier Rail Voltage | V5VDUAL | – | 4.5 | 5.0 | 5.5 | V |
| BOOT Supplier Rail Voltage at S0 | VBOOT | – | 10.5 | 12 | 13.2 | V |
| **SUPPLY CURRENT** | | | | | | |
| S0 Mode Supply Current from 5VDUAL | I5VDL_S0 | $\overline{SLP\_S5}$ = HIGH, $\overline{SLP\_S3}$ = HIGH, BOOT = 12 V, TG_1P5 and BG_1P5 Open | – | – | 10 | mA |
| S3 Mode Supply Current from 5VDUAL | I5VDL_S3 | $\overline{SLP\_S5}$ = HIGH, $\overline{SLP\_S3}$ = LOW, TG_1P5 and BG_1P5 Open | – | – | 5.0 | mA |
| S5 Mode Supply Current from 5VDUAL | I5VDL_S5 | $\overline{SLP\_S5}$ = LOW, BOOT = 0 V, TG_1P5 and BG_1P5 Open | – | – | 1.0 | mA |
| S0 Mode Supply Current from BOOT | IBOOT_S0 | $\overline{SLP\_S5}$ = HIGH, $\overline{SLP\_S3}$ = HIGH, BOOT = 12 V, TG_1P5 and BG_1P5 Open | – | – | 25 | mA |
| S3 Mode Supply Current from BOOT | IBOOT_S3 | $\overline{SLP\_S5}$ = HIGH, $\overline{SLP\_S3}$ = LOW, TG_1P5 and BG_1P5 Open | – | – | 25 | mA |
| **UNDERVOLTAGE−MONITOR** | | | | | | |
| 5VDUAL UVLO Upper Threshold | V5VDLUV+ | – | – | – | 4.4 | V |
| 5VDUAL UVLO Hysteresis | V5VDLhys | – | 250 | 400 | 550 | mV |
| BOOT UVLO Upper Threshold | VBOOTUV+ | – | 8.8 | – | 10.4 | V |
| BOOT UVLO Hysteresis | VBOOThys | – | – | 1.0 | 1.3 | V |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown | Tsd | (Note 3) | – | 145 | – | °C |
| Thermal Shutdown Hysteresis | Tsdhys | (Note 3) | – | 25 | – | °C |
| **DDQ SWITCHING REGULATOR** | | | | | | |
| FBDDQ Feedback Voltage, Control Loop in Regulation | VFBQ | $T_A$ = 25°C<br>$T_A$ = 0°C to 70°C | 1.178<br>1.166 | 1.190<br>– | 1.202<br>1.214 | V |
| Feedback Input Current | IDDQFB | V(FBDDQ) = 1.3 V | – | – | 1.0 | μA |
| Oscillator Frequency in S0 Mode | FDDQS0 | – | 217 | 250 | 283 | KHz |
| Oscillator Frequency in S3 Mode | FDDQS3 | – | 434 | 500 | 566 | KHz |
| Oscillator Ramp Amplitude | dVOSC | (Note 3) | – | 1.3 | – | Vp−p |
| Current Limit Blanking Time in S0 Mode | TDDQbk | (Note 3) | 400 | – | – | nS |
| Current Limit Threshold Offset from 5VDUAL | VOCP | (Note 3) | 0.8 | – | – | V |
| Minimum Duty Cycle | Dmin | – | 0 | – | – | % |
| Maximum Duty Cycle | Dmax | – | – | – | 100 | % |
| Soft−Start Pin Current for DDQ | Iss1 | V(SS) = 0 V | 3.0 | 4.0 | – | μA |
| **DDQ ERROR AMPLIFIER** | | | | | | |
| DC Gain | GAINDDQ | (Note 3) | – | 70 | – | dB |
| Gain−Bandwidth Product | GBWDDQ | COMP PIN to GND = 220 nF, 1.0 Ω in Series (Note 3) | – | 12 | – | MHz |
| Slew Rate | SRDDQ | COMP PIN TO GND = 10 pF | – | 8.0 | – | V/uS |

3. Guaranteed by design, not tested in production.

**ELECTRICAL CHARACTERISTICS** (5VDUAL = 5.0 V, BOOT = 12 V, $T_A$ = 0°C to 70°C, L = 1.7 μH, COUT1 = 3770 μF, COUT2 = 470 μF, COUT3 = NA, CSS = 33 nF, R1 = 2.166 kΩ, R2 = 2.0 kΩ, RZ1 = 20 kΩ, RZ2 = 8.0 Ω, CP1 = 10 nF, CZ1 = 6.8 nF, CZ2 = 100 nF, RM1 = 2.166 kΩ, RM2 = 2.0 kΩ, RZM1 = 20 kΩ, RZM2 = 8.0 Ω, CPM1 = 10 nF, CZM1 = 6.8 nF, CZM2 = 100 nf for min/max values unless otherwise noted). Duplicate component values of MCH regulator from DDQ.

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VTT ACTIVE TERMINATION REGULATOR** | | | | | | |
| VTT Tracking DDQ_REF/2 at S0 Mode | DVTTS0 | IOUT= 0 to 2.0 A (Sink Current)<br>IOUT= 0 to –2.0 A (Source Current) | −30 | − | 30 | mV |
| VTT Source Current Limit | ILIMVTsrc | The current limit is valid only after finishing soft−start | 2.0 | − | − | A |
| VTT Sink Current Limit | ILIMVTsnk | − | 2.0 | − | − | A |
| **CONTROL SECTION** | | | | | | |
| $\overline{\text{SLP\_S5}}$, $\overline{\text{SLP\_S3}}$ Input Logic HIGH | Logic_H | − | 2.0 | − | − | V |
| $\overline{\text{SLP\_S5}}$, $\overline{\text{SLP\_S3}}$ Input Logic LOW | Logic_L | − | − | − | 0.8 | V |
| $\overline{\text{SLP\_S5}}$, $\overline{\text{SLP\_S3}}$ Input Current | Ilogic | − | − | − | 1.0 | μA |
| **GATE DRIVERS** | | | | | | |
| TGDDQ Gate Pull−HIGH Resistance | RH_TG | VCC = 12 V, V(TGDDQ) = 11.9 V | − | 3.0 | − | Ω |
| TGDDQ Gate Pull−LOW Resistance | RL_TG | VCC = 12 V, V(TGDDQ) = 0.1 V | − | 2.5 | − | Ω |
| BGDDQ Gate Pull−HIGH Resistance | RH_BG | VCC = 12 V, V(BGDDQ) = 11.9 V | − | 3.0 | − | Ω |
| BGDDQ Gate Pull−LOW Resistance | RL_BG | VCC = 12 V, V(BGDDQ) = 0.1 V | − | 1.3 | − | Ω |
| TG1P5 Gate Pull−HIGH Resistance | RH_TPG | VCC = 12 V, V(TG1P5) = 11.9 V | − | 3.0 | − | Ω |
| TG1P5 Gate Pull−LOW Resistance | RL_TPG | VCC = 12 V, V(TG1P5) = 0.1 V | − | 2.5 | − | Ω |
| BG1P5 Gate Pull−HIGH Resistance | RH_BPG | VCC = 12 V, V(BG1P5) = 11.9 V | − | 3.0 | − | Ω |
| BG1P5 Gate Pull−LOW Resistance | RL_BPG | VCC = 12 V, V(BG1P5) = 0.1 V | − | 1.3 | − | Ω |
| **MCH SWITCHING REGULATOR** | | | | | | |
| VFB1P5 Feedback Voltage, Control Loo in Regulation | VFB1P5 | $T_A$ = 0°C to 70°C | 0.784 | 0.8 | 0.816 | V |
| Feedback Input Current | I1P5FB | − | − | − | 1.0 | μA |
| Oscillator Frequency | F1P5 | − | 217 | 250 | 283 | KHz |
| Oscillator Ramp Amplitude | dV1P5OSC | (Note 4) | − | 1.3 | − | Vp−p |
| Minimum Duty Cycle | Dmin_1P5 | − | 0 | − | − | % |
| Maximum Duty Cycle | Dmax_1P5 | − | − | − | 100 | % |
| Soft−Start Pin Current for V1P5 Regulator | ISS2 | (Note 4) | 3.0 | 4.0 | − | μA |

4. Guaranteed by design, not tested in production.

## TYPICAL OPERATING CHARACTERISTICS

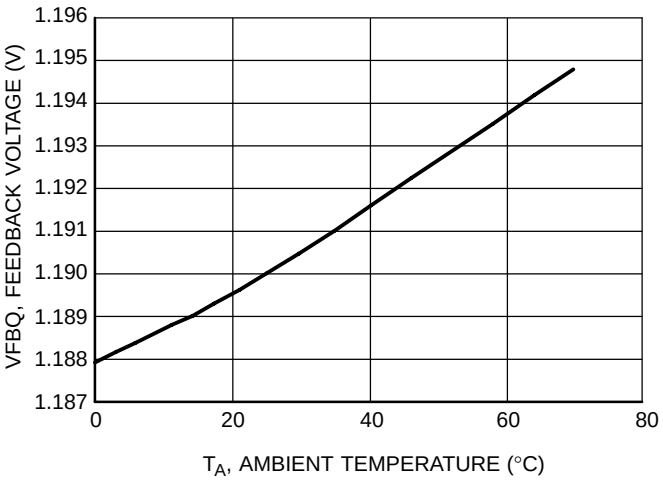



**Figure 3. VFBQ Feedback Voltage vs. Ambient Temperature**

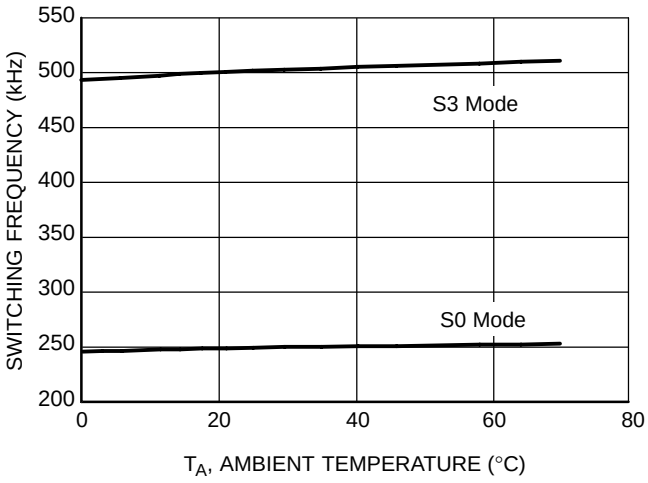



**Figure 4. Oscillation Frequency in S0/S3 vs. Ambient Temperature**

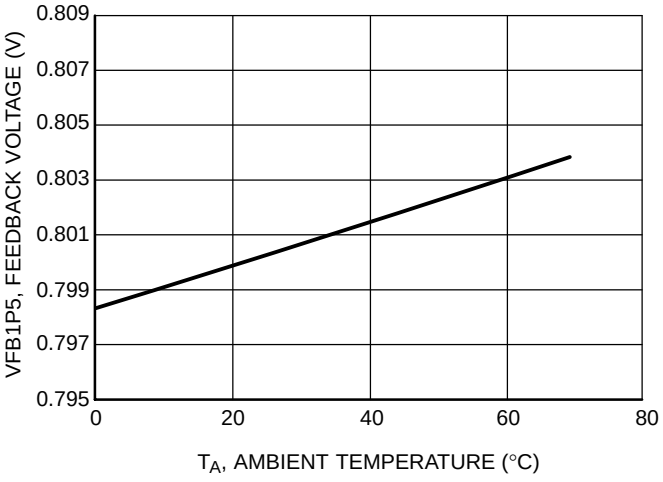



**Figure 5. VFB1P5 Feedback Voltage vs. Ambient Temperature**

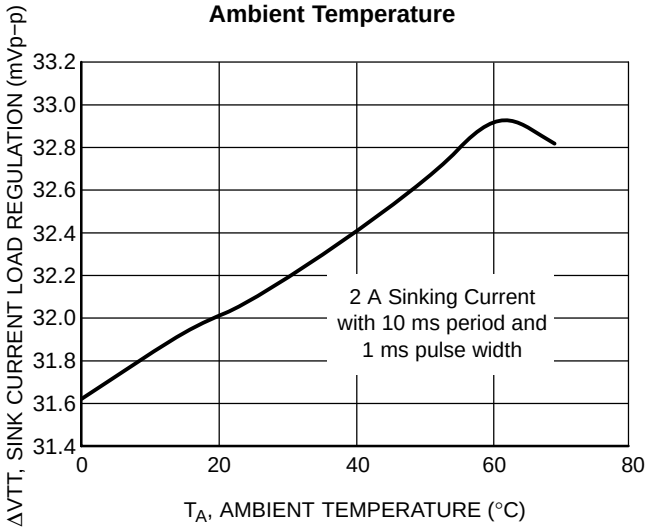



**Figure 6. VTT Sink Current Load Regulation vs. Ambient Temperature**

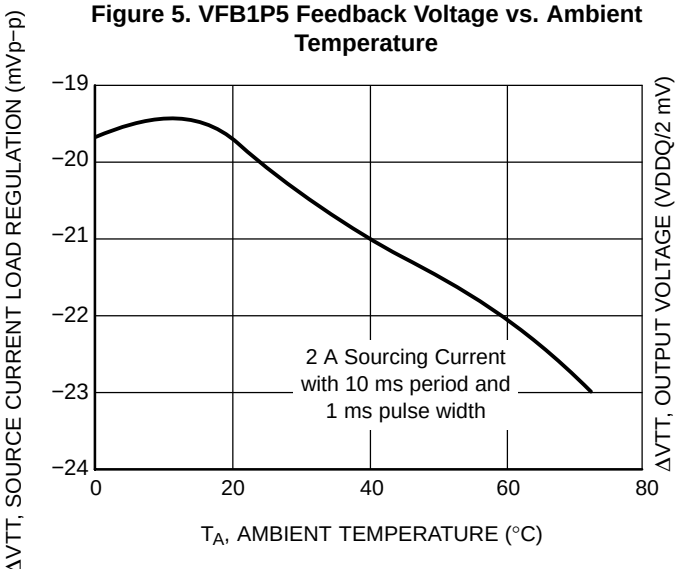



**Figure 7. VTT Source Current Load Regulation vs. Ambient Temperature**

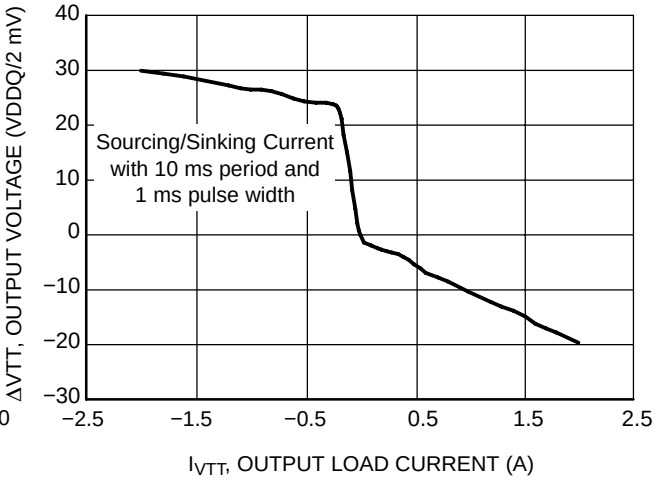
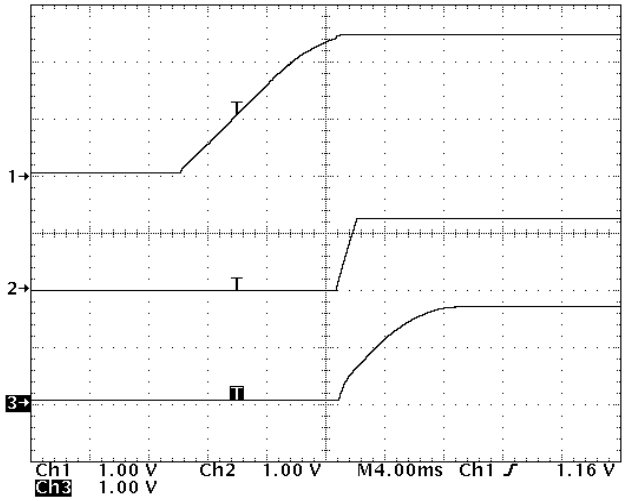


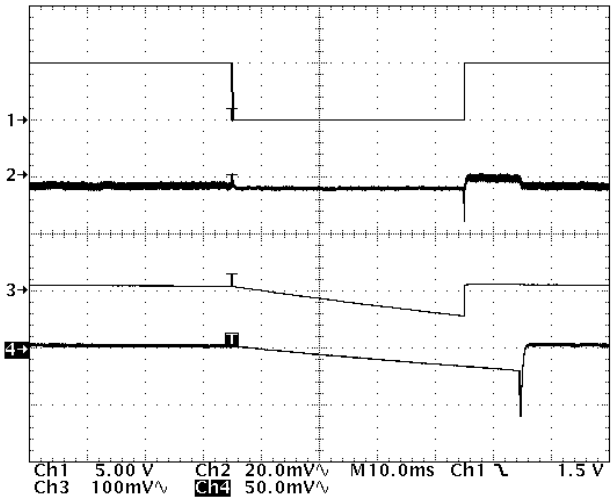

**Figure 8. VTT Output Voltage vs. Load Current**

## TYPICAL OPERATING WAVEFORMS



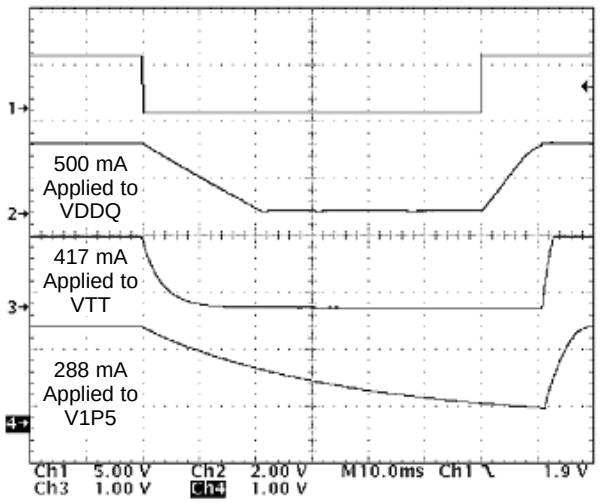

Channel 1: VDDQ output voltage, 1.0 V/div
Channel 2: VTT output voltage, 1.0 V/div
Channel 3: V1P5 output voltage, 1.0 V/div
Time base: 4.0 ms/div

**Figure 9. Power−up Sequence**



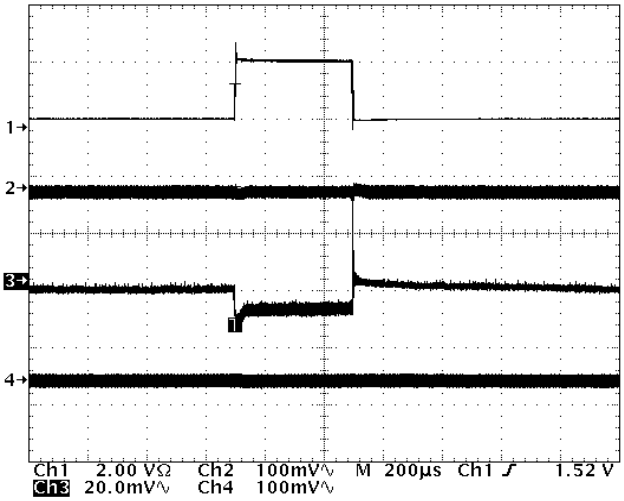

Channel 1: $\overline{\text{SLP\_S3}}$ pin voltage, 5.0 V/div
Channel 2: VDDQ output voltage, AC−coupled, 20 mV/div
Channel 3: VTT output voltage, AC−coupled, 100 mV/div
Channel 4: V1P5 output voltage, 50 mV/div
Time base: 10 ms/div

**Figure 10. S0−S3−S0 Transition**




Channel 1: $\overline{\text{SLP\_S5}}$ pin voltage, 5.0 V/div
Channel 2: VDDQ output voltage, 2.0 V/div
Channel 3: VTT output voltage, 1.0 V/div
Channel 4: V1P5 output voltage, 1.0 V/div
Time base: 10 ms/div

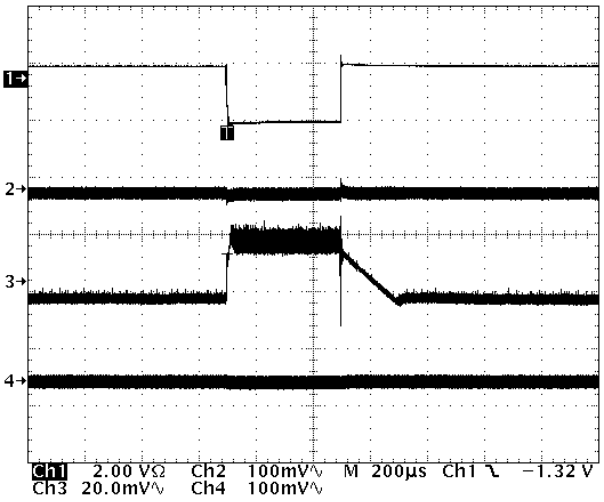
**Figure 11. S0−S5−S0 Transition**




Channel 1: Current sourced out of VTT, 2.0 A/div
Channel 2: VDDQ output voltage, AC−coupled, 100 mV/div
Channel 3: VTT output voltage, AC−coupled, 20 mV/div
Channel 4: V1P5 output voltage, AC−coupled, 100 mV/div
Time base: 200 µs/div

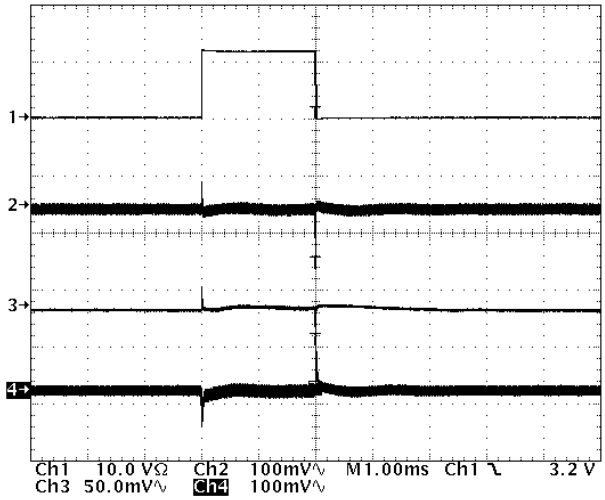
**Figure 12. $V_{TT}$ Source Current Transient, 0A−2A−0A**

## TYPICAL OPERATING WAVEFORMS



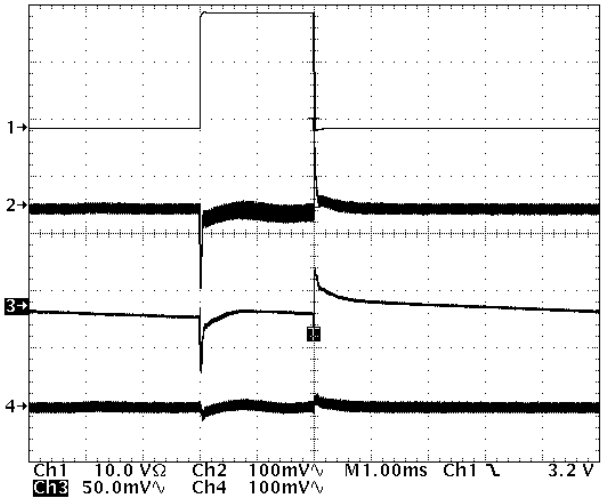

Channel 1: Current sunk into of VTT, 2.0 A/div
Channel 2: VDDQ output voltage, AC−coupled, 100 mV/div
Channel 3: VTT output voltage, AC−coupled, 20 mV/div
Channel 4: V1P5 output voltage, AC−coupled, 100 mV/div
Time base: 200 µs/div

**Figure 13. $V_{TT}$ Sink Current Transient, 0A−2A−0A**



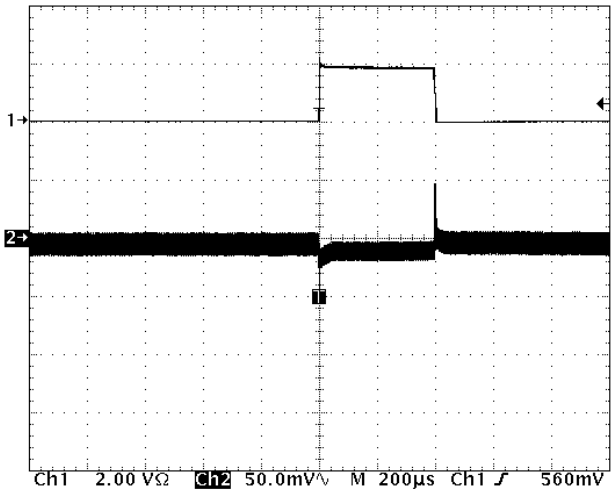

Channel 1: Current sourced into of V1P5, 10 A/div
Channel 2: VDDQ output voltage, AC−coupled, 100 mV/div
Channel 3: VTT output voltage, AC−coupled, 50 mV/div
Channel 4: V1P5 output voltage, AC−coupled, 100 mV/div
Time base: 1.0 ms/div

**Figure 14. $V_{1P5}$ Source Current Transient, 0A−12A−0A**




Channel 1: Current sourced into of VDDQ, 10 A/div
Channel 2: VDDQ output voltage, AC−coupled, 100 mV/div
Channel 3: VTT output voltage, AC−coupled, 50 mV/div
Channel 4: V1P5 output voltage, AC−coupled, 100 mV/div
Time base: 1.0 ms/div

**Figure 15. $V_{DDQ}$ Source Current Transient, 0A−20A−0A**




Channel 1: Current sourced into of VDDQ, 2.0 A/div
Channel 2: VDDQ output voltage, AC−coupled, 50 mV/div
Time base: 200 µs/div

**Figure 16. S3 Mode without 12VATX, 0A−2A−0A**

## DETAILED OPERATION DESCRIPTIONS

### General

The NCP5220A 3−in−1 PWM Dual Buck Linear DDR Power Controller contains two high efficiency PWM controllers and an integrated two−quadrant linear regulator.

The VDDQ supply is produced by a PWM switching controller with two external N−Ch FETs. The VTT termination voltage is an integrated linear regulator with sourcing and sinking current capability which tracks at one−half VDDQ. The MCH core voltage is created by the secondary switching controller.

The inclusion of soft−start, supply undervoltage monitors and thermal shutdown, makes this device a total power solution for the MCH and DDR memory system. This device is packaged in a DFN−20.

### ACPI Control Logic

The ACPI control logic is powered by the 5VDUAL supply. It accepts external controls at the $\overline{\text{SLP\_S3}}$, $\overline{\text{SLP\_S5}}$ inputs and internal supply voltage monitoring signals from two UVLOs to decode the operating mode in accordance with the state transition diagram in Figure 18.

These UVLOs monitor the external supplies, 5VDUAL and 12VATX, through 5VDUAL and BOOT pins respectively. Two control signals, _5VDUALGD and _BOOTGD, are asserted when the supply voltages are good.

When the device is powered up initially, it is in the S5 shutdown mode to minimize the power consumption. When all three supply voltages are good with $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S5}}$ remaining HIGH, the device enters the S0 normal operating mode. The transition of $\overline{\text{SLP\_S3}}$ from HIGH to LOW while in the S0 mode, triggers the device into the S3 sleep mode. In S3 mode the 12VATX supply collapses. On transition of $\overline{\text{SLP\_S3}}$ from LOW to HIGH, the device returns to S0 mode. The IC can re−enter S5 mode by setting $\overline{\text{SLP\_S5}}$ LOW. A timing diagram is shown in Figure 17.

Table 1 summarizes the operating states of all the regulators, as well as the conditions of the output pins.

### Internal Bandgap Voltage Reference

An internal bandgap reference is generated whenever 5VDUAL exceeds 2.7 V. Once this bandgap reference is in regulation, an internal signal _VREFGD will be asserted.

### S5 to S0 Mode Power−Up Sequence

The ACPI control logic is enabled by the assertion of _VREFGD. Once the ACPI control is activated, the power−up sequence starts by waking up the 5VDUAL voltage monitor block. If the 5VDUAL supply is within the preset levels, the BOOT undervoltage monitor block is then enabled. After 12VATX is ready and the BOOT UVLO is asserted LOW, the ACPI control triggers this device from S5 shutdown mode into S0 normal operating mode by activating the soft−start of DDQ switching regulator, providing $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S5}}$ remain HIGH.

Once the DDQ regulator is in regulation and the soft−start interval is completed, the _InRegDDQ signal is asserted HIGH to enable the VTT regulator as well as the V1P5 switching regulator.

### DDQ Switching Regulator

In S0 mode the DDQ regulator is a switching synchronous rectification buck controller driving two external power N−Ch FETs to supply up to 20 A. It employs voltage mode fixed frequency PWM control with external compensation switching at 250 kHz ± 13.2%. As shown in Figure 2, the VDDQ output voltage is divided down and fed back to the inverting input of an internal amplifier through the FBDDQ pin to close the loop at VDDQ = VFBQ × (1 + R1/R2). This amplifier compares the feedback voltage with an internal reference voltage of 1.190 V to generate an error signal for the PWM comparator. This error signal is compared with a fixed frequency RAMP waveform derived from the internal oscillator to generate a pulse−width−modulated signal. This PWM signal drives the external N−Ch FETs via the TG_DDQ and BG_DDQ pins. External inductor L and capacitor COUT1 filter the output waveform. When the IC leaves the S5 state, the VDDQ output voltage ramps up at a soft−start rate controlled by the capacitor at the SS pin. When the regulation of VDDQ is detected in S0 mode, _INREGDDQ goes HIGH to notify the control block.

In S3 standby mode, the switching frequency is doubled to reduce the conduction loss in the external N−Ch FETs.

**Table 1. Mode, Operation and Output Pin Conditions**

| MODE | OPERATING CONDITIONS | | | OUTPUT PIN CONDITIONS | | | |
|---|---|---|---|---|---|---|---|
| | DDQ | VTT | MCH | TG_DDQ | BG_DDQ | TP_1P5 | BG_1P5 |
| S0 | Normal | Normal | Normal | Normal | Normal | Normal | Normal |
| S3 | Standby | H−Z | OFF | Standby | Standby | Low | Low |
| S5 | OFF | H−Z | OFF | Low | Low | Low | Low |

For enhanced efficiency, an active synchronous switch is used to eliminate the conduction loss contributed by the forward voltage of a diode or Schottky diode rectifier. Adaptive non−overlap timing control of the complementary gate drive output signals is provided to reduce shoot−through current that degrades efficiency.

### Tolerance of VDDQ

Both the tolerance of VFBQ and the ratio of the external resistor divider R1/R2 impact the precision of VDDQ. With the control loop in regulation, VDDQ = VFBQ × (1 + R1/R2). With a worst case (for all valid operating conditions) VFBQ tolerance of ±1.5%, a worst case range of ±2% for VDDQ will be assured if the ratio R1/R2 is specified as 1.100 ±1%.

### Fault Protection of VDDQ Regulator

In S0 mode, an internal voltage (VOCP) = 5VDUAL – 0.8 sets the current limit for the high−side switch. The voltage VOCP pin is compared to the voltage at SWDDQ pin when the high−side gate drive is turned on after a fixed period of blanking time to avoid false current limit triggering. When the voltage at SWDDQ is lower than VOCP, an overcurrent condition occurs and all regulators are latched off to protect against overcurrent. The IC will be powered up again if one of the supply voltages, 5VDUAL, SLP_S5 or 12VATX, is recycled. The main purpose is for fault protection, not for precise current limit.

In S3 mode, this overcurrent protection feature is disabled.

### Feedback Compensation of VDDQ Regulator

The compensation network is shown in Figure 2.

### VTT Active Terminator

The VTT active terminator is a two quadrant linear regulator with two internal N−Ch FETs to provide current sink and source capability up to 2.0 A. It is activated only when the DDQ regulator is in regulation in S0 mode. It draws power from VDDQ with the internal gate drive power derived from 5VDUAL. While VTT output is connecting to the FBVTT pin directly, VTT voltage is designed to automatically track at the half of VDDQ. This regulator is stable with any value of output capacitor greater than 470 μF, and is insensitive to ESR ranging from 1.0 mΩ to 400 mΩ.

### Fault Protection of VTT Active Terminator

To provide protection for the internal FETs, bi−directional current limit preset at 2.4 A magnitude is implemented. The VTT with current limit at 1.0 A provides a soft−start function during startup in order to avoid overloading at S3 mode.

### MCH Switching Regulator

The secondary switching regulator is identical to the DDQ regulator except the output is 10 A. No fault protection is implemented and the soft−start timing is twice as fast with respect to CSS.

### BOOT Pin Supply Voltage

In typical application, a flying capacitor is connected between SWDDQ and BOOT pins. In S0 mode, 12VATX is tied to BOOT pin through a Schottky diode as well. A 13 V Zener clamp circuit must clamp this boot strapping voltage produced by the flying capacitor in S0 mode.

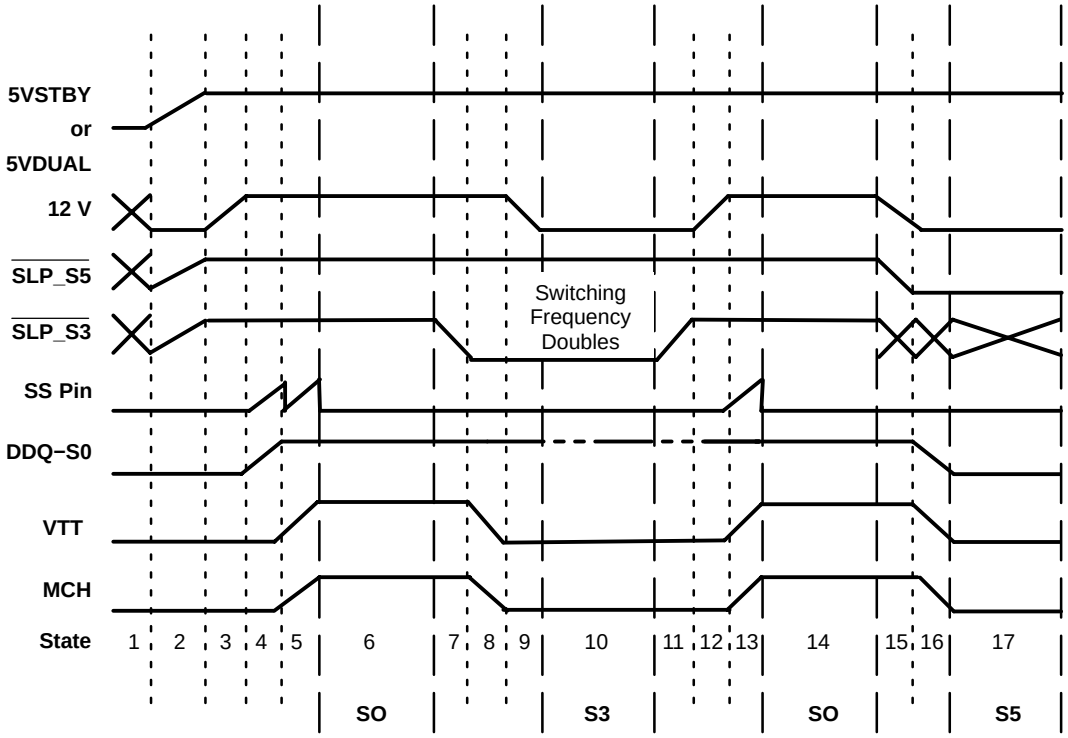
In S3 mode the 12VATX is collapsed and the BOOT voltage is created by the Schottky diode between 5VDUAL and BOOT pins as well as the flying capacitor. The BOOT_UVLO works specially. The _BOOTGD goes low and the IC remains in S3 mode.

### Thermal Consideration

Assuming an ambient temperature of 50°C, the maximum allowed dissipated power of DFN−20 is 2.8 W, which is enough to handle the internal power dissipation in S0 mode. **To take full advantage of the thermal capability of this package, the exposed pad underneath must be soldered directly onto a PCB metal substrate to allow good thermal contact.**

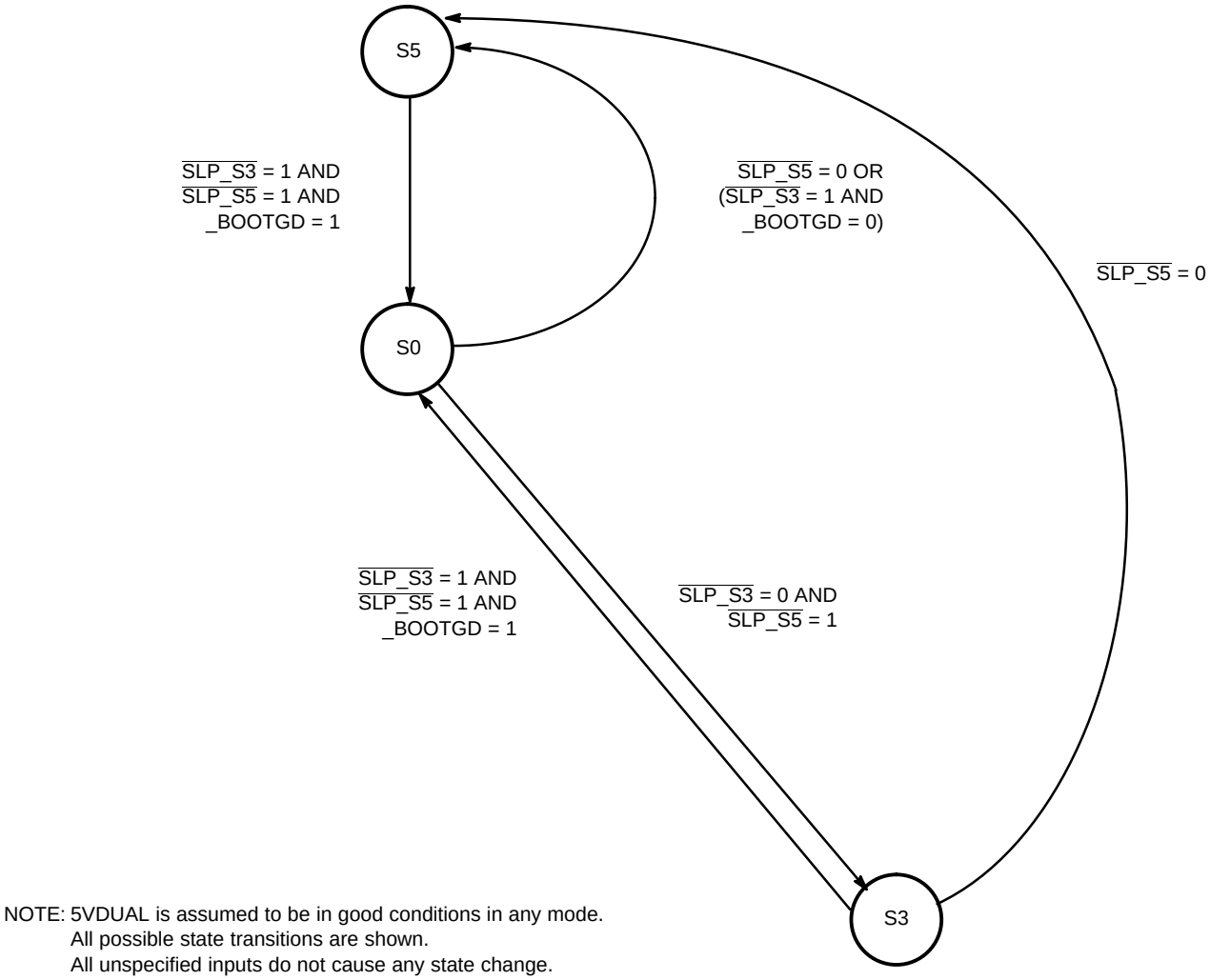
### Thermal Shutdown

When the junction temperature of the IC exceeds 145°C, the entire IC is shutdown. When the junction temperature drops below 120°C, the chip resumes normal operation.




2. 5VSTBY or 5VSTB is the ultimate chip enable, $\overline{\text{SLP\_S5}}$ and $\overline{\text{SLP\_S3}}$ go HIGH. This supply has to be up first to ensure gates are in known state.
3. 12 V supply ramp.
4. DDQ will ramp with the tracking of SS pin, timing is 1.2 * $C_{SS}$ / 4.0 μ (sec).
5. DDQ SS is completed, timing is 1.2 * $C_{SS}$ / 4.0 μ (sec), then SS pin is released from DDQ. SS pin is shorted to ground.
5. MCH ramps with the tracking of SS pin ramp, timing is 0.8 * $C_{SS}$ / 4.0 μ (sec). VTT start up with current limit and reaches VTT output voltage.
6. MCH SS is completed, then SS pin is released from MCH, SS pin is shorted to ground. S0 Mode.
7. S3 MODE −− $\overline{\text{SLP\_S3}}$ = L.
8. VTT and MCH will be turned off.
9. 12 V ramps to 0 V.
10. Standard S3 State.
11. $\overline{\text{SLP\_S3}}$ goes HIGH.
12. 12 V ramps back to regulation.
13. 12 V UVLO = L and $\overline{\text{SLP\_S3}}$ = H. MCH ramps with SS pin, timing is 0.8 * $C_{SS}$ / 4.0 μ (sec) SS rises in timing 1.2 * $C_{SS}$ / 4.0 μ (sec). VTT rises.
14. S0 Mode.
15. S5 Mode −− $\overline{\text{SLP\_S5}}$ = L.
16. DDQ, VTT and MCH Turned OFF.
17. S5 Mode.

**Figure 17. NCP5220A Power−Up and Power−Down**




NOTE: 5VDUAL is assumed to be in good conditions in any mode.
All possible state transitions are shown.
All unspecified inputs do not cause any state change.

**Figure 18. Transitions State Diagram of NCP5220A**

## APPLICATION INFORMATION

### Application Circuit

Figure 20 shows the typical application circuit for NCP5220A. The NCP5220A is specifically designed as a total power solution for the MCH and DDR memory system. This diagram contains NCP5220A for driving four external N−Ch FETs to form the DDR memory supply voltage (VDDQ) and the MCH regulator.

### Output Inductor Selection

The value of the output inductor is chosen by balancing ripple current with transient response capability. A value of 1.7 μH will yield about 3.0 A peak−peak ripple current when converting from 5.0 V to 2.5 V at 250 kHz. It is important that the rated inductor current is not exceeded during full load, and that the saturation current is not less than the expected peak current. Low ESR inductors may be required to minimize DC losses and temperature rise.

### Input Capacitor Selection

Input capacitors for PWM power supplies are required to provide a stable, low impedance source node for the buck regulator to convert from. The usual practice is to use a combination of electrolytic capacitors and multi−layer ceramic capacitors to provide bulk capacitance and high frequency noise suppression. It is important that the capacitors are rated to handle the AC ripple current at the input of the buck regulators, as well as the input voltage. In the NCP5220A the DDQ and MCH regulators are interleaved (out of phase by 180°) to reduce the peak AC input current.

### Output Capacitor Selection

Output capacitors are chosen by balancing the cost with the requirements for low output ripple voltage and transient voltage. Low ESR electrolytic capacitors can be effective at reducing ripple voltage at 250 kHz. Low ESR ceramic capacitors are most effective at reducing output voltage excursions caused by fast load steps of system memory and the memory controller.

### Power MOSFET Selection

Power MOSFETs are chosen by balancing the cost with the requirements for the current load of the memory system and the efficiency of the converter provided. The selections criteria can be based on drain−source voltage, drain current, on−resistance $R_{DS(on)}$ and input gate capacitance. Low $R_{DS(on)}$ and high drain current power MOSFETs are usually preferred to achieve the high current requirement of the DDR memory system and MCH, as well as the high efficiency of the converter. The tradeoff is a corresponding increase in the input gate capacitor of the power MOSFETs.

### PCB Layout Considerations

With careful PCB layout the NCP5220A can supply 20 A or more of current. It is very important to use wide traces or large copper shapes to carry current from the input node through the MOSFET switches, inductor and to the output filters and load. Reducing the length of high current nodes will reduce losses and reduce parasitic inductance. It is usually best to locate the input capacitors the MOSFET switches and the output inductor in close proximity to reduce DC losses, parasitic inductance losses and radiated EMI.

The sensitive voltage feedback and compensation networks should be placed near the NCP5220A and away from the switch nodes and other noisy circuit elements. Placing compensation components near each other will minimize the loop area and further reduce noise susceptibility.

### Optional Boost Voltage Configuration

The charge pump circuit in Figure 19 can be used instead of boost voltage scheme of Figure 20. The advantage in Figure 19 is the elimination of the requirement for the Zener clamp.

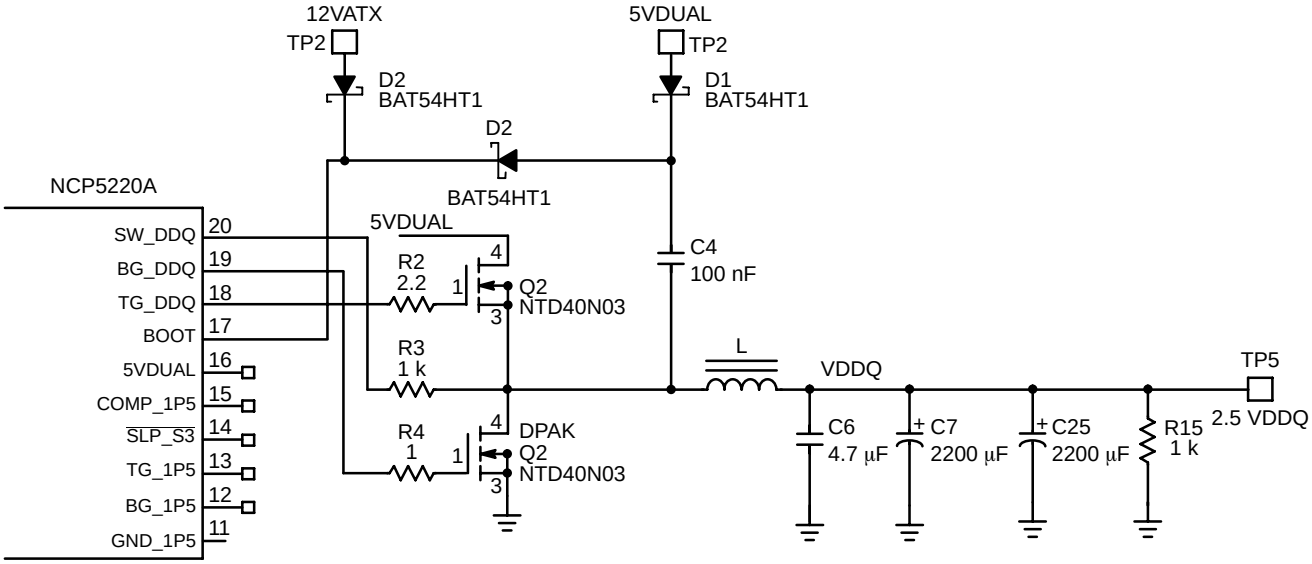



**Figure 19. Charge Pump Circuit at BOOT Pin**

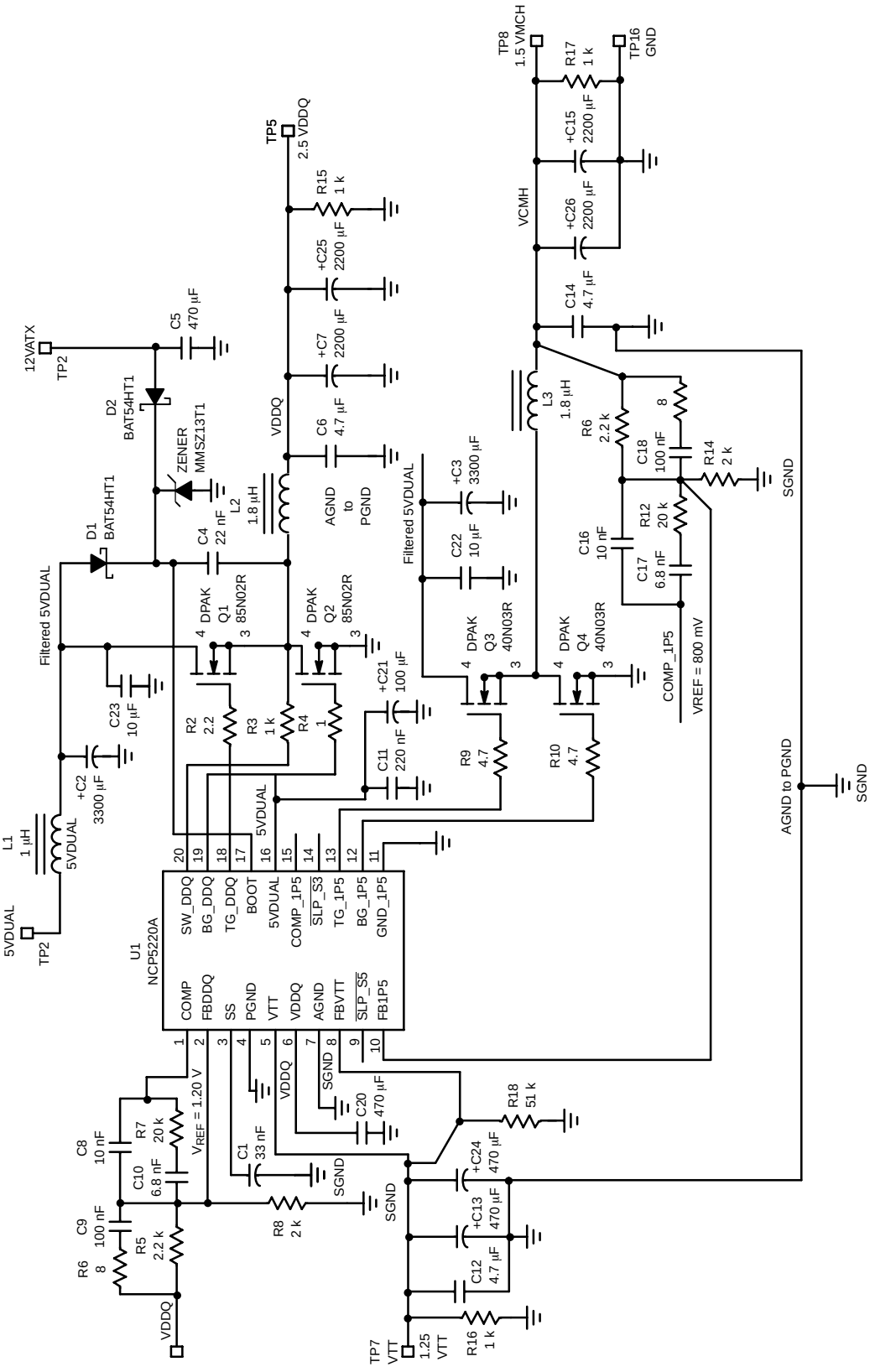



**Figure 20. NCP5220A Typical Application Circuit**

**Table 2. Bill of Material of NCP5220A Application Circuit**

| Reference Design | Description | Value | Qty | Part Number | Manufacturer |
|---|---|---|---|---|---|
| Q1, Q2 | Power MOSFET N−Channel | 24 V, 4.8 mΩ, 85 A | 2 | NTD85N02R | ON Semiconductor |
| Q3, Q4 | Power MOSFET N−Channel | 25 V, 12.6 mΩ, 40 A | 2 | NTD40N03R | ON Semiconductor |
| D1, D2 | Rectifier Schottky Diode | 30 V | 2 | BAT54HT1 | ON Semiconductor |
| U1 | Controller | 3−in−1 PWM Dual Buck and Linear Power Controller | 1 | NCP5220A | ON Semiconductor |
| Zener | Zener Diode | 13 V, 0.5 W | 1 | MMSZ13T1 | ON Semiconductor |
| L1 | Toroidal Choke | 1.0 μH, 25 A | 1 | T60−26(6T) | |
| L2, L3 | Toroidal Choke | 1.8 μH, 25 A | 2 | T50−26B(6T) | |
| C2, C3 | Aluminum Electrolytic Capacitor | 3300 μF, 6.3 V | 2 | EEUFJ0J332U | Panasonic |
| C5 | Aluminum Electrolytic Capacitor | 470 μF, 35 V | 1 | EEUFC1V471 | Panasonic |
| C21 | Aluminum Electrolytic Capacitor | 100 μF, 50 V | 1 | EEUFC1H101 | Panasonic |
| C20 | Aluminum Electrolytic Capacitor | 470 μF, 16 V | 1 | EEUFC1C471 | Panasonic |
| C13, C24 | Aluminum Electrolytic Capacitor | 470 μF, 10 V | 2 | EEUFC1A471 | Panasonic |
| C7, C25, C15, C26 | Aluminum Electrolytic Capacitor | 2200 μF, 6.3 V | 4 | EEUFC0J222S(H) | Panasonic |
| C11 | Ceramic Capacitor | 220 nF, 10 V | 1 | ECJ1VB1A224K | Panasonic |
| C6, C12, C14 | Ceramic Capacitor | 4.7 μF, 6.3 V | 3 | ECJHVB0J475M | Panasonic |
| C22, C23 | Ceramic Capacitor | 10 μF, 25 V | 2 | ECJ4YB1E106M | Panasonic |
| C4 | Ceramic Capacitor | 22 nF, 25 V | 1 | ECJ1VB1E223K | Panasonic |
| C10, C17 | Ceramic Capacitor | 6.8 nF, 50 V | 2 | ECJ1VB1H682K | Panasonic |
| C9, C18 | Ceramic Capacitor | 100 nF, 16 V | 2 | ECJ1VB1C104K | Panasonic |
| C8, C16 | Ceramic Capacitor | 10 nF, 50 V | 2 | ECJ1VB1H103K | Panasonic |
| C1 | Ceramic Capacitor | 33 nF, 25 V | 1 | ECJ1VB1E333K | Panasonic |
| R2 | Resistor | 2.2 Ω | 1 | | |
| R4 | Resistor | 1.0 Ω | 1 | | |
| R9, R10 | Resistor | 4.7 Ω | 2 | | |
| R3, R15, R16, R17 | Resistor | 1.0 kΩ | 4 | | |
| R7, R12 | Resistor | 20 kΩ | 2 | | |
| R6, R13 | Resistor | 8.2 Ω | 2 | | |
| R8, R14 | Resistor | 2.0 kΩ | 2 | | |
| R5, R11 | Resistor | 2.2 kΩ | 2 | | |
| R18 | Resistor | 51 kΩ | 1 | | |

## PACKAGE DIMENSIONS

**DFN−20**
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CASE 505AB−01
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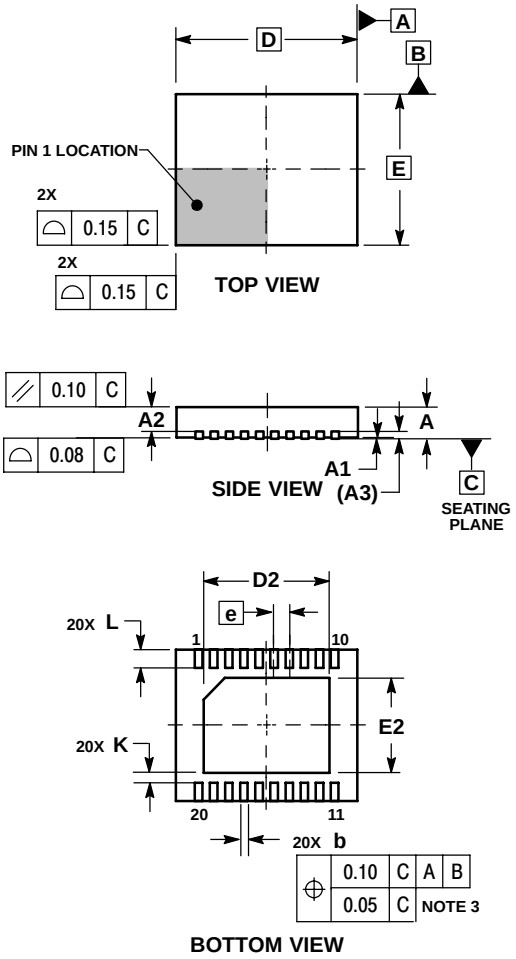


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A2 | 0.65 | 0.75 |
| A3 | 0.20 REF | |
| b | 0.23 | 0.28 |
| D | 6.00 BSC | |
| D2 | 3.98 | 4.28 |
| E | 5.00 BSC | |
| E2 | 2.98 | 3.28 |
| e | 0.50 BSC | |
| K | 0.20 | −−− |
| L | 0.50 | 0.60 |



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