NCP5203

2-in-1 DDR Power Controller

The NCP5203 2−in−1 DDR Power Controller is a complete power solution for an ACPI compliant high current DDR memory system. This IC combines the efficiency of a PWM controller for the VDDQ supply with the simplicity of linear regulator for the VTT termination voltage. The NCP5203 contains a synchronous PWM buck controller for driving two external NFETs to form the DDR memory supply voltage (VDDQ). The ±2.0 A user adjustable VTT terminator regulator has short circuit protection. An internal power good function monitors both the VDDQ and VTT outputs and signals if a fault occurs. Protective features include soft−start, undervoltage monitoring of 5VDUAL, over protection current (OCP), and thermal shutdown. The IC is packaged in 18−lead QFN.

Features

- Supports DDR I and DDR II
- Incorporates VDDQ, VTT Regulators
- Operates from Single 5 V Supply
- VTT Regulator includes Integrated Power FETs Sourcing/Sinking up to 2.0 A
- All External Power MOSFETs are N−Channel
- Adjustable VDDQ
- Adjustable VTT
- Fixed Switching Frequency of 300 kHz for VDDQ in S0
- Fixed Switching Frequency of 600 kHz for VDDQ in S3
- Soft−Start Protection for VDDQ
- Undervoltage Monitor of 5VDUAL
- Short−Circuit Protection for VDDQ and VTT
- Thermal Shutdown
- Housed in QFN−18
- Pb−Free Package is Available*

Typical Applications

- DDR Memory Supply and Termination Voltage
- Active Termination Busses (SSTL−2, SSTL−3)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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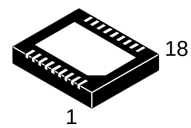
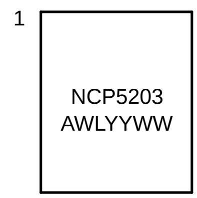
MARKING DIAGRAM

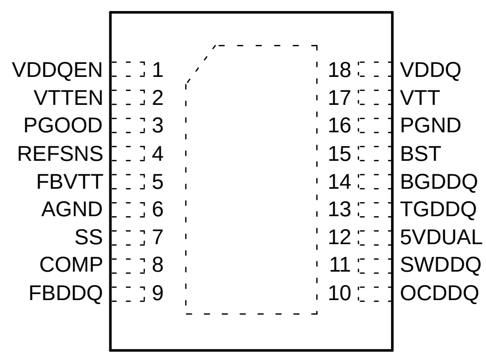


18−LEAD QFN, 5 x 6 mm
MN SUFFIX
CASE 505



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP5203MNR2	QFN	2500 Tape & Reel
NCP5203MNR2G	QFN (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

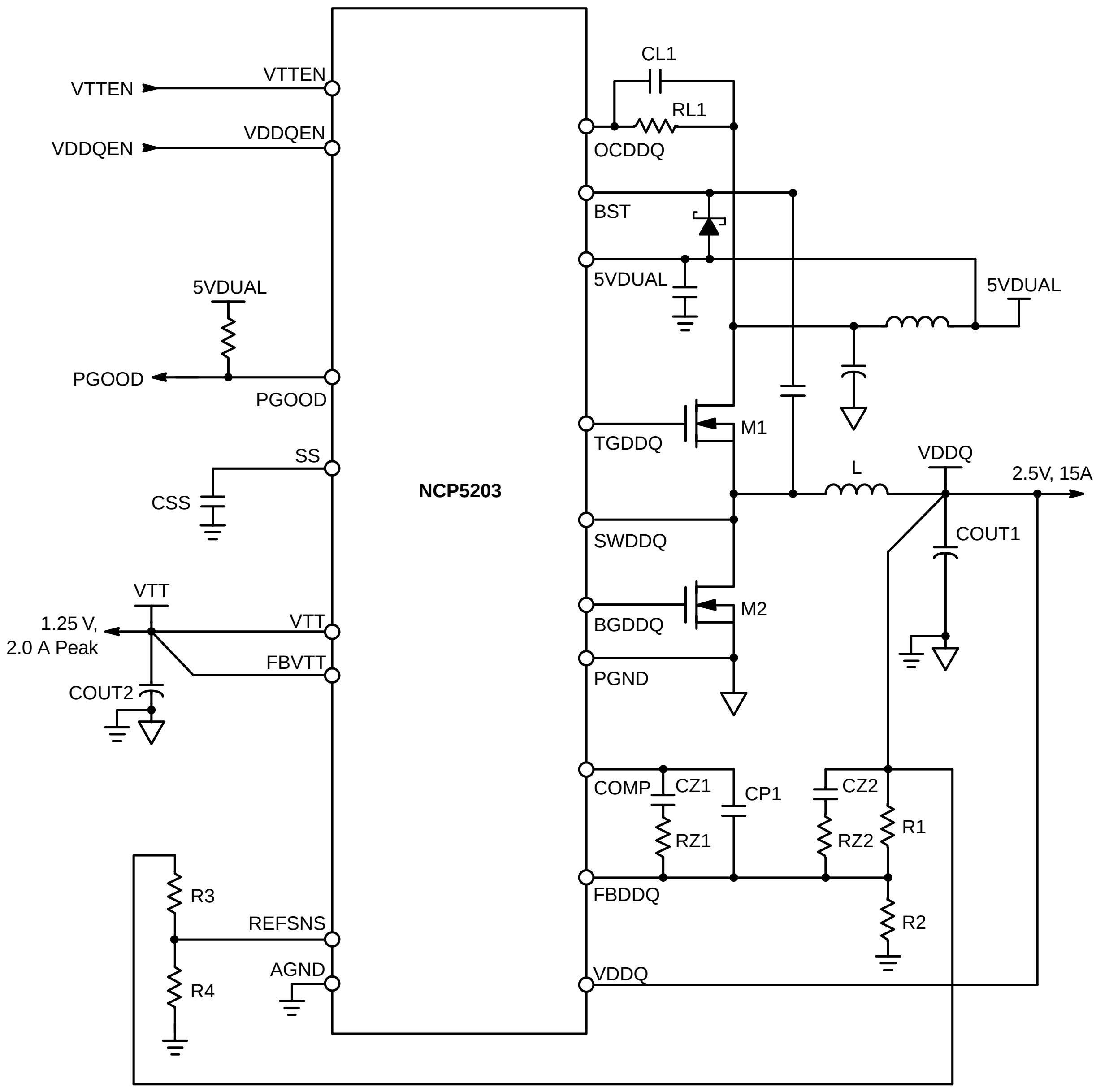


Figure 1. Typical Application Diagram

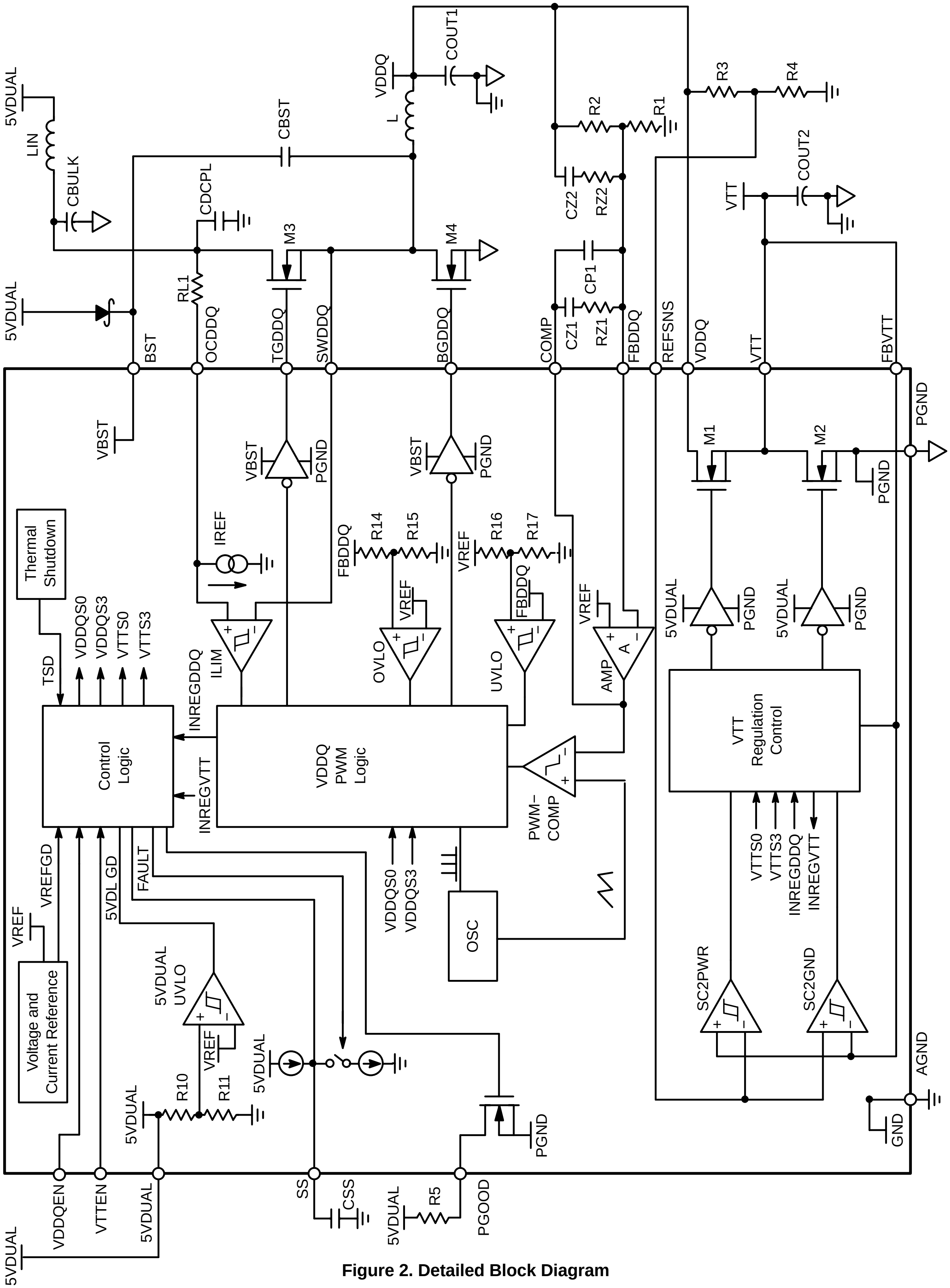


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	VDDQEN	VDDQ regulator enable input. Active high.
2	VTTEN	VTT regulator enable input. Active high.
3	PGOOD	Power good signal open−drain output.
4	REFSNS	Reference voltage input of VTT regulator.
5	FBVTT	VTT regulator feedback pin for closed loop regulation.
6	AGND	Analog ground connection and remote ground sense.
7	SS	Soft−start capacitor connection to ground.
8	COMP	VDDQ error amplifier compensation node.
9	FBDDQ	VDDQ regulator feedback pin for closed loop regulation.
10	OCDDQ	Overcurrent sense and program input for the high−side FET of VDDQ regulator.
11	SWDDQ	VDDQ regulator inductor driven node and current limit sense input.
12	5VDUAL	5VDUAL supply input.
13	TGDDQ	Gate driver output for DDQ regulator high−side N−Channel power FET.
14	BGDDQ	Gate driver output for DDQ regulator low−side N−Channel power FET.
15	BST	Supply input of VDDQ regulator and 5 V boost capacitor connection.
16	PGND	Power ground.
17	VTT	VTT regulator output.
18	VDDQ	Power input for VTT regulator.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 12, 18)	5VDUAL	−0.3, 6.5	V
Gate Drive Supply/Output Voltage (Pin 13, 14, 15)	VBST, Vg	−0.3, 14	V
Switch DDQ (Pin 11)	SWDDQ	−1.0, 5VDUAL	V
Input/Output Pins (Pin 1, 2, 7; 4, 5, 17; 3, 8, 9, 10)	V_{IO}	−0.3, 6.5	V
Thermal Characteristics QFN−18 Plastic Package Thermal Resistance Junction−to−Ambient	$R_{\theta JA}$	35	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	2.0	−
Electro Static Discharge (ESD) Human Body Model Machine Model	HBM MM	2.0 200	kV V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. All voltages are with respect to AGND (Pin 6) and PGND (Pin 16).

ELECTRICAL CHARACTERISTICS (5VDUAL = 5.0 V, T_A = 0 to 70°C)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Supply Voltage					
5VDUAL Operating Voltage	−	4.5	5.0	5.5	V
BST Operating Voltage	−	4.0	10	13.2	V
Supply Current					
Quiescent Supply Current (5VDUAL)	−	−	5.0	10	mA
Shutdown Current	VDDQEN = 0 V, VTTEN = 0 V	−	−	1.0	mA
Undervoltage Monitor					
5VDUAL UVLO Lower Threshold	Falling Edge	3.6	3.95	4.3	V
5VDUAL UVLO Hysteresis	−	−	0.2	−	V
Thermal Shutdown					
Thermal Trip Point	(Note 2)	−	150	−	°C
VDDQ Switching Regulator					
FBDDQ Feedback Voltage, Control Loop in Regulation	T_A = 0 to 70°C T_A = 25°C	1.225 1.232	1.25 1.25	1.275 1.268	V
Feedback Input Current	VFBDDQ = 1.25 V	−	−	1.0	μA
Oscillator Frequency in S0 Mode	VDDQEN = VTTEN = 5 V	262.5	300	337.5	kHz
Oscillator Frequency in S3 Mode	VDDQEN = 5 V, VTTEN = 0 V	500	600	700	kHz
Ramp−Amplitude Voltage	At Max Duty Cycle	−	1.25	−	V
OCDDQ Pin Current Sink	VOCDDQ = 4.0 V, T_A = 25°C	23	35	47	μA
OCDDQ Pin Current Sink Temperature Coefficient	(Note 2)	−	3200	−	ppm/°C
Minimum Duty Cycle	−	0	−	−	%
Maximum Duty Cycle	−	−	90	−	%
Soft−start Current	DDQEN = 5.0 V; V_{SS} = 0 V	3.5	5.0	6.5	μA
Overvoltage Trip Threshold	With respect to Error Comparator Threshold	115	130	−	%
Undervoltage Trip Threshold	With respect to Error Comparator Threshold	−	65	75	%
Error Amplifier					
DC Gain	(Note 2)	−	70	−	dB
Unity Gain Bandwidth	COMP_GND = 220 nF, 1.0 Ω in series (Note 2)	−	2.0	−	MHz
Slew Rate	COMP_GND = 10 pF (Note 2)	−	8.0	−	V/μS
Gate Drivers					
TGDDQ Gate Pull−HIGH Resistance	I_{OUT} = 400 mA, VBST = 10 V	−	3.5	−	Ω
TGDDQ Gate Pull−LOW Resistance	I_{OUT} = 400 mA, VBST = 10 V	−	2.5	−	Ω
BGDDQ Gate Pull−HIGH Resistance	I_{OUT} = 400 mA, VBST = 10 V	−	3.5	−	Ω
BGDDQ Gate Pull−LOW Resistance	I_{OUT} = 400 mA, VBST = 10 V	−	1.3	−	Ω

2. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued) (5VDUAL = 5.0 V, T_A = 0 to 70°C)

Characteristic	Test Conditions	Min	Typ	Max	Unit
VTT Active Terminator					
VTT with Respect to REFSNS	REFSNS – VTT, IOUT = 0 to 2.0 A (Sink Current) IOUT = 0 to –2.0 A (Source Current)	 −30 −	 − −	 − 30	mV
Source Current Limit	−	−	−2.5	−2.05	A
Sink Current Limit	−	2.05	2.75	−	A
Control Section					
VDDQEN Pin Threshold High	−	1.4	−	−	V
VDDQEN Pin Threshold Low	−	−	−	0.5	V
VDDQEN Pin Input Current	VDDQEN = 5 V	−	5.0	−	μA
VTTEN Pin Threshold High	−	1.4	−	−	V
VTTEN Pin Threshold Low	−	−	−	0.5	V
VTTEN Pin Input Current	VDDQEN = VTTEN = 5 V	−	5.0	−	μA
PGOOD Pin ON Resistance	I_PGOOD = 5.0 mA	−	80	−	Ω
PGOOD Pin OFF Current	−	−	−	1.0	μA

DETAILED OPERATING DESCRIPTION

General

The NCP5203 2−in−1 DDR Power Controller combines the efficiency of a VDDQ PWM controller with the simplicity of a linear regulator for VTT termination. Both VDDQ and VTT outputs can be user adjusted.

The inclusion of both VDDQ and VTT power good voltage monitors, soft−start, VDDQ overvoltage and undervoltage detection, supply undervoltage monitors, and thermal shutdown, makes this device a total power solution for high current DDR memory systems.

VDDQ Switching Regulator in Normal (S0) Mode

The VDDQ regulator is a switching synchronous rectification buck controller directly driving two external N−Channel power FETs. An external resistor divider sets the nominal output voltage. The control architecture is voltage mode fixed frequency PWM (300 kHz ± 12.5%) with external compensation. The VDDQ output voltage is divided down and fed back to the inverting input of an internal amplifier through the FBDDQ pin to close the loop at VDDQ = VFBDDQ × (1 + R2/R1). This amplifier compares the feedback voltage with an internal VREF1 (= 1.25 V) to generate an error signal for the PWM comparator. This error signal is further compared with a fixed frequency Ramp waveform derived from the internal oscillator to generate a pulse−width−modulated signal. This PWM signal drives the external N−Channel Power FETs via the TGDDQ and BGDDQ pins. External inductor L and capacitor COUT1 filter the output. The VDDQ output voltage ramps up at a pre−defined soft−start rate each time the IC exits S5. When in normal mode, and regulation of VDDQ is detected, signal INREGDDQ will go high to notify the control logic block.

For enhanced efficiency, an active synchronous switch is used to eliminate the conduction loss contributed by the forward voltage of a diode or Schottky diode rectifier. Adaptive non−overlap timing control of the complementary gate drive output signals is provided to reduce shoot−through current.

Tolerance of VDDQ

The tolerance of VFBDDQ and the ratio of the external resistor divider R2/R1 both impact the precision of VDDQ. When the control loop is in regulation, VDDQ = VFBDDQ × (1 + R2/R1). With a worst case (overtemperature) VFBDDQ tolerance of ±2%, a worst case range of 2.5% for VDDQ will be assured if the ratio R2/R1 is specified as 0.98985 ±1%.

Table 1. State, Operation, Input and Output Condition Table

	USER INPUTS			OPERATING CONDITIONS		OUTPUT CONDITIONS		
MODE	5VDUAL UVLO	VDDQEN	VTTEN	VDDQ	VTT	TGDDQ	BGDDQ	PGOOD
S5	Low	X	X	H−Z	H−Z	Low	Low	Low
S0	High	High	High	Normal	Normal	Normal (300 kHz)	Normal (300 kHz)	H−Z
S3	High	High	Low	Standby	H−Z	Normal (600 kHz)	Low	Low
S5	High	Low	X	H−Z	H−Z	Low	Low	Low

VDDQ Regulator in Standby Mode (S3)

During S3, the VDDQ regulator operates in asynchronous switch mode. The switching frequency is increased to 600 kHz, the low−side FET is disabled, and the body diode of the low side FET is used. The regulator will operate in discontinuous conduction mode (DCM) and the switching frequency is doubled to reduce peak conduction current.

VDDQ Regulator Fault Protection

During S0 and S3, the external resistor (RL1) sets the current limit for the high−side switch. An internal 35 μA current sink at OCDDQ pin establishes a voltage drop across this resistor. This voltage is compared to the voltage at SWDDQ pin when the TGDDQ is high after a fixed blanking period of 500 ns to avoid false current limit triggering. When the voltage at SWDDQ is lower than OCDDQ, an overcurrent condition occurs, upon which all outputs will be latched off to protect against a short−to−ground condition on SWDDQ or VDDQ. The IC will be reset once 5VDUAL or VDDQEN is cycled.

VDDQ Regulator Feedback Compensation

The recommended compensation network is shown in Figure 2.

VTT Active Terminator in Normal Mode (S0)

The VTT active terminator is a two−quadrant linear regulator with two internal N−channel power FETs to provide transient current sink and source capability up to 2.0 A. It is activated in normal mode in S0 when the VTTEN pin is high and VDDQ is in regulation. When in the S0 state and VTT is in regulation, signal INREGVTT will go high to notify the control logic block. The VTT regulator is powered from VDDQ with the internal FET's gate drive power derived from 5VDUAL. The VTT output voltage can be adjusted by using an external resistor divider connected to the REFSNS pin. This regulator is stable with any value of output capacitor greater than 470 μF, and is insensitive to ESR ranging from 2.0 mΩ to 400 mΩ.

VTT Active Terminator in Normal Mode (S3)

VTT output is high−impedance in S3 mode.

VTT Active Terminator Fault Protection

To provide protection for the internal FETs, bi−directional current limit is implemented, preset at 2.4 A magnitude. This current limit is also used as constant current source during VTT startup.

VTT Active Terminator Thermal Consideration

The VTT terminator is designed to handle large transient output currents. If large currents are required for very long duration, then care should be taken to ensure the maximum junction temperature is not exceed. The 5x6 QFN−18 has a thermal resistance of 35°C/W (dependent on air flow, grade of copper, and number of vias). In order to take full advantage of this thermal capability, the thermal pad underneath must be soldered directly to a PCB metal substrate.

Supply Voltages Undervoltage Monitor

The IC continuously monitors 5VDUAL through the 5VDUAL pin. 5VDLGD is set high if 5VDUAL is higher than its preset threshold (derived from VREF with hysteresis). The IC will later latch off if 5VDUAL is in S0 providing both VDDQEN and VTTEN remain high.

Thermal Shutdown

If the chip junction temperature exceeds 150°C, the entire IC will shutdown. The IC resumes normal operation only after 5VDUAL or VDDQEN is cycled.

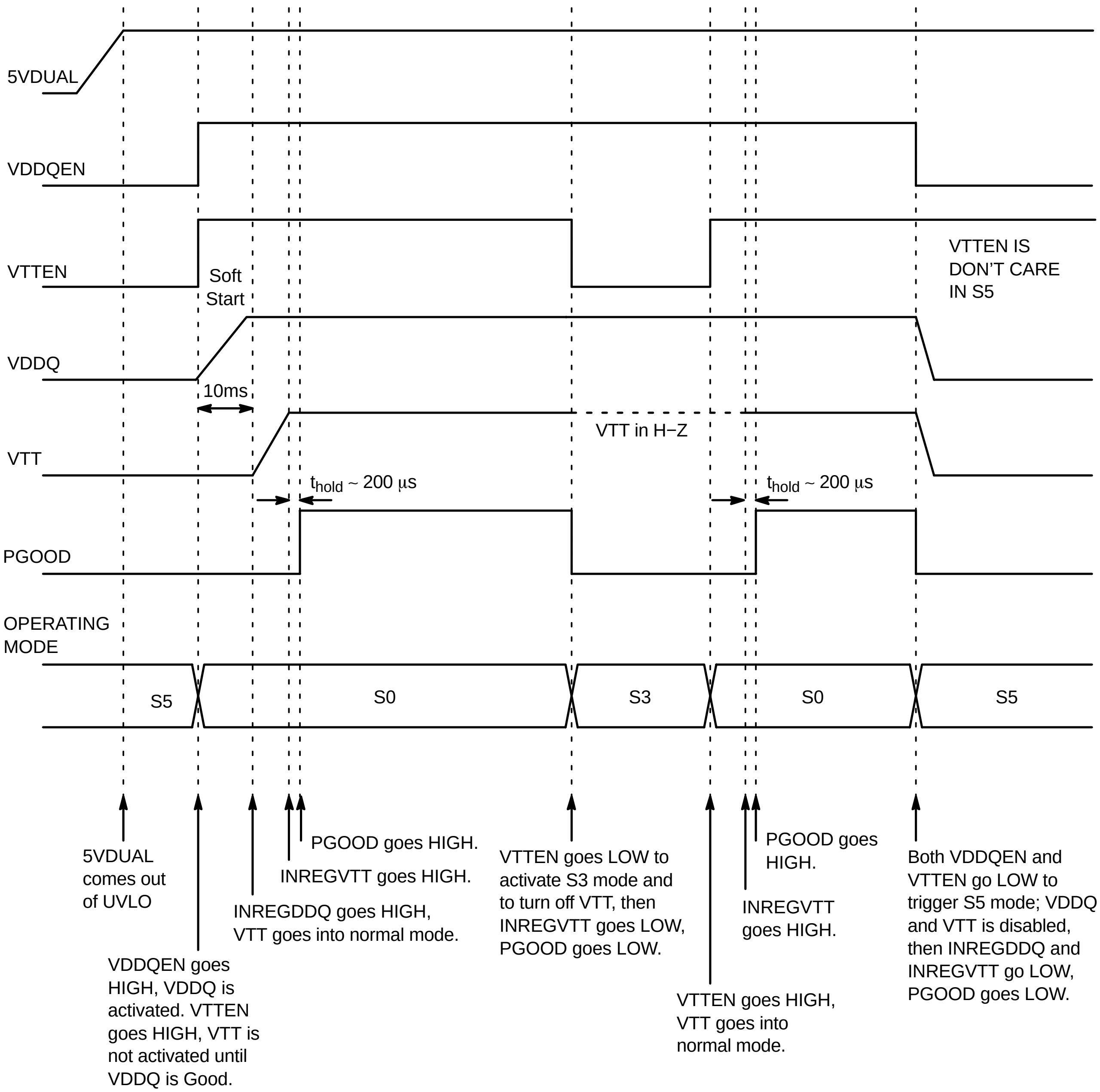
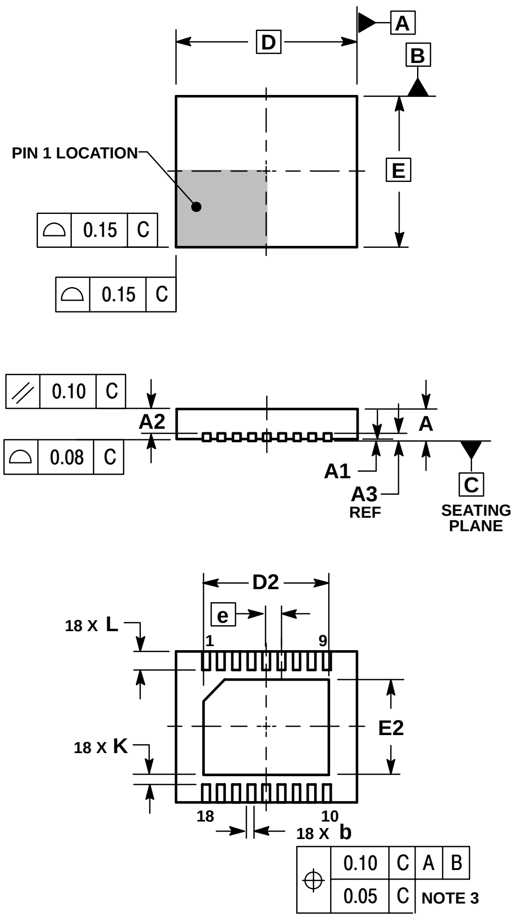


Figure 3. Powerup and Powerdown Timing Diagram

18−LEAD QFN, 5 x 6 mm
MN SUFFIX
CASE 505−01
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.65	0.75
A3	0.20 REF	
b	0.23	0.28
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	−−−
L	0.50	0.60

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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