NCP5372

Specification Document

Revision 0.3
Mar 19th, 2008

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ON Semiconductor

Abstract
This document contains the technical specifications for an IMVP-6.5 compliant power controller.

Revision History

Rev	Description	Date
0.0	Initial specification	6/21/2007
0.1	1. Detailed block diagram: changed IMON gain from 2 to 4 (follow Paul's suggestion). 2. Electrical table, a. IMON section: 1. changed IMON Amp Gain from 1.99 min, 2 typ, 2.01 max to 3.98 min, 4 typ, 4.02 max. 2. changed the Gaindrp and GainIMON in the IMON output test condition from 1.6 and 2 to 0.8 and 4. b. PWRGD and Protection Monitor section: 1. added "Note" to the test condition of Tpwrdown1 to indicate guaranteed by design. 2. added "Note" to the test condition of Tpwrdown2 to indicate guaranteed by design. 3. Operating Description section, Operation Mode table: under the condition of MODE=0, DPRSLPVR=0, & PSI=0; changed operation mode from "Forced CCM" to "allow DCM at light load" with FCCM cycles at transition to meet Intel's efficiency requirement of IMVP-6.5 spec.	7/25/2007
0.2	1. VDROOP AMPLIFIER section in Electrical table, a. Added Input Offset Voltage parameters: -1.5mV min, +1.5mV max b. Deleted CS1 to Voltage of DRPGain. c. Deleted CD2 to Voltage of DRPGain. 2. Added a new CSSUM AMPLIFIER section in Electrical table with the following parameter: a. Current Sense Input to CSSUM Gain: -6.06V/V min, -6.0V/V typ, -5.94V/V max b. -3dB Bandwidth: 20MHz typ c. Slew Rate: ± 2.0 V/µs typ d. CSSUM Output Offset Voltage: -6mV min, 6mV max e. Maximum CSSUM Output Voltage: 3.0V min f. Minimum CSSUM Output Voltage: 0.3V max g. Source Current: 1.0mA min h. Sink Current: 4.0mA min i. CS Amp Common Mode Input Voltage Range: -0.3V min, 2.0V max j. CS Amp Differential Mode Input Voltage Range: -120V min, 120mV max 3. IMON section in Electrical table, a. Added Input Offset Voltage parameters: -1.5mV min, 1.5mV max b. Added "reference to VS-" condition below the IMON Output Voltage. c. Added VIMONMIN parameter: 50mV max d. Added Maximum Clamp Voltage parameter: 1.15V max e. Changed IMON Amp. Gain parameters from 3.98V/V min & 4.02V/V max to 3.96V/V min & 4.04V/V max. f. Added -3dB Bandwidth: 20MHz typ g. Added Slew Rate: ± 0.5 V/µs typ 4. PWRGD and PROTECTION MONITOR section in Electrical table, Remove the "Note" to the test condition of the Tpwrdown1. 5. CLK_EN# section in Electrical table, a. Added a "Note" to the test condition of Delay from Vboot to indicate guaranteed by design. b. Changed Delay from Vboot parameters from 20ns min and 100ns max to 70ns typ. 6. Changed wording "0V Shutdown" to "Shutdown" in the State Diagram.	8/30/2007
0.3	1. CSSUM AMPLIFIER section in Electrical Characteristics table, Sink Current spec is changed from 4.0mA min to 1.0mA min with test condition changed from VCSSUM = 0.3V to VCSSUM = 1.2V. 2. Remote Sense Amplifier section in Electrical Characteristics table, Due to no test mode for measuring the parameters of the Remote Sense Amplifier, a "(Note)" is added to the test condition of the following items to denote guaranteed by design: Max Output Voltage Swing, Min Output Voltage Swing, Input Signal Range, -3dB Bandwidth, Source Current, Sink Current.	3/19/2008

Distribution

Group Function	Name(s)
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NCP5372

Product Specification

High Efficiency Two-Phase Step-Down Power Controller for IMVP-6.5 Mobile CPU Core Power Supplies

Description

This controller is specifically designed to support the INTEL notebook RS – IMVP-6.5 Mobile Processor power delivery requirements. The current mode variable frequency architecture provides ultra fast dynamic response with virtually no overshoot for dynamic loads and dynamic VID changes. The feed-forward on time control virtually eliminates the effects of input voltage variations. The gate drivers are optimized to drive large Qg low-side trench devices for maximum overall system efficiency.

Features

- Automatic Variable Frequency Operation for Light Load Power Savings
- 2-Phase Control
- 7-bit VID Input
- Differential Remote Die Voltage Sensing
- Active Voltage Positioning
- Differential Lossless Inductor current sensing
- Programmable Switching Frequency
- Under-Voltage Lockout
- Output Overvoltage Protection
- Output Undervoltage Protection
- Overcurrent Protection
- Programmable Soft-Start
- Power Good Indication
- Current Monitor Output with Adjustable Gain
- Drives Large Synchronous-Rectifier FETs
- Thermal Shutdown Protection

Application

- IMVP6.5 CPU Core Supply
- Notebook/Desktop Computers
- Voltage-Positioned Step-Down Converters

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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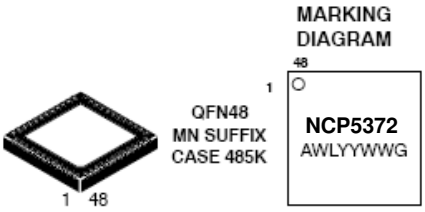
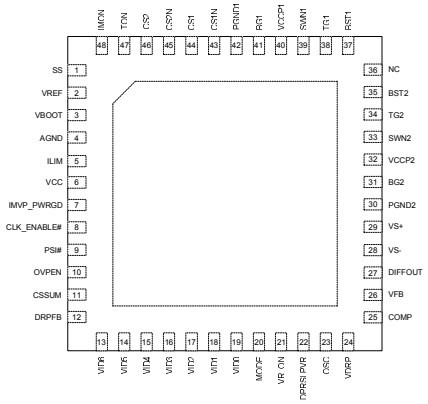
PACKAGE AND MARKING INFORMATION



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Device

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP5372MNR2G	QFN-48 7x7 (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

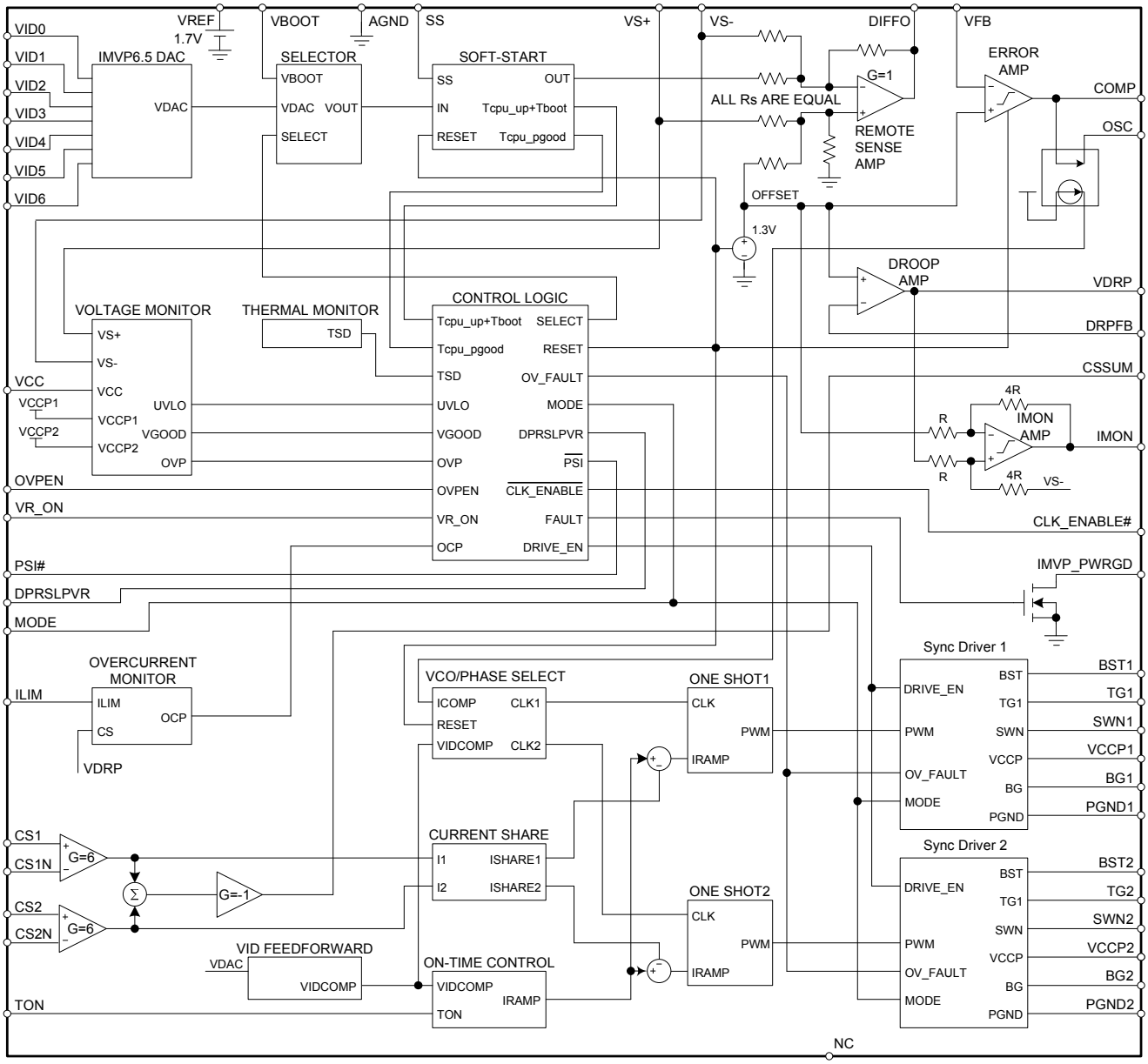


Figure 1. Detailed Block Diagram

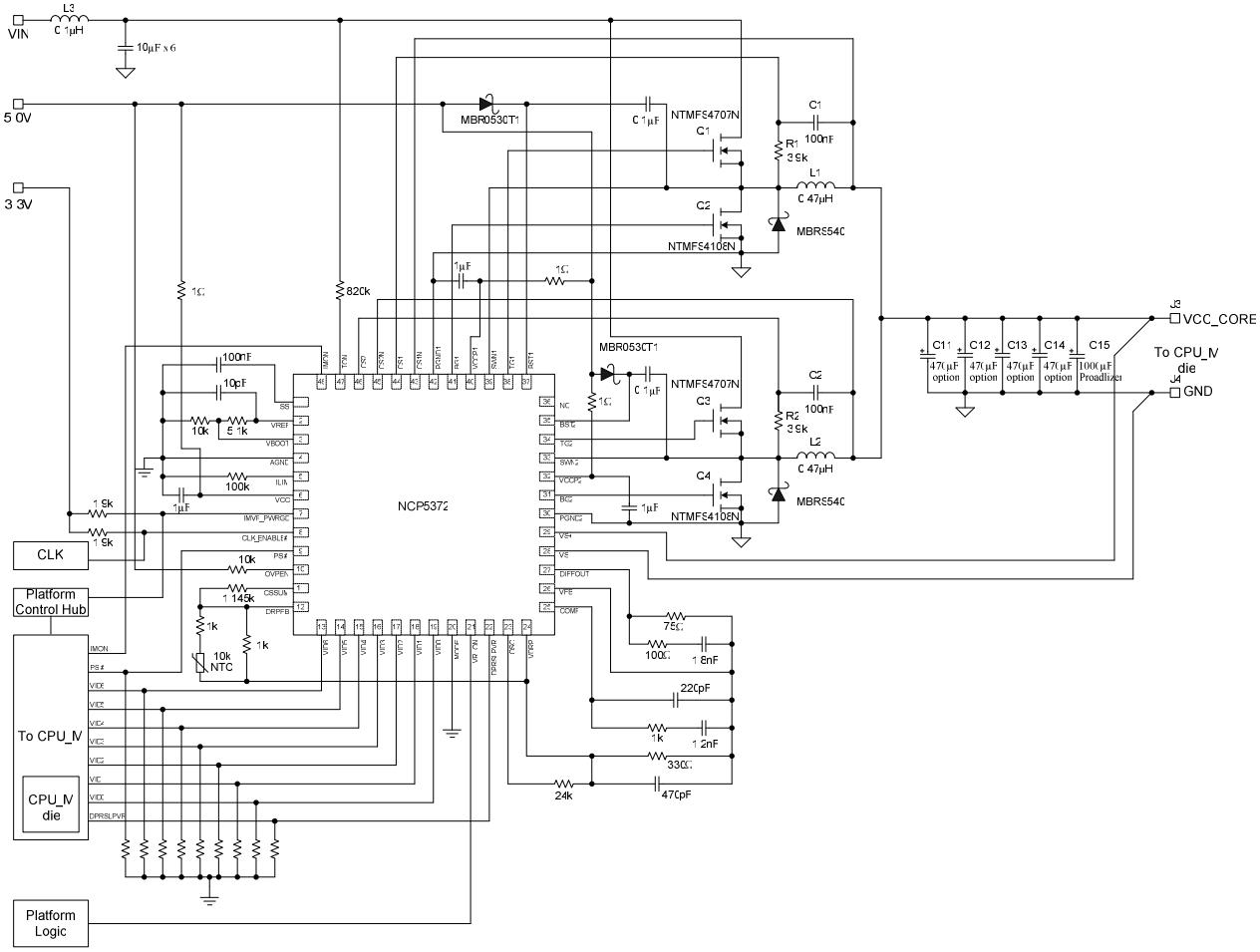


Figure 2. Typical Application Circuit

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VCC to PGND	V_{CC}	-0.3, 7.0	V
VCCP1, VCCP2 to PGND	V_{CCP}	-0.3, 7.0	V
TON to AGND	V_{TON}	-0.3, 30	V
BST1 to SWN1, BST2 to SWN2	V_{BST}-V_{SWN}	-0.3, 7.0	V
SWN1, SWN2 to PGND	V_{SWN}	-5.0(<100ns), -0.3(DC), 30	V
TG1 to SWN1, TG2 to SWN2	V_{TG}- V_{SWN}	-4.0(<100ns), -0.3(DC), 7.0	V
BG1 to PGND1, BG2 to PGND2	V_{BG}	-2.0(<100ns), -0.3(DC), 7.0	V
VS+, VS- to PGND	V_S	-0.3, 7.0	V
CS1, CS1N, CS2, CS2N to PGND	V_{CS}	-0.3, 7.0	V
VID0-VID6, MODE, VR_ON to PGND	V_{VID}	-0.3, 7.0	V
SS, IMVP_PWRGD, CLK_ENABLE#, IMON, DPRSLPVR, PSI#, OVPEN, OSC, VDRP, DRPFB, CSSUM, DIFFO, VFB, COMP to PGND	V_{IO}	-0.3, 7.0	V
PGND1, PGND2 to AGND	V_{GND}	-0.3, 0.3	V
VREF to PGND	V_{REF}	-0.3, 7.0	V
VBOOT to PGND	V_{BOOT}	-0.3, 7.0	V
ILIM to PGND	V_{ILIM}	-0.3, 7.0	V
THERMAL CHARACTERISTICS QFN-32 Thermal Resistance Junction-to-Ambient (Note 3)	$R_{\theta JA}$	35	°C/W
Operating Junction Temperature Range	T_J	0 to + 150	°C
Operating Ambient Temperature Range	T_A	-40 to + 85	°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Lead Temperature, Reflow (Soldering 10s)	-	260 Peak	°C
Moisture Sensitivity Level	MSL	1	-

1. This device series incorporates ESD protection and exceeds the following ratings:
   Human Body Model (HBM) ≤ 2.0 kV per JEDEC standard: JESD22–A114.
   Machine Model (MM) ≤ 200 V per JEDEC standard: JESD22–A115.
2. Latch–up Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78.
3. $R_{\theta JA}$ is measured in free air by mounting the device on a high effective thermal conductivity test board with direct thermal attachment mechanisms.

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	SS	Soft Start control pin with 40uA (typical) current pulling out
2	VREF	1.7V Reference for VBOOT
3	VBOOT	Boot Voltage Input
4	AGND	Analog ground connection and remote ground sense
5	ILIM	Current limit adjustment pin (pull to VCC to disable ILIM)
6	VCC	Power for the analog and control sections of the IC
7	IMVP_PWRGD	IMVP6.5 Power good signal open-drain output
8	CLK_ENABLE#	Clock Enable Signal open-drain output
9	PSI#	Power Status Indicator II low load input from CPU
10	OVPEN	Over Voltage Protection enable pin
11	CSSUM	Current sense summation output
12	DRPFB	Droop amplifier non-inverting input
13	VID6	DAC BIT
14	VID5	DAC BIT
15	VID4	DAC BIT
16	VID3	DAC BIT
17	VID2	DAC BIT
18	VID1	DAC BIT
19	VID0	DAC BIT
20	MODE	Mode selection pin. Pulls High to enable negative current detection and select Auto Power-saving, and pulls Low to allow DPRSLPVR and PSI# to control for power-saving.
21	VR_ON	Logic Input that enables, disables, and resets the controller
22	DPRSLPVR	Deeper Sleep Mode control signal input
23	OSC	Voltage control oscillator (VCO) gain control pin
24	VDRP	Total inductor current signal output for droop compensation
25	COMP	Error amplifier output for feedback compensation
26	VFB	Error amplifier inverting input for feedback compensation
27	DIFFOUT	Differential amplifier output
28	VS-	Output voltage remote ground sense
29	VS+	Output voltage remote sense
30	PGND2	Ground return for the high current in phase 2
31	BG2	Phase 2 bottom gate drive output
32	VCCP2	Phase 2 bottom gate driver power input
33	SWN2	Phase 2 top gate floating switch node return

34	TG2	Phase 2 top gate drive output
35	BST2	Phase 2 top gate driver power input
36	NC	No connection
37	BST1	Phase 1 top gate driver power input
38	TG1	Phase 1 top gate drive output
39	SWN1	Phase 1 top gate floating switch node return
40	VCCP1	Phase 1 bottom gate driver power input
41	BG1	Phase 1 bottom gate drive output
42	PGND1	Ground return for the high current in phase 1
43	CS1N	Negative differential current sense pin for phase 1
44	CS1	Positive differential current sense pin for phase 1
45	CS2N	Negative differential current sense pin for phase 2
46	CS2	Positive differential current sense pin for phase 2
47	TON	On time control pin (Provides VIN Feed Forward and Frequency Control)
48	IMON	Current Monitor output

Electrical Characteristics

(Circuit of Figure 2, VCC = VCCP1 = VCCP2 = 5.0V, V(V_{s+},V_{S-}) = VID(0011000) = 1.2V, T_A = -40 to 85°C, unless other noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
CONTROLLER						
Input Voltage Range	VBAT	Battery Voltage (Feedforward Voltage from VBAT to TON connected by a 1M Ω Resistor)	7	12	28	V
	VCC, VCCP1, VCCP2	-	4.5	5.0	5.5	V
DC Output Voltage Accuracy	V(VS+, VS-)	VID codes for 1.5V to 0.7625V, 52A Maximum Load	-	-	± 1.5	%
		VID codes for 0.75V to 0.5V, 52A Maximum Load	-	-	± 11.5	mV
		VID codes for 0.4875V to 0.3V, 3.0A Maximum Load	-	-	± 25	mV
VCC POWER SUPPLY						
Supply Current, Normal Operating	I_{VCC}	Fsw = 400kHz	-	10	20	mA
Supply Current, Shutdown	I_{VCC_SD}	-	-	10	40	µA
VCCP1 POWER SUPPLY						
Supply Current, Normal Operating	I_{VCCP1}	Fsw = 400kHz (3.3nF capacitor in BG)	-	10	-	mA
Supply Current, Shutdown	I_{VCCP1_SD}	-	-	10	20	µA
VCCP2 POWER SUPPLY						
Supply Current, Normal Operating	I_{VCCP2}	Fsw = 400kHz (3.3nF capacitor in BG)	-	10	-	mA
Supply Current, Shutdown	I_{VCCP2_SD}	-	-	10	20	µA
BST1 POWER SUPPLY						
Supply Current, Shutdown	I_{BST1_SD}	-	-	10	20	µA
BST2 POWER SUPPLY						
Supply Current, Shutdown	I_{BST2_SD}	-	-	10	20	µA
THERMAL SHUTDOWN						
Over Temperature Trip Point	TSD	-	-	150	-	°C
Hysteresis	TSD_{hys}	-	-	30	-	°C
Under-Voltage Lockout						
V_{CC} Start Threshold	VCC_{th}	-	4.05	4.25	4.48	V
Hysteresis	VCC_{hys}	-	-	275	-	mV
V_{CCP} Start Threshold	$VCCP_{th}$	-	4.05	4.25	4.48	V
Hysteresis	$VCCP_{hys}$	-	-	275	-	mV
VDAC OUTPUT						
Slew Rate	SRvs	-	8.75	-	-	mV/µs
SOFT-START						
SS Soft-start Current	I_{SS}	-	32	40	48	µA
VREF						
Output Voltage	VREF	-	-	1.7V	-	V
Tolerance	$VREF_{tol}$	No load	-	-	±1.0	%
Source Current	$IREF_{out}$	-	100	-	-	µA

* Note: Guaranteed by design

Electrical Characteristics

(Circuit of Figure 2, VCC = VCCP1 = VCCP2 = 5.0V, $V(V_{S+},V_{S-})$ = VID(0011000) = 1.2V, T_A = -40 to 85°C, unless other noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
NEGATIVE CURRENT DETECTION						
Trip Threshold (SWN to GND)	$NCUR_{th}$	-	-	-1	-	mV
Blanking Delay	$NCUR_{BDly}$	-	-	100	-	ns
HIGH SIDE DRIVE						
Non-Overlap Time, TG Going High	$tpdh_{TG}$	BG 90% to TG 10%	-	40	-	ns
Output Resistance (Sourcing)	RHS_{source}	Force 5.0V-0.4V to TG	-	1.0	4.0	Ω
Output Resistance (Sinking)	RHS_{sink}	Force 0.4V to TG	-	1.0	4.0	Ω
Upper Gate Drive Pull Down Resistor	RHS_{PD}	Force 0.4V to TG	-	60k	-	Ω
LOW SIDE DRIVE						
Non-Overlap time, LG Going High	$tpdh_{LG}$	TG 90% to BG 10%	-	25	-	ns
Output Resistance (Sourcing)	RLS_{source}	Force 5.0V-0.4V to BG	-	1	4	Ω
Output Resistance (Sinking)	RLS_{sink}	Force 0.4V to BG	-	0.4	2	Ω
Lower Gate Drive Pull Down Resistor	RLS_{PD}	Force 0.4V to BG	-	60 k	-	Ω
ERROR AMPLIFIER						
Input Offset Voltage	VOS_{EA}	(Note)	-1.5	-	1.5	mV
Output Voltage Swing	$VOSwing_{EA}$	-	1.0	-	3.0	V
Gain-Bandwidth Product	GBW_{EA}	Load = 100pF to GND	-	15	-	MHz
Phase Margin	PM_{EA}	Unity Gain with 100pF Load	-	40	-	deg
Gain	$Gain_{EA(open)}$	RL=10kΩ to GND, inputs at 1.0V	-	81	-	dB
Slew Rate	SR_{EA}	Capacitive Load of 100pF, ± 100mV Steps	-	±2.0	-	V/µs
Source Current	$Isource_{EA}$	COMP = 3.0V,	2.0	4.0	-	mA
Sink Current	$Isink_{EA}$	COMP = 3.0V,	2.0	4.0	-	mA
REMOTE SENSE AMPLIFIER						
Input Offset Voltage	VOS_{RSA}	(Note)	-1.5	-	1.5	mV
V(VS+, VS-) to DIFFOUT Gain	$Gain_{RSA}$	-	0.99	1	1.01	V/V
Max Output Voltage Swing	$VOSwingmax_{RSA}$	VS+ = 3V, Max RSA voltage, (Note)	3.0	-	-	V
Min Output Voltage Swing	$VOSwingmin_{RSA}$	VS+ = 0.1V, Min RSA voltage, (Note)	-	-	0.4	V
VS+ and VS- Input Signal Range	VIN_{RSA}	(Note)	0.1	-	3.0	V
-3dB Bandwidth	BW_{RSA}	(Note)	-	20	-	MHz
Source Current	$Isource_{RSA}$	(Note)	3.0	5.0	-	mA
Sink Current	$Isink_{RSA}$	(Note)	1.0	1.5	-	mA

* Note: Guaranteed by design

Electrical Characteristics

(Circuit of Figure 2, VCC = VCCP1 = VCCP2 = 5.0V, V(V_{s+},V_{S-}) = VID(0011000) = 1.2V, T_A = -40 to 85°C, unless other noted.)

Characteristic	Symbol	Test Conditions/ Notes	Min	Typ	Max	Unit
VDROOP AMPLIFIER						
Input Offset Voltage	VOS_{DRP}	(Note)	-1.5	-	1.5	mV
Max Output Voltage Swing	$VOmax_{Drp}$	(Note)	3.0	-	-	V
Min Output Voltage Swing	$VOmin_{Drp}$	(Note)	-	-	1.0	V
Gain-Bandwidth Product	GBW_{Drp}	Load = 100pF to GND	-	15	-	MHz
Phase Margin	PM_{Drp}	Unity Gain	-	40	-	deg
Gain	$Gain_{Drp(open)}$	RL=10kΩ to GND	-	81	-	dB
Slew Rate	SR_{Drp}	Capacitive Load of 100pF, ± 100mV Steps	-	±2.0	-	V/µs
Source Current	$Isource_{Drp}$	V_{RDOOP} = 3.0V, 0.2V of overdrive	1.0	4.0	-	mA
Sink Current	$Isink_{Drp}$	V_{RDOOP} = 1.2V, 0.2V of overdrive	1.0	4.0	-	mA
CSSUM AMPLIFIER						
Current Sense Input to CSSUM Gain	$Gain_{CSxCSSUM}$	0V < CSx-CSxN ≤ 0.1V	-6.06	-6.0	-5.94	V/V
-3dB Bandwidth	BW_{CSSUM}	(Note)	-	20	-	MHz
Slew Rate	SR_{CSSUM}	(Note)	-	±2.0	-	V/µs
CSSUM Output Offset Voltage	VOS_{CSSUM}	(Note)	-6.0	-	6.0	mV
Maximum CSSUM Output Voltage	$V_{MAXCSSUM}$		3.0	-	-	V
Minimum CSSUM Output Voltage	$V_{MINCSSUM}$		-	-	0.3	V
Source Current	$Isource_{CSSUM}$	VCSSUM = 3.0V	1.0	-	-	mA
Sink Current	$Isink_{CSSUM}$	VCSSUM = 1.2V	1.0	-	-	mA
Current Sense Amplifiers Common Mode Input Voltage Range	VIN_{CSCM}		-0.3	-	2.0	V
Current Sense Amplifiers Differential Mode Input Voltage Range	VIN_{CSDM}		-120	-	120	mV
OSCILLATOR						
Minimum Operating Frequency	$Fosc_{min}$	-	-	0	-	Hz
Maximum Operating Frequency	$Fosc_{max}$	Each phase, ROSC = 30kΩ, $V_{COMP} - V_{OSC} = 3.0V$	-	3.0	-	MHz
OSC Current to Frequency Gain	VCO_{Gain}	-	-	25	-	MHz/mA
ONE SHOT						
Minimum On Time Allowed	TON_{min}	(Note)	-	-	100	ns
Phase to Phase On Time Matching	Ph_{match}	CSx-CSxN = 0	-10	-	10	%
TON						
On Time for Each Phase	TON	RTON = 2.0M, VBAT = 12V, CSx-CSxN = 0	-	850	-	ns
		RTON = 1.0M, VBAT = 12V, CSx-CSxN = 0	400	500	600	ns
		RTON = 500k, VBAT = 12V, CSx-CSxN = 0	-	290	-	ns
Input Bias Current When Disabled	$ITON_{SD}$	VTON = 18V	-	-	10	µA

* Note: Guaranteed by design

Electrical Characteristics

(Circuit of Figure 2, VCC = VCCP1 = VCCP2 = 5.0V, V(V_{s+},V_{S-}) = VID(0011000) = 1.2V, T_A = -40 to 85°C, unless other noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
IMON						
Input Offset Voltage	VOS_{IMON}	(Note)	-1.5	-	1.5	mV
IMON Output Voltage (reference to VS-)	VIMONMAX	100% I_{MAX}, VCSSUM = 52mV , Gaindrp = 0.8, GainIMON = 4,	900	1000	1100	mV
	VIMON50%MAX	50% I_{MAX}, VCSSUM = 26mV , Gaindrp = 0.8, GainIMON = 4	450	530	610	mV
	VIMON25%MAX	25% I_{MAX}, VCSSUM = 13mV , Gaindrp = 0.8, GainIMON = 4	225	320	415	mV
	VIMONMIN	0% I_{MAX}, VCSSUM = 0mV, Gaindrp = 0.8, GainIMON = 4	0	-	50	mV
Maximum Clamp Voltage	$V_{MAXCLAMP}$	VIMON – VS-	-	-	1.15	V
IMON Amplifier Gain	$Gain_{IMON}$		3.96	4.0	4.04	V/V
-3dB Bandwidth	BW_{IMON}	(Note)	-	20	-	MHz
Slew Rate	SR_{IMON}	(Note)	-	±0.5	-	V/µs
Source Current	$Isource_{IMON}$	VIMON = 1.0V	-	500	-	µA
Sink Current	$Isink_{IMON}$	VIMON = 0.3V	-	500	-	µA
PWRGD and PROTECTION MONITOR						
Delay from CLK_ENABLE#	$TDlyCK_{PWRGD}$	-	3.0	-	10	ms
Delay between VR_ON de-assertion and PWRGD deassertion	$T_{PWRDOWN1}$	-	-	-	100	ns
Delay between PWRGD de-assertion and VR output rail ramping down	$T_{PWRDOWN2}$	(Note)	-	-	100	ns
Logic Low	$PWRGD_L$	500 Ω pull-up to 3.3V	-	-	0.3	V
OFF State Leakage Current	$IOFFL_{PWRGD}$	-	-	-	100	µA
Power Good Tolerance Positive Side	PWRGDTP	V(VS+,VS-) Rising Relative to VDAC for > 1ms	160	200	240	mV
Power Good Tolerance negative side	PWRGDTN	V(VS+,VS-) Falling Relative to VDAC for > 1ms	-360	-300	-240	mV
Power Not Good Indicate Blanking Time	TPWRNGD	From V(VS+,VS-) out of regulation window to PWRGD de-assertion	-	200	-	µs
Severe Output Overvoltage Threshold	SOVPth+	OVPEN = High, V(VS+,VS-) Relative to SOVPth+ for > 2µs	1.535	1.550	1.565	V
	SOVPth-	OVPEN = High, V(VS+,VS-) Relative to SOVPth-	-	0.3	-	V
CURRENT LIMIT						
ILIM Bias Current	$ILIM_{bias}$	-	9.0	10	11	µA
ILIM Threshold Accuracy, V(CS1, CS1N) + V(CS2, CS2N) - VLIM	Vth_{ILIM}	V(CSx, CSxN) = 25mV, Vth_{ILIM} = V_{LIM}-25mV*6	-	0	-	mV
Current Limit Range	$Range_{ILIM}$	(Note)	0.3	-	2.0	V

* Note: Guaranteed by design

Electrical Characteristics

(Circuit of Figure 2, VCC = VCCP1 = VCCP2 = 5.0V, V(V_{s+},V_{S-}) = VID(0011000) = 1.2V, T_A = -40 to 85°C, unless other noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
VR_ON INPUT						
Logic High Threshold	$VRON_H$	-	600	-	-	mV
Logic Low Threshold	$VRON_L$	-	-	-	400	mV
VR_ON Leakage Current	IRONL	-	-1.0	-	1.0	µA
CLK_ENABLE#						
Delay from Vboot	Tcpu_up + Tboot	(Note)	-	70	-	µs
Logic Low	$CKENB_L$	1.9 kΩ pull-up to 3.3V	-	-	0.8	V
OFF State Leakage Current	$IOFFL_{CKENB}$	-	-	-	10	µA
VID INPUTS						
De Bounce / De Skew Time	$TDeSkew_{VID}$	(Note)	100	-	-	ns
Logic High Threshold	VH_{VID}	-	650	-	-	mV
Logic Low Threshold	VL_{VID}	-	-	-	350	mV
Input Leakage Current	$ILEA_{VID}$	VID0, VID1, VID2, VID3, VID4, VID5, VID6	-	-	10	µA
DPRSLPVR, PSI#, MODE INPUTS						
Logic High Threshold	VH_{Logic}	-	650	-	-	mV
Logic Low Threshold	VL_{Logic}	-	-	-	350	mV
Input Leakage Current	$ILEA_{Logic}$	DPRSLPVR, PSI#, MODE, OVPEN	-	-	10	µA
OVPEN INPUTS						
Logic High Threshold	VH_{Logic}	-	650	-	-	mV
Logic Low Threshold	VL_{Logic}	-	-	-	350	mV
Input Leakage Current	$ILEA_{Logic}$	OVPEN	-	-	10	µA

* Note: Guaranteed by design

OPERATING DESCRIPTION

General

The NCP5372 is a 2 phase PWM controller specifically designed to address the requirements of Intel IMVP6.5 specification. The variable frequency architecture is designed to provide high efficiency under light load conditions, excellent input rejection, fast dynamic VID response, and rapid recovery from transient load conditions.

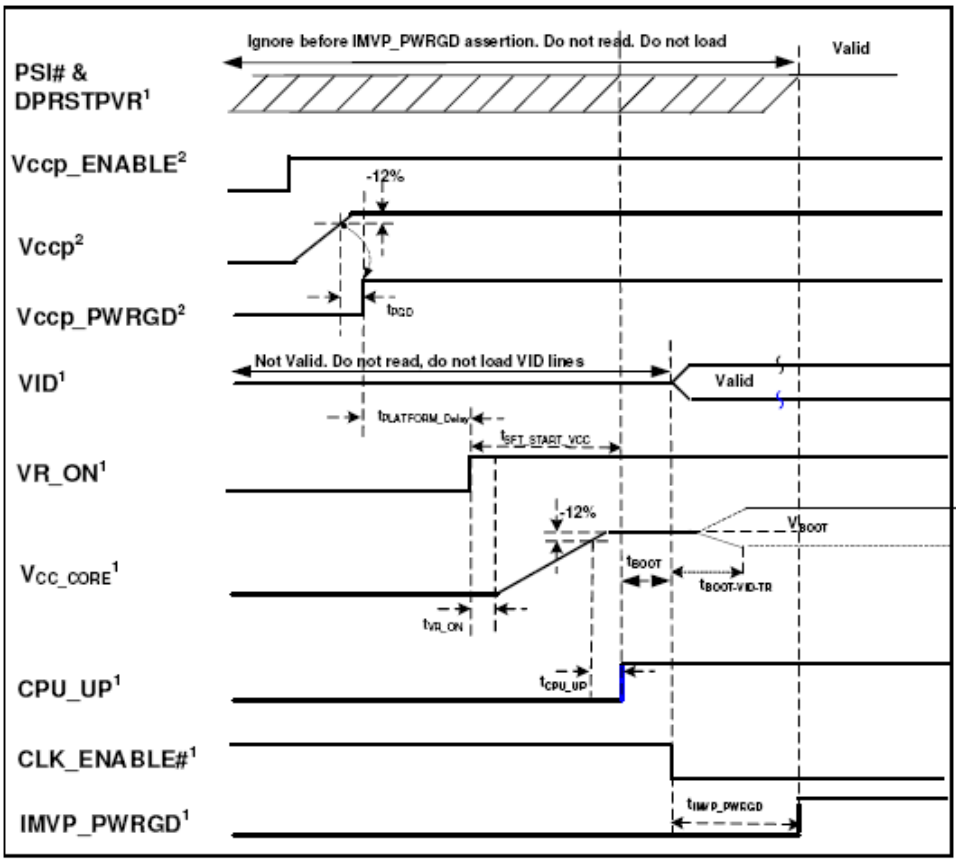
Under Voltage Lock Out

The device input supply voltages VCC, VCCP1 and VCCP2 are monitored by UVLO circuits. The controller is in UVLO mode when either one of its supply voltages has not ramped up above the upper threshold or has dropped below the lower threshold. When a UVLO occurs, the UVLO fault is set and the controller is disabled. The controller can be reset by cycling the VCC, VCCP1, and VCCP2.

Soft Start

During soft start, the output voltage must ramp up linearly in a slowly controlled manner to Vboot voltage. The Vboot voltage for IMVP6.5 is 1.1V. The SS pin will be loaded with a 0.1uF capacitor. The capacitor would be ensured discharge before charging. A 40uA bias current is applied to the SS pin to create the soft start ramp signal. The DAC voltage will be limited by the rising soft start voltage which creates a ramped reference for the controller to follow up in a controlled manner.

After the soft start operation, the capacitor will be discharged.



NOTES:
1. IMVP-6.5 compliant controller feature
2. Shown for reference only

Figure 3. Power On Sequencing Timing Diagram

VID Inputs
Once the output almost achieves Vboot, a 75uS (+/- 30uS) timer will be initialized and the VID code will not be valid until the CLK_ENABLE# pulled low when the timer expires. After the timer expires, the new DAC voltage will be applied to the controller to follow but the change will NOT be limited by the soft start ramp any more.

However, when the reference is switched from 0V to a DAC voltage, the soft start ramp control will be applied in order to limit the transient input current consumption from VBAT.

VID SELECTOR
The VID at startup will be externally programmed by a resistor divider from Vref. When Vcc_core almost reaches Vboot, the external VID code is selected and applied to controller after the timing of Tcpu+Tboot. See Soft Start Timing shown in figure 3.

OUTPUT TOLERANCE ANALYSIS
The DAC Tolerance minimum requirement was back calculated from the overall system regulation requirements. **The DAC regulation requirement is measured across VS+ and VS- pins.**

Requirements

-2.0mOhm Load Line

1.5V – 0.7625V	+/- 1.5% Total System Tolerance (Excludes Ripple)	52A Maximum Load
0.75V – 0.5V	+/- 11.5mV Total System Tolerance (Excludes Ripple)	52A Maximum Load
0.4875 – 0.3V	+/- 25mV Total System Tolerance (Excludes Ripple)	3A Maximum Load

Note: CODE 1111111 is a special OFF code condition. After receiving OFF code, the controller initiates power off sequencing. IMVP_PWRGD is de-asserted within $T_{PWRDOWN1}$ after power off sequencing initialization.

Table 1. VID vs. Output Voltage Table (Only monotonicity can be guaranteed to decrement when Vout is lower than 0.25V)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500

0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500

1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500

1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

DAC slew rate

The DAC output is slew rate limited to prevent overshoot of the system output voltage. If the DAC voltage rises significantly faster than that the control system can be achieved, the output voltage will overshoot. The DAC slew rate is limited between 10mV/uS and 15mV/us.

Voltage Controlled Oscillator

The VCO is critical to the transient response of the overall system. When the load is stepped, the clock will turn on the next phase's one shot as fast as possible.

Current Sharing Function

By default, the one shot on times for both phases will be determined by the external resistor connected to TON, which is used to ramp up the coil currents. Because of various reasons, the coil currents would not be match.

If V(CS1,CS1N) is larger than V(CS2,CS2N), the on time for Phase 1 and Phase 2 will be reduced and increased respectively. The amount of adjustment will be based on their difference proportionally. (The detail amount of the adjustment will be provided later.) The same operation would be applied when V(CS2,CS2N) is greater than V(CS1,CS1N).

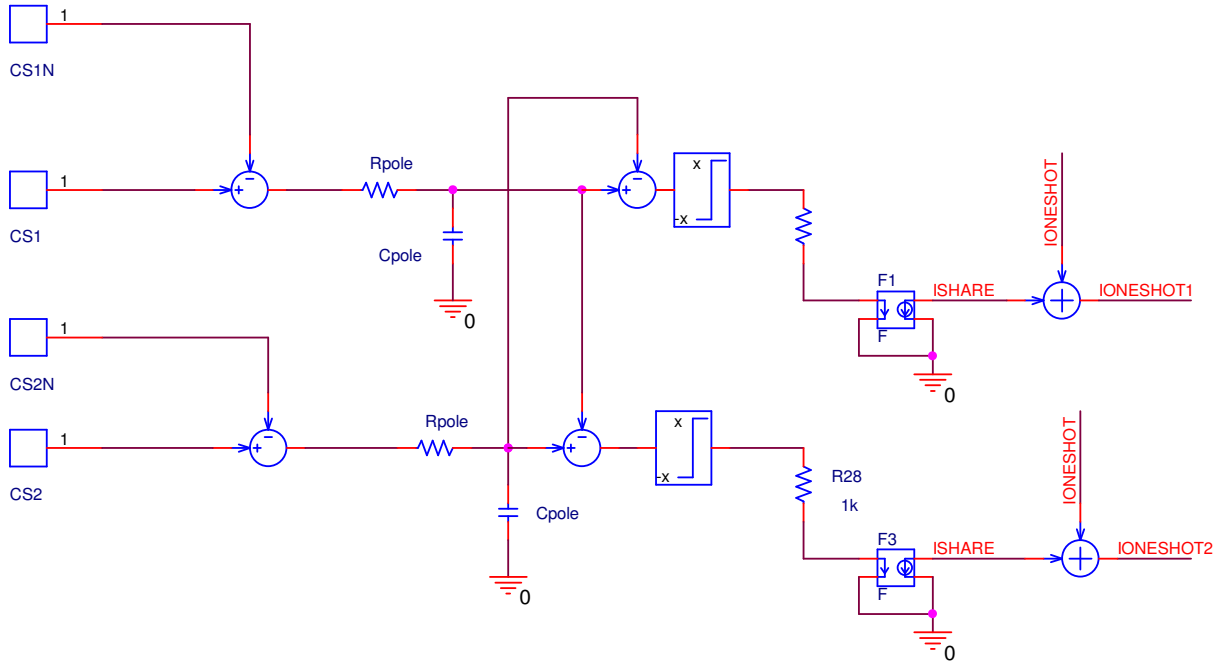


Figure 4. Forced Current Sharing Block Diagram

Auto Skip Power-saving Mode, Forced-CCM Mode and DCM DIODE EMULATION MODE
When the MODE pin is pulled high, the negative current detector is enabled and the controller is selected to operate in auto power-saving mode. When the MODE pin is pulled low, the controller has two modes of operation which depends on the combination of the DPSLPVR and PSI# pins as shown in the Table 2. One is Forced-CCM and another one is diode emulation mode in DCM. The forced-CCM mode disables the zero-crossing comparator, allowing the inductor current to reverse at light loads. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. *Forced-CCM mode is required during downward output voltage transitions.* While in diode emulation mode, the zero-crossing comparator is enabled and this allows DCM operation at light-load. In diode emulation mode, the low-side MOSFET is turned off when the zero-crossing is detected and the switching frequency is reduced with load. The combination of inputs to the DPRSLPVR and PSI# pins determine the operation mode of the controller. The following table shows the logic combination of pin DPRSLPVR and PSI#.

MODE	DPRSLPVR	PSI#	OPERATION MODE
1	X	X	Auto Power-saving (Allow DCM)
0	0	0	Allow DCM at Light Load
0	0	1	Forced CCM
0	1	0	Allow DCM at Light Load
0	1	1	Allow DCM at Light Load

Table 2. Operation Mode

Current Sensing
The current sense amplifiers must provide enough bandwidth and slew rate to generate an accurate representation of the sensed current waveform at the maximum operating frequency. The current sensing has very low offset voltage so as to provide accurate droop control and current sharing. The sensed current voltage is gained by 6 and summed with the offset reference voltage from the droop amplifier. The individual current sense signals are reused in the current sharing function. The current sense signals for each phase is typically max. 100mV.

Current Sense to Droop Transfer Function and Amplifiers
The droop signal should be an accurate representation of the summed current sense waveforms and the amplifiers must be stable over a wide range of external loads.

VR_ON
It is the enable for the controller. When the controller is disabled by VR_ON the internal state machines must be reset into a known starting state to prepare for Soft start. For the fault conditions of over-voltage or over-current, it is used to restart the power cycle.

Feed-forward
The controller provides both VIN and VOUT feed-forward. For the VIN feed-forward, TON depends on VIN change. When VIN increases, TON decreases accordingly to fix the time of period. Similarly, for the VOUT feed-forward, TON also depends on VOUT change. When VOUT increases, TON increases accordingly to fix the time of period. They give the equation.

$$Tperiod=VIN/VOUT*TON \quad \text{(eq. 1)}$$

TON Selection
With minimum VOUT and maximum VIN, the TON must be NOT LESS than 100nSec. Otherwise, if TON is smaller than 100nSec, the controller may cause problem.

Current Limit
The current limit is set by voltage developed across an external resistor on the ILIM pin. An accurate bias current flows out the ILIM pin to create a voltage across the resistor to ground. The voltage signal is heavily low

pass filtered internally to avoid switching noise issues. The current limit threshold voltage is compared to the total sensed inductor current. An over current condition for about 50us will cause a fault condition and shutdown the PWM controller. The controller must be reset by cycling VR_ON, VCC, VCCP1, VCCP2, or VIN.

IMVP Power Good Output

Once VR_ON is activated, Vcc_core ramps to about Vboot. Then, the first VID code is captured and a timer starts to wait for Tboot+Tcpu_up. At the end of the timing, CLK_ENABLE# is set low and Vcc_core is regulated to a DAC voltage determined by the VID code. When CLK_ENABLE# goes low, another timer starts and waits for Tcpu_pwrgd,

At the end of the timing, the output voltage will be monitored whether it is within the Power Good Window, about +200mV/-300mV of the expected voltage. If yes, IMVP_PWRGD is set high. If otherwise, there is a 200us blanking window to allow for undershoot/overshoot before IMVP_PWRGD is set low. Then, the controller must be reset by cycling VR_ON, VCC, VCCP1, VCCP2 or VIN.

When the controller is the DCM mode operation, the upper threshold will be disabled.

Severe Over Voltage Protection (Protection against a shorted high side MOSFET)

The output voltage is sensed via VS+ and VS- inputs and is compared to a fixed threshold of 1.55V. If the output voltage exceeds 1.55V, the severe OVP fault is tripped within 2µs. The high side MOSFETs are shut off and the low side MOSFETs are turned on to discharge the excess voltage at the output. The low side MOSFETs will continue to turn on until the output falls below the release threshold of about 0.3V. The controller will continue monitor for the severe overvoltage condition. If the output voltage rises again and reaches the 1.55V, the low side MOSFETs will turn on again to discharge the over voltage. The low side MOSFETs will repeatedly switch on and off if the over voltage condition persists. This action provides greatest protection against severe over voltage fault and avoids the generation of large negative voltage at the output. The severe OVP fault can be reset by cycling VR_ON, VCC, VCCP1 or VCCP2.

Thermal Shutdown

The thermal shutdown is tripped when the device junction temperature reaches 150°C. When the thermal shutdown is triggered, the TG, BG, and PWRGD are latched low. The output voltage is then discharged through the 106Ω internal MOSFET. The thermal shutdown can be reset and the controller can be re-started again by toggling the VR_ON, VCC, VCCP1, VCCP2 or VIN after the device junction temperature is dropped by 30°C.

Current Monitor

The controller includes an IMON output voltage which is proportional to the core supply output current. The IMON proportional gain is external programmable. The IMON reference is internally connected to VS- and the IMON output can source/sink up to 500uA. Therefore, the current monitor output voltage can be given by the following equation:

$$V_{IMON} = \sum V(CS_{N+}, CS_{N-}) \times 6 \times GAIN_{DRPAMP} \times GAIN_{IMON} \quad \text{(eq. 2)}$$

V_{IMON} = 900mV at IOUT = Imax,

V_{IMON} = 0mV at IOUT = 0A.

The IMON output voltage maximum will be clamped at 1.15V.

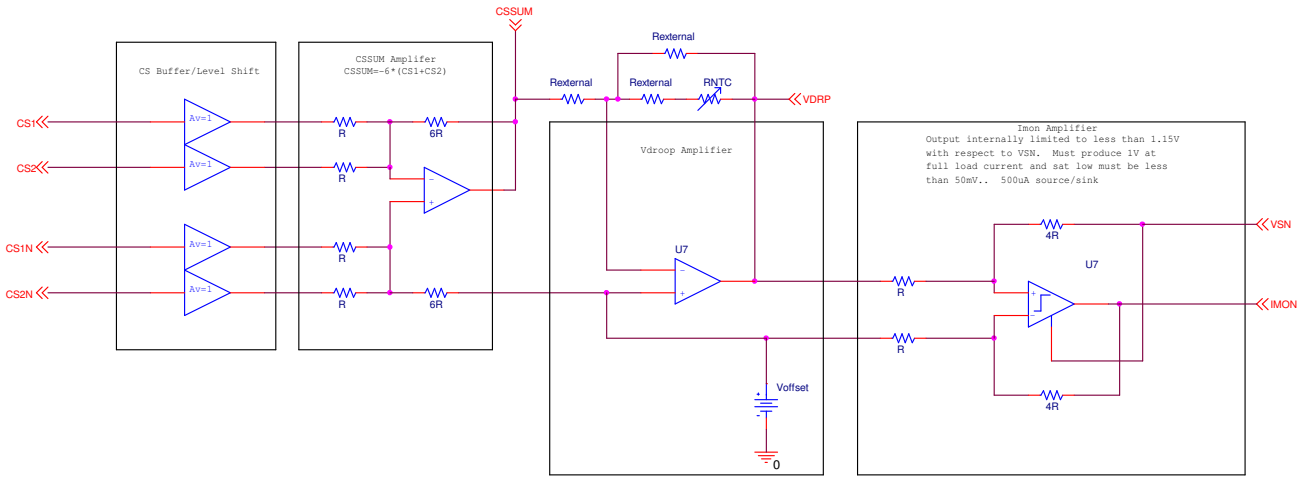


Figure 5. Thermally Compensated Vdroop and Imon Circuit Diagram

CONTROL LOGIC

The control logic will provide timing and sequencing for Startup, Soft start, and Power Down.

POWER DOWN

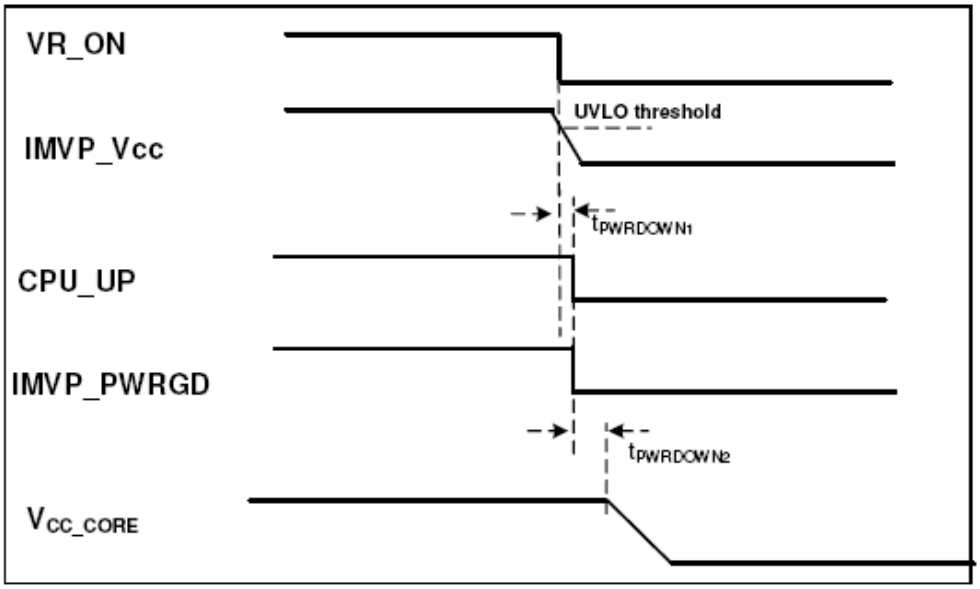


Figure 6. Power Off Sequencing Timing Diagram

Table 3. Fault Protection Summary

Fault	Duration Before Protection	Actions	Fault Reset
Overcurrent	50µs	TG, BG, and PWRGD latched low	Toggle VR_ON, VCC, VCCP1, VCCP2, or VIN
Overvoltage (+200mV)	200µs	TG, BG, and PWRGD latched low	Toggle VR_ON, VCC, VCCP1, VCCP2, or VIN
Severe Overvoltage (>1.55V)	2µs	TG and PWRGD latched low, BG switches ON when V_{CC_CORE} > 1.55V, BG switches OFF when V_{CC_CORE} < 0.3V, Continue monitor and response for OV condition according to the above thresholds	Toggle VR_ON, VCC, VCCP1, VCCP2
Undervoltage (-300mV)	200µs	TG, BG, and PWRGD latched low	Toggle VR_ON, VCC, VCCP1, VCCP2, or VIN
Thermal Shutdown (Tj >150°C)	-	Device disabled, TG, BG, and PWRGD latched low	Toggle VR_ON, VCC, VCCP1, VCCP2, or VIN after Tj falls by 30°C.
UVLO	-	Device disabled, TG, BG latched low	Raising VCC, VCCP1, or VCCP2 above their respective upper thresholds.

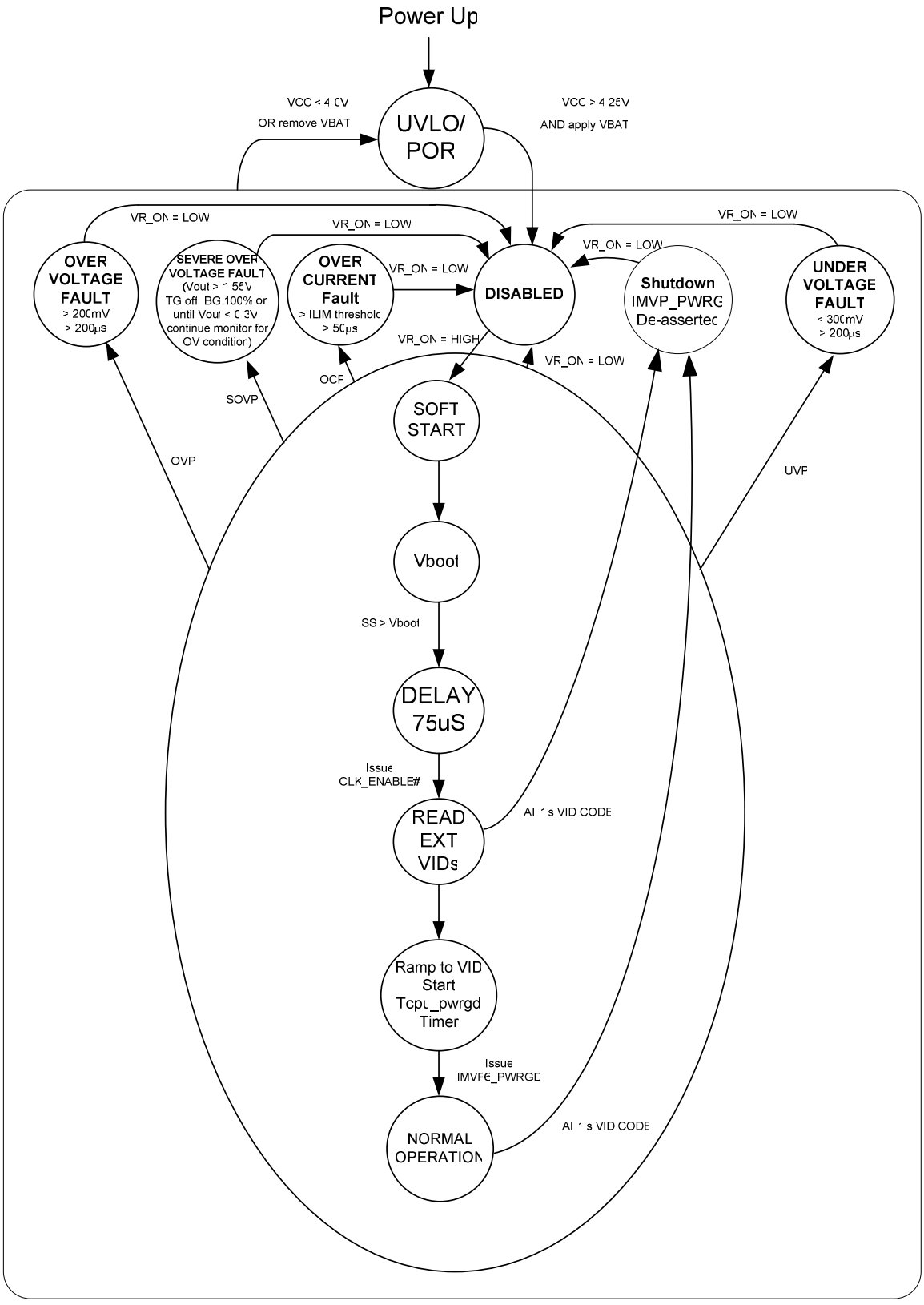


Figure 7. State Diagram

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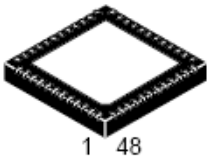
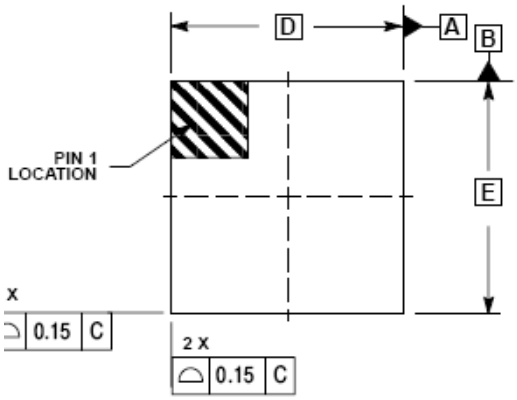
ISSUE C

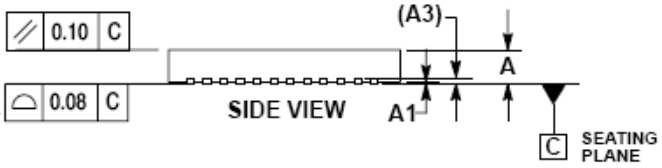
DATE 20 JUL 2004

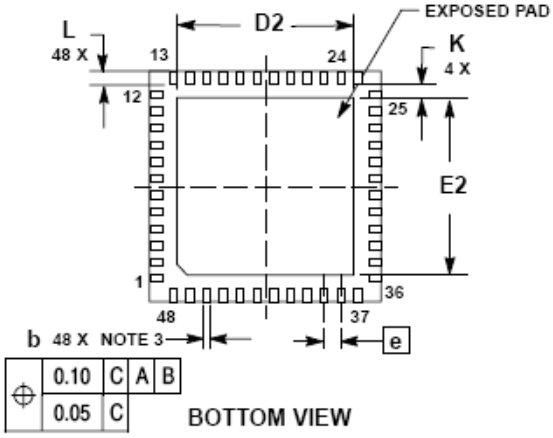


SCALE 2:1



TOP VIEW



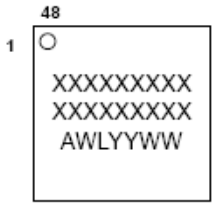


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		7.000 BSC	
D2	5.260	5.360	5.460
E		7.000 BSC	
E2	5.260	5.360	5.460
e		0.500 BSC	
K	0.200	----	----
L	0.300	0.400	0.500

GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.