

NCP5391

2/3 Phase Buck Controller for VR11 Pentium IV Processor Applications

The NCP5391 is a two- or three-phase buck controller which combines differential voltage and current sensing, and adaptive voltage positioning to power Intel's most demanding Pentium® IV Processors and low voltage, high current power supplies. Dual-edge pulse-width modulation (PWM) combined with inductor current sensing reduces system cost by providing the fastest initial response to transient loads thereby requiring less bulk and ceramic output capacitors to satisfy transient load-line requirements.

A high performance operational error amplifier is provided, which allows easy compensation of the system. The proprietary method of Dynamic Reference Injection (Patented) makes the error amplifier compensation virtually independent of the system response to VID changes, eliminating the need for tradeoffs between load transients and Dynamic VID performance.

Features

- Meets Intel's VR 11.0 Specification
- Dual-Edge PWM for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Supports VR11 Soft-Start Mode
- Dynamic Reference Injection (Patent# 7057381)
- 8-Bit DAC per Intel's VR11 Specifications
- DAC Range from 0.5 V to 1.6 V
- ±0.5% System Voltage Accuracy
- 2 or 3-Phase Operation
- True Differential Remote Voltage Sensing Amplifier
- Phase-to-Phase Current Balancing
- "Lossless" Differential Inductor Current Sensing
- Differential Current Sense Amplifiers for each Phase
- Adaptive Voltage Positioning (AVP)
- Fixed No-Load Voltage Positioning at -19 mV
- Frequency Range: 100 kHz – 1.0 MHz
- Threshold Sensitive Enable Pin for VTT Sensing
- Power Good Output with Internal Delays
- Programmable Soft-Start Time
- Operates from 12 V
- This is a Pb-Free Device*

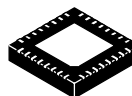
Applications

- Pentium IV Processors
- VRM Modules
- Graphics Cards
- Low Voltage, High Current Power Supplies



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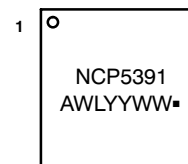
<http://onsemi.com>



1 32

QFN32, 5x5
MN SUFFIX
CASE 488AM

MARKING DIAGRAM



NCP5391 = Specific Device Code

A = Assembly Location

WL = Wafer Lot

YY = Year

WW = Work Week

▪ = Pb-Free Package

*Pin 33 is the thermal pad on the bottom of the device.

ORDERING INFORMATION

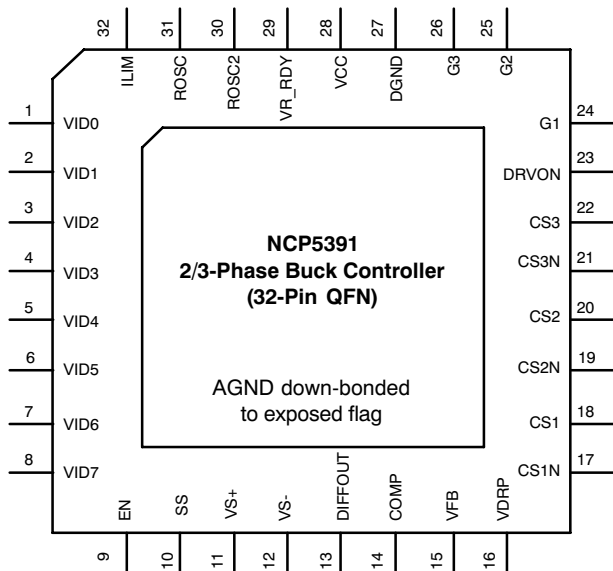
| Device | Package | Shipping† |
|--------------|--------------------|--------------------|
| NCP5391MNR2G | QFN32 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PIN CONNECTIONS



NCP5391

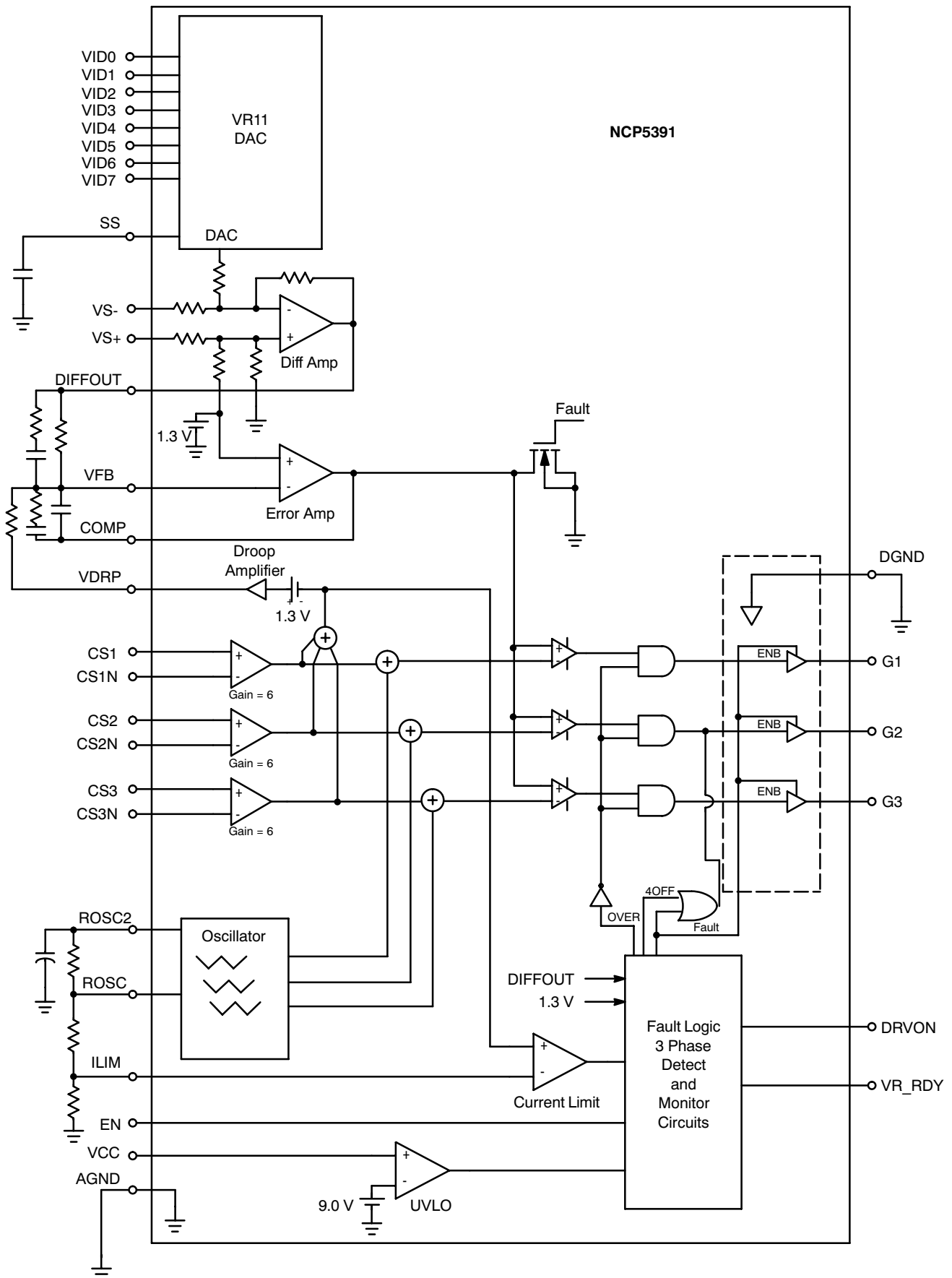


Figure 1. Simplified Block Diagram

NCP5391

PIN DESCRIPTIONS

| Pin No. | Symbol | Description |
|------------|----------------|--|
| 1 - 8 | VID0–VID7 | Voltage ID DAC inputs. |
| 9 | EN | Pull this pin high to enable controller. Pull this pin low to disable controller. Either an open-collector output (with a pull-up resistor) or a logic gate (CMOS or totem-pole output) may be used to drive this pin. A Low to High transition on this pin will initiate a soft start. If the Enable function is not required, this pin should be tied directly to VREF. |
| 10 | SS | A capacitor from this pin to ground programs the soft-start time. |
| 11 | VS+ | Non-inverting input to the internal differential remote V_{CORE} sense amplifier. |
| 12 | VS- | Inverting input to the internal differential remote V_{CORE} sense amplifier. |
| 13 | DIFFOUT | Output of the differential remote sense amplifier. |
| 14 | COMP | Output of the error amplifier. |
| 15 | VFB | Error amplifier inverting input. Connect a resistor from this pin to DIFFOUT. The value of this resistor and the amount of current from the droop resistor (R_{DRP}) will set the amount of output voltage droop (AVP) during load. |
| 16 | VDRP | Current signal output for Adaptive Voltage Positioning (AVP). The voltage of this pin minus 1.3 V is proportional to the output current. Connect a resistor from this pin to V_{FB} to set the amount of AVP current into the feedback resistor (R_{FB}) to produce an output voltage droop. Leave this pin open for no AVP. |
| 17, 19, 21 | CSxN | Inverting input to current sense amplifier #x, x = 1, 2, 3 |
| 18, 20, 22 | CSx | Non-inverting input to current sense amplifier #x, x = 1, 2, 3 |
| 23 | DRVON | Gate Driver enable output. This pin produces a logic HIGH to enable gate drivers and a logic LOW to disable gate drivers and has an internal 70 k Ω to ground. |
| 24, 25, 26 | G1 – G3 | PWM control signal outputs to gate drivers. |
| 27 | DGND | Power supply return for the digital circuits. Connect to AGND. |
| 28 | VCC | Power for the internal control circuits. |
| 29 | VR_RDY | Voltage Regulator Ready (PowerGood) output. Open drain type output with internal delays that will transition High when V_{CORE} is higher than 300 mV below DAC, Low when V_{CORE} is lower than 380 mV below DAC, and Low when V_{CORE} is higher than DAC+185 mV. This output is latched Low if V_{CORE} exceeds DAC+185 mV until V_{CC} is removed. |
| 30 | ROSC2 | Use for Enhanced Performance |
| 31 | ROSC | A resistance from this pin to ground programs the oscillator frequency. Also, this pin supplies a regulated 2.0 V which may be used with a voltage divider to the ILIM pin to set the over current shutdown threshold as shown in the Applications Schematics. |
| 32 | ILIM | Over current shutdown threshold. To program the shutdown threshold, connect this pin to the ROSC pin via a resistor divider as shown in the Applications Schematics. To disable the over current feature connect this pin directly to the ROSC pin. To guarantee correct operation, this pin should only be connected to the voltage generated by the ROSC pin – do not connect this pin to any externally generated voltages. |
| 33 | THPAD/ AGND | Copper pad on the bottom of the IC for heatsinking. This pin should be connected to the ground plane under the IC. Power supply return for the analog circuits that control output voltage. |

NCP5391

MAXIMUM RATINGS

| Rating | Value | Unit |
|---|------------|------|
| Operating Ambient Temperature Range | 0 to 70 | °C |
| Operating Junction Temperature Range | 0 to 85 | °C |
| Storage Temperature Range | -55 to 150 | °C |
| Lead Temperature Soldering, Reflow (60 to 120 seconds minimum above 237°C) | 260 | °C |
| Thermal Resistance, Junction-to-Ambient ($R_{\theta JA}$) on a thermally conductive PCB in free air | 56 | °C/W |
| JEDEC Moisture Sensitivity Level | ≤ 1 | MSL |
| Maximum Voltage – VCC pin with respect to AGND | 15 | V |
| Maximum Voltage – all other pins with respect to AGND | 5.5 | V |
| Minimum Voltage – all pins with respect to AGND | -0.3 | V |
| Maximum Current into pins: COMP, VDRP, DIFFOUT | 3.0 | mA |
| Maximum Current into pins: VR_RDY, G1, G2, G3, SS, DRVON | 20 | mA |
| Maximum Current out of pins: COMP, VDRP, DIFFOUT, ROSC | 3.0 | mA |
| Maximum Current out of pins: G1, G2, G3 | 20 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: ESD Sensitive Device

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ELECTRICAL CHARACTERISTICS

(0°C < T_A < 70°C; 0°C < T_J < 85°C; 10.8 V < V_{CC} < 13.2 V; All DAC Codes; C_{VCC} = 0.1 μF, F_{SW} = 400 kHz, unless otherwise stated)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|------|-----|-----|------|
| ERROR AMPLIFIER | | | | | |
| Input Bias Current | | -200 | -50 | -10 | nA |
| Inverting Input Voltage | 1.0 kΩ between VFB and COMP Pins | - | 1.3 | - | V |
| Input Offset Voltage (Note 1) | | -1.0 | - | 1.0 | mV |
| Open Loop DC Gain (Note 1) | C _L = 60 pF to GND, R _L = 10 kΩ to GND | - | 78 | - | dB |
| Open Loop Unity Gain Bandwidth (Note 1) | C _L = 60 pF to GND, R _L = 10 kΩ to GND | - | 15 | - | MHz |
| Open Loop Phase Margin (Note 1) | C _L = 60 pF to GND, R _L = 10 kΩ to GND | - | 65 | - | ° |
| Slew Rate (Note 1) | ΔV _{in} = 100 mV, G = -1.0 V/V, 1.2 V < V _{out} < 2.2 V, C _L = 60 pF, DC Load = ±125 μA | - | 5.0 | - | V/μs |
| Maximum Output Voltage | I _{SOURCE} = 1.0 mA | 3.0 | 3.3 | - | V |
| Minimum Output Voltage | I _{SINK} = 1.0 mA | - | 0.9 | 1.0 | V |
| Output Source Current (Note 1) | V _{out} = 3.0 V | - | 2.0 | - | mA |
| Output Sink Current (Note 1) | V _{out} = 1.0 V | - | 2.0 | - | mA |

REMOTE SENSE DIFFERENTIAL AMPLIFIER

| | | | | | |
|---|--|--------|----------------------------|--------|------|
| VS+ Input Resistance (Note 1) | DRVON = High DRVON = Low | - - | 17 0.5 | - - | kΩ |
| VS+ Input Open Circuit Voltage (Note 1) | DRVON = High DRVON = Low | - - | 0.67 0.05 | - - | V |
| VS- Input Resistance (Note 1) | VS+ = DAC Voltage DRVON = High | - | 10 | - | kΩ |
| VS- Input Open Circuit Voltage (Note 1) | DRVON = High VS+ = DAC Voltage | | = 0.333* DAC + 0.433 | | V |
| Input Voltage Range | | -0.3 | - | 3.0 | V |
| Input Offset Voltage (Note 1) | | -1.0 | - | 1.0 | mV |
| -3dB Bandwidth (Note 1) | C _L = 80 pF to GND, R _L = 10 kΩ to GND | - | 12 | - | MHz |
| DC Gain | I _{DIFFOUT} = 100 μA | 0.982 | 1.0 | 1.018 | V/V |
| Slew Rate (Note 1) | ΔV _{in} = 1.0 V, ΔV _{out} = 1.0 V to 2.0 V, C _L = 80 pF to GND, Load = ±125 μA | - | 10 | - | V/μs |
| Maximum Output Voltage | I _{SOURCE} = 1.0 mA | 3.0 | - | - | V |
| Minimum Output Voltage | I _{SINK} = 1.0 mA | - | - | 0.5 | V |
| Output Source Current (Note 1) | V _{out} = 2.1 V | - | 25 | - | mA |
| Output Sink Current (Note 1) | V _{out} = 1.0 V | - | 1.4 | - | mA |

V_{DRP} ADAPTIVE VOLTAGE POSITIONING AMPLIFIER

| | | | | | |
|---|--|-----|-----|-----|-----|
| Current Sense Input to V _{DRP} Gain | -60 mV < (CSx-CSxN) < +60 mV, T _A = 25°C | 5.7 | 6.0 | 6.3 | V/V |
| Current Sense Input to V _{DRP} Output -3dB Bandwidth (Note 1) | C _L = 330 pF to GND, R _L = 10 kΩ to GND | - | 7.2 | - | MHz |

1. Guaranteed by design. Not tested in production.

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ELECTRICAL CHARACTERISTICS

(0°C < T_A < 70°C; 0°C < T_J < 85°C; 10.8 V < V_{CC} < 13.2 V; All DAC Codes; C_{VCC} = 0.1 μF, F_{SW} = 400 kHz, unless otherwise stated)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|------|-----|-----|------|
| V_{DRP} ADAPTIVE VOLTAGE POSITIONING AMPLIFIER | | | | | |
| Current Sense Input to V _{DRP} Output Slew Rate (Note 1) | ΔV(CSx-CSxN) = 25 mV (all phases), 1.3 V < V _{out} < 1.9 V, C _L = 330 pF to GND, Load = ±400 μA | - | 3.7 | - | V/μs |
| Current Summing Amp Output Offset Voltage | CSx - CSxN = 0, CSx = 1.0 V | -15 | - | +15 | mV |
| Maximum V _{DRP} Output Voltage | CSx - CSxN = 0.12 V (all phases), I _{SOURCE} = 1.0 mA | 3.02 | - | - | V |
| Minimum V _{DRP} Output Voltage | CSx - CSxN = -0.12 V (all phases), I _{SINK} = 1.0 mA | - | - | 0.5 | V |
| Output Source Current (Note 1) | V _{DRP} = 2.9 V | - | 9.0 | - | mA |
| Output Sink Current (Note 1) | V _{DRP} = 1.0 V | - | 2.0 | - | mA |

CURRENT SENSE AMPLIFIERS

| | | | | | |
|--|--|------|-----|-----|-----|
| Input Bias Current | CSx = CSxN = 1.4 V | -200 | -50 | -10 | nA |
| Common Mode Input Voltage Range (Note 1) | | -0.3 | - | 2.0 | V |
| Differential Mode Input Voltage Range | | -120 | - | 120 | mV |
| Input Offset Voltage (Note 1) | CSx = CSxN = 1.0 V | -3.0 | - | 3.0 | mV |
| Current Sense Input to PWM Comparator Input Gain | 0 mV < (CSx-CSxN) < 25 mV T _A = 25°C | 5.7 | 6.0 | 6.3 | V/V |

OSCILLATOR

| | | | | | |
|--|-------------------------------------|-------|------|-------|-----|
| Switching Frequency Range (Note 1) | | 100 | - | 1000 | kHz |
| Switching Frequency Accuracy (Note 1) | R _{OSC} = 100 kΩ, 2-phase | 93.6 | 104 | 114.4 | kHz |
| Switching Frequency Accuracy | R _{OSC} = 49.9 kΩ, 2-phase | 184.5 | 205 | 225.5 | kHz |
| Switching Frequency Accuracy | R _{OSC} = 24.9 kΩ, 2-phase | 360 | 400 | 440 | kHz |
| Switching Frequency Accuracy | R _{OSC} = 10 kΩ, 2-phase | 829 | 921 | 1013 | kHz |
| Switching Frequency Accuracy (Note 1) | R _{OSC} = 100 kΩ, 3-phase | 90 | 100 | 110 | kHz |
| Switching Frequency Accuracy | R _{OSC} = 49.9 kΩ, 3-phase | 178.2 | 198 | 217.8 | kHz |
| Switching Frequency Accuracy | R _{OSC} = 24.9 kΩ, 3-phase | 351 | 390 | 429 | kHz |
| Switching Frequency Accuracy | R _{OSC} = 10 kΩ, 3-phase | 818 | 909 | 1000 | kHz |
| R _{OSC} Output Voltage | 10 kΩ < R _{OSC} < 49.9 kΩ | 1.92 | 2.00 | 2.08 | V |
| R _{OSC} Output Voltage (Note 1) | 49.9 kΩ < R _{OSC} < 100 kΩ | - | 2.00 | - | V |

MODULATORS (PWM COMPARATORS)

| | | | | | |
|--|---|---|-----|----|----|
| Minimum Pulse Width | F _S = 400 kHz | - | 30 | 40 | ns |
| Magnitude of the PWM Ramp | | - | 1.0 | - | V |
| 0% Duty Cycle | COMP voltage when the PWM outputs remain LO | - | 1.2 | - | V |
| 100% Duty Cycle | COMP voltage when the PWM outputs remain HI | - | 2.3 | - | V |
| Minimum PWM Linear Duty Cycle (Note 1) | F _S = 400 kHz | - | 90 | - | % |

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ELECTRICAL CHARACTERISTICS

(0°C < T_A < 70°C; 0°C < T_J < 85°C; 10.8 V < V_{CC} < 13.2 V; All DAC Codes; C_{VCC} = 0.1 μF, F_{SW} = 400 kHz, unless otherwise stated)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|-----------|-----------------|-----|-----|-----|------|
|-----------|-----------------|-----|-----|-----|------|

MODULATORS (PWM COMPARATORS)

| | | | | | |
|---|---|-----|----|----|----|
| PWM Comparator Offset Mismatch (Note 1) | Between any 2 phases, F _S = 400 kHz | - | - | 40 | mV |
| Phase Angle Error | Between adjacent phases, F _S = 400 kHz | -15 | - | 15 | ° |
| Propagation Delay (Note 1) | Ramp/Comp crossing to Gx high | - | 20 | - | ns |
| Propagation Delay (Note 1) | Ramp/Comp crossing to Gx low | - | 20 | - | ns |

PWM OUTPUTS

| | | | | | |
|--|---|-----|-----|-----|----|
| Output High Voltage | Sourcing 500 μA | 3.3 | 4.0 | 4.7 | V |
| Output Low Voltage | Sinking 500 μA | - | 25 | 100 | mV |
| Rise Time | C _L = 20 pF, ΔV _o = 0.3 to 2.0 V | - | 10 | - | ns |
| Fall Time | C _L = 20 pF, ΔV _o = V _{max} to 0.7 V | - | 10 | - | ns |
| Output Impedance – LO State | Resistance to GND (Gx = LO) | - | 50 | - | Ω |
| G3 Gate Pin Source Current during Phase Detect | | - | 70 | - | μA |
| Phase Detection Period | | - | 50 | - | μs |
| G3 Phase Detect Threshold Resistance | | - | - | 1.0 | kΩ |

GATE DRIVER ENABLE (DRVON)

| | | | | | |
|------------------------------|--|-----|-----|-----|----|
| Output High Voltage | Sourcing 500 μA | 4.0 | 5.3 | 5.5 | V |
| Output Low Voltage | Sinking 500 μA | - | 50 | 200 | mV |
| Rise Time | C _L (PCB) = 20 pF, ΔV _o = 10% to 90% | - | 25 | - | ns |
| Fall Time | C _L (PCB) = 20 pF, ΔV _o = 10% to 90% | - | 25 | - | ns |
| Internal Pulldown Resistance | V _{CC} < UVLO Threshold | - | 70 | 140 | kΩ |

VR_RDY (POWER GOOD) OUTPUT

| | | | | | |
|-------------------------------------|--|-----|------|-----|--------------|
| Saturation Voltage | I _{SINK} = 10 mA | - | - | 0.4 | V |
| Rise Time | External pullup of 1.0 kΩ to 1.25 V, C _{LOAD} = 20 pF, ΔV _o = 10% to 90% | - | - | 150 | ns |
| Output Voltage at Power-up (Note 1) | External VR_RDY pullup resistor of 2.0 kΩ to 5.0 V, t _{R_VCC} ≤ 3 × t _{R_SV} , 100 μs ≤ t _{R_VCC} ≤ 20 ms | - | - | 1.0 | V |
| High – Output Leakage Current | VR_RDY = 5.5 V via 1.0 K | - | - | 1.0 | μA |
| Upper Threshold Voltage | VCORE increasing, DAC = 1.3 V | - | 300 | - | mV below DAC |
| Rising Delay | VCORE increasing | 0.3 | 1.40 | 2.0 | ms |
| Falling Delay | VCORE decreasing | - | 5.0 | - | μs |

SOFT-START

| | | | | | |
|--------------------------|--|-----|-----|-----|----|
| SS Pin Source Current | ENABLE = HI, V _{SS PIN} < 1.1 V | - | 5.0 | - | μA |
| SS Pin Source Current | ENABLE = HI, V _{SS PIN} > 1.15 V, VR11 SS Mode Only | 125 | - | - | μA |
| Soft-Start Ramp Time | C _{SS} = 0.01 μF, DRVON = HI to V _{SS PIN} = 1.1 V | 1.5 | 2.2 | 3.0 | ms |
| SS Pin Discharge Voltage | ENABLE = LO | - | - | 50 | mV |

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ELECTRICAL CHARACTERISTICS

(0°C < T_A < 70°C; 0°C < T_J < 85°C; 10.8 V < V_{CC} < 13.2 V; All DAC Codes; C_{VCC} = 0.1 μF, F_{SW} = 400 kHz, unless otherwise stated)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|-----------|-----------------|-----|-----|-----|------|
|-----------|-----------------|-----|-----|-----|------|

SOFT-START

| | | | | | |
|---|--|----|-------|-----|----|
| Soft-Start Discharge Time | From ENABLE = LO to V _{SS} PIN < max Discharge Voltage, C _{SS} = 0.01 μF | - | 5.0 | - | μs |
| VR11 V _{BOOT} Threshold Voltage | | - | 1.081 | - | V |
| VR11 Dwell Time at V _{BOOT} (Note 1) | | 50 | 225 | 900 | μs |

ENABLE INPUT

| | | | | | |
|-----------------------------------|---|------|------|------|----|
| Enable High Input Leakage Current | EN = 3.0 V | - | - | 10 | μA |
| Upper Threshold | V _{UPPER} | 0.80 | 0.85 | 0.90 | V |
| Lower Threshold | V _{LOWER} | 0.67 | 0.75 | 0.83 | V |
| Total Hysteresis | V _{UPPER} - V _{LOWER} | 70 | 100 | 130 | mV |
| Enable Delay Time | Enable transitioning HI to start of SS voltage rise | 0.5 | 1.5 | 3.0 | ms |
| Disable Delay Time | Enable transitioning Low to DRVON = Low | - | - | 200 | ns |

CURRENT LIMIT

| | | | | | |
|--|--|-----|-----|-----|-----|
| Current Sense Inputs to I _{LIM} Gain (Note 1) | 20 mV < (CSx-CSxN) < 60 mV T _A = 25°C (all CS channels together) | 5.7 | 6.0 | 6.3 | V/V |
| ILIM Pin Input Bias Current | V _{ILIM} = 2.0 V | - | 0.1 | 1.0 | μA |
| ILIM Pin Working Voltage Range (Note 1) | | 0.3 | - | 2.0 | V |
| ILIM Input Offset Voltage (Note 1) | | -50 | - | 50 | mV |

OVERVOLTAGE PROTECTION

| | | | | | |
|--------------------------------|--|----------|-------------|----------|----|
| Overvoltage Threshold (Note 1) | | DAC +160 | DAC+18 0 | DAC +200 | mV |
|--------------------------------|--|----------|-------------|----------|----|

UNDERVOLTAGE PROTECTION

| | | | | | |
|----------------------|--|-----|-----|-----|---|
| UVLO Start Threshold | | 8.2 | 9.0 | 9.5 | V |
| UVLO Stop Threshold | | 7.2 | 8.0 | 8.5 | V |
| UVLO Hysteresis | | - | 1.0 | - | V |

VID INPUTS

| | | | | | |
|---|--|-----|-----|------|----|
| Upper Threshold | V _{UPPER} | - | - | 800 | mV |
| Lower Threshold | V _{LOWER} | 400 | - | - | mV |
| Input Bias Current | V _{VIDX} = 1.25 V | - | 100 | 500 | nA |
| Delay before Latching VID Change (VID De-Skewing) | Measured from the 1 st edge of a VID change | 400 | - | 1000 | ns |

INTERNAL DAC SLEW RATE LIMITER

| | | | | | |
|--------------------------|-----------------------------------|---|-----|---|-------|
| Positive Slew Rate Limit | VID step range of +10mV to +500mV | - | 7.3 | - | mV/μs |
| Negative Slew Rate Limit | VID step range of -10mV to -500mV | - | 7.3 | - | mV/μs |

INPUT SUPPLY CURRENT

| | | | | | |
|-----------------------------------|---------------------------|---|----|---|----|
| V _{CC} Operating Current | F _{SW} = 400 kHz | - | 20 | - | mA |
|-----------------------------------|---------------------------|---|----|---|----|

VR 11 DAC

| | | | | | |
|---|---|---|-----|----------------------|---------------|
| System Voltage Accuracy | 1.0 V < DAC < 1.6 V 0.8 V < DAC < 1.0 V 0.5 V < DAC < 0.8 V | - | - | ±0.5 ±5.0 ±8.0 | % mV mV |
| No-Load Offset Voltage from Nominal DAC Specification | With CS Input ΔVin = 0 V | | -19 | | mV |

1. Guaranteed by design. Not tested in production.

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Table 2: VR11 VID Codes

| VID7 800 mV | VID6 400 mV | VID5 200 mV | VID4 100 mV | VID3 50 mV | VID2 25 mV | VID1 12.5 mV | VID0 6.25 mV | Nominal DAC Voltage (V) | HEX |
|----------------|----------------|----------------|----------------|---------------|---------------|-----------------|-----------------|-------------------------------|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OFF | 00 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | OFF | 01 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.60000 | 02 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.59375 | 03 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.58750 | 04 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.58125 | 05 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.57500 | 06 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.56875 | 07 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.56250 | 08 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.55625 | 09 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.55000 | 0A |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.54375 | 0B |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.53750 | 0C |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.53125 | 0D |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1.52500 | 0E |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.51875 | 0F |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1.51250 | 10 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.50625 | 11 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.50000 | 12 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1.49375 | 13 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1.48750 | 14 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1.48125 | 15 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1.47500 | 16 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1.46875 | 17 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1.46250 | 18 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1.45625 | 19 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1.45000 | 1A |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1.44375 | 1B |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1.43750 | 1C |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1.43125 | 1D |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1.42500 | 1E |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1.41875 | 1F |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1.41250 | 20 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1.40625 | 21 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1.40000 | 22 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1.39375 | 23 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.38750 | 24 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.38125 | 25 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1.37500 | 26 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.36875 | 27 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1.36250 | 28 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1.35625 | 29 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1.35000 | 2A |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1.34375 | 2B |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1.33750 | 2C |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1.33125 | 2D |

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Table 2: VR11 VID Codes

| VID7 800 mV | VID6 400 mV | VID5 200 mV | VID4 100 mV | VID3 50 mV | VID2 25 mV | VID1 12.5 mV | VID0 6.25 mV | Nominal DAC Voltage (V) | HEX |
|----------------|----------------|----------------|----------------|---------------|---------------|-----------------|-----------------|-------------------------------|-----|
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1.32500 | 2E |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1.31875 | 2F |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1.31250 | 30 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1.30625 | 31 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1.30000 | 32 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1.29375 | 33 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1.28750 | 34 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1.28125 | 35 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1.27500 | 36 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1.26875 | 37 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1.26250 | 38 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1.25625 | 39 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1.25000 | 3A |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1.24375 | 3B |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1.23750 | 3C |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1.23125 | 3D |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1.22500 | 3E |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1.21875 | 3F |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1.21250 | 40 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1.20625 | 41 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1.20000 | 42 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1.19375 | 43 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1.18750 | 44 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1.18125 | 45 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1.17500 | 46 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1.16875 | 47 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1.16250 | 48 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1.15625 | 49 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1.15000 | 4A |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1.14375 | 4B |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1.13750 | 4C |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1.13125 | 4D |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1.12500 | 4E |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1.11875 | 4F |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1.11250 | 50 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1.10625 | 51 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1.10000 | 52 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1.09375 | 53 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1.08750 | 54 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1.08125 | 55 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1.07500 | 56 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1.06875 | 57 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1.06250 | 58 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1.05625 | 59 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1.05000 | 5A |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1.04375 | 5B |

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Table 2: VR11 VID Codes

| VID7 800 mV | VID6 400 mV | VID5 200 mV | VID4 100 mV | VID3 50 mV | VID2 25 mV | VID1 12.5 mV | VID0 6.25 mV | Nominal DAC Voltage (V) | HEX |
|----------------|----------------|----------------|----------------|---------------|---------------|-----------------|-----------------|-------------------------------|-----|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1.03750 | 5C |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1.03125 | 5D |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1.02500 | 5E |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1.01875 | 5F |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1.01250 | 60 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1.00625 | 61 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1.00000 | 62 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.99375 | 63 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.98750 | 64 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.98125 | 65 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.97500 | 66 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.96875 | 67 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.96250 | 68 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.95625 | 69 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.95000 | 6A |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.94375 | 6B |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.93750 | 6C |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.93125 | 6D |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.92500 | 6E |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.91875 | 6F |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.91250 | 70 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.90625 | 71 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.90000 | 72 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.89375 | 73 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.88750 | 74 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.88125 | 75 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.87500 | 76 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.86875 | 77 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0.86250 | 78 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0.85625 | 79 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0.85000 | 7A |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0.84375 | 7B |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0.83750 | 7C |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0.83125 | 7D |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.82500 | 7E |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.81875 | 7F |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.81250 | 80 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.80625 | 81 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.80000 | 82 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.79375 | 83 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0.78750 | 84 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0.78125 | 85 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0.77500 | 86 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0.76875 | 87 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0.76250 | 88 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0.75625 | 89 |

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Table 2: VR11 VID Codes

| VID7 800 mV | VID6 400 mV | VID5 200 mV | VID4 100 mV | VID3 50 mV | VID2 25 mV | VID1 12.5 mV | VID0 6.25 mV | Nominal DAC Voltage (V) | HEX |
|----------------|----------------|----------------|----------------|---------------|---------------|-----------------|-----------------|-------------------------------|----------|
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0.75000 | 8A |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0.74375 | 8B |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0.73750 | 8C |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0.73125 | 8D |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0.72500 | 8E |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0.71875 | 8F |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0.71250 | 90 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0.70625 | 91 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0.70000 | 92 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0.69375 | 93 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0.68750 | 94 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0.68125 | 95 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0.67500 | 96 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0.66875 | 97 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0.66250 | 98 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0.65625 | 99 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0.65000 | 9A |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0.64375 | 9B |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0.63750 | 9C |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0.63125 | 9D |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0.62500 | 9E |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0.61875 | 9F |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0.61250 | A0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0.60625 | A1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0.60000 | A2 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0.59375 | A3 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0.58750 | A4 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0.58125 | A5 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0.57500 | A6 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0.56875 | A7 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0.56250 | A8 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.55625 | A9 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0.55000 | AA |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0.54375 | AB |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0.53750 | AC |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0.53125 | AD |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0.52500 | AE |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0.51875 | AF |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0.51250 | B0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0.50625 | B1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0.50000 | B2 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | OFF | FE |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | OFF | FF |
| | | | | | | | | OFF | B3 to FD |

TYPICAL CHARACTERISTICS

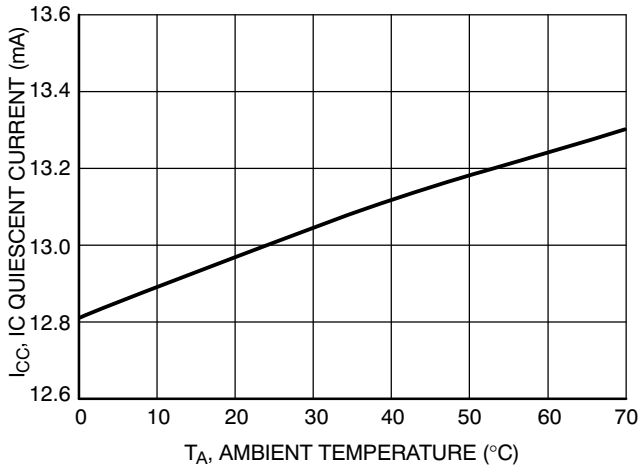


Figure 4. IC Quiescent Current vs. Ambient Temperature

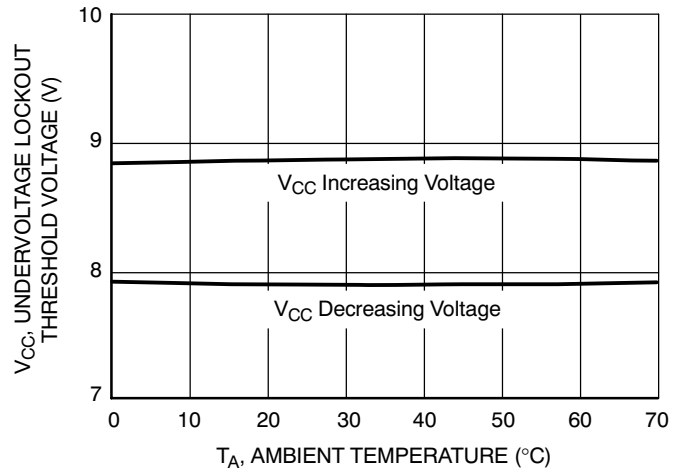


Figure 5. VCC Undervoltage Lockout Threshold Voltage vs. Ambient Temperature

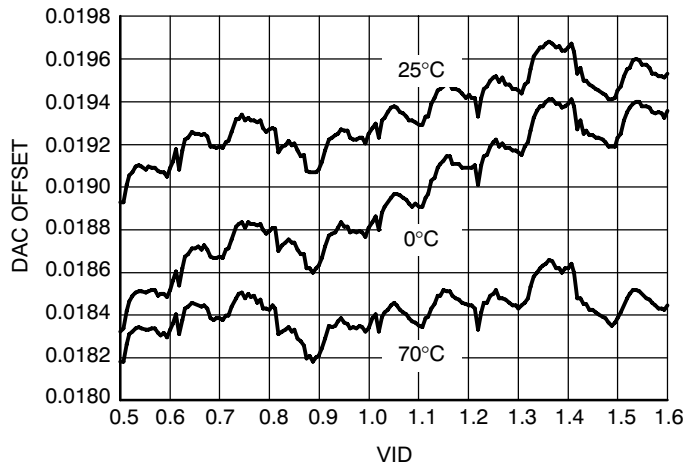


Figure 6. Typical DAC Voltage Offset vs. Temperature

FUNCTIONAL DESCRIPTION

General

The NCP5391 dual edge modulated multiphase PWM controller is specifically designed with the necessary features for a high current VR11 CPU power system. The IC consists of the following blocks: Precision Programmable DAC, Differential Remote Voltage Sense Amplifier, High Performance Voltage Error Amplifier, Differential Current Feedback Amplifiers, Precision Oscillator and Triangle Wave Generators, and PWM Comparators. Protection features include Undervoltage Lockout, Soft-Start, Overcurrent Protection, Overvoltage Protection, and Power Good Monitor.

Remote Output Sensing Amplifier (RSA)

A true differential amplifier allows the NCP5391 to measure Vcore voltage feedback with respect to the Vcore ground reference point by connecting the Vcore reference point to VS+, and the Vcore ground reference point to VS-. This configuration keeps ground potential differences between the local controller ground and the Vcore ground reference point from affecting regulation of Vcore between Vcore and Vcore ground reference points. The RSA also subtracts the DAC (minus VID offset) voltage, thereby producing an unamplified output error voltage at the DIFFOUT pin. This output also has a 1.3 V bias voltage to allow both positive and negative error voltages.

Precision DAC

A precision programmable DAC is provided. This DAC has 0.5% accuracy over the entire operating temperature range of the part.

High Performance Voltage Error Amplifier

The error amplifier is designed to provide high slew rate and bandwidth. Although not required when operating as a voltage regulator, a capacitor from COMP to VFB is required for stable unity gain test configurations.

Gate Driver Outputs and 2/3 Phase Operation

The part can be configured to run in 2- or 3-phase mode. In 2-phase mode, phases 1 and 3 should be used to drive the external gate drivers as shown in the 2-phase Applications Schematic. In 2-phase mode, gate output G2 must be grounded as shown in the 2-phase Applications Schematic. The following truth table summarizes the modes of operation:

| Mode | Gate Output Connections | | |
|---------|-------------------------|------------|--------|
| | G1 | G2 | G3 |
| 2-Phase | Normal | GND | Normal |
| 3-Phase | Normal | Normal | Normal |

These are the only allowable connection schemes to program the modes of operation.

Differential Current Sense Amplifiers

Three differential amplifiers are provided to sense the output current of each phase. The inputs of each current sense amplifier must be connected across the current sensing element of the phase controlled by the corresponding gate output (G1, G2 or G3). **If 2 phase is unused, the differential inputs to that phase's current sense amplifier must be shorted together and connected to VCCP as shown in the 2-phase Application Schematics.**

A voltage is generated across the current sense element (such as an inductor or sense resistor) by the current flowing in that phase. The output of the current sense amplifiers are used to control three functions. First, the output controls the adaptive voltage positioning, where the output voltage is actively controlled according to the output current. In this function, all of the current sense outputs are summed so that the total output current is used for output voltage positioning. Second, the output signal is fed to the current limit circuit. This again is the summed current of all phases in operation. Finally, the individual phase current is connected to the PWM comparator. In this way current balance is accomplished.

Oscillator and Triangle Wave Generator

A programmable precision oscillator is provided. The oscillator's frequency is programmed by the resistance connected from the ROSC pin to ground. The user will usually form this resistance from two resistors in order to create a voltage divider that uses the ROSC output voltage as the reference for creating the current limit setpoint voltage. The oscillator frequency range is 100 kHz/phase to 1.0 MHz/phase. The oscillator generates up to 3 triangle waveforms (symmetrical rising and falling slopes) between 1.3 V and 2.3 V. The triangle waves have a phase delay between them such that for 2-, 3-phase operation the PWM outputs are separated by 180 and 120 angular degrees, respectively.

PWM Comparators with Hysteresis

Three PWM comparators receive the error amplifier output signal at their noninverting input. Each comparator receives one of the triangle waves offset by 1.3 V at it's inverting input. The output of the comparator generates the PWM outputs G1, G2 and G3.

During steady state operation, the duty cycle will center on the valley of the triangle waveform, with steady state duty cycle calculated by V_{out}/V_{in} . During a transient event, both high and low comparator output transitions shift phase to the points where the error amplifier output intersects the down and up ramp of the triangle wave.

PROTECTION FEATURES

Undervoltage Lockout

An undervoltage lockout (UVLO) senses the VCC input. During powerup, the input voltage to the controller is monitored, and the PWM outputs and the soft-start circuit are disabled until the input voltage exceeds the threshold voltage of the UVLO comparator. The UVLO comparator incorporates hysteresis to avoid chattering, since VCC is likely to decrease as soon as the converter initiates soft-start.

Overcurrent Shutdown

A programmable overcurrent function is incorporated within the IC. A comparator and latch makeup this function. The inverting input of the comparator is connected to the ILIM pin. The voltage at this pin sets the maximum output current the converter can produce. The ROSC pin provides a convenient and accurate reference voltage from which a resistor divider can create the overcurrent setpoint voltage. Although not actually disabled, tying the ILIM pin directly to the ROSC pin sets the limit above useful levels – effectively disabling overcurrent shutdown. The comparator noninverting input

is the summed current information from the current sense amplifiers. The overcurrent latch is set when the current information exceeds the voltage at the ILIM pin. The outputs are immediately disabled, the VR_RDY and DRVON pins are pulled low, and the soft-start is pulled low. The outputs will remain disabled until the VCC voltage is removed and re-applied, or the ENABLE input is brought low and then high.

Overvoltage Protection and Power Good Monitor

An output voltage monitor is incorporated. During normal operation, if the voltage at the DIFFOUT pin exceeds 1.3 V, the VR_RDY pin goes low, the DRVON signal remains high, the PWM outputs are set low. The outputs will remain disabled until the VCC voltage is removed and reapplied. During normal operation, if the output voltage falls more than 300 mV below the DAC setting, the VR_RDY pin will be set low until the output rises.

Soft-Start

The NCP5391 incorporates an externally programmable soft-start. The soft-start circuit works by controlling the ramp-up of the DAC voltage during powerup. The initial soft-start pin voltage is 0 V. The soft-start circuitry clamps the DAC input of the Remote Sense Amplifier to the SS pin voltage until the SS pin voltage exceeds the DAC setting minus VID offset. The soft-start pin is pulled to 0 V if there is an overcurrent shutdown, if the ENABLE pin is low, if VCC is below the UVLO threshold, or if an overvoltage condition exists.

The NCP5391 ramps Vcore to 1.1 V at the SS capacitor charge rate, pauses at 1.1 V for 170 μs, reads the VID pins to determine the DAC setting, then ramps Vcore to the final DAC setting at the Dynamic VID slew rate of 7.3 mV/μs. Typical soft-start sequence is shown in the following graph.

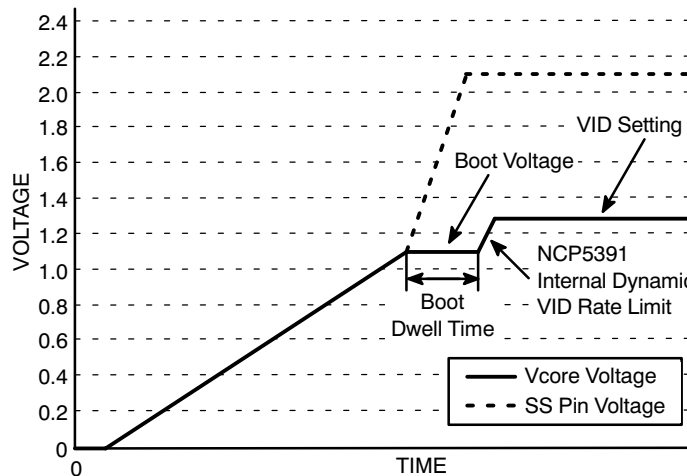


Figure 7. Typical VR11 Soft-Start Sequence to Vcore = 1.3 V

APPLICATION INFORMATION

The NCP5391 is a high performance multiphase controller optimized to meet the Intel VR11 Specifications. The demo board for the NCP5391 is available by request. It is configured as a three phase solution with decoupling designed to provide a 1.0 mΩ load line under a 50 A step load. A schematic is available upon request from ON Semiconductor.

Startup Procedure

The demo board comes with a Socket 775 and requires an Intel dynamic load tool (VTT Tool) available through a third party supplier, Cascade Systems. The web page is <http://www.cascadesystems.net/>.

Start by installing the test tool software. It's best to power the test tool from a separate ATX power supply. The test tool should be set to a valid VID code of 0.5 V or above in-order for the controller to start. Consult the VTT help manual for more detailed instructions.

Startup Sequence

1. Make sure the VTT software is installed.
2. Powerup the PC or Laptop do not start the VTT software.
3. Insert the VTT Test Tool adapter into the socket and lock it down.
4. Insert the socket saver pin field into the bottom of the VTT test tool.
5. Carefully line up the tool with the socket in the board and press tool into the board.
6. Connect the scope probe, or DMM to the voltage sense lines on the test tool. When using a scope probe it is best to isolate the scope from the AC ground. Make the ground connection on the scope probe as short as possible.
7. Connect the first ATX supply to the VTT tool.
8. Powerup the first ATX supply to the VTT tool.
9. Start the VTT tool software in VR11 mode with the current limit set to 150 A.
10. Using the VTT tool software, select a VID code that is 0.5 V or above.
11. Connect the second ATX supply to the demo board.
12. Set the VID DIP switches. All the VID switches should be up or open.
13. Set the VR_ENABLE DIP switch down or closed.
14. Start the second ATX supply by turning it on and setting the PSON DIP switch low. The green VID

lights should light up to match the VTT tool VID setting.

15. Set the VR_ENABLE DIP switch up to start the NCP5391.
16. Check that the output voltage is about 19 mV below the VID setting.

Step Load Testing

The VTT tool is used to generate the high di/dt step load. Select the dynamic loading option in the VTT test tool software. Set the desired step load size, frequency, duty, and slew rate. See Figures 8 and 9.

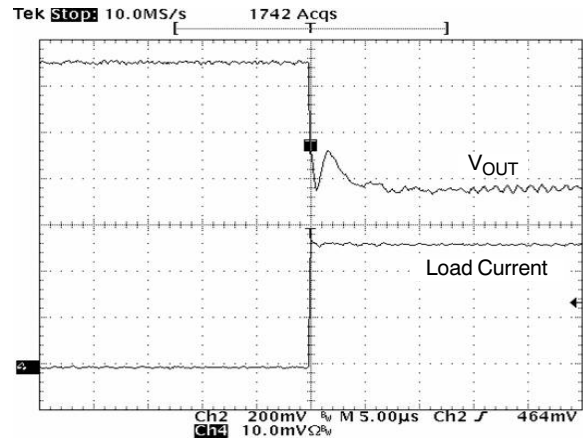


Figure 8. Typical Step Load Response

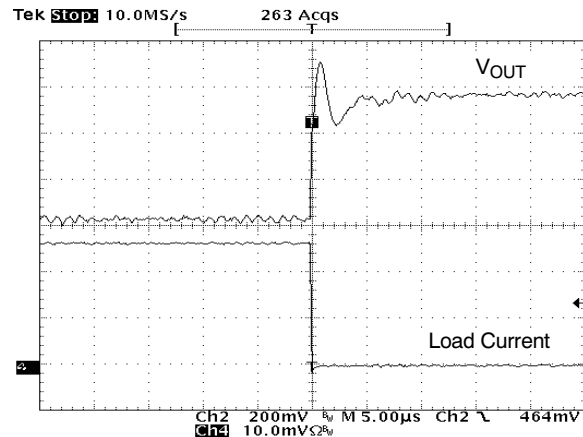


Figure 9. Typical Load Release Event

Dynamic VID Testing

The VTT tool provides for VID stepping based on the Intel Requirements. Select the Dynamic VID option. Before enabling the test set the lowest VID to 0.5 V or greater and set the highest VID to a value that is greater than the lowest VID selection, then enable the test. See Figures 10 through 12.

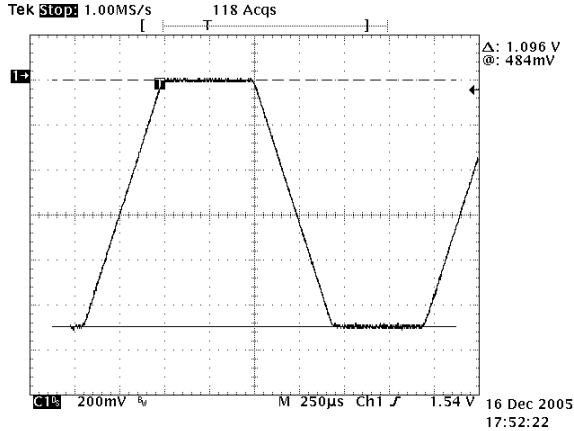


Figure 10. 1.6 to 0.5 Dynamic VID Response

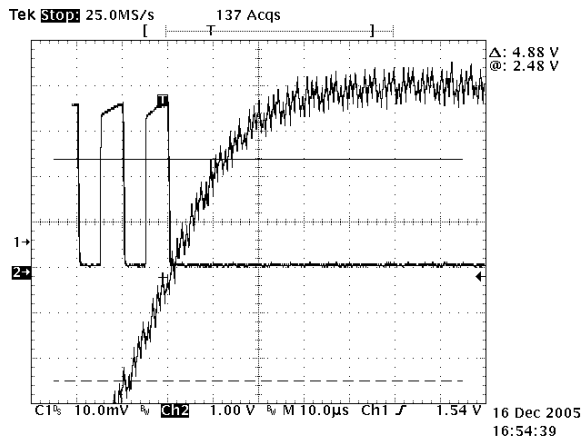


Figure 11. Dynamic VID Settling Time Rising

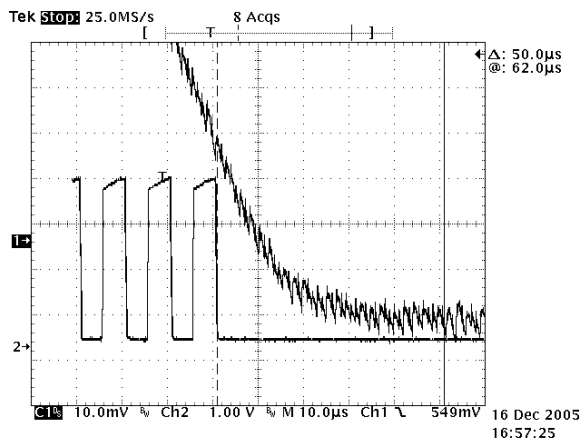


Figure 12. Dynamic VID Settling Time Falling

Design Methodology

Decoupling the V_{CC} Pin on the IC

An RC input filter is required as shown in the V_{CC} pin to minimize supply noise on the IC. The resistor should be sized such that it does not generate a large voltage drop between the 12 V supply and the IC. See the schematic values.

Understanding Soft-Start

The controller will ramp to the 1.1 V, with a pause to capture the VID code then resume ramping to target value based on an internal slew rate limit. See Figure 13. The controller is designed to regulate to the voltage on the SS pin until it reaches the internal DAC voltage. The soft-start cap sets the initial ramp rate using a typical 5.0 μA current. The typical value to use for the soft-start cap (SS), is typically set to 0.01 μF. This results in a ramp time to 1.1 V of 2.2 ms based on equation 1.

$$C_{SS} \approx i_{SS} \frac{dt_{SS}}{dv_{SS}}$$

$$\frac{1.1 \cdot V}{2.2 \cdot ms} = \frac{dv_{SS}}{dt_{SS}} \text{ and } i_{SS} = 5 \cdot \mu A \quad (\text{eq. 1})$$

$$C_{SS} = 0.01 \cdot \mu F$$

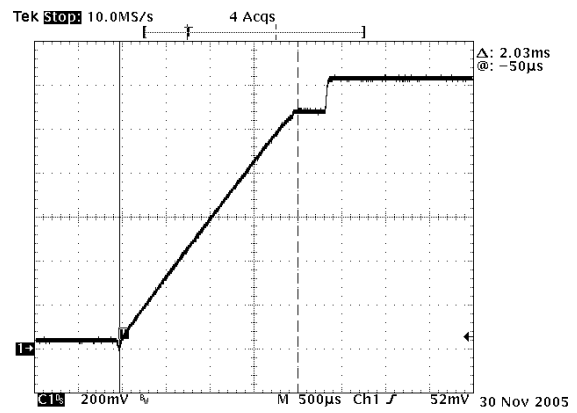


Figure 13. VR11 Startup

Programming the Current Limit and the Oscillator Frequency

The demo board is set for an operating frequency of approximately 300 kHz. The OSC pin provides a 2.0 V reference voltage which is divided down with a resistor divider and fed into the current limit pin ILIM. Calculate the total series resistance to set the frequency and then calculate the individual values for current limit divider.

The series resistors RLIM1 and RLIM2 sink current to ground. This current is internally mirrored into a capacitor to create an oscillator. The period is proportional to the resistance and frequency is inversely proportional to the resistance. The resistance may be estimated by equation 2.

This equation is valid for the individual phase frequency in both three and four phase mode.

$$32.36 \text{ k}\Omega \cong \frac{10.14 \times 10^9}{300 \cdot k} - 1440 \tag{eq. 2}$$

2 Phase Mode

$$R_{OSC} = \frac{10.14 \times 10^9}{\text{Frequency}} - 1440 \tag{eq. 3}$$

3 Phase Mode

$$R_{OSC} = \frac{9.711 \times 10^9}{\text{Frequency}} - 1111$$

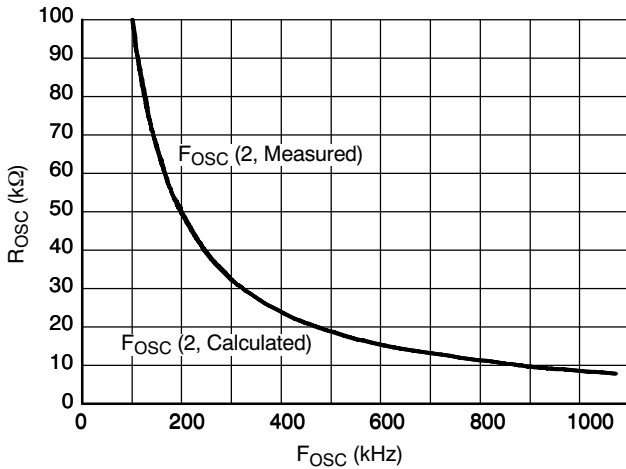


Figure 14. ROSC vs. 2-Phase Mode

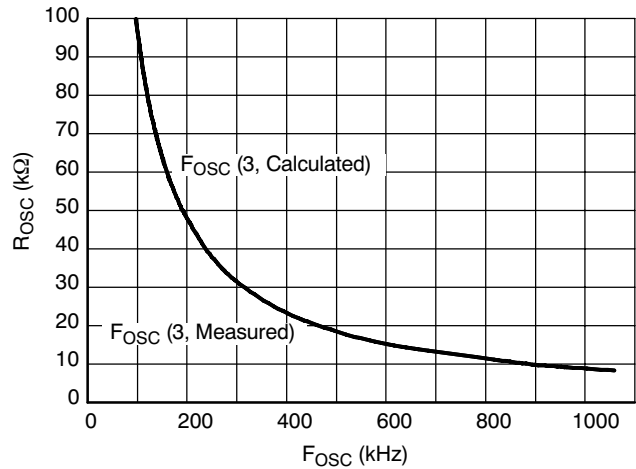


Figure 15. ROSC vs. 3-Phase Mode

The current limit function is based on the total sensed current of all phases multiplied by a gain of 5.94. DCR sensed inductor current is function of the winding temperature. The best approach is to set the maximum Calculate the current limit voltage:

current limit based on the expected average maximum temperature of the inductor windings.

$$DCR_{Tmax} = DCR_{25C} \cdot (1 + 0.00393 \cdot C^{-1} (T_{Tmax} - 25 \cdot C)) \tag{eq. 4}$$

$$V_{LIMIT} \cong 5.94 \cdot \left(I_{MIN_OCP} \cdot DCR_{Tmax} + \frac{DCR_{50C} \cdot V_{out}}{2 \cdot V_{in} \cdot F_s} \cdot \left(\frac{V_{in} - V_{out}}{L} - (N-1) \cdot \frac{V_{out}}{L} \right) \right) - 0.02 \tag{eq. 5}$$

Solve for the individual resistors:

$$RLIM2 = \frac{V_{LIMIT} \cdot R_{OSC}}{2 \cdot V} \tag{eq. 6}$$

$$RLIM1 = R_{OSC} - RLIM2$$

Final Equation for the Current Limit Threshold

$$I_{LIMIT}(T_{inductor}) \cong \frac{\left(\frac{2 \cdot V \cdot RLIM2}{RLIM1 + RLIM2} \right) + 0.02}{5.94 \cdot (DCR_{25C} \cdot (1 + 0.00393 \cdot C^{-1} (T_{Inductor} - 25 \cdot C)))} - \frac{V_{out}}{2 \cdot V_{in} \cdot F_s} \cdot \left(\frac{V_{in} - V_{out}}{L} - (N-1) \cdot \frac{V_{out}}{L} \right) \tag{eq. 7}$$

The inductors on the demo board have a DCR at 25°C of 0.75 mΩ. Selecting the closest available values of 16.9 kΩ for RLIM1 and 15.8 kΩ for RLIM2 yield a nominal operating frequency of 305 kHz and an approximate current limit of 180 A at 100°C. The total sensed current can be observed as a scaled voltage at the VDRP pin added to a positive, no-load offset of approximately 1.3 V.

Inductor Selection

When using inductor current sensing it is recommended that the inductor does not saturate by more than 10% at maximum load. The inductor also must not go into hard saturation before current limit trips. The demo board includes a four phase output filter using the T50-8 core from Micrometals with 4turns and a DCR target of 0.75 mΩ @ 25°C. Smaller DCR values can be used, however, current sharing accuracy and droop accuracy decrease as DCR decreases. Use the excel spreadsheet for regulation accuracy calculations for a specific value of DCR.

Inductor Current Sense Compensation

The NCP5391 uses the inductor current sensing method. This method uses an RC filter to cancel out the inductance of the inductor and recover the voltage that is the result of

the current flowing through the inductor's DCR. This is done by matching the RC time constant of the current sense filter to the L/DCR time constant. The first cut approach is to use a 0.47 μF capacitor for C and then solve for R.

$$R_{sense}(T) = \frac{L}{0.47 \cdot \mu F \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot C \cdot 1 \cdot (T - 25 \cdot C))} \tag{eq. 8}$$

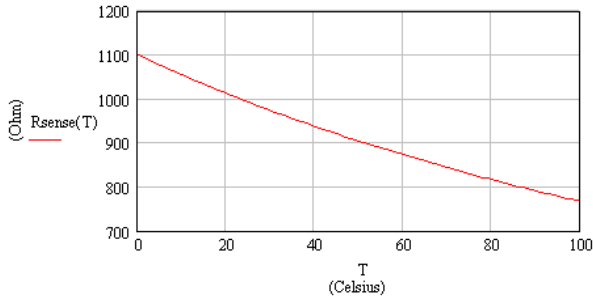


Figure 16.

The demoboard inductor measured 350 nH and 0.75 mΩ at room temp. The actual value used for Rsense was 953 Ω which matches the equation for Rsense at approximately 50C. Because the inductor value is a function of load and

inductor temperature final selection of R is best done experimentally on the bench by monitoring the Vdroop pin and performing a step load test on the actual solution.

It is desirable to keep the Rsense resistor value below 1.0 k whenever possible by increasing the capacitor values in the inductor compensation network. The bias current flowing out of the current sense pins is approximately 100 nA. This current flows through the current sense resistor and creates an offset at the capacitor which will appear as a load current at the Vdroop pin. A 1.0 k resistor will keep this offset at the droop pin below 2.5 mV.

Simple Average PSPICE Model

A simple state average model shown in Figure 17 can be used to determine a stable solution and provide insight into the control system.

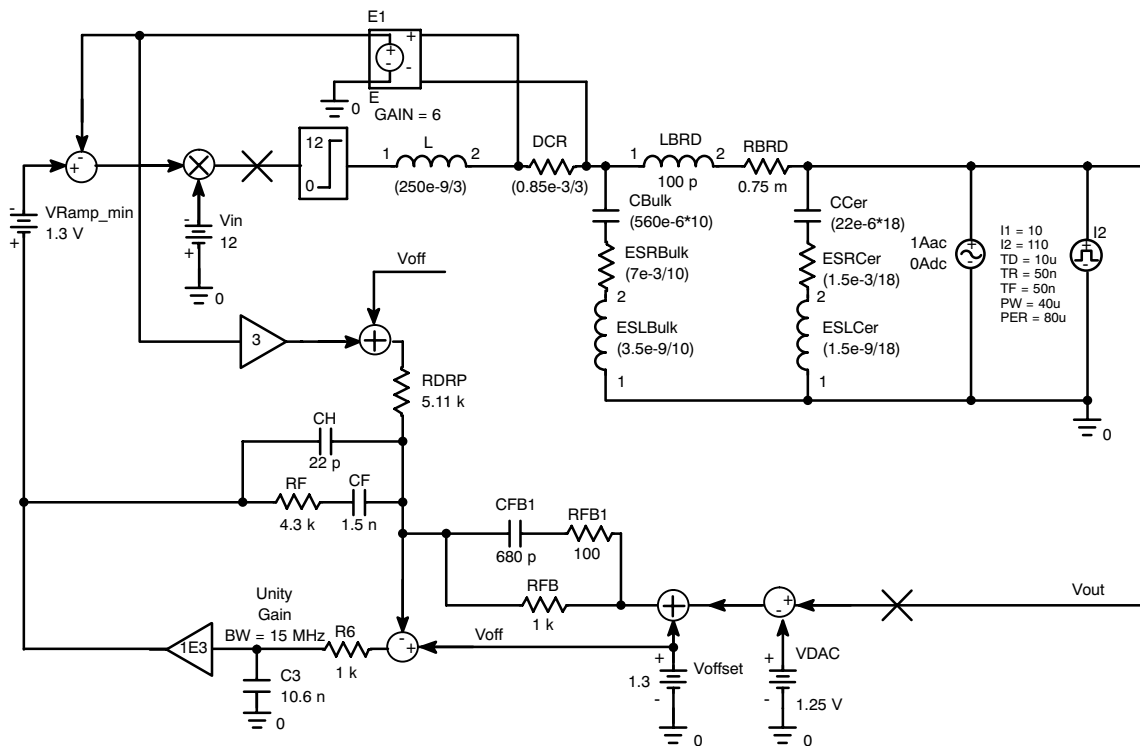


Figure 17.

A complex switching model is available by request which includes a more detailed board parasitic for this demo board.

Compensation and Output Filter Design

The values shown on the demo board are a good place to start for any similar output filter solution. The dynamic performance can then be adjusted by swapping out various individual components.

If the required output filter and switching frequency are significantly different, it's best to use the available PSPICE models to design the compensation and output filter from scratch.

The design target for this demo board was 1.0 mΩ out to 2.0 MHz. The phase switching frequency is currently set to 300 kHz. It can easily be seen that the board impedance of 0.75 mΩ between the load and the bulk capacitance has a large effect on the output filter. In this case the ten 560 μF

bulk capacitors have an ESR of 7.0 mΩ. Thus the bulk ESR plus the board impedance is 0.7 mΩ + 0.75 mΩ or 1.45 mΩ. The actual output filter impedance does not drop to 1.0 mΩ until the ceramic breaks in at over 375 kHz. The controller must provide some loop gain slightly less than one out to a frequency in excess 300 kHz. At frequencies below where the bulk capacitance ESR breaks with the bulk capacitance, the DC-DC converter must have sufficiently high gain to control the output impedance completely. Standard Type-3 compensation works well with the NCP5391. RFB1 should be kept above 50 Ω for amplifier stability reasons.

The goal is to compensate the system such that the resulting gain generates constant output impedance from DC up to the frequency where the ceramic takes over holding the impedance below 1.0 mΩ. See the example of the locations of the poles and zeros that were set to optimize the model above.

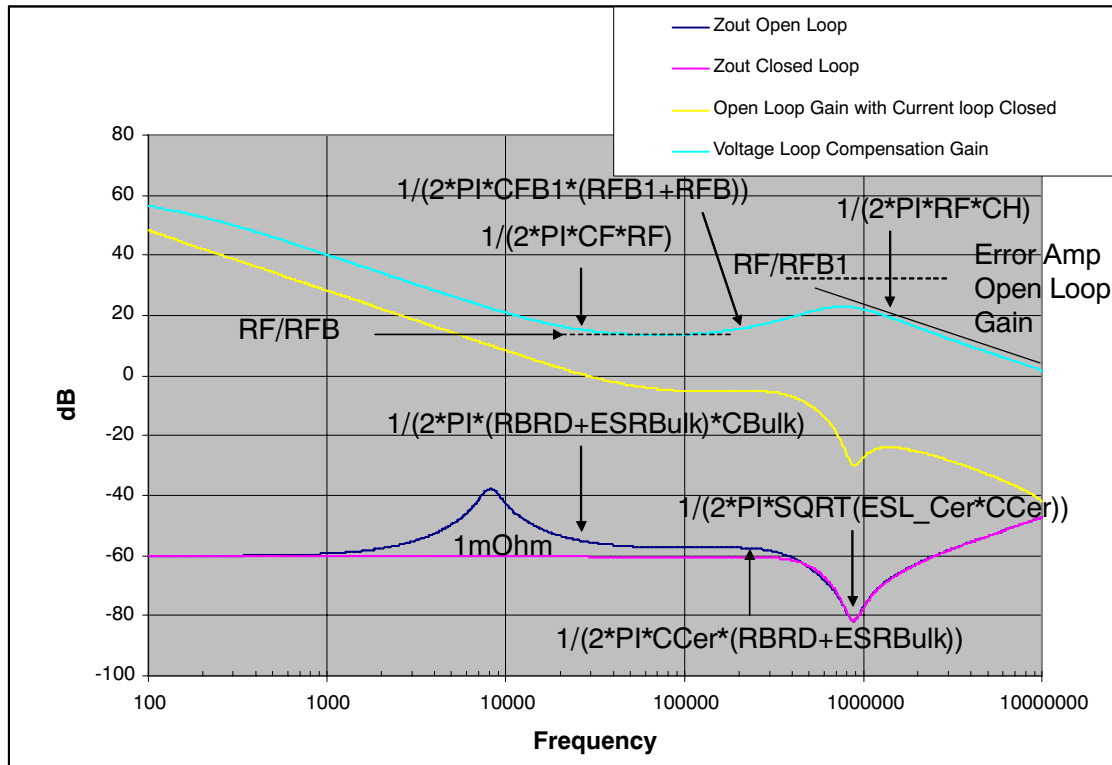


Figure 18.

By matching the following equations a good set of starting compensation values can be found for a typical mixed bulk and ceramic capacitor type output filter.

$$\frac{1}{2\pi \cdot CF \cdot RF} = \frac{1}{2\pi \cdot (RBRD + ESRBulk) \cdot CBulk} \tag{eq. 9}$$

$$\frac{1}{2\pi \cdot CFBI \cdot (RFB1 + RFB)} = \frac{1}{2\pi \cdot CCer \cdot (RBRD + ESRBulk)}$$

RFB is always set to 1.0 kΩ and RFB1 is usually set to 100 Ω for maximum phase boost. The value of RF is typically set to 4.0 kΩ.

Droop Injection and Thermal Compensation

The VDRP signal is generated by summing the sensed output currents for each phase and applying a gain of approximately six. VDRP is externally summed into the feedback network by the resistor RDRP. This induces an offset which is proportional to the output current thereby forcing the controlled resistive output impedance.

$$DCR_{Tmax} = DCR_{25C} \cdot (1 + 0.00393 \cdot C^{-1}(T_{Tmax} - 25 \cdot C)) \tag{eq. 11}$$

The system can be thermally compensated to cancel this effect out to a great degree by adding an NTC (negative temperature coefficient resistor) in parallel with RFB to reduce the droop gain as the temperature increases. The NTC device is nonlinear. Putting a resistor in series with the

RRDP determines the target output impedance by the basic equation:

$$\frac{V_{out}}{I_{out}} = Z_{out} = \frac{RFB \cdot DCR \cdot 5.94}{RDRP} \tag{eq. 10}$$

$$RDRP = \frac{RFB \cdot DCR \cdot 5.94}{Z_{out}}$$

The value of the inductor’s DCR varies with temperature according to the following equation 10:

NTC helps make the device appear more linear with temperature. The series resistor is split and inserted on both sides of the NTC to reduce noise injection into the feedback loop. The recommended value for RISO1 and RISO2 is approximately 1.0 kΩ.

The output impedance varies with inductor temperature by the equation:

$$Z_{out}(T) = \frac{RFB \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot C^{-1}(T_{max} - 25C)) \cdot 5.94}{R_{droop}} \tag{eq. 12}$$

By including the NTC RT2 and the series isolation resistors the new equation becomes:

$$Z_{out}(T) = \frac{\frac{RFB \cdot (RISO1 + RT2(T) + RISO2)}{RFB + RISO1 + RT2(T) + RISO2} \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot C^{-1}(T_{max} - 25C)) \cdot 5.94}{R_{droop}} \tag{eq. 13}$$

The typical equation of a NTC is based on a curve fit equation 13.

$$RT2(T) = RT_{25C} \cdot e^{\beta \left[\left(\frac{1}{273 + T} \right) - \left(\frac{1}{298} \right) \right]} \tag{eq. 14}$$

The demo board is populated with a 10 kΩ NTC with a Beta of 4300. Figure 19 shows the uncompensated and compensated output impedance versus temperature.

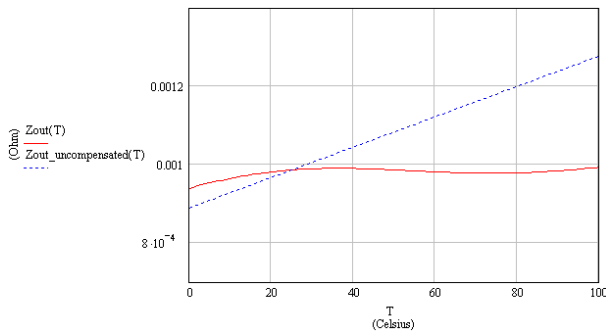


Figure 19. Uncompensated and Compensated Output Impedance vs. Temperature

ON Semiconductor provides an excel spreadsheet to help with the selection of the NTC. The actual selection of the NTC will be effected by the location of the output inductor with respect to the NTC and airflow, and should be verified with an actual system thermal solution.

OVP

The overvoltage protection threshold is not adjustable. OVP protection is enabled as soon as soft-start begins and is disabled when the part is disabled. When OVP is tripped, the controller commands all four gate drivers to enable their low side MOSFETs, and VR_RDY transitions low. The OVP is non-latching and auto recovers. The OVP circuit monitors the output of DIFFOUT. If the DIFFOUT signal reaches 180 mV above the nominal 1.3 V offset the OVP will trip. The DIFFOUT signal is the difference between the output voltage and the DAC voltage plus the 1.3 V internal offset. This results in the OVP tracking the DAC voltage even during a dynamic change in the VID setting during operation.

Gate Driver and MOSFET Selection

ON Semiconductor provides the companion gate driver IC (NCP3418B). The NCP3418B driver is optimized to work with a range of MOSFETs commonly used in CPU applications. The NCP3418B provides special functionality and is required for the high performance dynamic VID operation of the part. Contact your local ON Semiconductor applications engineer for MOSFET recommendations.

Board Stack-Up

The demo board follows the recommended Intel Stack-up and copper thickness as shown.

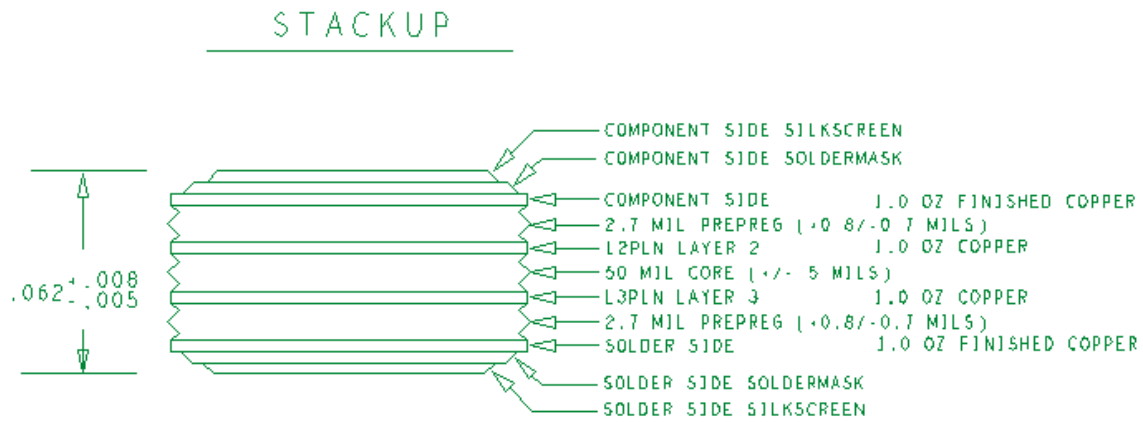


Figure 20.

Board Layout

A complete Allegro ATX and BTX demo board layout file and schematics are available by request at www.onsemi.com and can be viewed using the Allegro Free Physical Viewer 15.x from the Cadence website <http://www.cadence.com/>.

Close attention should be paid to the routing of the sense traces and control lines that propagate away from the controller IC. Routing should follow the demo board example. For further information or layout review contact ON Semiconductor.

