INTEGRATED CIRCUITS

DATA SHEET

PCF1174C
4-digit static LCD car clock

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC16

1997 Apr 16

Philips Semiconductors

PHILIPS

FEATURES

- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: –40 to +85 °C
- 40-lead plastic SMD, face down (VSO40).

GENERAL DESCRIPTION

The PCF1174C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit static liquid crystal display (LCD).

Two external single-pole, single-throw switches will accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1174CT	VSO40	plastic very small outline package; 40 leads; face down(1)	SOT158-2
PCF1174CU	–	uncased chip in tray(2)	–

Notes

1. See Fig.1 and Chapter “Package outline” for pin layout and package details.
2. See Chapter “Chip dimensions and bonding pad locations” for pad layout and package details.

PINNING

SYMBOL	PIN	DESCRIPTION
BP	1	backplane output
PM	2	segment driver
AM	3	segment driver
ADEG1	4	segment driver
C1	5	segment driver
E2	6	segment driver
D2	7	segment driver
C2	8	segment driver
E3	9	segment driver
C3	10	segment driver
E4	11	segment driver
D4	12	segment driver
C4	13	segment driver
B4	14	segment driver
S1	15	hour adjustment input
DATA	16	EEPROM data input
OSC IN	17	oscillator input
OSC OUT	18	oscillator output
V_{SS}	19	negative supply
MODE	20	12/24-hour mode select input
V_{PP}	21	programming voltage input
TS	22	test speed-up mode input
ENABLE	23	set enable input for S1 and S2
V_{DD}	24	positive supply voltage
FLASH	25	colon option input
SEL	26	EEPROM select input
S2	27	minute adjustment input
A4	28	segment driver
F4	29	segment driver
G4	30	segment driver
B3	31	segment driver
AD3	32	segment driver
F3	33	segment driver
G3	34	segment driver
COL	35	segment driver
B2	36	segment driver
A2	37	segment driver
F2	38	segment driver
G2	39	segment driver
B1	40	segment driver

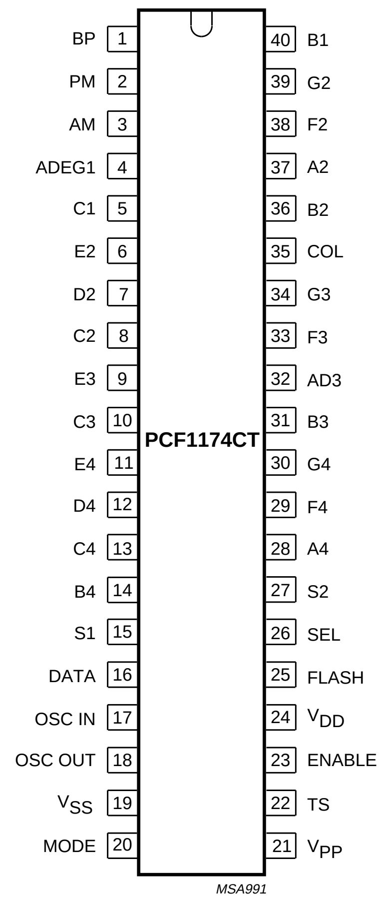


Fig.1 Pin configuration, PCF1174CT, (VSO40).

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs static data to the LCD. Generation of BP and the output signals are shown in Fig.4.

The average voltages across the segments are:

1. $V_{ON(RMS)} = V_{DD}$
2. $V_{OFF(RMS)} = 0$ V.

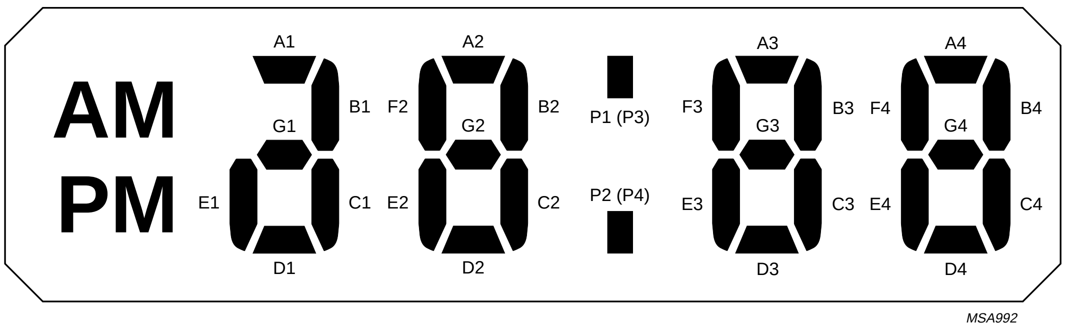
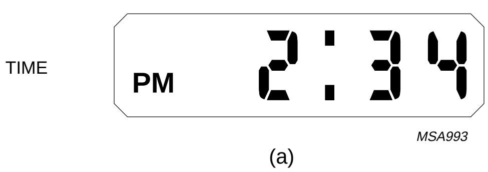
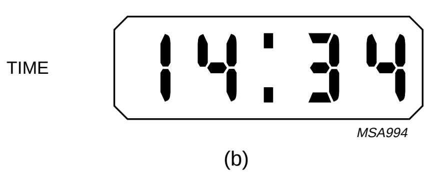


Fig.2 Segment designation of LCD.



a. 12-hour mode.



b. 24-hour mode.

Fig.3 Typical displays.

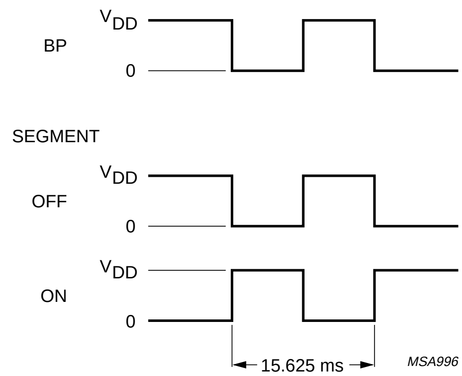


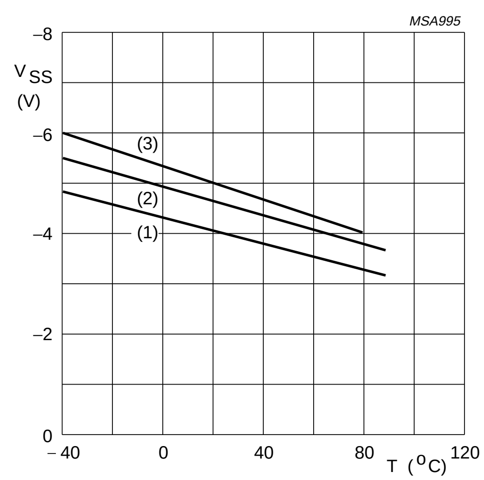
Fig.4 Backplane and output signals.

LCD voltage (see Fig.5)

The adjustable voltage regulator controls the supply voltage (see Section “LCD voltage programming”) in relation to temperature for good contrast, for example when V_{DD} = 4.5 V at +25 °C, then:

V_{DD} = 3 to 4 V at +85 °C.

V_{DD} = 5 to 6 V at –40 °C.



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).
(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).
(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.5 Regulated voltage as a function of temperature (typical).

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively.

Power-on

After connecting the supply, the start-up mode is:

1:00 AM; 12-hour mode.

0:00; 24-hour mode.

Colon

If FLASH is connected to V_{DD} the colon pulses at 1 Hz. If FLASH is connected to V_{SS} the colon is static.

Time setting

Switch inputs S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing switches S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of V_{DD} – 5 V is applied to V_{PP} (see Fig.6). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C).
For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation $+60 \times 10^{-6}$) by capacitors at the oscillator input and output, a number (n) of 262 144 Hz pulses are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.6):

1. Set SEL to V_{SS} and a level of V_{DD} – 5 V to V_{PP}
2. The quartz-frequency deviation Δf/f is measured and (n) is calculated (see Table 1)
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and (when correct) fixed by applying the store pulse t_W
6. Release SEL and V_{PP}.

Table 1 Time calibration (Δt = 3.81 µs; SEL at V_{SS})

OSCILLATOR-FREQUENCY DEVIATION Δf/f ($\times 10^{-6}$)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.629
+7.6	2	15.633
+11.4	3	15.636
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+117.8	31	15.743

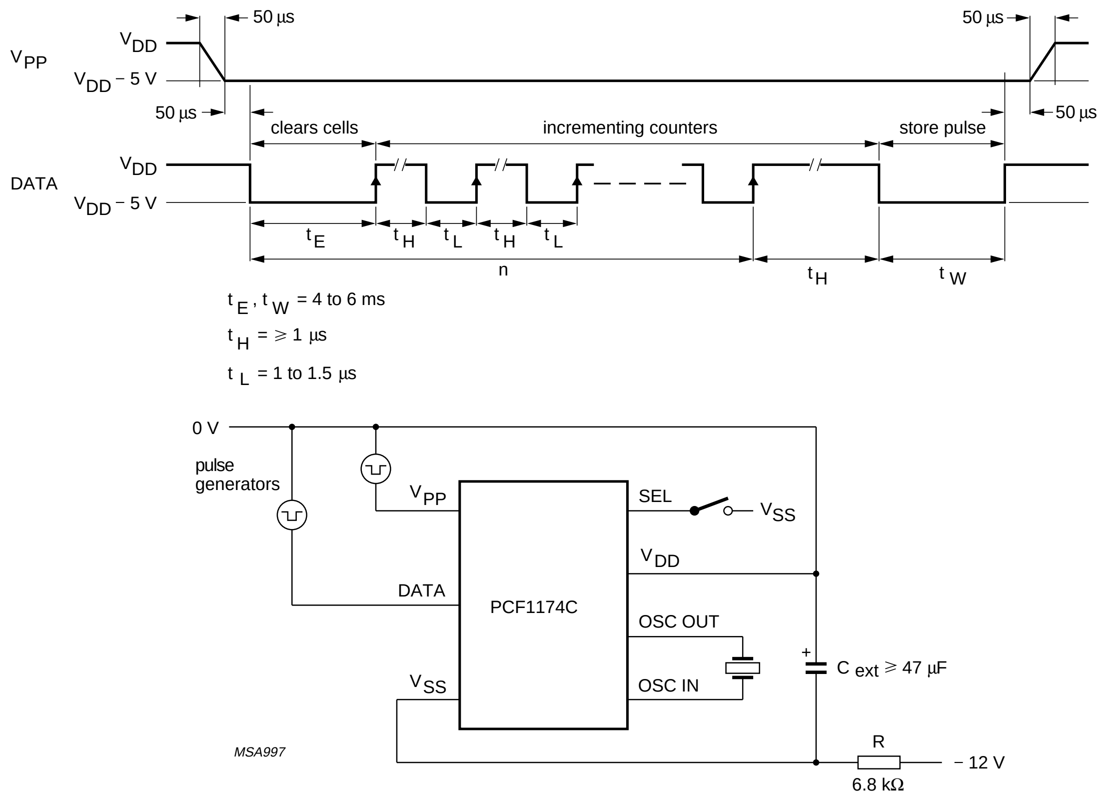


Fig.6 Programming diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	V_{SS} = 0 V; note 1	–	3	mA
V_I	input voltage	all pins except V_{PP} and DATA	–0.3	V_{DD} + 0.3	V
		pins V_{PP} and DATA	–3	V_{DD} + 0.3	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *“Data Handbook IC16, General, Handling MOS Devices”*.

CHARACTERISTICS

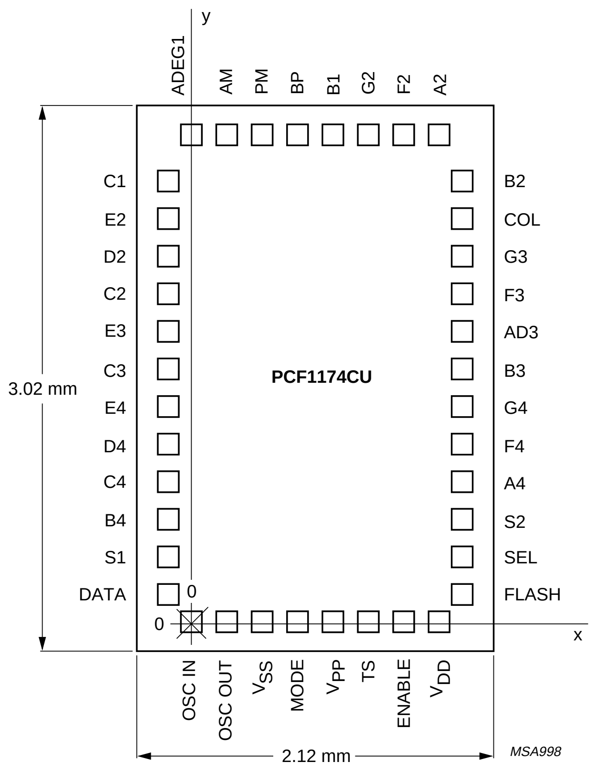
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = ±30 × 10^{-6}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	–	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	–0.35	–	%/K
		V_{DD} = 4.5 V	–	–16	–	mV/K
I_{DD}	supply current	note 1	700	950	–	µA
C_{EXT}	capacitance	external capacitor	47	–	–	µF
Oscillator						
t_{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60 × 10^{-6}	110 × 10^{-6}	
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	–	1 × 10^{-6}	
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		–	16	–	pF
C_o	output capacitance		–	27	–	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
I_{IL}	leakage current	FLASH, ENABLE, MODE	–	–	2	µA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	V_{PP} = V_{DD} – 5 V	70	–	700	µA
		during programming	–	500	–	µA
Backplane (high and low levels)						
R_{BP}	output resistance	±100 µA	–	–	3	kΩ
Segment						
R_{SEG}	output resistance	±100 µA	–	–	5	kΩ
LCD						
$V_{offset(DC)}$	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

Note

1. A suitable resistor (R) must be selected (example):
   a) V_{DD} = 5 V; R max. (12 V – 5 V)/700 µA = 10 kΩ.
   b) V_{DD} = 5 V; R typ. (12 V – 5 V)/900 µA = 7.8 kΩ (more reserve).
   c) I_{DD} must not exceed 3 mA.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 6.4 mm^2.

Bonding pad dimensions: 110 µm × 110 µm.

Chip thickness: 381 ±25 mm.

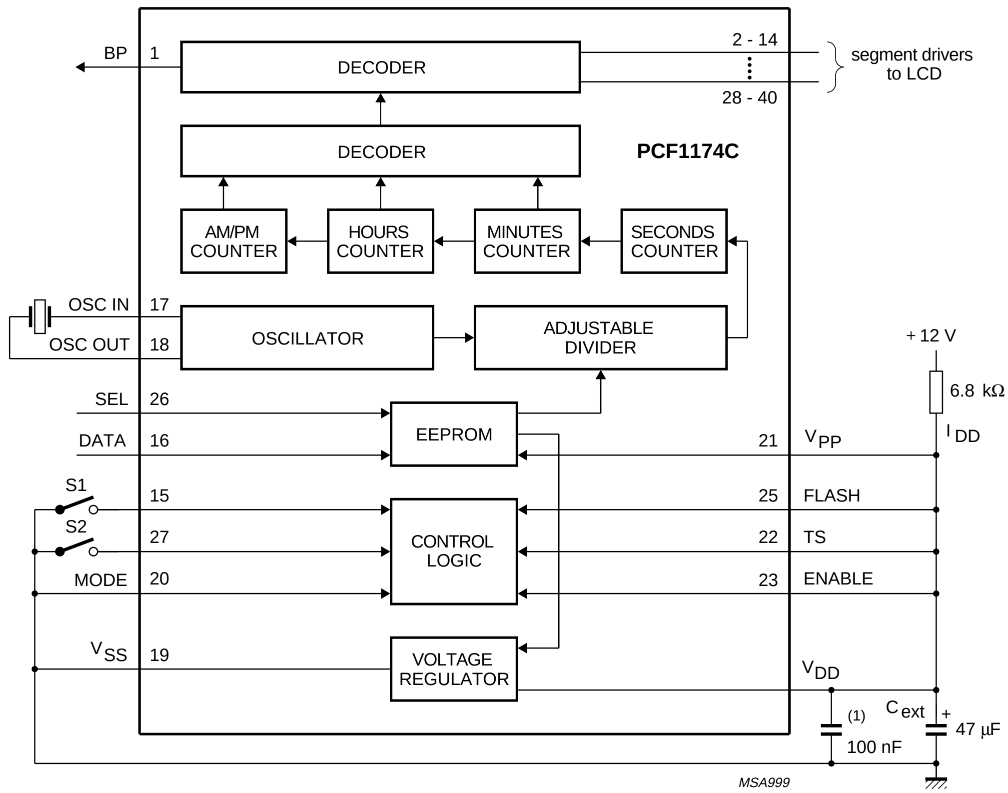
Fig.7 Bonding pad locations, PCF1174CU; 40 terminals.

Table 2 Bonding pad locations (dimensions in µm)

All x/y coordinates are referenced to the bottom left pad (OSC IN), see Fig.7.

PAD	x	y	PAD	x	y
BP	600	2676	V_{PP}	800	0
PM	400	2676	TS	1000	0
AM	200	2676	ENABLE	1200	0
ADEG1	0	2676	V_{DD}	1400	0
C1	–138	2448	FLASH	1538	168
E2	–138	2228	SEL	1538	388
D2	–138	2008	S2	1538	608
C2	–138	1808	A4	1538	808
E3	–138	1608	F4	1538	1008
C3	–138	1408	G4	1538	1208
E4	–138	1208	B3	1538	1408
D4	–138	1008	AD3	1538	1608
C4	–138	808	F3	1538	1808
B4	–138	608	G3	1538	2008
S1	–138	388	COL	1538	2208
DATA	–138	168	B2	1538	2448
OSC IN	0	0	A2	1400	2676
OSC OUT	200	0	F2	1200	2676
V_{SS}	400	0	G2	1000	2676
MODE	600	0	B1	800	2676
chip corner (max. value)	–360	–170			

APPLICATION INFORMATION

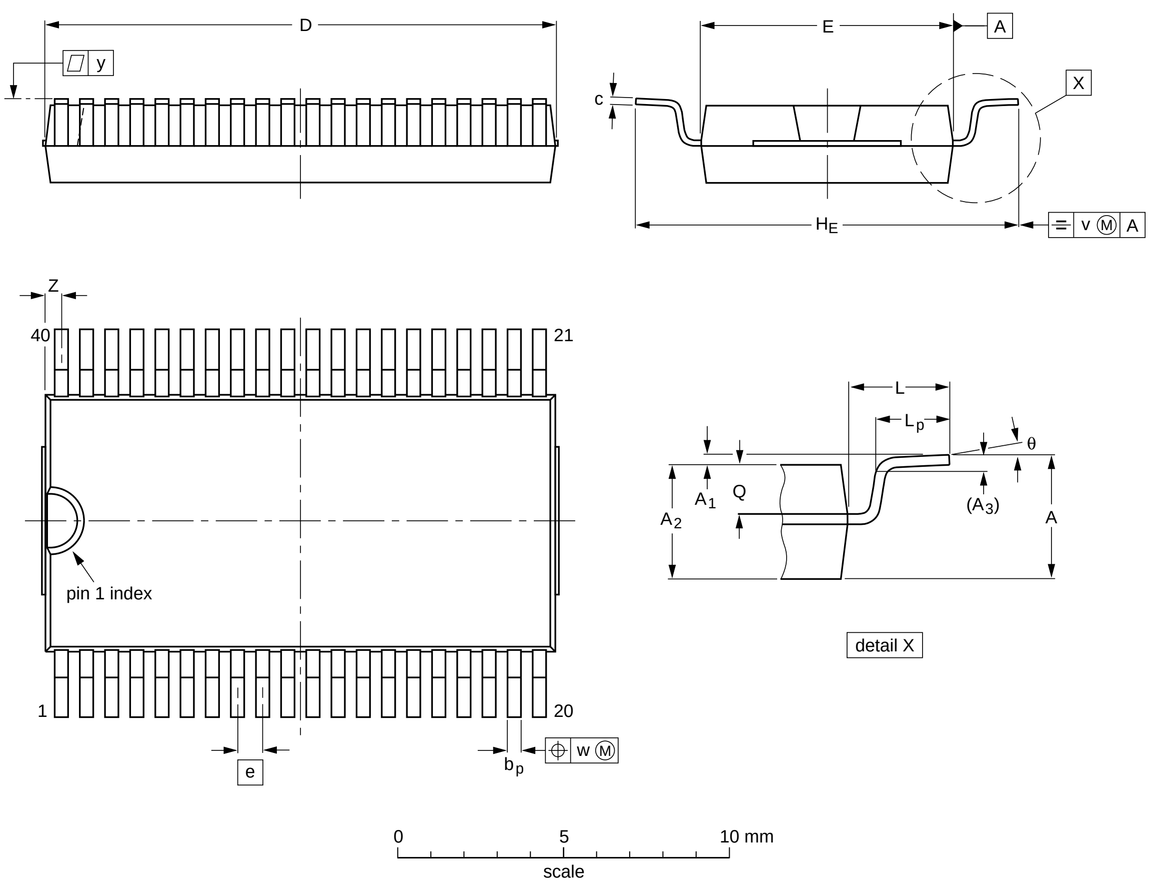


(1) To be placed close to the IC.

Fig.8 Typical application diagram.

PACKAGE OUTLINE

VSO40: plastic very small outline package; 40 leads; face down **SOT158-2**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Note

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-2						~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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