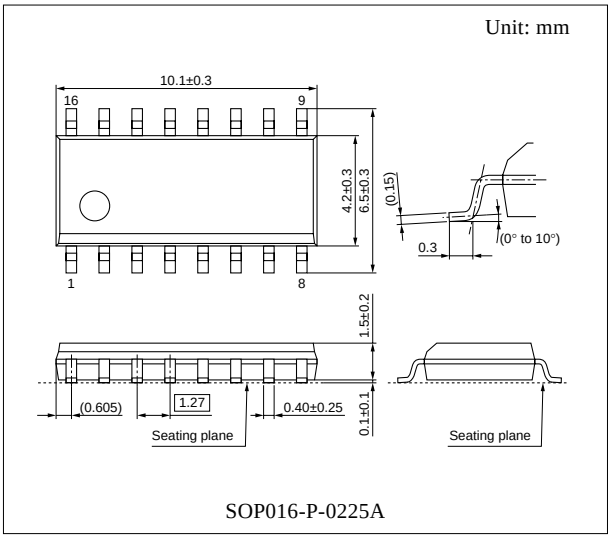
AN8041S

Liquid crystal backlight control IC

■ Overview

The AN8041S is an inverter control IC for liquid crystal backlight using PWM method. The output voltage of DC-DC converter and the current of cathode-ray tube can be controlled by using two error amplifiers, so that the system is designed easily.

Since the n-channel MOSFET can be directly driven, it is possible to construct a highly effective power supply.



SOP016-P-0225A

■ Features

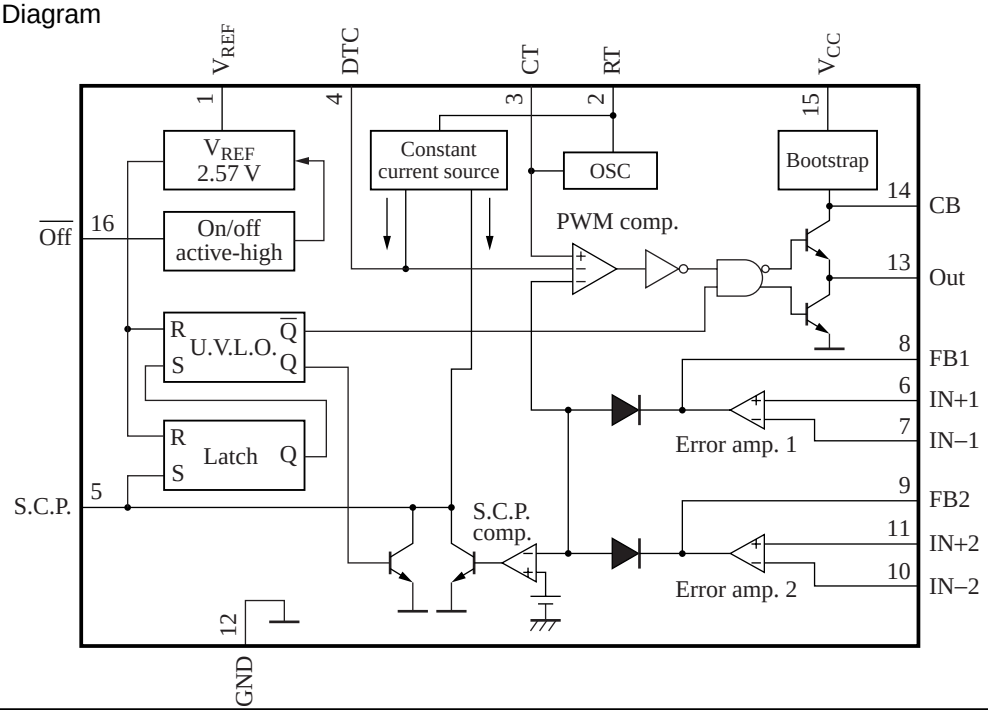
- Operating supply voltage: 3.6 V to 34 V *
- Totem pole output circuit: Output current of ±500 mA
- Built-in bootstrap circuit
- N-channel power MOSFET can be directly driven
- Built-in two error amplifier circuits allow both the voltage and current control
- Incorporating on/off functions (active-high control input, standby mode current is 5 μA or less)
- Built-in timer latch short-circuit protection circuit
- Maximum oscillation frequency: 500 kHz

Note) ∗: The voltage is limited to the range of 3.6 V to 17 V if used in a step-down circuit.

■ Applications

- LCD displays, digital still cameras, and PDAs

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	V_{REF}	Reference voltage output pin	7	IN–1	Error amplifier 1 inverted input pin
2	RT	Pin for connecting oscillator timing resistor	8	FB1	Error amplifier 1 output pin
			9	FB2	Error amplifier 2 output pin
3	CT	Pin for connecting oscillator timing capacitor	10	IN–2	Error amplifier 2 inverted input pin
			11	IN+2	Error amplifier 2 noninverted input pin
4	DTC	Dead-time control pin	12	GND	Grounding pin
5	S.C.P.	Pin for connecting the time constant setting capacitor for short-circuit protection	13	Out	Output pin
			14	CB	Bootstrap output circuit
			15	V_{CC}	Power supply voltage application pin
6	IN+1	Error amplifier 1 noninverted input pin	16	Off	On/off control pin

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	35	V
$\overline{\text{Off}}$ terminal application voltage	$V_{\overline{OFF}}$	35	V
Error amplifier input voltage	V_I	– 0.3 to V_{REF}	V
DTC terminal application voltage	V_{DTC}	– 0.3 to V_{REF}	V
Out terminal application voltage	V_{OUT}	35	V
CB terminal application voltage	V_{CB}	35	V
Out terminal constant output current	I_O	±100	mA
Out terminal peak output current	$I_{O(PEAK)}$	±500	mA
Power dissipation *	P_D	143	mW
Operating ambient temperature *	T_{opr}	–30 to +85	°C
Storage temperature *	T_{stg}	–40 to +125	°C

Note) *: Expect for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage (when using step-down circuit)	V_{CC}	3.6 to 17	V
Supply voltage (when using step-up circuit)	V_{CC}	3.6 to 34	V
Oscillation frequency	f_{OUT}	5 to 500	kHz
Oscillator timing resistance	R_T	5.1 to 30	kΩ
Oscillator timing capacitance	C_T	100 to 10 000	pF
Error amplifier input voltage	V_{IN}	– 0.1 to +0.8	V
Reference voltage output current	I_{REF}	–1 to 0	mA

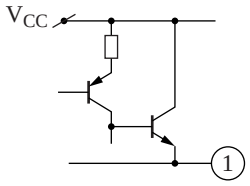
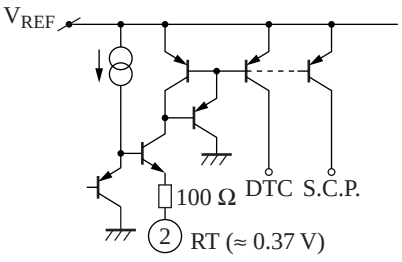
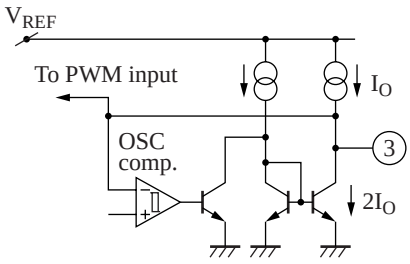
■ Electrical Characteristics at V_{CC} = 12 V, R_T = 15 kΩ, C_T = 120 pF, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage block						
Output voltage	V_{REF}	I_{REF} = –1 mA	2.483	2.57	2.647	V
Input regulation with input fluctuation	Line	V_{CC} = 3.6 V to 34 V	—	7	25	mV
Load regulation	Load	I_{REF} = – 0.1 mA to –1 mA	—	1	10	mV
Output voltage temperature characteristics 1	V_{TC1}	T_a = –30°C to +25°C	—	±1	—	%
Output voltage temperature characteristics 2	V_{TC2}	T_a = 25°C to 85°C	—	±1	—	%
Output short-circuit current	I_{OS}		—	–10	—	mA
U.V.L.O. block						
Circuit operation start voltage	V_{UON}		2.8	3.1	3.4	V
Hysteresis width	V_{HYS}		60	140	220	mV
Error amplifier block						
Input offset voltage	V_{IO}		–6	—	6	mV
Input bias current	I_B		–500	–25	—	nA
Common-mode input voltage range	V_{ICR}		– 0.1	—	0.8	V
High-level output voltage 1	V_{EH}		V_{REF} – 0.3	V_{REF} – 0.1	—	V
Low-level output voltage 1	V_{EL}		—	0.1	0.3	V
Output sink current	I_{SINK}	V_{FB} = 0.9 V	—	8	—	mA
Output source current	I_{SOURCE}	V_{FB} = 0.9 V	—	–110	—	µA
Open-loop gain	A_G		—	70	—	dB
Dead-time control circuit block						
Input current	I_{DTC}	R_T = 15 kΩ	–14.8	–12.3	–9.8	µA
Low-level input threshold voltage	V_{DT-L}	Duty = 0%	—	0.45	0.65	V
High-level input threshold voltage	V_{DT-H}	Duty = 100%	1.2	1.4	—	V
Output block						
Oscillation frequency	f_{OUT}	R_T = 15 kΩ, C_T = 120 pF	180	200	220	kHz
Output duty ratio	Du	R_{DTC} = 75 kΩ	45	50	55	%
Low-level output voltage	V_{OL}	I_O = 70 mA	—	1.0	1.3	V
High-level output voltage	V_{OH}	I_O = –70 mA	V_{CB}–2.0	V_{CB}–1.0	—	V
Frequency supply voltage characteristics	f_{dV}	f_{OUT} = 200 kHz, V_{CC} = 3.6 V to 34 V	—	±3	—	V
Frequency temperature characteristics 1	f_{dT1}	f_{OUT} = 200 kHz, T_a = –30°C to +25°C	—	±9	—	V
Frequency temperature characteristics 2	f_{dT2}	f_{OUT} = 200 kHz, T_a = 25°C to 85°C	—	±9	—	V

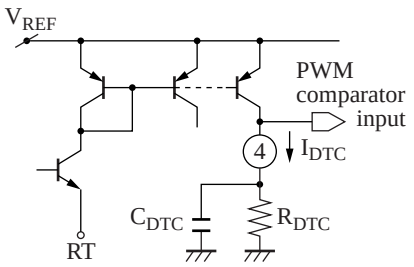
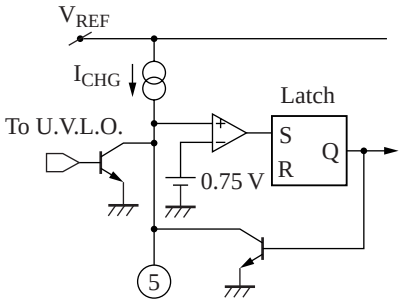
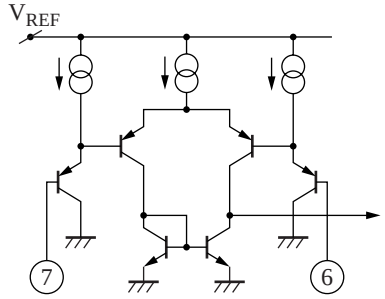
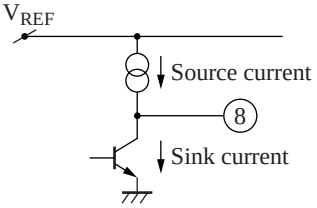
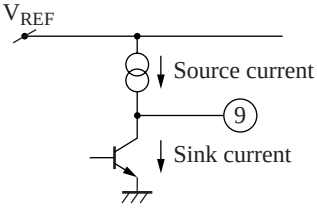
■ Electrical Characteristics at V_{CC} = 12 V, R_T = 15 kΩ, C_T = 120 pF, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bootstrap circuit block						
Input standby voltage	V_{INCB}	I_{CB} = −70 mA	V_{CC}−1.2	V_{CC}−1.0	V_{CC}− 0.8	V
Oscillator block						
RT terminal voltage	V_{RT}		—	0.37	—	V
Short-circuit protection block						
Input threshold voltage	V_{THPC}		0.70	0.75	0.80	V
Input standby voltage	V_{STBY}		—	30	120	mV
Input latch voltage	V_{IN}		—	30	120	mV
Charge current	I_{CHG}		–2.76	–2.3	–1.84	µA
Comparator threshold voltage	V_{THL}		—	1.82	—	V
On/off control block						
Threshold voltage	V_{TH}		0.8	—	2.0	V
Whole device						
Total consumption current	I_{CC}		—	3.9	5.0	mA
Standby current	$I_{CC(SB)}$		—	—	5	µA

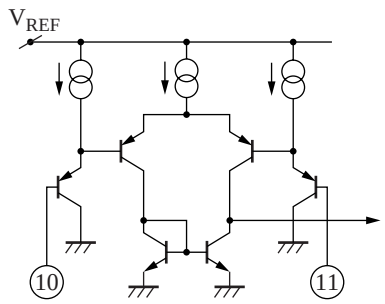
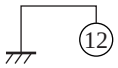
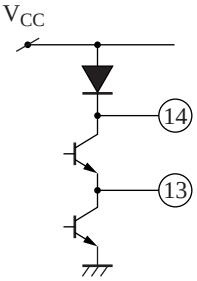
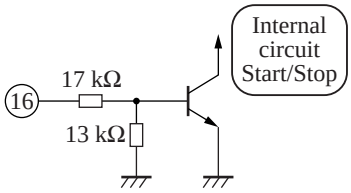
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1		V_{REF}: The reference voltage output terminal (2.57 V (allowance: ±3%)). Incorporating short-circuit protection against GND.	O
2		RT: The terminal used for connecting a timing resistor to set oscillator's frequency. Use a resistance value within the range of 5.1 kΩ to 30 kΩ. The terminal voltage is approx. 0.37 V.	—
3		CT: The terminal used for connecting a timing capacitor to set oscillator's frequency. Use a capacitance value within the range of 100 pF to 10 000 pF. For frequency setting method, refer to the " Application Notes, [3] Function descriptions " section. Use an oscillation frequency in the range of 5 kHz to 500 kHz.	—

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
4		DTC: The terminal for connecting a resistor and capacitor to set the dead-time and soft start period of PWM output. Input current I_{DTC} is determined by the timing resistor R_T , so that dispersion and fluctuation with temperature are suppressed. It is approx. –12.3 µA when R_T = 15 kΩ. $I_{DTC} = \frac{V_{RT}}{R_T} \times \frac{1}{2}$ [A]	—
5		S.C.P.: The terminal for connecting a capacitor to set the time constant of soft start and timer latch short-circuit protection circuit. Use a capacitance value in the range of more than 1 000 pF. The charge current I_{CHG} is determined by the timing resistor R_T , so that dispersion and fluctuation with temperature are suppressed. It is approx. –1.3 µA when R_T = 15 kΩ. $I_{CHG} = \frac{V_{RT}}{R_T} \times \frac{1}{11}$ [A]	—
6		IN+1: The noninverted input terminal of the error amplifier 1. For common-mode input, use in the range of – 0.1 V to +0.8 V.	I
7		IN–1: The inverted input terminal of the error amplifier 1. For common-mode input, use in the range of – 0.1 V to +0.8 V.	I
8		FB1: The output terminal of the error amplifier 1. Source current: approx. –120 µA Sink current : approx. 8 mA Correct the frequency characteristics of the gain and the phase by connecting a resistor and a capacitor between this terminal and IN–1 terminal.	O
9		FB2: The output terminal of the error amplifier 2. Source current: approx. –120 µA Sink current : approx. 8 mA Correct the frequency characteristics of the gain and the phase by connecting a resistor and a capacitor between this terminal and IN–2 terminal.	O

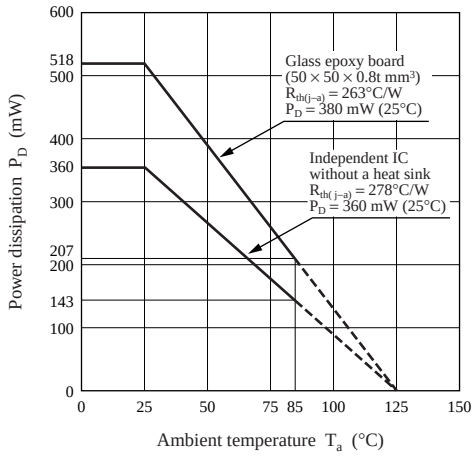
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
10		IN−2: The inverted input terminal of the error amplifier 2. For common-mode input, use in the range of − 0.1 V to +0.8 V.	I
11		IN+2: The noninverted input terminal of the error amplifier 2. For common-mode input, use in the range of − 0.1 V to +0.8 V.	I
12		GND: Grounding terminal.	—
13		Out: Totem pole type output terminal. A constant output current of ±100 mA and a peak output current of ±1 A can be obtained.	O
14		CB: Bootstrap output terminal. When using step-down circuit, connect the capacitor for boost between this terminal and the n-channel MOSFET source side of the switching device. When using step-up circuit, short circuit this terminal with V_{CC} terminal.	O
15		V_{CC}: Power supply application terminal.	I
16		Off: On/off control terminal. High-level input: normal operation ($V_{\overline{OFF}}$ > 2.0 V) Low-level input: standby condition ($V_{\overline{OFF}}$ < 0.8 V) The total consumption current can be suppressed to 10 µA or less.	I

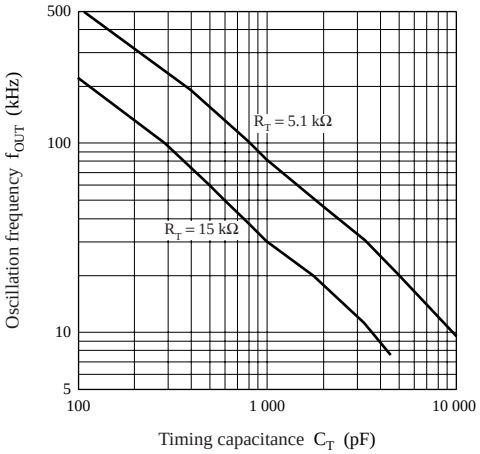
■ Application Notes

[1] Main characteristics

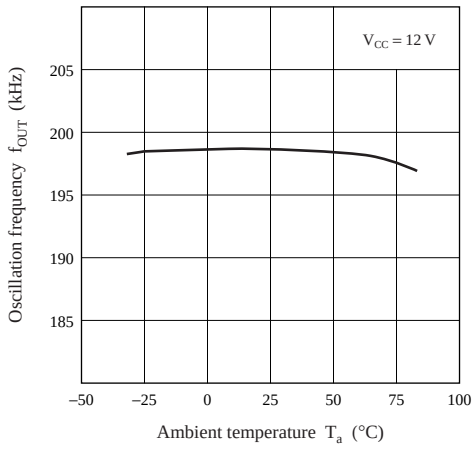
P_D — T_a



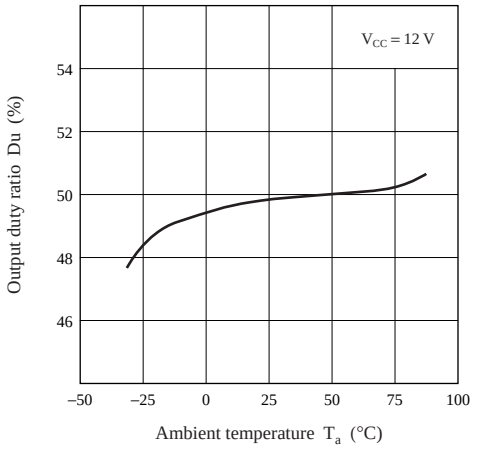
Oscillation frequency — Timing capacitance



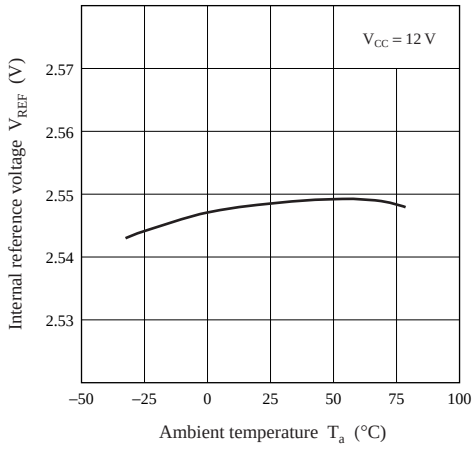
Oscillation frequency temperature characteristics



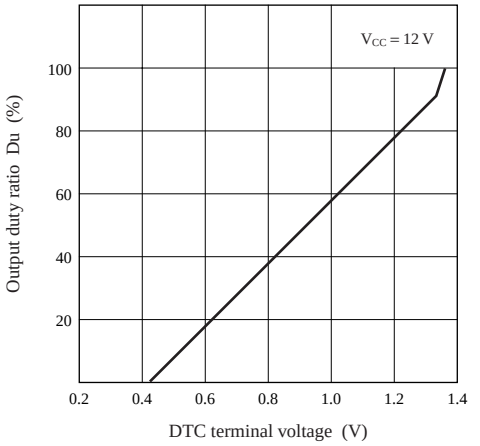
Output duty ratio temperature characteristics



Internal reference voltage temperature characteristics



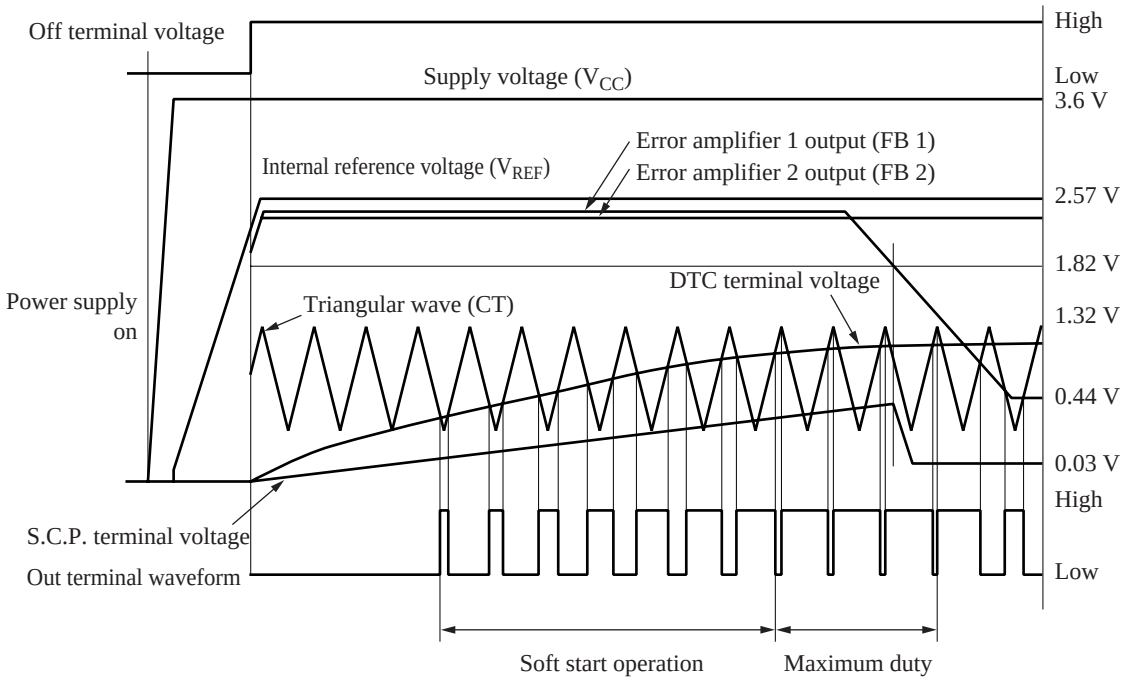
Output duty ratio — DTC terminal voltage



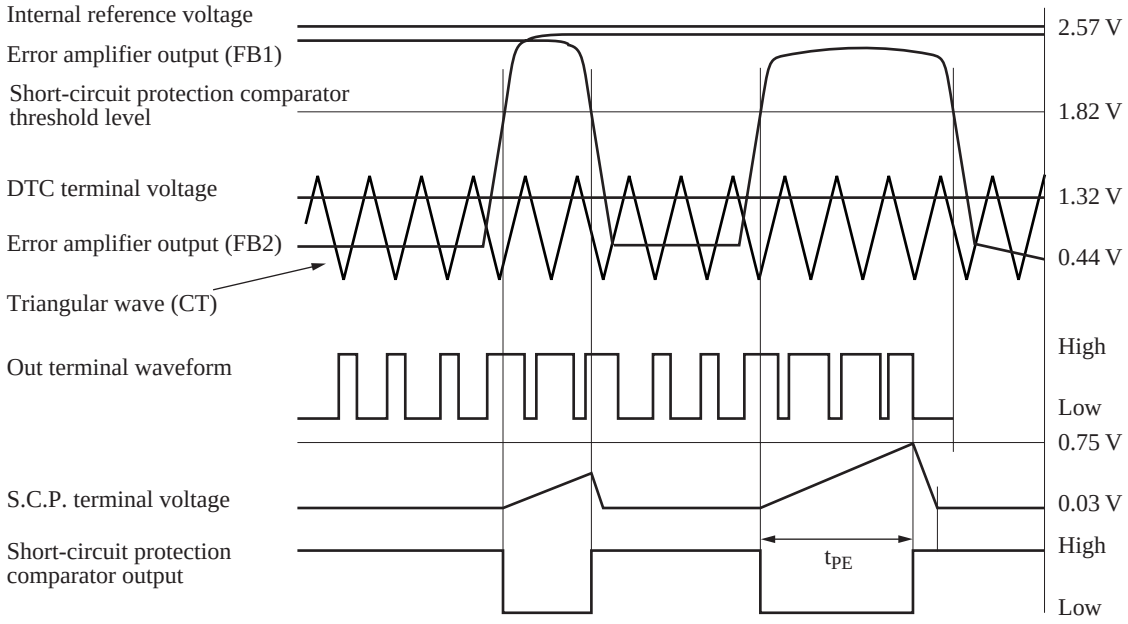
■ Application Notes (continued)

[2] Timing chart

1. PWM comparator operation waveform



2. Short-ciruit protection operation waveform



■ Application Notes (continued)

[3] Function descriptions

1. Reference voltage block

This block is composed of the band gap circuit, and outputs the temperature-compensated 2.57 V reference voltage to the V_{REF} terminal (pin 16). The reference voltage is stabilized when the supply voltage is 3.6 V or higher, and used as the operating power supply for the IC inside. It is possible to take out a load current of up to −1 mA.

2. Triangular wave oscillation block (OSC)

The triangular wave which swings from the upper limit value V_{OSCH} of approximately 1.32 V to the lowest limit value V_{OSCL} of approximately 0.44 V will be generated by connecting a timing capacitor C_T and a resistor R_T to the C_T terminal (pin 2) and R_T terminal (pin 3) respectively. The oscillation frequency can be arbitrarily decided by the value of timing capacitor C_T and resistor R_T connected externally. The oscillation frequency f_{OSC} is obtained by the following calculations:

$$f_{OSC} = \frac{1}{t_1 + t_2} = \frac{I_O}{2 \times C_T \times (V_{CTH} - V_{CHL})}$$

$$I_O = \frac{1.7 \times V_{RT}}{R_T} = \frac{1.7 \times 0.37}{R_T}$$

Since $V_{CTH} - V_{CTL} = 0.88$ V,

therefore $f_{OSC} \approx \frac{1}{2.80 \times C_T \times R_T}$ [Hz]

Example) When $C_T = 100$ [pF], $R_T = 15$ [kΩ],
$f_{OSC} \approx 238$ [kHz].

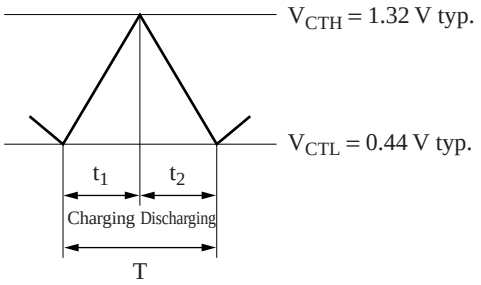


Figure 1. Triangular wave oscillation waveform

It is possible to use the circuit in the recommended operating range of 5 kHz to 500 kHz of the oscillation frequency. In addition, when the oscillation frequency becomes high, overshoot and undershoot are generated due to the operation delay of the triangular oscillation comparator. Care should be taken because the actual measurement values deviate from the above calculation values.

In the case of this IC, the output source current of S.C.P. terminal and DTC terminal are set by the timing resistor R_T externally attached to RT terminal. For this reason, the AN8041S can not be used as a slave IC when multiple ICs are synchronously operating in parallel.

3. Error amplifier 1 block and error amplifier 2 block

DC-DC output voltage and a detected lamp current of back-light are amplified through the PNP transistor input type error amplifier, and the amplified signal are inputted to PWM comparator.

Figure 2 shows the connection method of the error amplifier when the backlight inverter is controlled. Select the connection of error amplifier 1 block or 2 block arbitrarily.

The common-mode input range is from – 0.1 V to +0.8 V. The voltage which is resistor-dividing of the reference voltage is given to the noninverted input. Also, any desired gain setting and phase compensation can be obtained by connecting the feedback resistor and capacitor from the error amplifier output terminals (pin 8 and pin 9) to the inverted input terminals (pin 7 and pin 10).

The overshoot at operation start due to feedback delay can be suppressed by providing the large output source current (110 μA) and the large output sink current (8 mA).

The output voltage V_{OUT} and the detection voltage of the lamp current V_{C1} are given from the following calculation:

$$V_{IN+} = V_{REF} \times \frac{R_4}{R_3 + R_4}$$

$$V_{OUT} = V_{IN+1} \times \frac{R_1 + R_2}{R_2}$$

$$V_{C1} = V_{IN+2} \times \frac{R_5 + V_R + R_6}{R_5 + V_R}$$

■ Application Notes (continued)

[3] Function descriptions (continued)

3. Error amplifier 1 block and error amplifier 2 block (continued)

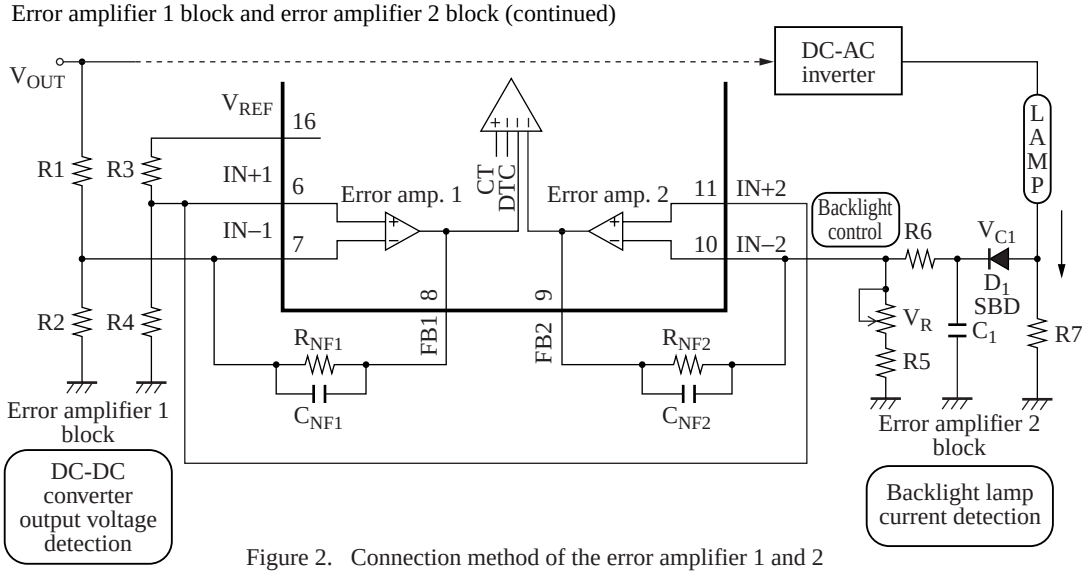


Figure 2. Connection method of the error amplifier 1 and 2

The control modes of backlight are described below:

1) Power-on mode

When the power supply is turned on, the DC-DC converter which is connected to the error amplifier 1 block starts the control.

The output voltage V_{OUT} which has been set by the equation in the previous page is reached, and the high voltage of several kV is generated in the lamp through the DC-AC inverter, and the backlight is lighted up. During this period, since the lamp current does not flow in the error amplifier 2 block, the error amplifier output (FB2) becomes high-level, so that its control does not work.

2) Normal control mode

When the backlight is turned on, discharging starts and the current starts to flow in the resistor R7.

When the voltage V_{C1} rectified by diode D1, and capacitor C1 reaches the voltage set by resistors R5, R6, and volume control V_R ; The control function is switched over from the error amplifier 1 block to the error amplifier 2 block. The output voltage of the DC-DC converter V_{OUT} decreases to a voltage lower than the set voltage, and the lamp voltage is maintained at several hundred volts.

3) Light-regulation operation mode

For the light regulation of the backlight, the "voltage light-regulation" method is used, and the light is regulated by the input voltage of the inverter. By adding volume V_R to the inverted input terminal of error amplifier 2 block to make the detection voltage V_{C1} variable, the input voltage of the inverter is regulated so as to make the lamp current variable for light regulation.

Also, the addition of the volume to the noninverted input side of the error amplifier makes the light regulation possible.

- Usage notes

When this IC is used to control the DC-DC converter, one of two error amplifiers is not used. Connection should be made so that the FB terminal is fixed to high-level as shown in figure 3.

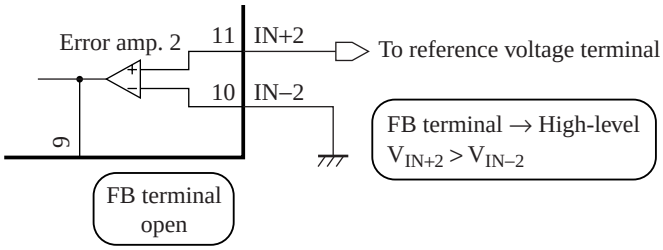


Figure 3. Connection when the error amplifier 2 block is not used

■ Application Note (continued)

[3] Function descriptions (continued)

4. Timer latch short-circuit protection circuit

When the short-circuit or overload of the power supply output continues for a certain period, this circuit prevents the parts such as external main switch device, flywheel diode, the choke coil from destruction or deterioration.

The short-circuit protection circuit is shown in figure 4. The timer latch short-circuit protection circuit detects the output level of the error amplifier 1 and 2 blocks. When either the DC-DC converter output voltage or the lamp current detection voltage is stable, the output of that error amplifier is stabilized and the short-circuit protection comparator also maintains balance.

When the load conditions are suddenly changed, and both of the outputs of the error amplifier 1 block and 2 block (FB1, FB2) become 1.82 V or higher, the short-circuit protection comparator outputs low-level and cut off the transistor Q1, thereby the external capacitor C_S of the S.C.P. terminal (pin 5) starts charging with current I_{CHG} given by the following equation:

$$V_{PE} = V_{STBY} + I_{CHG} \times \frac{t_{PE}}{C_S} \quad [V]$$

$$0.75\ V = 0.03\ V + I_{CHG} \times \frac{t_{PE}}{C_S}$$

$$C_S = I_{CHG} \times \frac{t_{PE}}{0.72} \quad [F]$$

I_{CHG} is constant current which is determined by the timing resistor R_T of the oscillator. It becomes approximately 2.3 µA when R_T = 15 kΩ.

$$I_{CHG} = \frac{V_{RT} \times 1}{R_T \times 11} \quad [A]$$

When the external capacitor C_S is charged to approximately 0.75 V, the latch circuit is set to fix the totem pole output terminal to low-level and sets the dead-time to 100%.

When the latch circuit is set, the S.C.P. terminal voltage is discharged to approximately 30 mV. However, once the latch circuit is set, it is not reset unless the power supply is turned off.

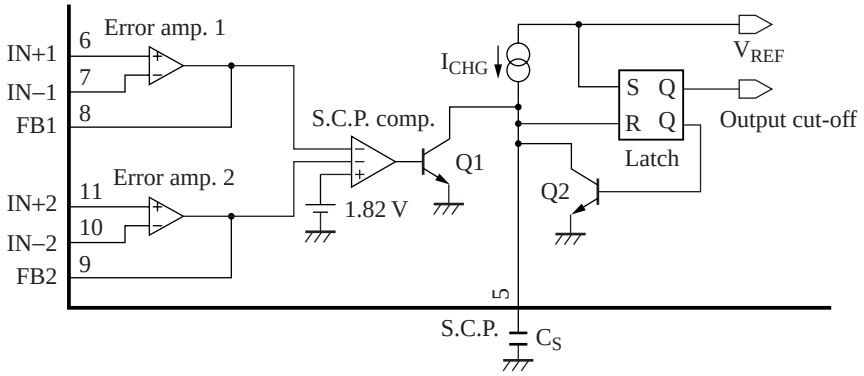


Figure 4. Short-circuit protection circuit

5. Low input voltage malfunction prevention circuit (U.V.L.O.)

When the supply voltage is dropped under the transient condition such as power-on or operation stop, this circuit protects the system from destruction or deterioration due to the malfunction of the control circuit.

This circuit detects the internal reference voltage which varies according to the supply voltage level. During the period from the time when the supply voltage starts to rise and to the time when it reaches 3.1 V, it keeps the dead-time of the Out terminal (pin 13) to 100% and maintains the DTC terminal (pin 4) and the S.C.P. terminal (pin 5) at low-level. When the supply voltage falls, it holds the hysteresis width of 140 mV and operates at a voltage under 2.96 V.

■ Application Notes (continued)

[3] Function descriptions (continued)

6. Remote circuit

The IC control function can be turned on or off by the external control. When the voltage of Off terminal (pin 16) is set under approximately 0.8 V, the internal reference voltage falls to stop the IC control function, and decrease the circuit current to a value under 5 µA, When the voltage of Off terminal is set at a value higher than approximately 2.0 V, the internal reference voltage rises, and starts the control operation.

7. PWM comparator block

The PWM comparator controls the on-period of the output pulse according to the input voltage. While the voltage of triangular wave of the CT terminal (pin 3) is lower than any one of the output of the error amplifier 1 and 2 block (pin 8 and pin 9) and the voltage of the DTC terminal (pin 4), it sets the Out terminal (pin 13) to high-level so that the switching device (n-channel MOSFET) turns on .

The dead-time is set by regulating the DTC terminal voltage V_{DTC} as shown in figure 5.

The DTC terminal is of a constant current output using the resistor R_T, so that the V_{DTC} is regulated by connecting the external resistor R_{DTC} between the DTC terminal and GND terminal.

At the oscillation frequency f_{OSC} of 200 kHz, the output duty ratio becomes 0% when V_{DTC} = 0.44 V typical, and 100% when V_{DTC} = 1.32 V typical.

However, pay attention to the peak value V_{CTH} and the trough value V_{CTL} of the triangular wave because their overshoot and undershoot amount differ depending on the oscillation frequency.

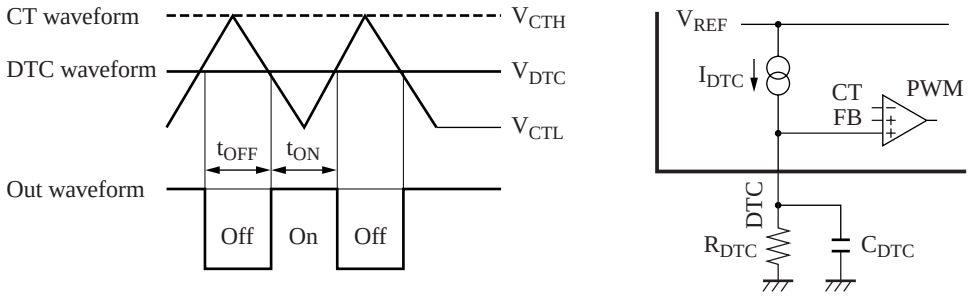


Figure 5. Setting the dead-time

The output duty ratio Du and the DTC terminal voltage V_{DTC} are given in the following equation:

$$Du = \frac{t_{ON}}{t_{ON} + t_{OFF}} \times 100 \ [\%] = \frac{V_{DTC} - V_{CTL}}{V_{CTH} - V_{CTL}} \times 100 \ [\%]$$

$$I_{DTC} = \frac{V_{RT}}{R_T} \times \frac{1}{2} \ [A]$$

$$V_{DTC} = I_{DTC} \times R_{DTC} = V_{RT} \times \frac{R_{DTC}}{R_T} \times \frac{1}{2} \ [A]$$

Example) When f_{OSC} = 200 [kHz] (R_T = 15 kΩ, C_T = 150 pF), R_{DTC} = 75 [kΩ]
$V_{CTH} \approx 1.32$ [V], $V_{CTL} \approx 0.44$ [V], $V_{DTC} \approx 0.37$ [V]
Therefore $I_{DTC} \approx 12.3$ [µA]
$V_{DTC} \approx 0.925$ [V]
Du ≈ 55.1 [%]

In addition, the operation delay of the PWM comparator, the deviation of the peak and trough triangular oscillation value may cause the deviation of the actual measurements value from the theoretical value. So, regulation on IC-mounted PCB should be required.

By adding the external resistor R_{DTC} and capacitor C_{DTC} , the soft start function can be installed, which gradually broadens the on-period of the output pulse at the time of the power supply operation start. The soft start operation prevents the overshoot of DC-DC comparator output.

■ Application Notes (continued)

[3] Function descriptions (continued)

8. Output block, bootstrap circuit

In the case of the step-down type DC-DC converter control, the bootstrap circuit is required if n-channel MOSFET is used as the switching device.

The bootstrap circuit is used for keeping the voltage between the gate and the source higher than the gate threshold voltage of n-channel MOSFET by increasing the high-level of the Out terminal (pin 13) to a level higher than V_{CC} when turning on the n-channel MOSFET. The output block including the external circuit and the bootstrap circuit are shown in figure 6, and the operation waveform in figure 7.

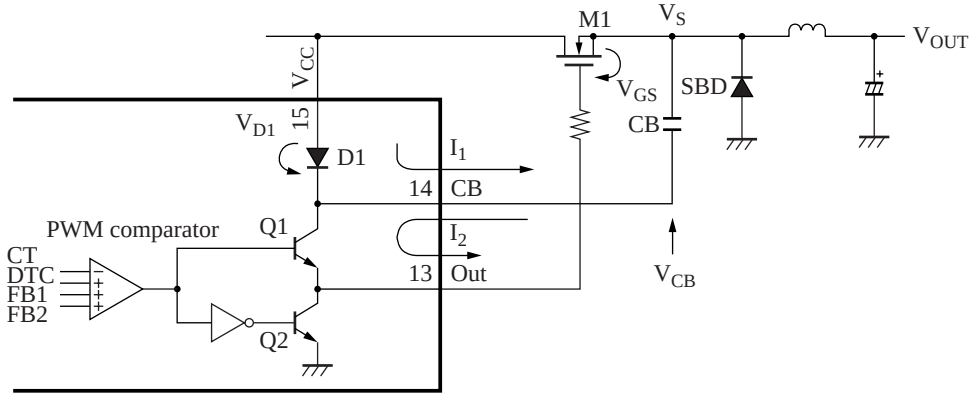


Figure 6. Output block and bootstrap circuit

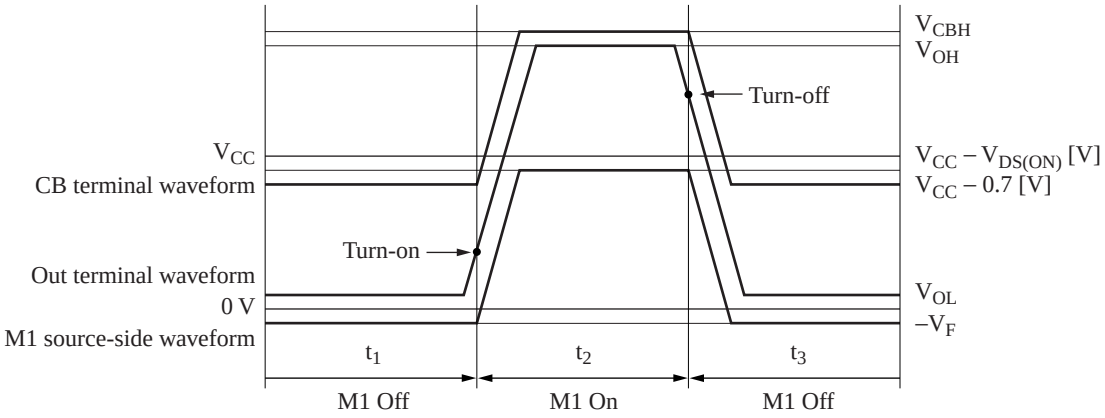


Figure 7. Bootstrap circuit operation waveform

The bootstrap circuit operation is described below.

1) N-channel MOSFET (M1) off time: t_1

While the M1 is off, energy is being supplied from the schottky barrier diode (SBD) to the choke coil, and the M1 source side voltage V_S is fixed to $-V_F$. The capacitor for boost C_B is charged from the V_{CC} terminal (pin 15) through the diode inside the IC (D1). The CB terminal voltage (pin 14) V_{CB} is given by the following equation:

$V_S = -V_F$

$V_{CB} = V_{CC} - V_{D1}$

V_F : forward voltage of SBD

V_{D1}: forward voltage of D1

Therefore, the charged voltage of boost C_B is given by the following equation:

$V_{CB} - V_S = V_{CC} - V_{D1} + V_F$

■ Application Notes (continued)

[3] Function descriptions (continued)

8. Output block, bootstrap circuit (continued)

2) N-channel MOSFET (M1) turn-on time: t_2

When the PWM comparator output reverses, the Out terminal (pin 13) is switched over to high-level. The Out terminal voltage V_O rises toward the CB terminal voltage.

$$V_O = V_{CB} - V_{CE}\ (sat)$$

At that time, M1 voltage between the gate and source becomes:

$$V_{GS} = V_O + V_F$$

When the Out terminal voltage V_O rises to the gate threshold voltage, the M1 is turned on. The M1 source-side voltage after the turn-on rises to the value expressed in the following equation:

$$V_S = V_{CC} - V_{DS(ON)}$$

Since the bootstrap capacitor C_B is connected between the M1 source-side and the CB terminal, the CB terminal voltage is capacitance-coupled, and rises according to the M1 source-side voltage. It is expressed in the following equation:

$$V_{CB} = V_S + V_{CC} - V_{D1} + V_F$$
$$= 2 \times V_{CC} - V_{D1} + V_{DS(ON)} + V_F$$

3) N-channel MOSFET (M1) turn-off time: t_3

The Out terminal voltage drops to the saturation voltage of the transistor Q1 and it is turned off.

The M1 source side voltage decreases to $-V_F$, and in the same way the CB terminal voltage is capacitance-coupled, and drops to $V_{CC} - V_{D1}$ volt, and returns to the condition described in a).

- Bootstrap circuit usage notes

(1) Operating supply voltage range when the step-down circuit is used

When the step-down circuit is used for the DC-DC converter control : As described in the above, when the n-channel MOSFET of the switching device turns on, the voltage of CB terminal (pin 14) rises to the voltage about two times higher than the V_{CC} . Since the allowable applied voltage for the CB terminal is 35 V, use the boost circuit at an operating supply voltage of 3.6 V or more.

$$V_{CB} = 2 \times V_{CC} - V_{D1} - V_{DS(ON)} + V_F < 35\ [V]$$

$$V_{CC} < \frac{35 + V_{D1} + V_{DS(ON)} - V_F}{2}\ [V]$$

$$< 17\ [V]$$

(2) Value setting for bootstrap capacitor

The bootstrap capacitor is capacitors-coupled with the n-channel MOSFET source-side at its turn-on time to increase the CB terminal voltage over the V_{CC} . At this time, the bootstrap capacitor is discharged by the n-channel MOSFET gate drive current. If the capacitance value of the bootstrap capacitor is set at too low value, it causes the efficiency decrease due to increase in switching loss.

Therefore, set the capacitance at a sufficiently high value compared with the n-channel MOSFET gate input capacitance.

$$CB >> Ciss$$

Study with the actual mounting board and set the optimum value.

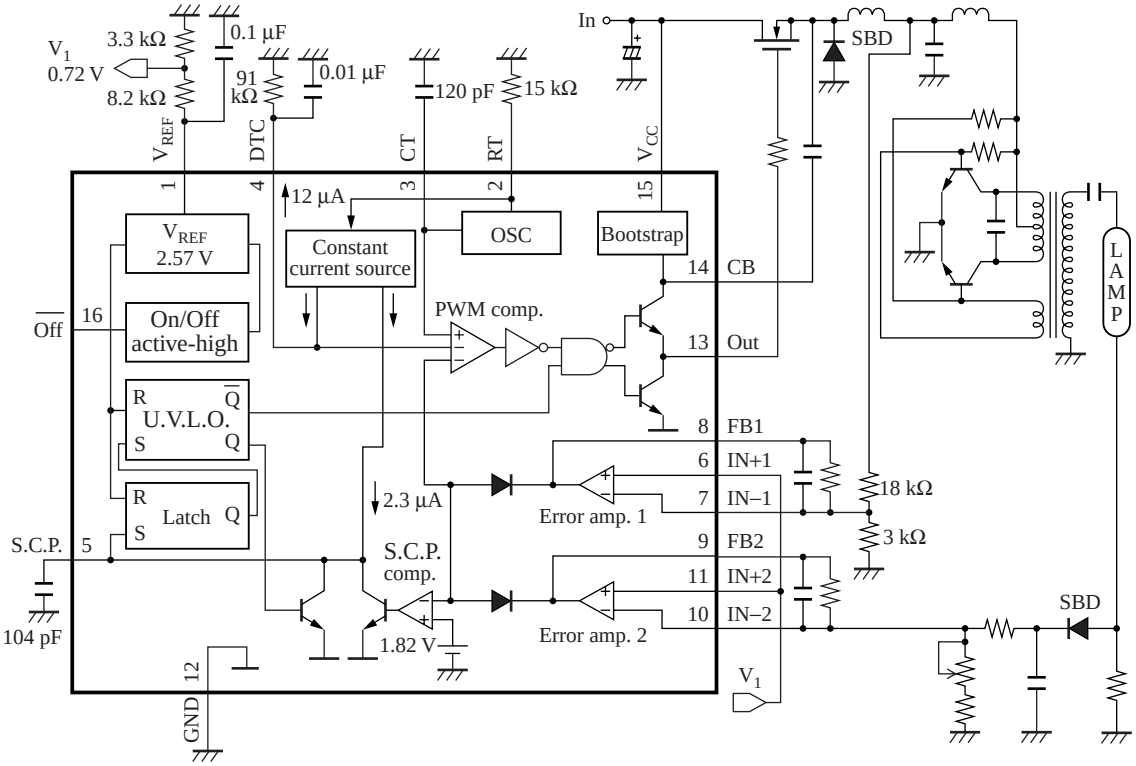
(3) CB terminal connection when the booster circuit is used

In the case of using the step-up type DC-DC converter control, the bootstrap circuit is not required since the n-channel MOSFET source side is grounded. Therefore, use it by short-circuiting the CB terminal (pin 14) to the V_{CC} terminal (pin 15).

For that reason, the operating supply voltage range is 3.6 V to 34 V in the case of using the step-up circuit type.

■ Application Circuit Examples

• Inverter control for liquid crystal backlight



• DC-DC converter control (step-up circuit example)