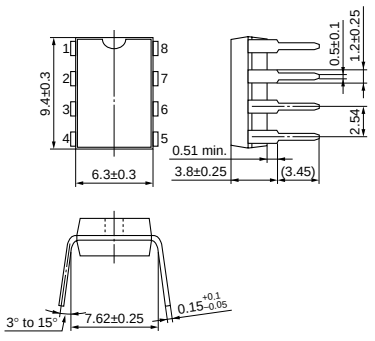
AN8038, AN8038S

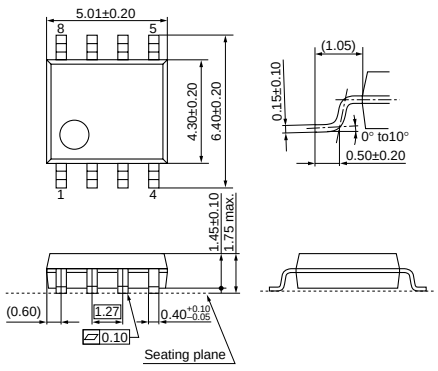
AC-DC switching power supply control IC with RCC local resonance circuit for improved conformance with energy conservation laws

AN8038 Unit: mm



DIP008-P-0300B

AN8038S Unit: mm



SOP008-P-0225C

■ Overview

The AN8038 and AN8038S are self-excited AC-DC switching power supply control IC that adopt RCC local resonance control. These ICs are designed to achieve high efficiency over a wide range of loads (light loads at the standby mode to heavy loads) for improved conformance with energy conservation laws, and support input levels used worldwide. They are particularly appropriate for use in AV and OA equipments.

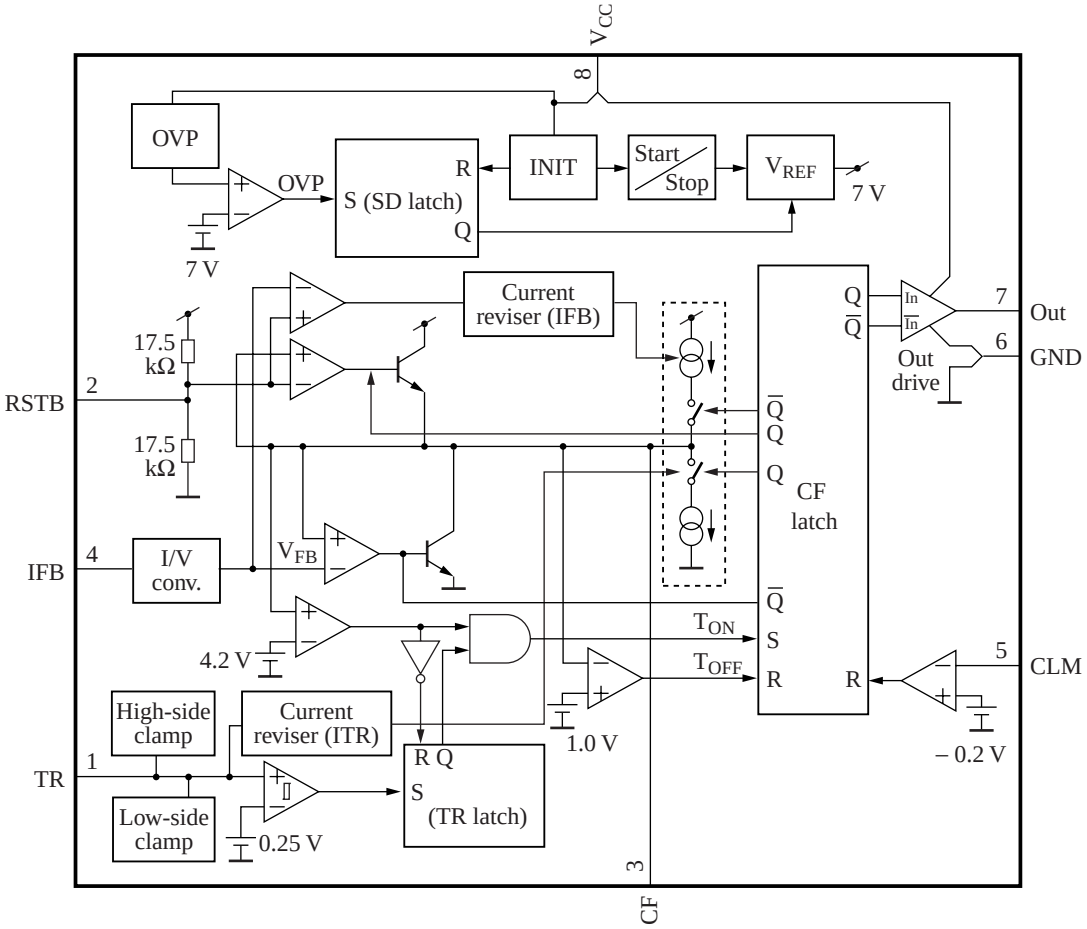
■ Features

- Supports improved conformance with energy conservation laws by providing two operating modes.
  With external resistors, it is possible to set the operating point at which the modes change over according to the load power, as shown below.
  1. Continuous (RCC) mode
     High efficiency achieved with local resonance operation (zero cross detection).
  2. Discontinuous mode (standby) mode
     Reduced switching loss and standby power due to reduced frequency
- Input voltage correction function. This function corrects the maximum on-period in a manner inversely proportional to the input voltage.
- Built-in overvoltage protection function (detects at V_{CC} pin)
- Pulse-by-pulse overcurrent protection function (single detection per one cycle)
- Packages: 8-pin DIP ···AN8038
  8-pin SOP ···AN8038S

■ Applications

- Facsimiles and other OA equipment
- Printers and other personal computer peripheral equipment
- AV equipment

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description
1	TR	Transformer reset. When a transformer reset is detected, i.e., a low level is input to this pin, the IC output goes high. However, the transformer reset signal is ignored during the minimum off-period determined by the CF pin. The maximum on-period is also corrected according to the current flowing out of this pin.
2	RSTB	Adjusts the light-load detection level that determines the when the IC switches from RCC to discontinuous operation. When the voltage (V_{FB}) which is I-V conversion of current feedback signal from IFB pin goes up higher than this pin, minimum off-period current at CF pin decreases, and operating frequency decreases. The detection level can be adjusted arbitrarily using an external pull-down resistor.
3	CF	Connection for the capacitor that determines the on and off periods for the IC output (Out).
4	IFB	Input for the current feedback signal from the power supply output photocoupler
5	CLM	Input of the pulse-by-pulse overcurrent protection circuit. Normally, it will be necessary to add an external filter for this input.
6	GND	Ground
7	V_{OUT}	Output to drive a power MOSFET directly
8	V_{CC}	Power supply. This pin watches V_{CC} , and has operating threshold voltages for the start, stop, OVP, and OVP reset levels.

■ Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Supply voltage		V_{CC}	28	V
Peak output current		I_{OP}	−1, +2	A
Power dissipation (Independent IC without a heat sink)	AN8038	P_D (T_a = 25°C)	500	mW
		P_D (T_a = 85°C)	260	
	AN8038S	P_D (T_a = 25°C)	306 *1	
		P_D (T_a = 85°C)	122 *2	
Operating temperature		T_{opr}	−30 to +85	°C
Storage temperature		T_{stg}	−55 to +150	°C

Note) ∗1: When mounted on a printed circuit board: 477 mW
∗2: When mounted on a printed circuit board: 191 mW

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	From the stop voltage to the OVP operating voltage	V

■ Electrical Characteristics at V_{CC} = 18 V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low voltage protection (U.V.L.O.) initial startup supply voltage.	Start V_{CC}		12.9	14.4	15.9	V
Low voltage protection (U.V.L.O.) operation stop supply voltage	Stop V_{CC}		8.0	8.9	9.8	V
Overvoltage protection (OVP) operating supply voltage	OVP V_{CC}		18.7	20.5	22.3	V
Overvoltage protection (OVP) release supply voltage	OVPC V_{CC}		6.6	7.5	8.4	V
Overvoltage protection (OVP) operating time circuit current 1	OVP I_{CC1}	V_{CC} = 22 V → 10 V	0.4	0.53	0.66	mA
Overvoltage protection (OVP) operating time circuit current 2	OVP I_{CC2}	V_{CC} = 22 V → 18 V	1.3	1.7	2.1	mA
Transformer reset detection (TR) threshold voltage	TR V_{TH}		0.15	0.25	0.35	V
Transformer reset detection (TR) upper limit clamp voltage	TR V_{CLH}	I_{TR} = 1 mA	1.2	1.5	1.8	V
Transformer reset detection (TR) lower limit clamp voltage	TR V_{CLL}	I_{TR} = –1 mA	– 0.3	– 0.15	0	V
Transformer reset detection (TR) pin source current	TR I_{TR}	V_{TR} = 0.5 V	–5	0	—	µA
Overcurrent protection (CLM) threshold voltage	CLM V_{TH}		–225	–205	–185	mV
Oscillator (CF) maximum on-period current gain	CF GI_{ON}	I_{FB} = Open	0.8	1.0	1.2	—
Oscillator (CF) maximum on-period current	CF I_{ON}	I_{TR} = 0 mA	210	280	350	µA
Oscillator (CF) minimum off-period current 1	CF I_{OFF1}	I_{IFB} = – 0.7 mA	–1 560	–1 250	–940	µA
Oscillator (CF) minimum off-period current 2	CF I_{OFF2}	I_{IFB} = –1.3 mA	–70	–55	–40	µA
Output oscillator frequency	f_{OSC}	CF = 1 000 pF, I_{TR} = –450 µA I_{IFB} = – 0.5 mA	105	140	175	kHz
Standby pin (RSTB) voltage	V_{RSTB}		3.2	3.5	3.8	V
Standby operation (RSTB) threshold voltage	RSTB V_{TH}		0.3	0.5	0.7	V
Current feedback pin (IFB) voltage	V_{IFB}	I_{IFB} = – 0.7 mA	5	5.6	6.2	V
Pre-startup low-level output voltage	STB V_{OL}	V_{CC} = 12 V	—	1.0	1.25	V
Low-level output voltage	V_{OL}	I_{OUT} = 0.2 A	—	0.9	2.0	V
High-level output voltage	V_{OH}	I_{OUT} = – 0.1 A	15.5	16.3	—	V
Circuit current during startup 1	I_{START1}		120	190	280	µA
Circuit current 1	OPR1 I_{CC1}	V_{CC} = 10 V	6.1	8.7	11.3	mA
Circuit current 2	OPR2 I_{CC2}	V_{CC} = 18 V	6.4	9.1	11.8	mA

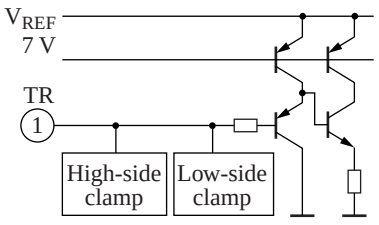
■ Electrical Characteristics at V_{CC} = 18 V, T_a = 25°C (continued)

• Design Reference Data

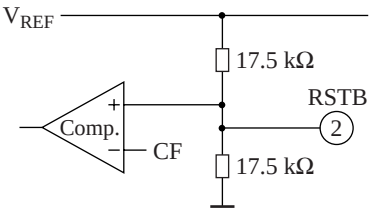
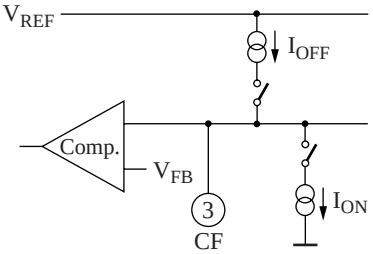
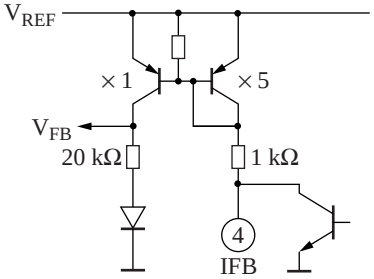
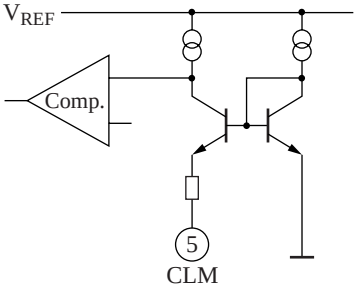
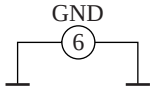
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low-voltage protection (U.V.L.O.) start/stop supply voltage difference	ΔV_{CC}		—	5.4	—	V
Transformer reset (TR) detection threshold hysteresis width	TR ΔV_{TH}		—	0.1	—	V
Oscillator (CF) upper limit voltage	V_{CLH}	I_{IFB} = – 0.5 mA, C_F = 1 000 pF	—	4.2	—	V
Oscillator (CF) lower limit voltage 1	V_{CFL1}	I_{IFB} = – 0.5 mA, C_F = 1 000 pF	—	1.0	—	V
Oscillator (CF) lower limit voltage 2	V_{CFL2}	I_{IFB} = – 0.2 mA, C_F = 1 000 pF	—	0.1	—	V
Maximum on-period	$t_{ON(max)}$	I_{IFB} = – 0.2 mA, C_F = 1 000 pF V_{TR} = 0.1 V	—	12	—	µs
Minimum off-period 1	$t_{OFF(min)1}$	I_{IFB} = – 0.2 mA, C_F = 1 000 pF V_{TR} = 0.1 V	—	2.6	—	µs
Minimum off-period 2	$t_{OFF(min)2}$	I_{IFB} = –1.3 mA, C_F = 1 000 pF I_{TR} = –450 µA	—	67	—	µs
Light-load oscillator frequency	f_{OSC2}	I_{IFB} = –1.3 mA, C_F = 1 000 pF I_{TR} = –450 µA	—	15	—	kHz
Output rise time	t_r	10% to 90%, I_{OUT} = 0 mA	—	40	—	ns
Output fall time	t_f	10% to 90%, I_{OUT} = 0 mA	—	20	—	ns
TR output response time	t_{TR}		—	400	—	ns
CLM output response time	t_{CLM}		—	100	—	ns
Circuit current during startup 2	I_{START2}	T_a = –30°C to +85°C	100	190	300	µA

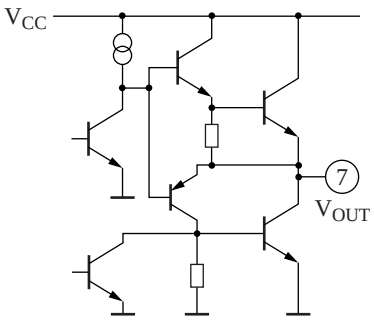
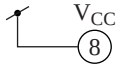
■ Terminal Equivalent Circuits

Pin No.	Equivalent Circuit	Description	I/O
1		TR: Transformer reset detection input. When a transformer reset is detected, i.e., a low level is input to this pin, the IC output goes high. However, the transformer reset signal is ignored if the signal is shorter than the minimum off-period determined by the C_F pin. Also note that the maximum on-period is corrected according to the source current.	I

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent Circuit	Description	I/O
2		RSTB: Adjusts the light-load detection level that determines the time when the IC switches from RCC to discontinuous operation. When the voltage which is I-V conversion of current feedback signal goes up higher than this pin, operating frequency is reduced. An arbitrary level can be set by inserting an external pull-down resistor.	—
3		CF: Connection for the capacitor that determines the on- and off-periods of the IC output (Out). The on- and off-periods are corrected by I_{ON} which is proportional to the flowing out current at the TR pin, and I_{OFF} which corresponds to the current at IFB pin.	—
4		IFB: Connection for the photocoupler used for the power supply output error-voltage feedback. This input can decrease the photocoupler dark current by about 250 μA.	I
5		CLM: Input to the pulse-by-pulse overcurrent protection circuit. Normally, we recommend adding an external filter for this input.	I
6		GND: IC ground.	—

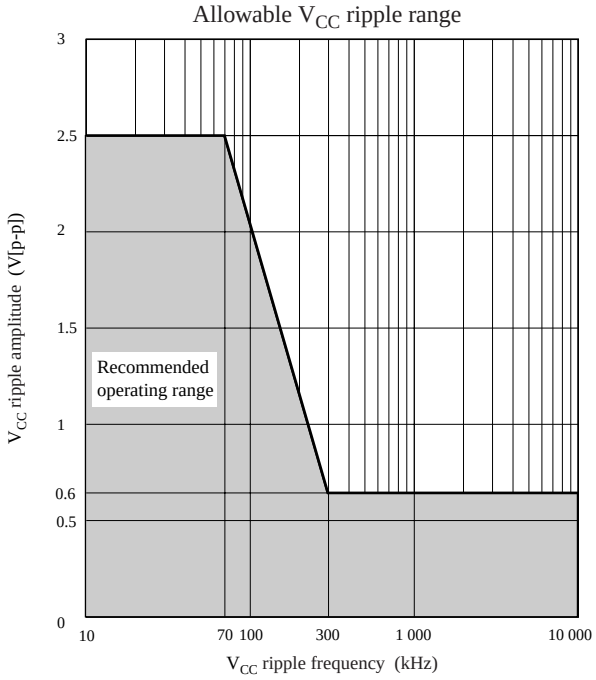
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent Circuit	Description	I/O
7		V_{OUT}: Output used to directly drive a power MOSFET. A totem pole structure is adopted in this output circuit. The absolute maximum ratings for the output current are: Peak: +2 A, –1 A DC: +200 mA, –100 mA	I
8		V_{CC}: Power supply. This pin monitors supply voltage and has the threshold for the start, stop, OVP, and OVP reset levels.	—

■ Usage Notes

The circuit current during startup is set to a low level to minimize power loss due to the startup resistor. However, V_{CC} ripple caused by the power transistor switching on and off may result in incorrect operation of the U.V.L.O. circuit and failure to start.

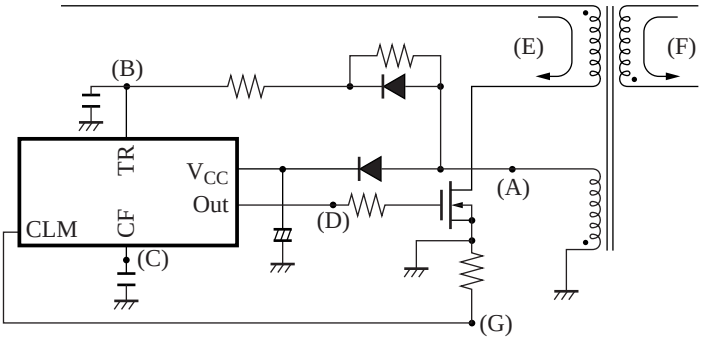
The figure shows the allowable range for V_{CC} ripple. Insert a capacitor near the IC's V_{CC} and GND pins to reduce V_{CC} ripple so that it remains within the allowable range.



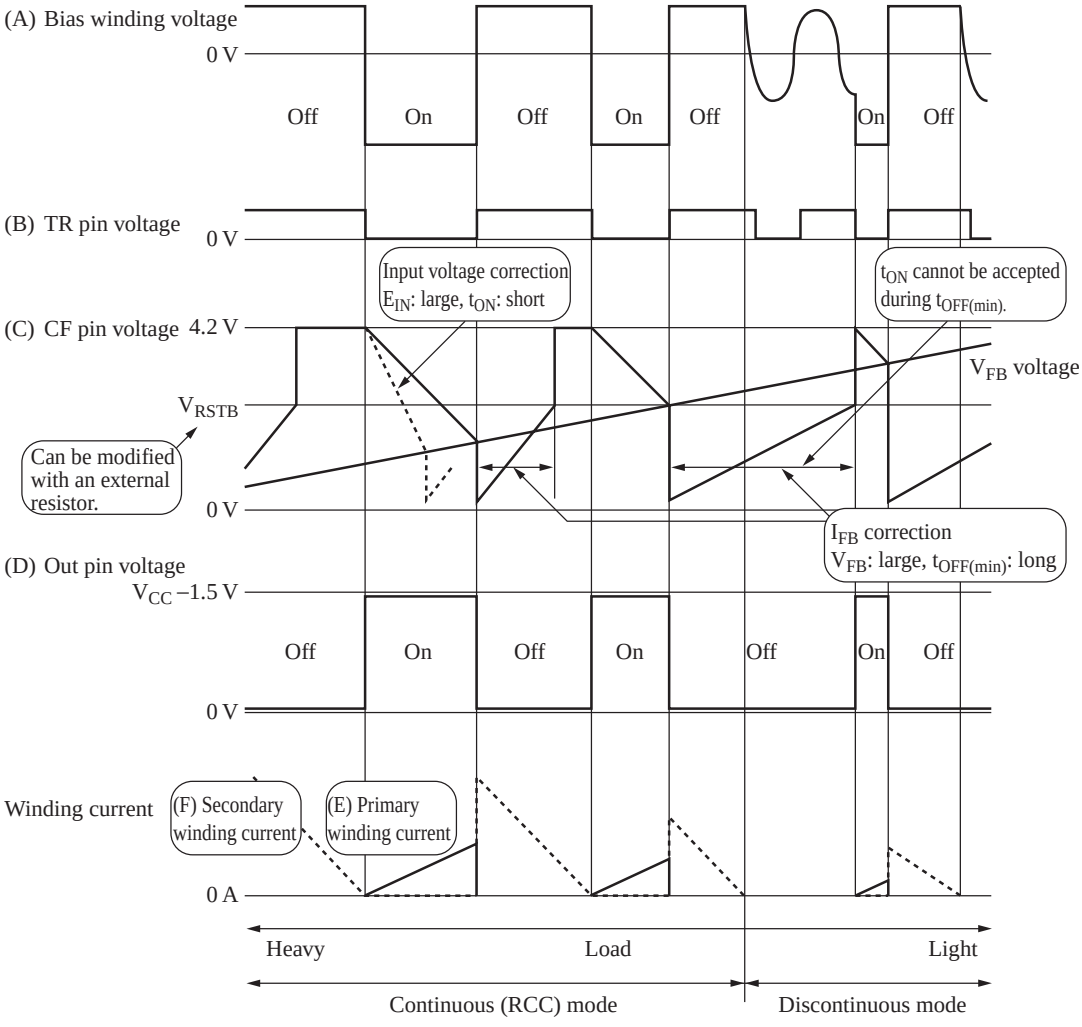
■ Application Notes

[1] Timing charts

- Circuit diagram



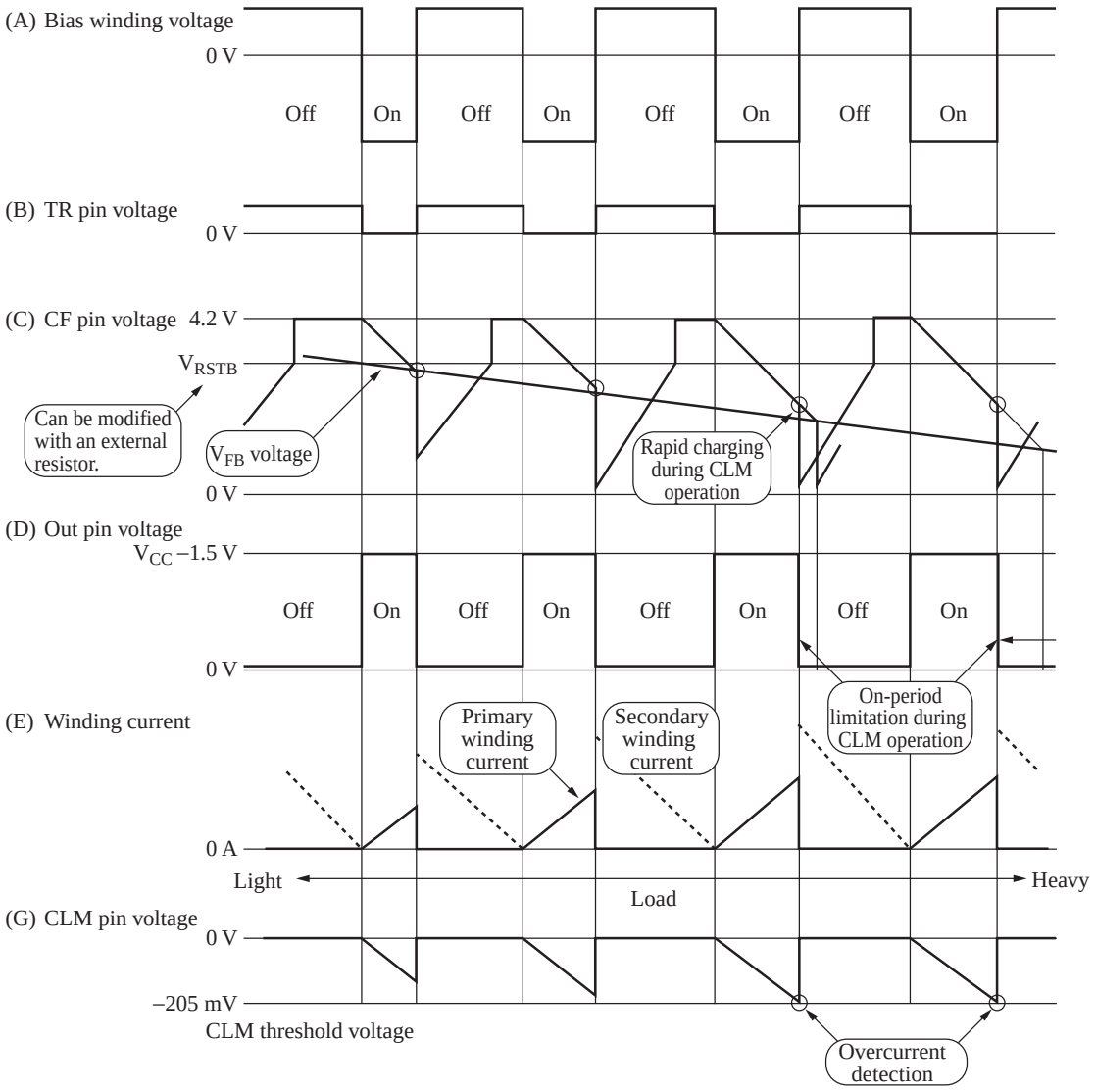
- Normal control waveforms



■ Application Notes (continued)

[1] Timing charts (continued)

- During pulse-by-pulse overcurrent operation



■ Application Notes (continued)

[2] Operation descriptions

1. Start/stop circuit block

- Startup mechanism

After the AC voltage is applied and the supply voltage due to the current in the startup resistor reaches the startup voltage and the IC begins to operate, drive of the power MOSFET begins. This causes a bias in the transformer, and the supply voltage is provided to the IC from the bias winding. (This is point a in figure 1.) During the period between the point when the startup voltage is reached, and the point when the bias winding can generate a voltage enough to supply the IC, the IC supply voltage is provided by the capacitor (C8) connected to V_{CC} . Since the supply voltage falls during this period (area b in figure 1), if the supply voltage falls below the IC stop-voltage before an adequate supply voltage can be provided by the bias winding, it will not be possible to start the power supply. (This is the state at point c in figure 1.)

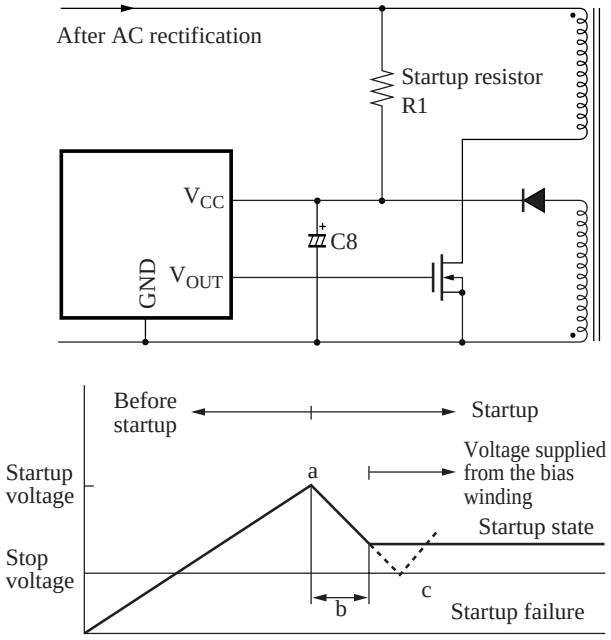


Figure 1

- Functions

This IC includes a function that monitors the V_{CC} voltage. It starts IC operation when V_{CC} reaches the startup voltage (14.4 V typical), and stops operation when the voltage falls below the stop voltage (8.9 V typical). Since a large voltage difference (5.5 V typical) is taken between the start and stop voltages, it is easy to select values for the start resistor and the capacitor connected to V_{CC} .

Since high voltages are applied across the startup resistor, measures must be taken to minimize the current that flows in this resistor. (To use a smaller startup resistor.) To achieve this, the circuit current at startup is set to as small as 190 µA (typical), and temperature variations, and also sample-to-sample variations are reduced as well. Since the bias current is reduced, the capacitor connected to V_{CC} can be miniaturized as well.

2. Oscillator circuit

The oscillator circuit determines the pulse width with which the main switch is turned on and off using the charge and discharge of the capacitor C_{CF} connected to the CF pin (pin 3). This IC implements a control scheme in which the main switch on-period is the discharge period of the CF pin waveform, and the off-period is the charge period of that waveform.

Constant-voltage control in a switching power supply using this IC is implemented during RCC (continuous) operation by holding the main switch off-period fixed and varying the on-period. This on-period is controlled by directly varying the output pulse-width of the oscillator circuit.

Additionally, the IC reduces the maximum on-period when the input voltage increases by detecting the input voltage through the flowing out current at the TR pin. (See figure 2.)

Furthermore, this IC features an added function that detects increases of the IFB feedback current, and reduces the off period, and lowers the operating frequency to reduce power loss during standby (light load) mode and to prevent being out of control.

During overcurrent protection operation, the IC performs a rapid discharge operation where the CLM pin voltage reaches the threshold voltage of –205 mV (typical).

■ Application Notes (continued)

[2] Operation descriptions (continued)

2. Oscillator circuit (continued)

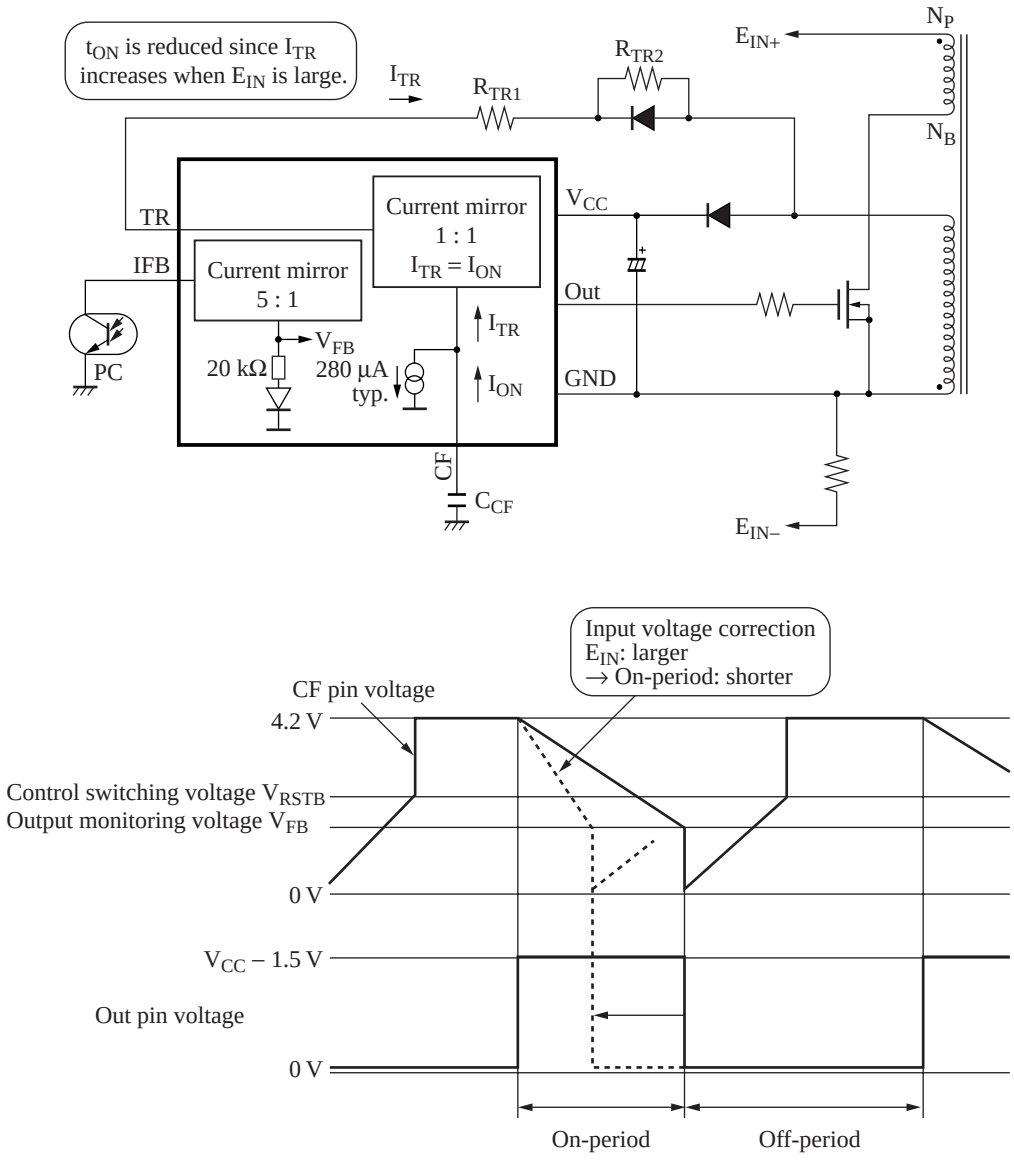


Figure 2. On-period block diagram and control waveforms

■ Application Notes (continued)

[2] Operation descriptions (continued)

2. Oscillator circuit (continued)

- Notes on switching from RCC operation to discontinuous operation

When the state changes from normal load to standby mode, the post-I-V conversion output monitor voltage V_{FB} increases along with the increase of the amount of feedback current. Then, when the IFB pin feedback current exceeds 1 mA (typical) and the VFB voltage becomes larger than the RSTB pin (pin 2) voltage, the minimum off-period current that is from the CF pin lower limit value until the RSTB pin voltage is reached, is rapidly reduced, and the operating frequency is lowered. (See figure 3.) This allows the switching loss to be reduced to the minimum, and allows the standby mode power to be reduced.

Furthermore, the RSTB pin voltage, which is operating point for switching from RCC operation to discontinuous operation, is set by resistor-division of the internal 7 V reference voltage to a typical value of 3.5 V. This value can be adjusted by connecting an external pull-down resistor, and this can be used to suppress increases of the minimum off-period.

Note that application designs must take into account the sample-to-sample variations of ±15% in the internal resistors and temperature coefficient of 2 400 ppm/°C.

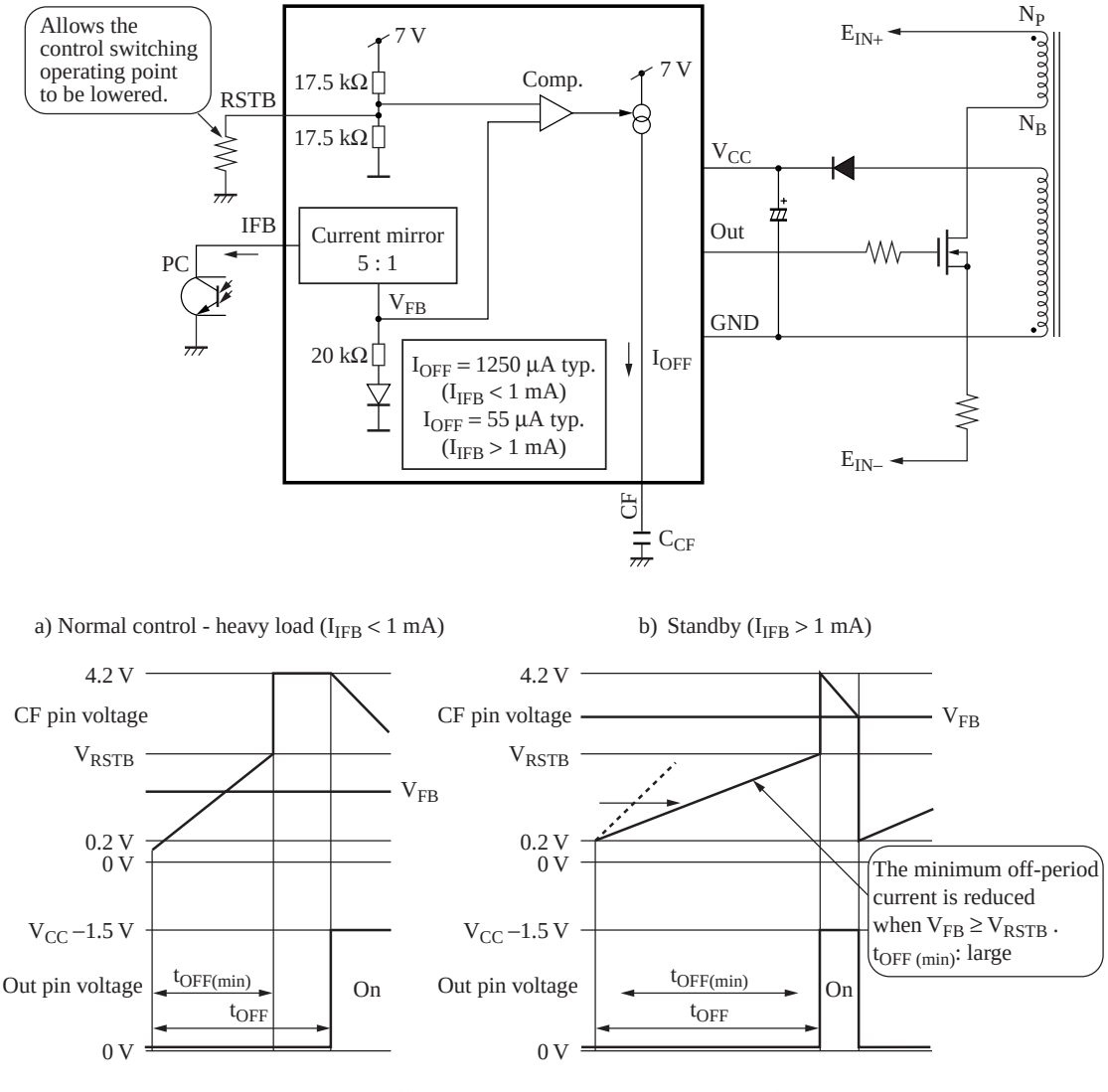


Figure 3. Off-period block diagram and control waveforms

■ Application Notes (continued)

[2] Operation descriptions (continued)

2. Oscillator circuit (continued)

- Notes on setting the oscillator frequency

This section describes the calculation of the on- and off-periods.

1) On-period: t_{ON}

The output on-period is the discharge period when the CF pin is between the peak value of V_{CFH} = 4.2 V (typical) and V_{FB} .

The following formula can be used to calculate the on-period of the power MOSFET as a reasonable approximation. (See figure 2.)

$$t_{ON} = C_{CF} \times (V_{CFH} - V_{FB}) / I_{ON}$$

Here, V_{CFH} = 4.2 V typ.
$I_{ON} = I_{TR}$ + 280 µA typ.
$I_{TR} = (E_{IN} \times NB/NP) / (R_{TR1} + R_{TR2})$
V_{FB} = 0.7 V typ.
(When $I_{IFB} \leq$ 250 µA)
V_{FB} = 4 kΩ × (I_{IFB} − 250 µA) + 0.7 V
(When I_{IFB} > 250 µA)

2) Off-period: t_{OFF}

The minimum off-period is the charging period from V_{CFL} = 0.2 V (typical) to V_{RSTB} .

The following formula can be used to calculate the minimum off-period as a reasonable approximation. (See figure 3.)

$$t_{OFF(min)} = C_{CF} \times \{V_{RSTB} - V_{CFL}\} / I_{OFF}$$

I_{OFF1} = 1250 µA typ. (V_{FB} 0.7 V typ. to V_{RSTB})
I_{OFF2} = 55 µA typ. (V_{FB} V_{RSTB} to 4.2 V typ.)

t_{ON}	: On-period
$t_{OFF(min)}$	: Minimum off-period
C_{CF}	: Capacitance of the capacitor connected to the CF pin
V_{CFH}	: Upper limit voltage for the CF pin. V_{CFH} = 4.2 V typ.
V_{CFL}	: Lower limit voltage for the CF pin
V_{RSTB}	: Pin voltage that sets the light load detection level. V_{RSTB} = 3.5 V typ. This voltage can be adjusted with an external resistor.
V_{FB}	: Value that results from IC internal conversion of feedback current I_{IFB}
I_{ON}	: On-period (CF pin discharge) current
I_{OFF1}	: Off-period (CF pin charge) current when I_{IFB} < 1 mA
I_{OFF2}	: Off-period (CF pin charge) current when I_{IFB} > 1 mA
I_{TR}	: Flowing current at TR pin
E_{IN}	: Primary winding voltage
N_B	: Number of turns in the bias winding
N_P	: Number of turns in the primary winding
R_{TR1}/R_{TR2}	: Resistors connected to the TR pin

However, the off-period for the local resonance circuit described later, is determined by the time for the voltage fed back to TR pin (pin 1) if that time is longer than the t_{OFF} time determined by C_{CF} .

The power MOSFET is turned on and off continuously by repeating the above operations.

■ Application Notes (continued)

[2] Operation descriptions (continued)

3. Local resonance operation (power MOSFET turn on delay circuit)

The AN8038 and AN8038S transformer reset detection functions detect a low-level input to the TR pin. (This is similar to earlier Panasonic ICs, in particular the AN8026, AN8027, AN8028, and AN8029.)

Local resonance operation is possible with circuits as shown in figure 4. C7 is the resonance capacitor, and R9 and C9 form a delay circuit for adjusting the power MOSFET turn on time.

When the power MOSFET is off, the voltage that occurs in the drive winding is input to the TR pin (pin 1) through R9 and C9. The power MOSFET will be held in the off state while a high level (a level higher than the threshold voltage, which is 0.25 V typical) is input to the TR pin.

The TR pin also has a clamping capability for upper and lower limit voltages. The upper limit voltage is clamped at 1.5 V typical (sink current is –3 mA), and the lower limit voltage is clamped at about – 0.15 V typical (source current: 3 mA). (See figure 5.) The power MOSFET off-period is determined by the longer period of the following two periods: the period until the TR pin input voltage becomes lower than the threshold voltage as the bias winding voltage falls after the transformer discharges its energy, and the minimum off-period $t_{OFF(min)}$ stipulated by the internal oscillator (see the description of the oscillator circuit). As a result, ringing in the bias winding does not be regarded as a turn on signal during the minimum off-period.

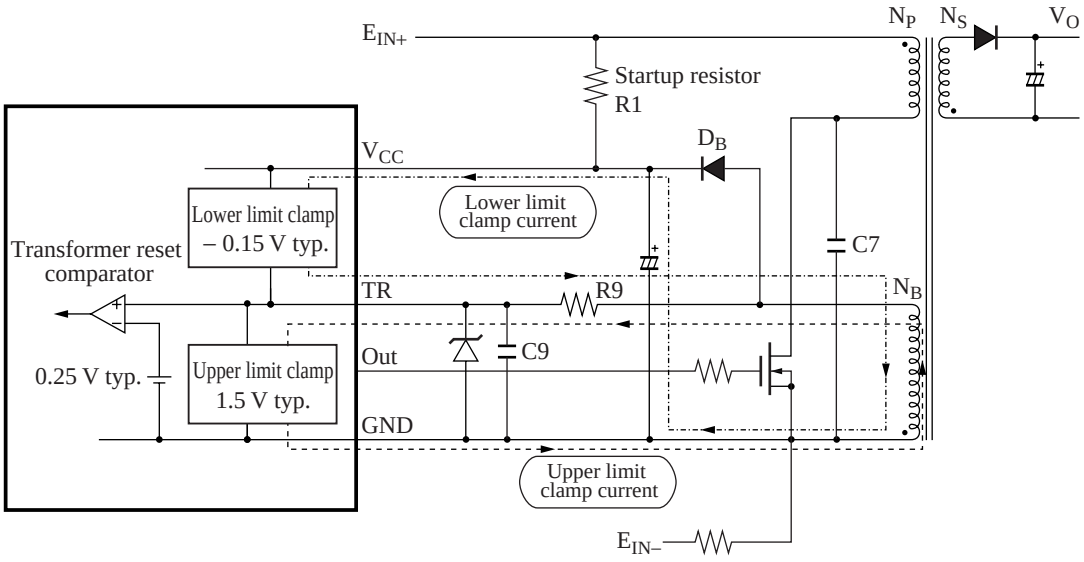


Figure 4

■ Application Notes (continued)

[2] Operation descriptions (continued)

3. Local resonance operation (power MOSFET turn on delay circuit) (continued)

- Notes on C7 value selection

Figure 5 shows the local resonance waveform.

Select values of R9 and C9 to determine the delay time so that the power MOSFET is turned on at the 1/2 cycle point in the resonant frequency waveform. Simply stated, select values so that the power MOSFET turns on at the zero voltage point in the voltage waveform. The resonant frequency can be roughly determined using the following formula.

$$f_{SYNC} = \frac{1}{2\pi\sqrt{L \cdot C_7}} \quad (Hz)$$

C_7 : Resonance capacitor
L : Inductance of the transformer primary winding

Accordingly, the turn on delay time $t_{PD(ON)}$ to turn on the power MOSFET at the 1/2 cycle point in the resonant frequency waveform is given by the following formula.

$$t_{PD(ON)} = \pi\sqrt{L \cdot C_7} \quad (s)$$

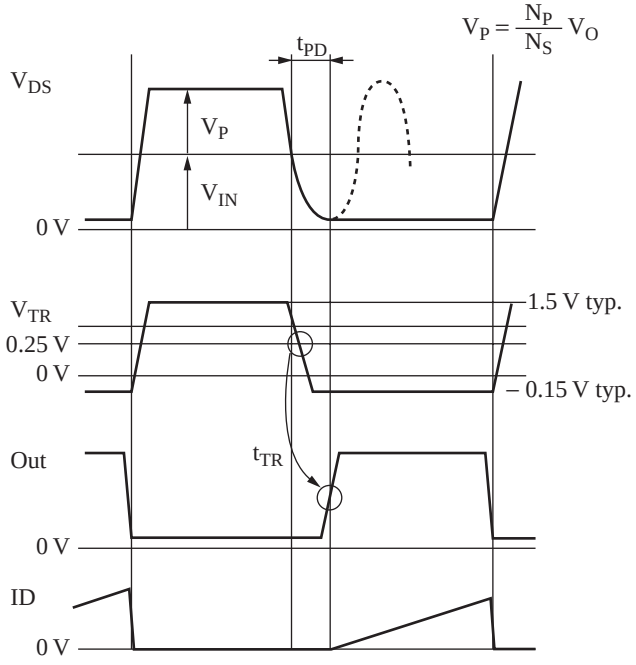


Figure 5. Local resonance waveform

Furthermore, $t_{PD(ON)}$ should be set to be larger than t_{TR}, since a response time t_{TR} that is the time between transistor detection and output changeover is about 400 ns.

Note that since insertion of the resonance capacitor C7 results in increased losses, using the parasitic capacitance of the power MOSFET itself should also be considered. However, in this case the sample-to-sample variations and temperature variations should be considered.

- Notes on R9 and C9 value selection

If an excessively low value is used for R9, the current flowing into the TR pin after power supply startup will exceed the maximum rating for the IC, and incorrect operation (or even, in the worst case, destruction of the device) may occur. We recommend using a value of R9 in the range that satisfies the following conditions.

$$\frac{V_{B(-)} - \text{The TR lower limit clamp voltage (– 0.15 V typical)}}{R9} \geq -3 \text{ mA}$$

$V_{B(-)}$: The peak voltage when the voltage is negative

$$\frac{V_{B(+)} - \text{The TR upper limit clamp voltage (1.5 V typical)}}{R9} \leq 3 \text{ mA}$$

$V_{B(+)}$: The peak voltage when the voltage is positive

$$V_{B(+)} = \frac{N_B}{N_S} V_O \qquad V_{B(-)} = -\frac{N_B}{N_P} E_{IN}$$

Also, adjust $t_{PD(ON)}$ by changing the value of C9 in consideration of the resonance capacitance and inductance of the transformer used.

■ Application Notes (continued)

[2] Operation descriptions (continued)

4. Power supply output control system (IFB: feedback)

Constant-voltage control of the power supply output is conducted by changing the on- and off-periods of the power MOSFET. On- and off-periods are controlled as follows: a feedback current responding to the output of output-voltage detection circuit formed at secondary output side is input to IFB pin through a photocoupler connected to IFB pin (pin 14), and is converted to V_{FB} voltage. (See figure 6.)

The more AC input voltage becomes higher and/or the more the load current decreases, the more the flowout current from IFB pin increases. This makes V_{FB} voltage higher and on-period shorter (at the standby, off-period becomes longer). Furthermore cancellation ability is about 250 µA for the dark current of photocoupler.

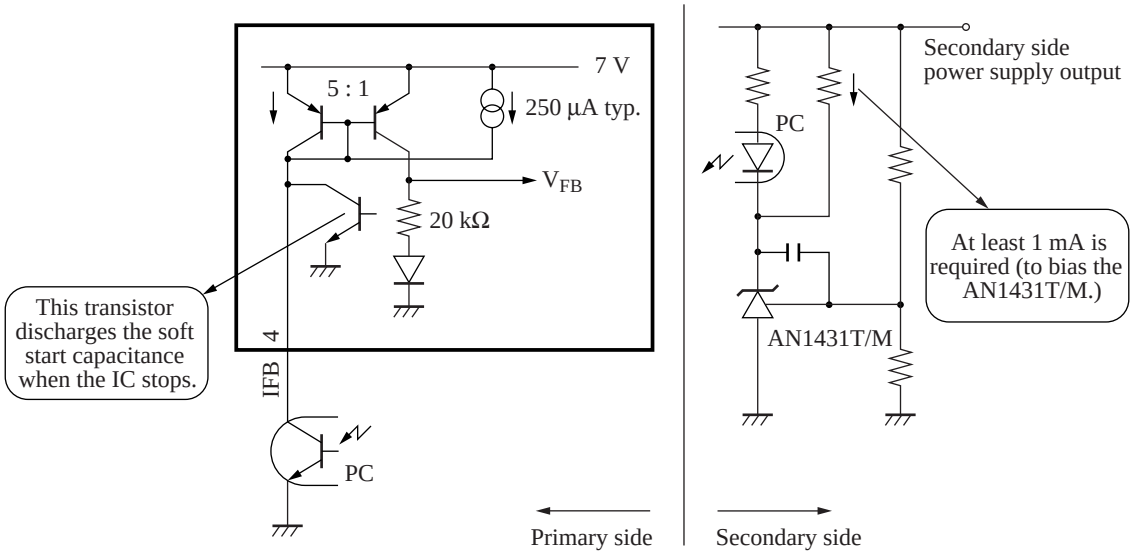


Figure 6. Power supply output control system

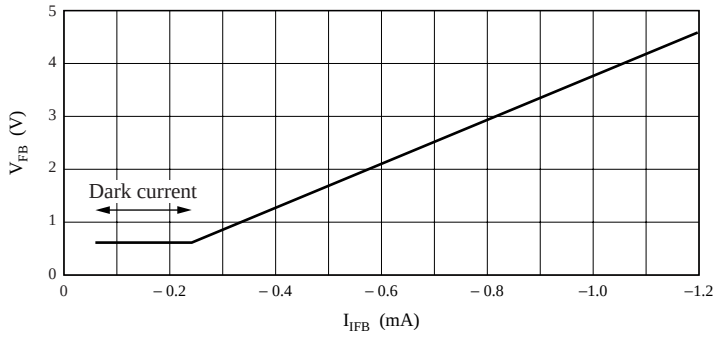


Figure 7. Feedback current vs. V_{FB} characteristics

■ Application Notes (continued)

[2] Operation descriptions (continued)

4. Power supply output control system (IFB: feedback) (continued)

- Soft start

When a power supply is started, it starts up in an overloaded state due to the capacitor connected to the power supply output. Since the power supply output voltage is low in this state, the normal constant-voltage control would rise the power supply to its maximum duty ratio. Although the pulse-by-pulse overcurrent protection circuit (CLM) would limit the current, due to filter and other delays, it cannot decrease the pulse width to zero, and thus large currents could flow in both the main switch (the power MOSFET) and the secondary side diode. This could result in destruction of these components in the worst case. To prevent this, soft start is used to suppress surge currents at power supply startup.

Soft start is installed by inserting R3 and C4 between the IFB pin (pin 4) and the GND pin (pin 6) as shown in figure 8. When the IC supply voltage reaches the startup voltage, and the start circuit operates, an open bias (about 6.4 V) is output to the IFB pin. A charging current (I_{IFB}) flows from the IFB pin into C4 due to this voltage. As a result, since startup begins at relatively high VFB, output control is started from short t_{ON}. Since the voltage across C4 rises according to the time constant determined by R3 and C4, I_{IFB} becomes smaller with time, and the t_{ON} time increases gradually.

Due to the above operation, the current that flows in the power MOSFET at power-on increases gradually. As a result, surge currents are suppressed.

However, this reduces the transient response of the feedback loop, so care is required in designing this circuit.

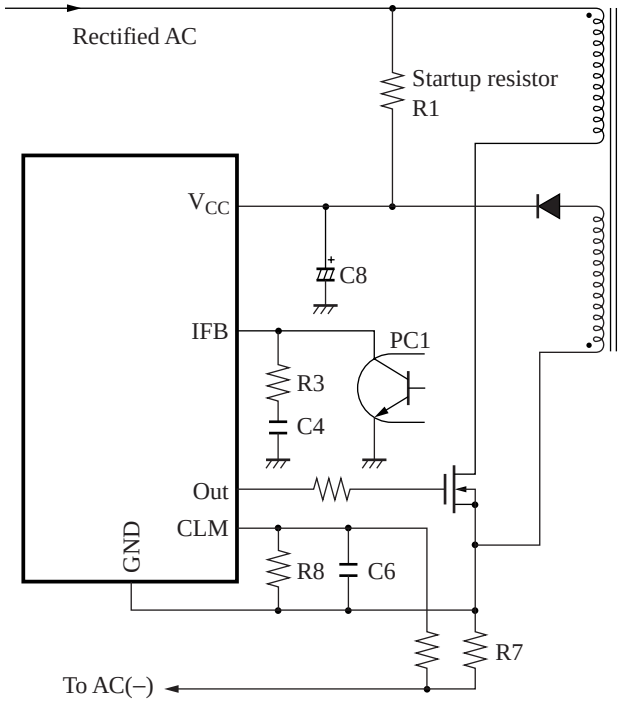


Figure 8

5. Output block

This IC adopts a totem pole (push-pull) structure output circuit in which NPN transistors as shown in figure 9 sinks and sources current to rapidly drive the power MOSFET which is a capacitive load.

This circuit provides maximum sink and source currents of – 0.1 A and +0.2 A (DC), and peak currents of –1 A and +2 A. Furthermore, this circuit has a sink capability of 1 mA (typical) even when the supply voltage has fallen under the stop voltage, and thus can turn off the power MOSFET reliably.

■ Application Notes (continued)

[2] Operation descriptions (continued)

5. Output block (continued)

The main requirement on the control IC in this type of power supply is the ability to provide a large peak current. That is to say, a high average current is not required in steady state operation. This is because the power MOSFET is a capacitive load, and while a large peak current is required to drive such a load rapidly, once the load has been charged or discharged a much smaller current suffices to retain that state.

This IC has a guaranteed peak current capability of −1 A and +2 A, values which were determined by considering the capacitance of the power MOSFETs that will be used.

The parasitic inductance and capacitance of the power MOSFET can cause ringing, and pull down the output pin below the ground level. If the output pin goes to a negative voltage that is larger than the voltage drop of the diode, this state can turn on the parasitic diode formed by the collector of the output NPN transistor and the substrate. Insert a Schottky barrier diode between the output and ground if this is a problem. (See figure 9.)

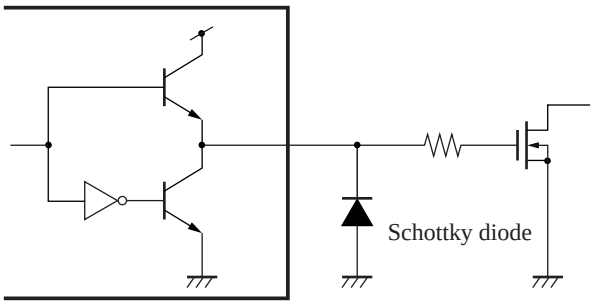


Figure 9

- Overvoltage protection circuit (OVP)

OVP stands for overvoltage protection. The overvoltage protection circuit is a self-diagnostic function that shuts down the power supply to protect the load if a voltage that is significantly and abnormally higher than the normal output voltage occurs in the power supply output, due to, for example, a malfunction in the control system or an abnormal voltage applied externally. (See figure 10.)

The overvoltage detection function monitors the V_{CC} pin voltage. Since the V_{CC} pin voltage is normally supplied from the transformer bias winding, this voltage is proportional to the secondary side output voltage. Thus the overvoltage protection circuit operates when an overvoltage occurs in the secondary side output.

1) If, as a result of an abnormality in the power supply output, the voltage input to the V_{CC} pin exceeds the threshold value (20.5 V typical), the IC internal reference voltage is shut down, and all control operation is stopped. The IC then holds this state.
2) The OVP circuit is released (reset) by lowering the supply voltage (V_{CC} < 7.5 V typical). (This is the OVP release supply voltage.)

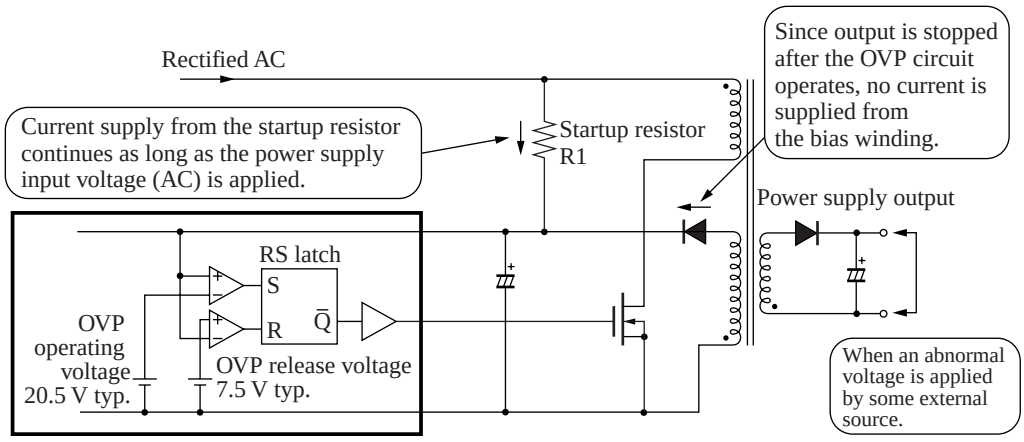


Figure 10. OVP operating circuit

■ Application Notes (continued)

[2] Operation descriptions (continued)

5. Output block (continued)

- Operating power supply current characteristics

When the OVP circuit operates and the power supply current drops, this can induce a rise of the supply voltage V_{CC}. In the worst case, it may exceed the IC's guaranteed breakdown voltage (28 V).

Therefore, the circuit is provided with characteristics that cause the supply current to rise in constant resistance mode when the OVP circuit operates, and thus the increases of the supply voltage.

Due to these characteristics, if the supply voltage V_{CC} when the OVP circuit operates is stabilized at a value (note that this value depends on the value of the startup resistor) that is larger than the OVP release voltage (7.5 V typical), the OVP circuit will not be reset as long as the AC input is not cut. (See figure 11.) Note that this does not apply to an external reset.

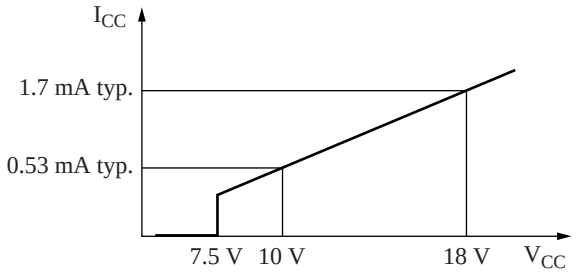


Figure 11. OVP operating circuit current

- Overcurrent protection circuit (pulse-by-pulse overcurrent protection)

This circuit uses the fact that overcurrents in the power supply output are proportional to the current flowing in the primary side main switch (power MOSFET). This circuit limits overcurrents in the power supply output by constraining the upper limit of the pulse current flowing in the main switch, and thus protects components sensitive to excessive current.

The current flowing in the main switch is detected by connecting a resistor between the power MOSFET source and ground and monitoring the voltage that appears across that resistor. When the power MOSFET is turned on and the CLM (current limit) threshold voltage is detected, the output is turned off. This controls the circuit so that a current in excess of that limit cannot flow by turning off the power MOSFET. The CLM threshold voltage is about –205 mV with respect to ground at $T_a = 25°C$. While this control operation is repeated every cycle, once an overcurrent is detected, the off state is held for the remainder of that cycle, and the circuit is not turned on until the next period. This type of overcurrent detection is called "pulse-by-pulse overcurrent detection."

R6 and C6 in figure 12 form a filter circuit that rejects noise generated due to the incidental equivalent parasitic capacitance when the power MOSFET is on.

For the grounding point, we recommend that the power MOSFET source pin and the IC GND pin be connected over as short a distance as possible.

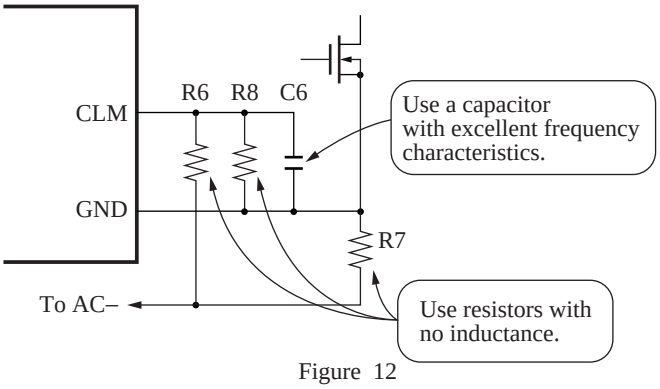


Figure 12

- Notes on the detection level precision

This overcurrent detection level is reflected on the operating current level of the power supply overcurrent protection function. Therefore, if this detection level varies with sample-to-sample variations or with temperature, the operating current level of the overcurrent protection function of the power supply itself will vary. Since variations in this level imply a need for increased ruggedness in parts used, or even the destruction of circuit components, we have increased the precision of this IC as much as possible.

■ Application Notes (continued)

[2] Operation descriptions (continued)

5. Output block (continued)

- Overcurrent protection circuit (input voltage correction function)

As an extended application, this section presents a circuit design that applies a correction so that the overcurrent protection operating point is held fixed with respect to variations in the input voltage. This circuit uses the proportional relationship between the input voltage and the inverted voltage of the bias winding, and superposes inverted voltage of the bias winding on the overcurrent protection operating voltage. (See figures 13 and 14.)

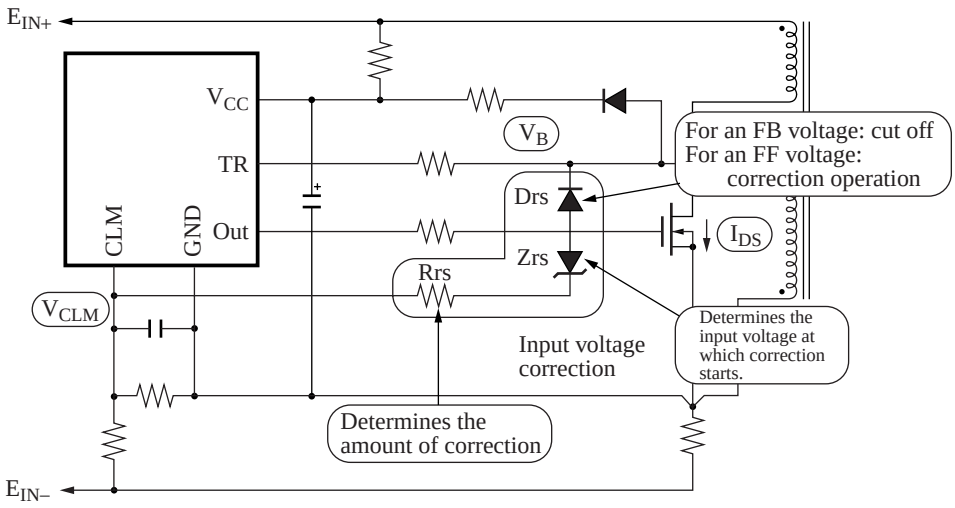


Figure 13

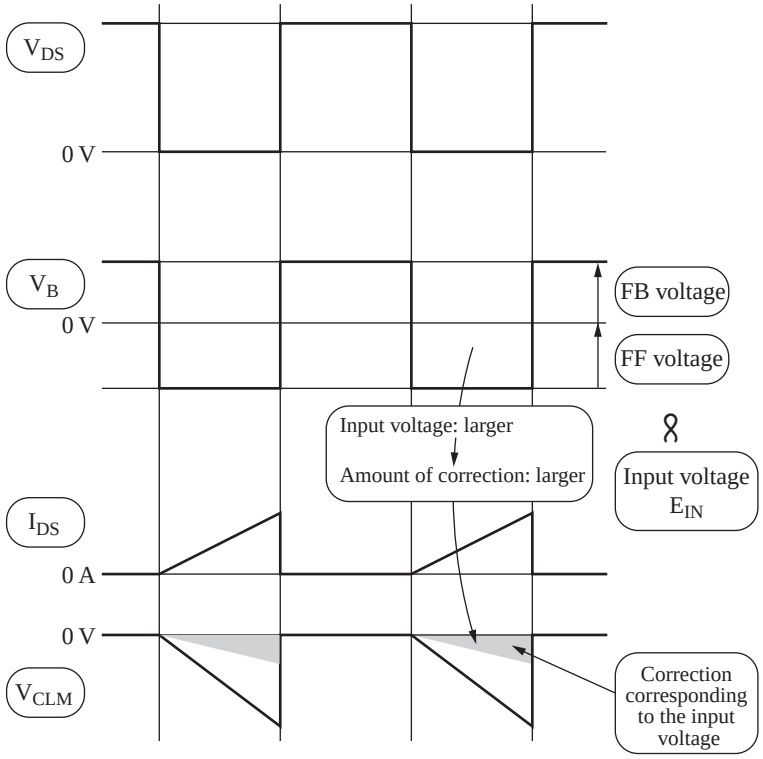


Figure 14

■ Application Notes (continued)

[2] Operation descriptions (continued)

6. Notes on feedback control

If the IC output pin (pin 7) falls to a negative voltage lower than that of the GND pin, the startup operation may fail or the output oscillation may become unstable.

ICs in general, not just this IC, do not respond well when negative voltages lower than the ground level are applied to their pins. (Except for special applications.) This is because parasitic device operations may be induced when negative voltages are applied due to the structure of ICs themselves.

In the case mentioned above, when the IC output (V_{OUT}) is turned off, the power MOSFET drain-to-source voltage, V_{DS}, jumps from a low voltage to a high voltage. The voltage chattering that occurs at this time is superposed on V_{OUT} through the parasitic capacitance C_{GD} between the power MOSFET gate and drain, and generates a negative voltage with respect to the pin. No problems occur if the peak voltage, VEX, of this negative voltage does not exceed the parasitic device conduction voltage (about – 0.7 V).

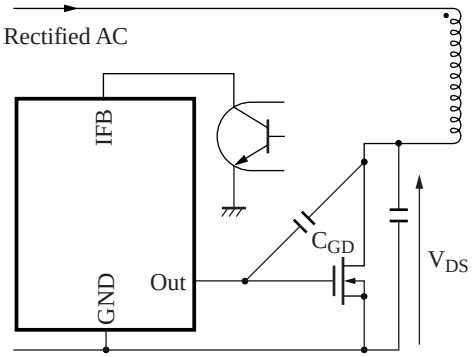


Figure 15

However, the amplitude of the chattering is larger for higher input voltages and for larger leakage inductance in the transformer used. Also, the influence of this phenomenon becomes more noticeable for the larger C_{GD} of the power MOSFET used, and the V_{EX} peak value also increases. If the parasitic device conduction voltage is exceeded, then, in this IC, the parts of the circuit around the feedback circuit (FB) (in particular, the FB discharge circuit) are influenced. This can cause momentary drops in the IFB pin voltage (the control voltage), and as a result increase the FB current (I_{IFB}) and thus does not allow the drive pulse on-period t_{ON} to be increased. It may also prevent stabilization of the circuit. These are symptoms of the case described here. (See figures 15 and 16.)

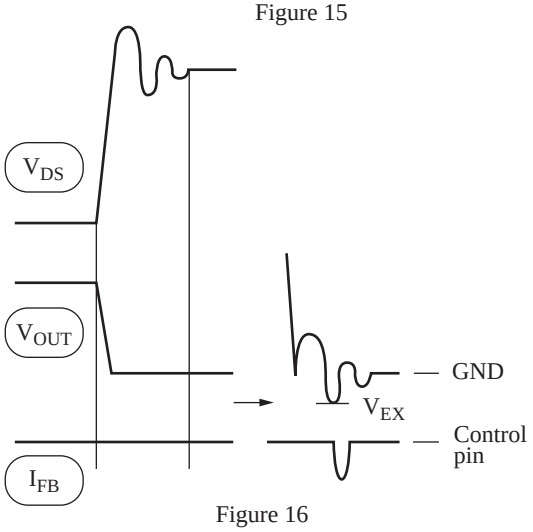


Figure 16

[Countermeasures]

If an application exhibits the symptoms of the case described above, or similar symptoms, first insert a Schottky diode between V_{OUT} and GND. It is not possible to completely remove the mechanism described above from a power supply system. It is also not possible to prevent levels from being pulled down to negative voltages in the control IC itself. Therefore, the most important point in designing countermeasures is to prevent such negative voltages from reaching the parasitic device conduction voltage.

Note) If a Schottky diode is added to the circuit and the condition improves initially but the symptoms reappear when the input voltage or other parameter is increased, try replacing the Schottky diode with one that has a larger forward current (both peak and average values). The current capability of the Schottky diode is sometime insufficient.

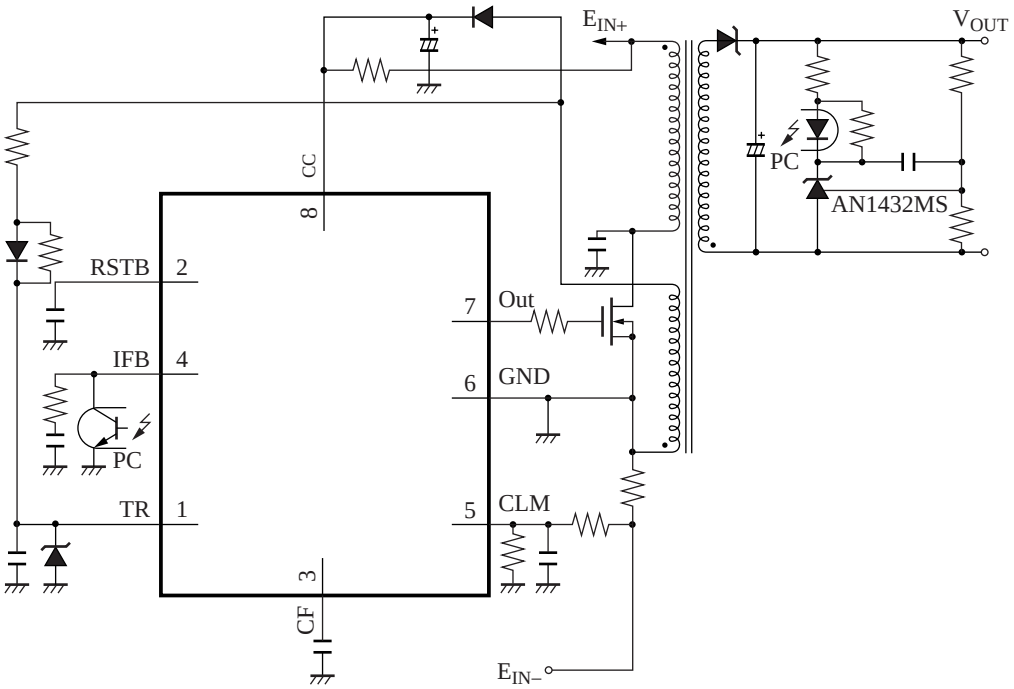
Reference: Panasonic Schottky Diode

Part No.	Reverse voltage	Forward current (average)	Forward current (peak)
MA2C700A (MA700A∗)	30 V	30 mA	150 mA
MA2C723 (MA723∗)	30 V	200 mA	300 mA
MA2C719 (MA719∗)	40 V	500 mA	1 A

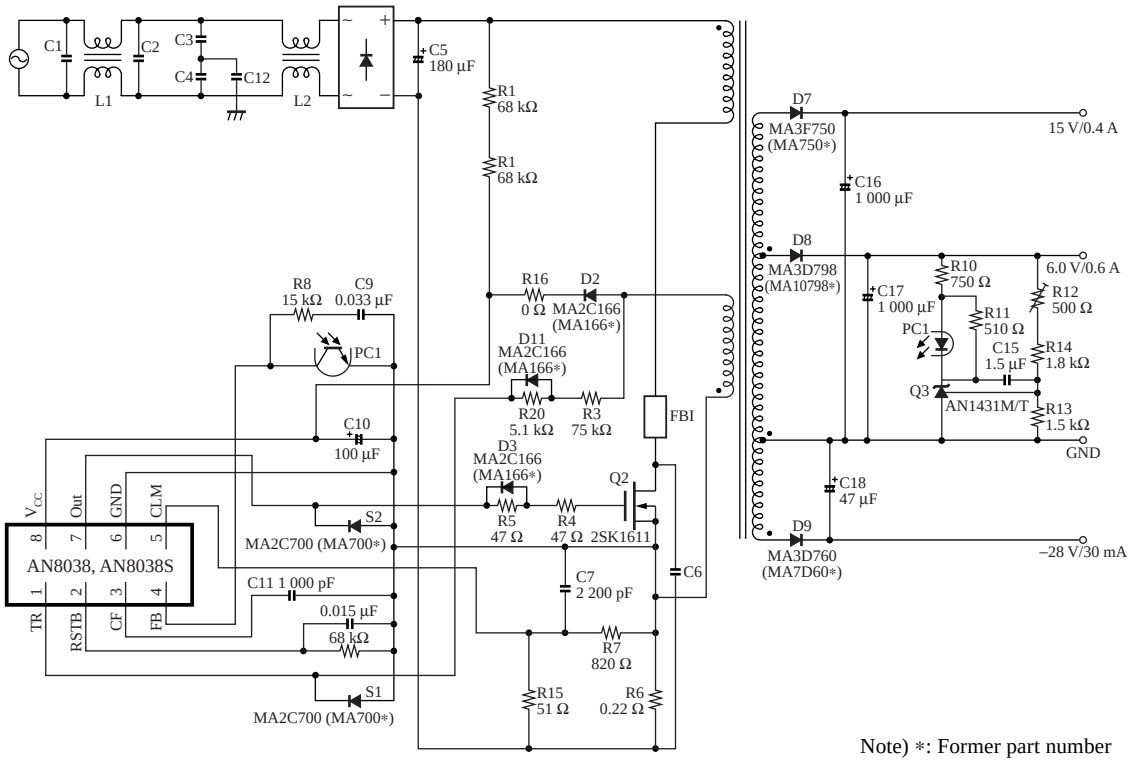
Note) ∗: Former part number

■ Application Circuit Examples

• Application circuit example 1



• Application circuit example 2



Note) ∗: Former part number