Q Surround Processor
Monolithic IC MM1454

Outline

This is an analog IC virtual surround processor that faithfully reproduces the sound algorithm developed by Q SOUND Labs, Inc.
In particular, when a stereo signal (L/Rch) encoded by Dolby Pro Logic is input to this IC, a virtual rear speaker is created spatially, and this allows reproduction of realistic, 3-dimensional sound from two speakers, without the addition of another speaker.
Q Xpander technology allows deep, spatially wide sound for input of normal stereo signals, as well.

* Virtual Dolby sound is a system developed by Dolby Labs, Inc. that reproduces realistic Pro Logic sound with just two front left and right speakers, so there is no need for the additional two rear speakers and center speaker normally required for Pro Logic sound.
* Dolby and Dolby Surround are registered trademarks of Dolby Laboratory Licensing Corporation.
* The Q Surround virtual processor (MM1454) was developed by Mitsumi Electric, and has not received the certification or authorization of Dolby Laboratory.
* Mitsumi Electric has no business ties or other relationship with Dolby Laboratory.

Features

1. Virtual rear speakers allow reproduction of 3-dimensional sound through only two speakers when a Pro Logic encoded source is input.
2. Also reproduces wide sound for a normal stereo source.
3. 2ch input - 2ch output.
4. Few external parts due to use of the active filter created using Mitsumi's bipolar technology.
5. Low noise design Q Surround ON: 15μVrms
   OFF: 10μVrms
6. Simple structure results in small size and low cost.

Package

SOP-16B

Applications

1. TV, VCR
2. Audio equipment
3. Computer monitors
4. Active speaker systems

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Storage Temperature	T_{STG}	−40~+125	°C
Operating Temperature	T_{OPR}	−20~+75	°C
Power Supply Voltage	V_{CC} max.	13	V
Input Voltage	V_{IN} max.	$0 \leq V_{IN} \leq V_{CC}$	V
Output Voltage	I_O max.	10	mA
Allowable loss	Pd	350	mW

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Operating temperature	T_{OPR}	–20~+75	°C
Operating voltage	V_{OP}	4.5~12.0	V
Power supply fall times *7	T_{VOFF}	0.1~1.0	s

Electrical Characteristics (Except where noted otherwise, V_{CC}=9V, Ta=25°C, Vbyp=5V, SW1,2,3: A)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}			16	22	mA
Voltage gain Q Surround 1	Gqs1	SG1 : 0.75Vrms, 1kHz SW2 : B TP1	8.5	9.5	10.5	dB
Voltage gain Q Surround 2	Gqs2	SG1 : 0.75Vrms, 1kHz SW2 : B TP2	4.0	5.0	6.0	dB
Voltage gain Q Surround 3	Gqs3	SG2 : 0.75Vrms, 1kHz SW3 : B TP2	8.5	9.5	10.5	dB
Voltage gain Q Surround 4	Gqs4	SG2 : 0.75Vrms, 1kHz SW3 : B TP1	4.0	5.0	6.0	dB
Voltage gain bias 1	Gby1	SG1 : 0.75Vrms, 1kHz Vbyp=0V SW2 : B TP1	–1	0	1	dB
Voltage gain bias 2	Gby2	SG2 : 0.75Vrms, 1kHz Vbyp=0V SW3 : B TP2	–1	0	1	dB
Input voltage amplitude (1)	$V_{IN}1$	V_{CC}=9V *1 SW2, 3 : B TP1, TP2	0.75	0.9		Vrms
Input voltage amplitude (2)	$V_{IN}2$	V_{CC}=9V *2 SW2, 3 : B TP1, TP2	0.35	0.45		Vrms
Total higher harmonic distortion Q Surround	THDqs	(a) SG1 : 0.75Vrms, 1kHz SW2 : B (b) SG2 : 0.75Vrms, 1kHz SW3 : B TP1, TP2		0.1	0.3	%
Total higher harmonic distortion bias	THDby	(a) SG1 : 0.75Vrms, 1kHz SW2 : B (b) SG2 : 0.75Vrms, 1kHz SW3 : B Vbyp=0V TP1, TP2		0.03	0.15	%
Output noise voltage Q Surround	Vnoqs	BW=20~20kHz, A Curve TP1, TP2		15	35	µVrms
Output noise voltage bias	Vnoby	BW=20~20kHz, A Curve Vbyp=0V TP1, TP2		10	25	µVrms
R-L channel balance	Cb	SG1, SG2 : 0.75Vrms, 1kHz Vbyp=0V SW2, 3 : B TP1, TP2	–1.0	0	1.0	dB
B/Q pin voltage (H)	Vbyph	*3	2.1			V
B/Q pin voltage (L)	Vbyp1	*4			0.7	V
B/Q pin voltage (H)	Ibyph	*5 Vbyp=5V TP5			350	µA
B/Q pin voltage (L)	Ibyp1	*6 Vbyp=0V TP5	–1			µA
DET pin voltage (H)	Vdeth	*7 TP6	8.5			V
DET pin voltage (L)	Vdetl	*7 TP6			0.7	V
Input resistance	R_{IN}	TP3, TP4	21	30	39	kΩ
Power supply voltage removal rate Q Surround	PSRRqx	SG3 : 100mVrms, 100Hz SW1 : B TP1, TP2		–80	–65	dB
Power supply voltage removal rate bias	PSRRby	SG3 : 100mVrms, 100Hz SW1 : B Vbyp=0V TP1, TP2		–85	–70	dB
Crosstalk (1)	Ct1	SG1 : 0.75Vrms, 1kHz SW2 : B *8 Vbyp=0V TP1, TP2		–85	–70	dB
Crosstalk (2)	Ct2	SG2 : 0.75Vrms, 1kHz SW3 : B *9 Vbyp=0V TP1, TP2		–85	–70	dB

Note 1: *1 Input voltage amplitude when output total higher harmonic distortion is 1%. However, the signals input to SG1 and SG2 must be the same phase (phase difference 0 degrees).

Note 2: *2 Input voltage amplitude when f = 1kHz and output total higher harmonic distortion is 1%. However, the signals input to SG1 and SG2 must be reverse phase (phase difference 180 degrees).

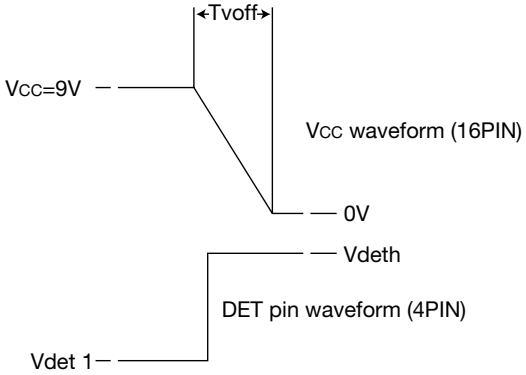
Note 3: *3 Voltage when B/Q pin (Pin 3) is considered to be H (Q Surround mode).

Note 4: *4 Voltage when B/Q pin (Pin 3) is considered to be L (by pass mode).

Note 5: *5 Current that flows in to B/Q pin (Pin 3) when Vbyp = 5V.

Note 6: *6 Current that flows out of B/Q pin (Pin 3) when Vbyp = 0V.

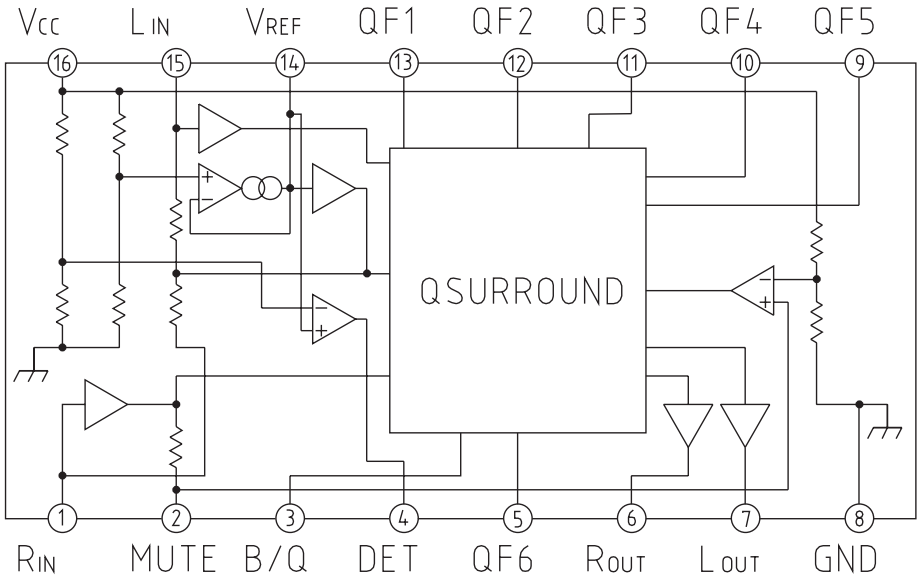
Note 7: *7 The mute signal for turning off the power amp power supply is output to Pin 4. On this IC, it is recommended that the pop noise generated during power supply fall be muted by turning off the power amp connected to the final stage of MM1454 before turning off the IC power supply.



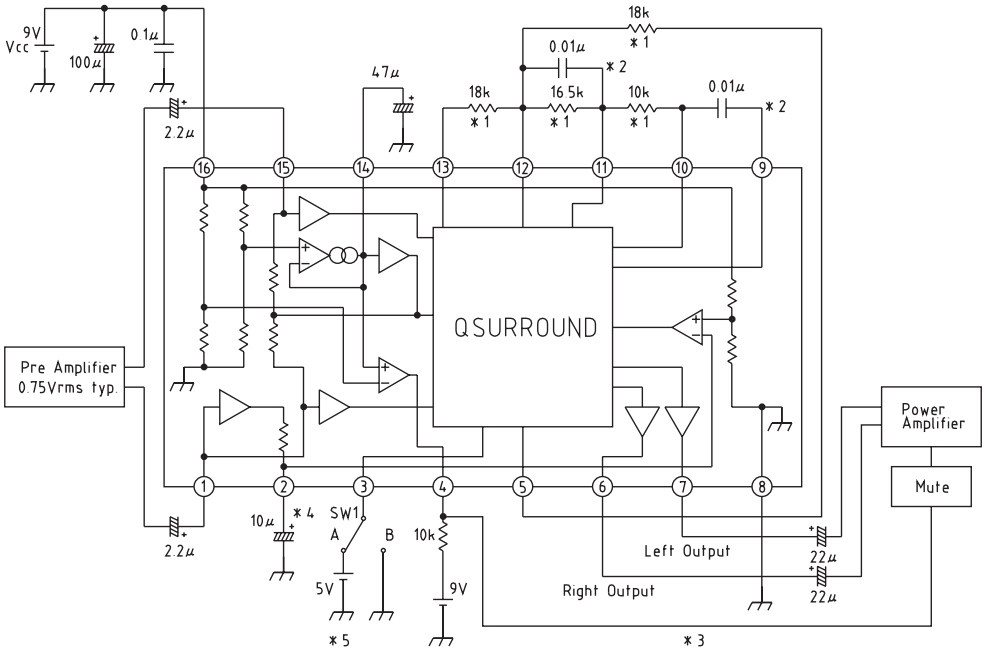
Note 8: *8 Defined as the ratio between Pin 6 output signal and Pin 7 output signal when a signal is input to SG1.

Note 9: *9 Defined as the ratio between Pin 7 output signal and Pin 6 output signal when a signal is input to SG2.

Block Diagram



Application Circuit



*1 Resistor Tolerance ±1%

*2 Capacitor Tolerance ±5%

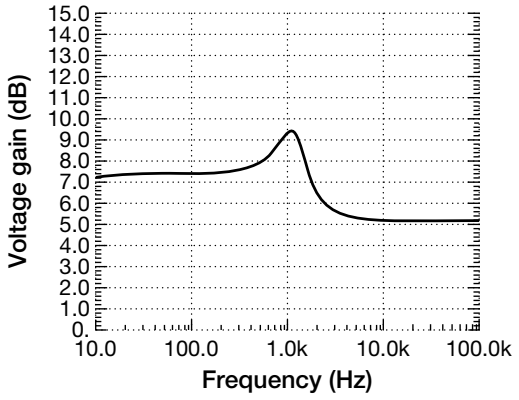
*3 The mute signal which switches off the power supply of a power amplifier that is connected with MM1454 appears in the 4 terminal. (NOTE 7)

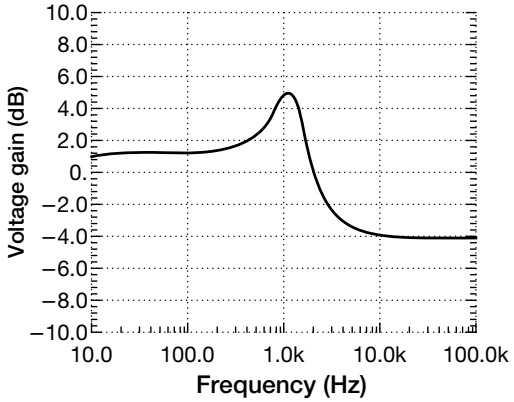
*4 The pop noise which occurs in a moment of the power supply switching on is reduced by connecting the capacitor (10uF) between 2PIN and GND. But if the reduced pop noise cause trouble for your application, we recommend muting the pop noise by the power amplifier that is connected with MM1454.

*5 SW1: A QSurround Mode
SW2: B Bypass Mode

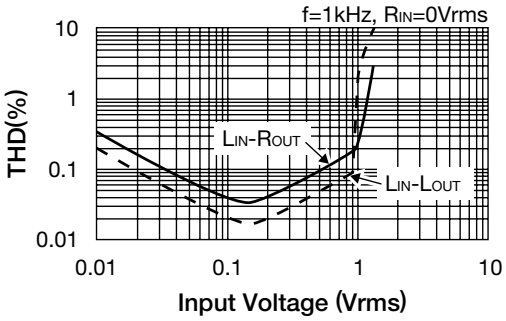
Characteristics

1. LIN-ROUT (RIN-LOUT) Frequency (Q Surround) 2. LIN-ROUT (RIN-ROUT) Frequency (Q Surround)

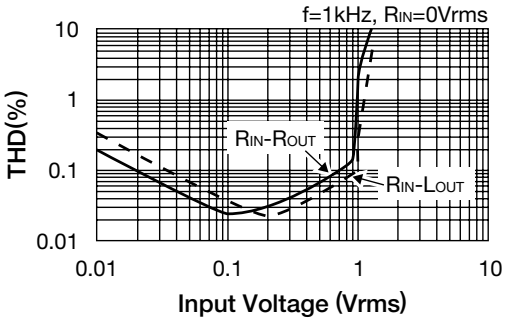




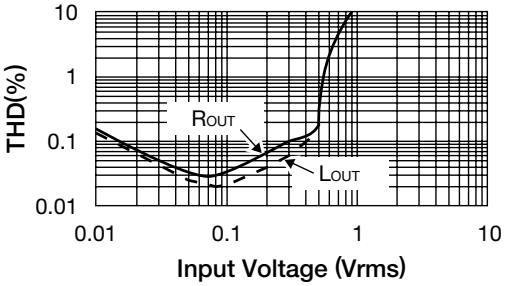
3. THD of output signal – Input voltage (L_{IN}) (QSrround)



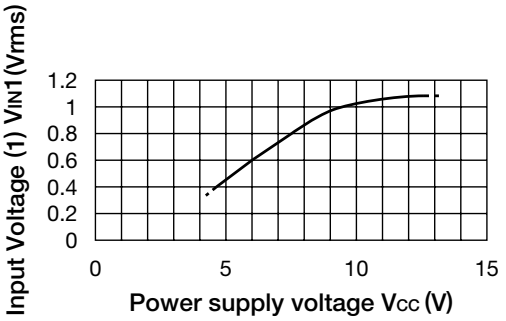
4. THD of output signal – Input voltage (R_{IN}) (QSrround)



5. THD of output signal – Input voltage (QSrround)
f=1kHz, The signals that are inputted in L_{IN} and R_{IN} are out out of phase and same amplitude.

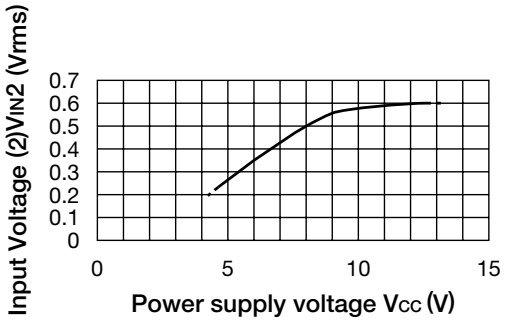


6. Input voltage (1) – Power supply voltage (QSrround)



See Electrical Characteristics Note 1

7. Input voltage (2) – Power supply voltage (QSrround)



See Electrical Characteristics Note 2