

### LCD Driver

- Controls up to 128 segments
- Supports static, 2-mux, 3-mux, and 4-mux displays
- On-chip bias generation with internal charge pump
- Low power blink capability

### GPIO Expander

- Expands GPIO count by up to 36 pins
- GPIO pins may be configured to push-pull or open-drain outputs with two drive levels. GPIO may also be used as digital inputs
- Port Match Capability can wake up host controller using interrupt pin
- 5 V Tolerant I/O

### Real Time Clock, SmaRTClock

- Precision time keeping with 32.768 kHz watch crystal; self-oscillate mode requires no external crystal; accepts external 32 kHz CMOS clock
- 36-hour programmable counter with wake up alarm
- Can wake up the host controller using interrupt pin
- Low power (<1.5  $\mu$ A)

### 256 Bytes RAM

- General purpose RAM expands the memory available to host controller.

### 16-bit Timers

- ┆ Two general purpose 16-bit timers

### Clock Sources

- 20 MHz Internal oscillator
- Can be clocked from an external CMOS clock

### Digital Bus Interface

- 4-wire SPI Interface (SPI device only) operates up to 2.5 Mbps with synchronous external clock or up to 1 Mbps with internal clock
- Dedicated  $\overline{\text{RST}}$  and  $\overline{\text{INT}}$  pins
- Optional  $\overline{\text{CLK}}$  pin can be used as a CMOS clock input.
- 2-wire SMBus/I<sup>2</sup>C interface (SMBus/I<sup>2</sup>C device only) operates up to 400 kHz with internal clock
- Optional PWR pin (SMBus/I<sup>2</sup>C device only) places the device in a low-power mode. SPI devices use the NSS pin to place device in a low-power mode

### Low Power

- 1.8–3.6 V operation with integrated LDO
- Ultra Low Power Mode w/ LCD (<3  $\mu$ A typical)
- Shutdown current (0.05  $\mu$ A typical)

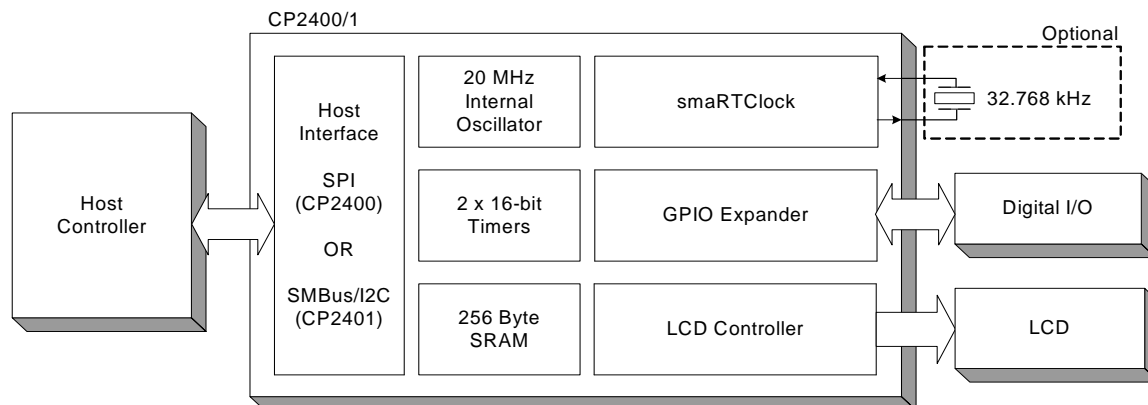
### Example Applications

- Handheld Equipment
- Utility Meters
- Thermostat Display
- Home Security Systems

### Temperature Range: –40 to +85 °C

### Full Technical Data Sheet

- CP2400/1/2/3



# CP2400-C-GDI

## 1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	RAM (Bytes)	SmaRTClock Real Time Clock	SMBus/I <sup>2</sup> C	Enhanced SPI	Timers (16-bit)	Digital Port I/Os	Package
CP2400-GDI <sup>1,2</sup>	20	256	✓	✓	✓	2	36	Tested Die in Wafer Form

**Notes:**

1. See "SPI Bonding Information" on page 7.
2. See "SMBus/I2C Bonding Information" on page 10.

## 2. Pin Definitions

Table 2.1 lists the pin definitions for the CP2400-C-GDI.

**Table 2.1. Pin Definitions for the CP2400-C-GDI**

Name	Physical Pad Number		Type	Description
	SPI	SMBus/ I <sup>2</sup> C		
XTAL1	2	2	A In	Crystal Input. This pin is the return for the external oscillator driver. This pin can be overdriven by an external CMOS clock.
XTAL2	3	3	A Out	Crystal Output. This pin is the excitation driver for a quartz crystal.
V <sub>DD</sub>	4	4	Power In	1.8–3.6 V Power Supply Voltage Input.
GND	5, 6, 43	5, 6, 43, 53	Ground	Ground
CAP	1	1	Power Out	LCD Power Supply Voltage Output. This pin requires a 10 µF decoupling capacitor.
$\overline{\text{CLK}}$	57	57	D In	CMOS clock input. This pin should not be left floating.
$\overline{\text{RST}}$	56	56	D In	Device Reset. An external source can initiate a system reset by driving this pin low for at least 15 µs. This pin has an internal weak pullup.
$\overline{\text{INT}}$	55	55	D Out	Interrupt Service Request. This pin provides notification to the host. This pin is a push-pull output.
NSS	52	—	D In	Slave select signal for SPI interface. This pin should not be left floating.
MOSI	51	—	D In	Master Out/Slave In data signal for SPI interface. This pin should not be left floating.
MISO	50	—	D Out	Master In/Slave Out data signal for SPI interface
SCK	49	—	D In	Clock signal for SPI interface. This pin should not be left floating.
$\overline{\text{PWR}}$	—	54	D In	Allows SMBus device to enter the Ultra Low Power mode. This pin should not be left floating.
SCL	—	52	D I/O	Clock signal for SMBus interface. This pin should not be left floating.
SDA	—	51	D I/O	Data signal for SMBus interface. This pin should not be left floating.

# CP2400-C-GDI

**Table 2.1. Pin Definitions for the CP2400-C-GDI (Continued)**

Name	Physical Pad Number		Type	Description
	SPI	SMBus/ I <sup>2</sup> C		
SMBA0	—	50	D In	Bit 0, SMBus Slave Address. This pin should not be left floating.
P0.0 LCD0	48	48	D I/O A Out	Bit 0, Port 0
P0.1 LCD1	47	47	D I/O A Out	Bit 1, Port 0
P0.2 LCD2	46	46	D I/O A Out	Bit 2, Port 0
P0.3 LCD3	45	45	D I/O A Out	Bit 3, Port 0
P0.4 LCD4	42	42	D I/O A Out	Bit 4, Port 0
P0.5 LCD5	41	41	D I/O A Out	Bit 5, Port 0
P0.6 LCD6	40	40	D I/O A Out	Bit 6, Port 0
P0.7 LCD7	39	39	D I/O A Out	Bit 7, Port 0
P1.0 LCD8	38	38	D I/O A Out	Bit 0, Port 1
P1.1 LCD9	37	37	D I/O A Out	Bit 1, Port 1
P1.2 LCD10	36	36	D I/O A Out	Bit 2, Port 1
P1.3 LCD11	35	35	D I/O A Out	Bit 3, Port 1
P1.4 LCD12	34	34	D I/O A Out	Bit 4, Port 1
P1.5 LCD13	33	33	D I/O A Out	Bit 5, Port 1
P1.6 LCD14	32	32	D I/O A Out	Bit 6, Port 1

**Table 2.1. Pin Definitions for the CP2400-C-GDI (Continued)**

Name	Physical Pad Number		Type	Description
	SPI	SMBus/ I <sup>2</sup> C		
P1.7 LCD15	31	31	D I/O A Out	Bit 7, Port 1
P2.0 LCD16	26	26	D I/O A Out	Bit 0, Port 2
P2.1 LCD17	25	25	D I/O A Out	Bit 1, Port 2
P2.2 LCD18	24	24	D I/O A Out	Bit 2, Port 2
P2.3 LCD19	23	23	D I/O A Out	Bit 3, Port 2
P2.4 LCD20	22	22	D I/O A Out	Bit 4, Port 2
P2.5 LCD21	21	21	D I/O A Out	Bit 5, Port 2
P2.6 LCD22	20	20	D I/O A Out	Bit 6, Port 2
P2.7 LCD23	19	19	D I/O A Out	Bit 7, Port 2
P3.0 LCD24	18	18	D I/O A Out	Bit 0, Port 3
P3.1 LCD25	17	17	D I/O A Out	Bit 1, Port 3
P3.2 LCD26	16	16	D I/O A Out	Bit 2, Port 3
P3.3 LCD27	15	15	D I/O A Out	Bit 3, Port 3
P3.4 LCD28	14	14	D I/O A Out	Bit 4, Port 3
P3.5 LCD29	13	13	D I/O A Out	Bit 5, Port 3
P3.6 LCD30	12	12	D I/O A Out	Bit 6, Port 3

# CP2400-C-GDI

Table 2.1. Pin Definitions for the CP2400-C-GDI (Continued)

Name	Physical Pad Number		Type	Description
	SPI	SMBus/ I <sup>2</sup> C		
P3.7 LCD31	11	11	D I/O A Out	Bit 7, Port 3
P4.0 COM0	10	10	D I/O A Out	Bit 0, Port 4
P4.1 COM1	9	9	D I/O A Out	Bit 1, Port 4
P4.2 COM2	8	8	D I/O A Out	Bit 2, Port 4
P4.3 COM3	7	7	D I/O A Out	Bit 3, Port 4

## 3. Bonding Information

### 3.1. SPI Bonding Information

Table 3.1. SPI Bonding Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (QFN-48)	Package Pin Name	Physical Pad X (μm)	Physical Pad Y (μm)
1	48	CAP	-858.75	545.41
2	1	XTAL1	-858.75	470.41
3	2	XTAL2	-858.75	395.41
4	3	VDD	-858.75	320.41
5	4	GND	-858.75	245.41
6	4	GND	-858.75	170.41
7	5	P4.3/COM3	-858.75	50.41
8	6	P4.2/COM2	-858.75	-24.59
9	7	P4.1/COM1	-858.75	-99.59
10	8	P4.0/COM0	-858.75	-174.59
11	9	P3.7/LCD31	-858.75	-249.59
12	10	P3.6/LCD30	-858.75	-324.59
13	11	P3.5/LCD29	-858.75	-399.59
14	12	P3.4/LCD28	-858.75	-474.59
15	13	P3.3/LCD27	-858.75	-549.59
16	14	P3.2/LCD26	-508.49	-739.5
17	15	P3.1/LCD25	-433.49	-739.5
18	16	P3.0/LCD24	-358.49	-739.5
19	17	P2.7/LCD23	-283.49	-739.5
20	18	P2.6/LCD22	-208.49	-739.5
21	19	P2.5/LCD21	-133.49	-739.5
22	20	P2.4/LCD20	-58.49	-739.5
23	21	P2.3/LCD19	61.51	-739.5
24	22	P2.2/LCD18	136.51	-739.5
25	23	P2.1/LCD17	211.51	-739.5
26	24	P2.0/LCD16	286.51	-739.5
27	Reserved*	—	361.51	-739.5
28	Reserved*	—	436.51	-739.5
29	Reserved*	—	511.51	-739.5

\*Note: Pins marked "Reserved" should not be connected.

# CP2400-C-GDI

**Table 3.1. SPI Bonding Pad Coordinates (Relative to Center of Die) (Continued)**

Physical Pad Number	Example Package Pin Number (QFN-48)	Package Pin Name	Physical Pad X (μm)	Physical Pad Y (μm)
30	Reserved*	—	858.75	-515.09
31	25	P1.7/LCD15	858.75	-440.09
32	26	P1.6/LCD14	858.75	-365.09
33	27	P1.5/LCD13	858.75	-290.09
34	28	P1.4/LCD12	858.75	-215.09
35	29	P1.3/LCD11	858.75	-140.09
36	30	P1.2/LCD10	858.75	-65.09
37	31	P1.1/LCD9	858.75	54.91
38	32	P1.0/LCD8	858.75	129.91
39	33	P0.7/LCD7	858.75	204.91
40	34	P0.6/LCD6	858.75	279.91
41	35	P0.5/LCD5	858.75	354.91
42	36	P0.4/LCD4	858.75	429.91
43	GND	GND	858.75	504.91
44	Reserved*	—	509.87	739.5
45	37	P0.3/LCD3	434.87	739.5
46	38	P0.2/LCD2	359.87	739.5
47	39	P0.1/LCD1	284.87	739.5
48	40	P0.0/LCD0	209.87	739.5
49	41	SCK	134.87	739.5
50	42	MISO	14.87	739.5
51	43	MOSI	-60.13	739.5
52	44	NSS	-135.13	739.5
53	Reserved*	—	-210.13	739.5
54	Reserved*	—	-285.13	739.5
55	45	INT	-360.13	739.5
56	46	RST	-435.13	739.5
57	47	CLK	-510.12	739.5

**\*Note:** Pins marked "Reserved" should not be connected.



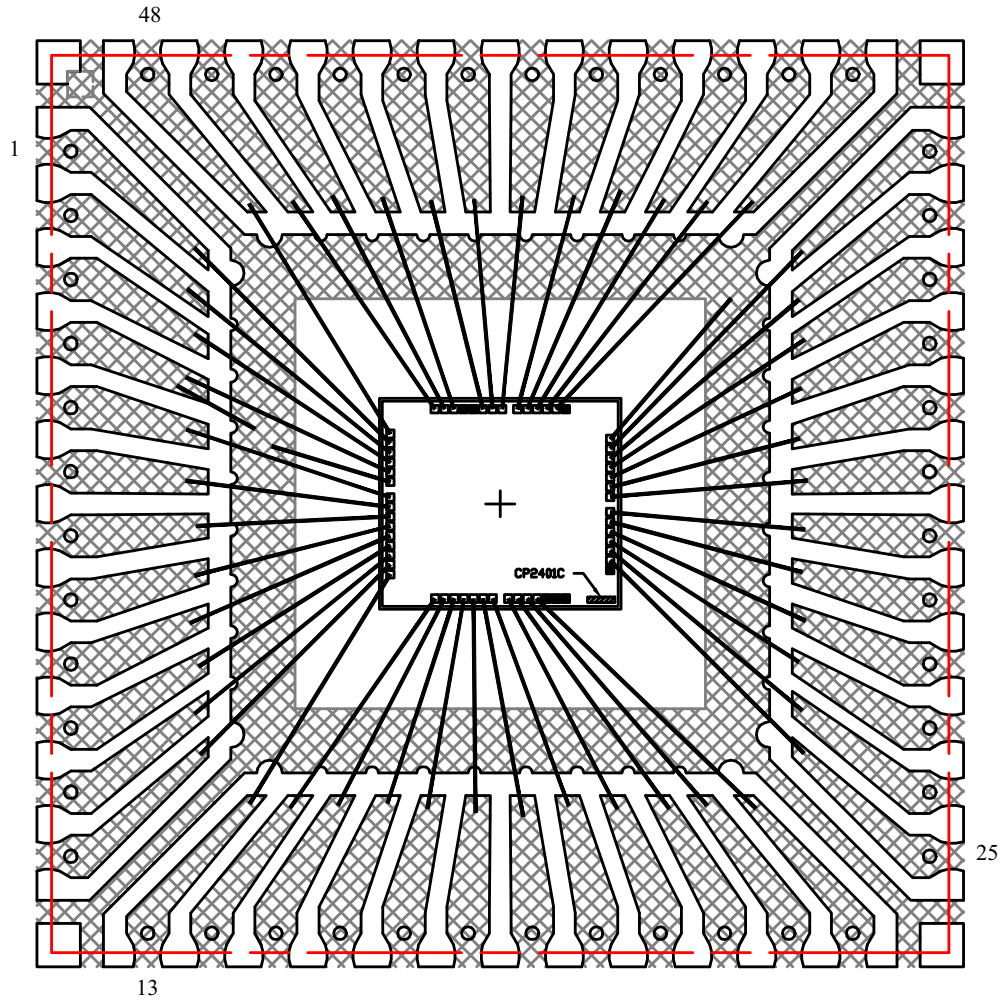


Figure 3.1. Example Die Bonding (QFN-48) for SPI

# CP2400-C-GDI

## 3.2. SMBus/I<sup>2</sup>C Bonding Information

Table 3.2. SMBus/I<sup>2</sup>C Bonding Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (QFP-48)	Package Pin Name	Physical Pad X (μm)	Physical Pad Y (μm)
1	48	CAP	-858.75	545.41
2	1	XTAL1	-858.75	470.41
3	2	XTAL2	-858.75	395.41
4	3	VDD	-858.75	320.41
5	4	GND	-858.75	245.41
6	4	GND	-858.75	170.41
7	5	P4.3/COM3	-858.75	50.41
8	6	P4.2/COM2	-858.75	-24.59
9	7	P4.1/COM1	-858.75	-99.59
10	8	P4.0/COM0	-858.75	-174.59
11	9	P3.7/LCD31	-858.75	-249.59
12	10	P3.6/LCD30	-858.75	-324.59
13	11	P3.5/LCD29	-858.75	-399.59
14	12	P3.4/LCD28	-858.75	-474.59
15	13	P3.3/LCD27	-858.75	-549.59
16	14	P3.2/LCD26	-508.49	-739.5
17	15	P3.1/LCD25	-433.49	-739.5
18	16	P3.0/LCD24	-358.49	-739.5
19	17	P2.7/LCD23	-283.49	-739.5
20	18	P2.6/LCD22	-208.49	-739.5
21	19	P2.5/LCD21	-133.49	-739.5
22	20	P2.4/LCD20	-58.49	-739.5
23	21	P2.3/LCD19	61.51	-739.5
24	22	P2.2/LCD18	136.51	-739.5
25	23	P2.1/LCD17	211.51	-739.5
26	24	P2.0/LCD16	286.51	-739.5
27	Reserved*	—	361.51	-739.5
28	Reserved*	—	436.51	-739.5
29	Reserved*	—	511.51	-739.5

**\*Note:** Pins marked “Reserved” should not be connected.

**Table 3.2. SMBus/I<sup>2</sup>C Bonding Pad Coordinates (Relative to Center of Die)**

Physical Pad Number	Example Package Pin Number (QFP-48)	Package Pin Name	Physical Pad X (μm)	Physical Pad Y (μm)
30	Reserved*	—	858.75	-515.09
31	25	P1.7/LCD15	858.75	-440.09
32	26	P1.6/LCD14	858.75	-365.09
33	27	P1.5/LCD13	858.75	-290.09
34	28	P1.4/LCD12	858.75	-215.09
35	29	P1.3/LCD11	858.75	-140.09
36	30	P1.2/LCD10	858.75	-65.09
37	31	P1.1/LCD9	858.75	54.91
38	32	P1.0/LCD8	858.75	129.91
39	33	P0.7/LCD7	858.75	204.91
40	34	P0.6/LCD6	858.75	279.91
41	35	P0.5/LCD5	858.75	354.91
42	36	P0.4/LCD4	858.75	429.91
43	GND	GND	858.75	504.91
44	Reserved*	—	509.87	739.5
45	37	P0.3/LCD3	434.87	739.5
46	38	P0.2/LCD2	359.87	739.5
47	39	P0.1/LCD1	284.87	739.5
48	40	P0.0/LCD0	209.87	739.5
49	Reserved*	—	134.87	739.5
50	41	SMBA0	14.87	739.5
51	42	SDA	-60.13	739.5
52	43	SCL	-135.13	739.5
53	GND	GND	-210.13	739.5
54	44	/PWR	-285.13	739.5
55	45	/INT	-360.13	739.5
56	46	/RST	-435.13	739.5
57	47	/CLK	-510.12	739.5

**\*Note:** Pins marked “Reserved” should not be connected.

# CP2400-C-GDI

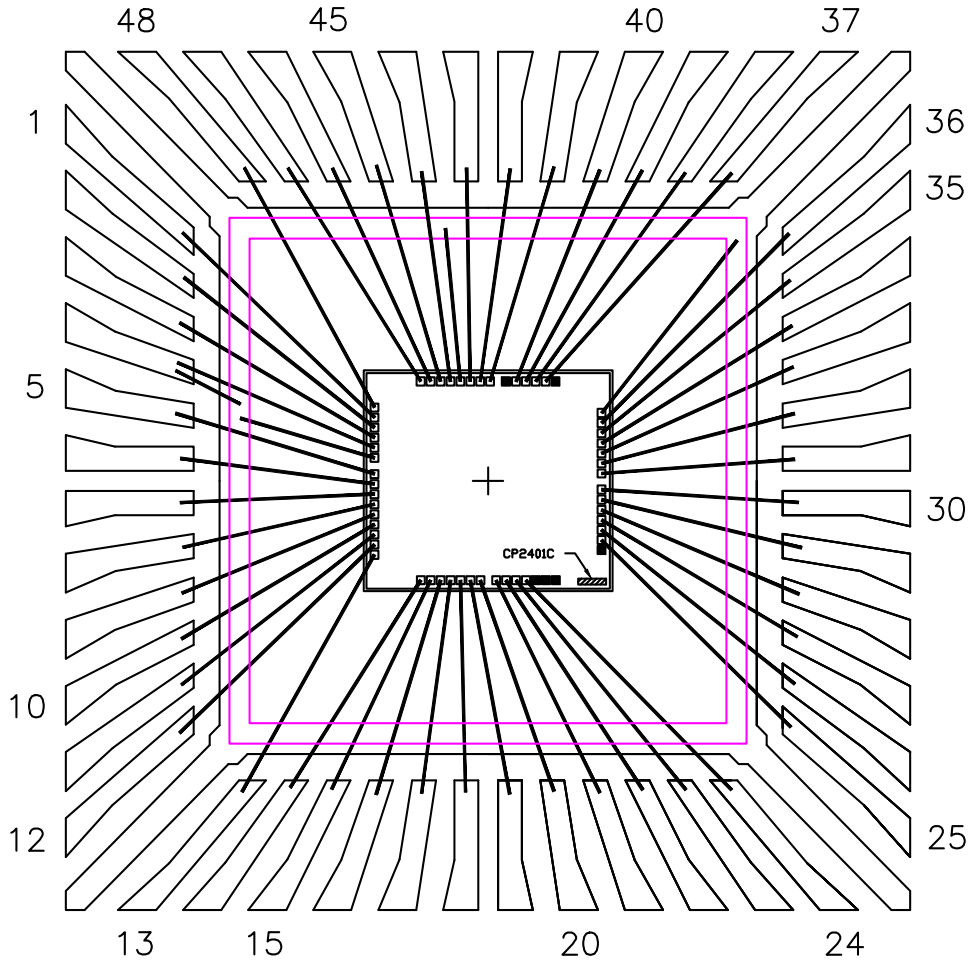


Figure 3.2. Example Die Bonding (QFP-48) for SMBus/I<sup>2</sup>C

**Table 3.3. Wafer and Die Information**

<b>Wafer ID</b>	CP2401C
<b>Wafer Dimensions</b>	8 in
<b>Die Dimensions</b>	1.88 mm x 1.64 mm
<b>Wafer Thickness</b>	12 mil ±1 mil
<b>Wafer Identification</b>	Notch
<b>Scribe Line Width</b>	80 µm
<b>Die Per Wafer*</b>	Contact Sales for info
<b>Passivation</b>	Standard
<b>Wafer Packaging Detail</b>	Wafer Crisper
<b>Bond Pad Dimensions</b>	60 µm x 60 µm
<b>Maximum Processing Temperature</b>	250 °C
<b>Electronic Die Map Format</b>	.txt
<b>Bond Pad Pitch Minimum</b>	65 µm
<b>*Note:</b> This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

# CP2400-C-GDI

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## 4. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

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**NOTES:**

# CP2400-C-GDI

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## CONTACT INFORMATION

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