STM8AF61xx
STM8AF51xx

Automotive 8-bit MCU, with up to 128 Kbytes Flash, EEPROM, 10-bit ADC, timers, LIN, CAN, USART, SPI, I²C, 3 V to 5.5 V

Preliminary Data

Features

Core

- Max f_{CPU}: Up to 24 MHz
- Advanced STM8 core with Harvard architecture and 3-stage pipeline
- Average 1.6 cycles/instruction resulting in 10 MIPS at 16 MHz f_{CPU} for industry standard benchmark

Memories

- Program memory: Up to 128 Kbytes Flash; data retention 20 years at 85°C after 1 kcycles
- Data memory: Up to 2 Kbytes true data EEPROM; endurance 300 kcycles
- RAM: Up to 6 Kbytes

Clock management

- Low power crystal resonator oscillator with external clock input
- Internal, user-trimmable 16 MHz RC and low power 128 kHz RC oscillators
- Clock security system with clock monitor

Reset and supply management

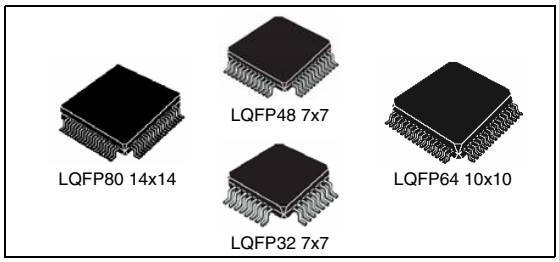
- Multiple low power modes (wait, slow, auto wake-up, halt) with user definable clock gating
- Permanently active, low consumption power-on and power-down reset

Interrupt management

- Nested interrupt controller with 32 interrupts
- Up to 38 external interrupts on 4 vectors

Timers

- 16-bit autoreload (AR) PWM timers with up to 3 CAPCOM channels each (IC, OC or PWM)
- Multipurpose timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
- 8-bit AR system timer with 8-bit prescaler
- Auto wake-up timer
- 2 watchdog timers: Window and standard



Communications interfaces

- High speed 1 Mbit/s active CAN 2.0B interface
- USART with clock output for synchronous operation - LIN master mode
- LINUART LIN 2.1 compliant, master/slave modes with automatic resynchronization
- SPI synchronous serial interface up to 8 Mbit/s or (f_{CPU}/2)
- I^2C interface up to 400 Kbit/s

Analog to digital converter (ADC)

- 10-bit, 3 LSB ADC with up to 16 multiplexed channels

I/Os

- Up to 68 I/Os on an 80-pin package including 10 high sink I/Os
- Highly robust I/O design, immune against current injection

Table 1. Device summary

Ref.	Root part number
STM8AF61xx	STM8AF61AA, STM8AF619A, STM8AF61A9, STM8AF6199, STM8AF6189, STM8AF6179, STM8AF6169, STM8AF61A8, STM8AF6198, STM8AF6188, STM8AF6178, STM8AF6168, STM8AF6148, STM8AF6186, STM8AF6176, STM8AF6166, STM8AF6146
STM8AF51xx	STM8AF51AA, STM8AF519A, STM8AF51A9, STM8AF5199, STM8AF5189, STM8AF5179, STM8AF5169, STM8AF51A8, STM8AF5198, STM8AF5188, STM8AF5178, STM8AF5168, STM8AF5186, STM8AF5176, STM8AF5166

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1 Introduction

This datasheet contains the description of the STM8AF61xx/STM8AF51xx family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to the STM8S/STM8A reference manual (RM0009)
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0047)
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470)
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044)

2 Description

The STM8AF51xx and STM8AF61xx automotive 8-bit microcontrollers offer from 16 Kbytes up to 128 Kbytes of program memory and integrated true data EEPROM.

The STM8AF51xx series features a CAN interface.

All devices of the STM8A product line provide the following benefits:

- Reduced system cost
  - Integrated true data EEPROM for up to 300 k write/erase cycles
  - High system integration level with internal clock oscillators, watchdog and brown-out reset
- Performance and robustness
  - Average 10 MIPS/100 ns instruction time at 16 MHz CPU clock frequency
  - Robust I/O, independent watchdogs with separate clock source
  - Clock security system
- Short development cycles
  - Applications scalability across a common family product architecture with compatible pinout, memory map and and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - Native automotiveProduct family operating both at 3.3 V and 5 V supply

All STM8A and ST7 microcontrollers are supported by the same tools including STVD/STVP development environment, the STice emulator and the the low-cost in-circuit debugging tool RLINK.

3 Product line-up

Table 2. STM8A common features

Order code	Common features
STMA8AF51xx STMA8AF61xx	STM8 CPU Single-wire ICP/ICD interface Nested interrupts: 32 vectors, 3 software priority levels Program memory read-out protection Window watchdog and standard watchdog timers Auto wake-up timer Clock security system for external clock sources Internal RC oscillator 16 MHz with trimming register Low-power internal RC oscillator 128 MHz Power-on reset and brown-out reset

Table 3. STM8AF51xx product line-up - with CAN

Order code	Package	Prog. (bytes)	RAM (bytes)	Data EE (bytes)	10-bit A/D ch.	Timers (IC/OC/PWM)	Serial interfaces	I/0s wakeup pins
STM8AF51AAT	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	CAN, LIN(UART), SPI, USART, I²C	72/38
STM8AF519AT		96 K						
STM8AF51A9T	LQFP64 (10x10)	128 K						56/37
STM8AF5199T		96 K						
STM8AF5189T		64 K	4 K	1.5 K				
STM8AF5179T		48 K	3 K					
STM8AF5169T		32 K	2 K	1 K				
STM8AF51A8T	LQFP48 (7x7)	128 K	6 K	2 K	10			40/36
STM8AF5198T		96 K						
STM8AF5188T		64 K	4 K	1.5 K				
STM8AF5178T		48 K	3 K					
STM8AF5168T		32 K	2 K	1 K				
STM8AF5186T(1)	LQFP32 (7x7)(2)	64 K	4 K	1.5 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	CAN, LIN(UART), SPI, I²C	25/24
STM8AF5176T(1)		48 K	3 K					
STM8AF5166T(1)		32 K	2 K	1 K				

1. Under development
2. Also QFN package available

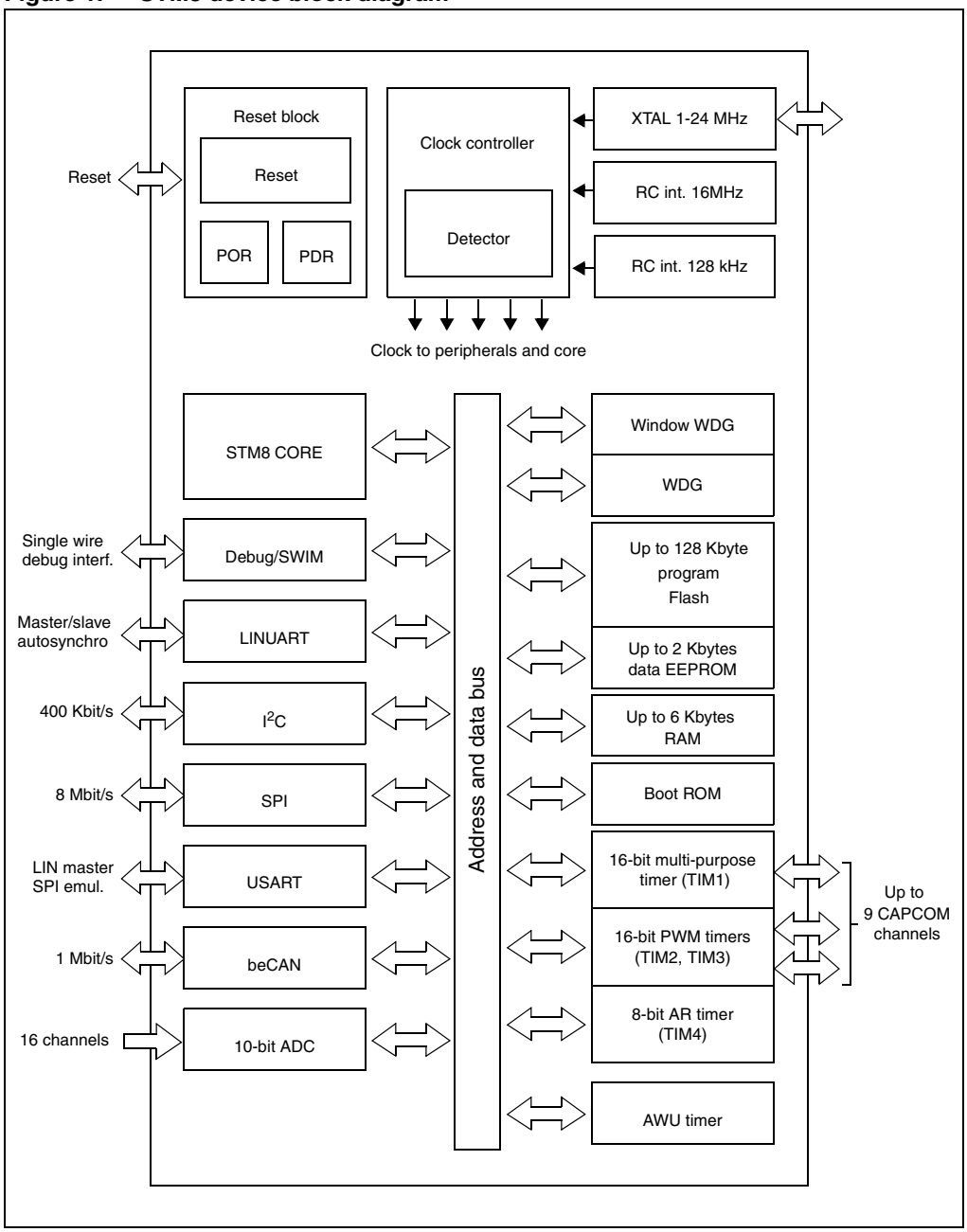
Table 4. STM8AF61xx product line-up - no CAN

Order code	Package	Prog. (bytes)	RAM (bytes)	Data EE (bytes)	10-bit A/D ch.	Timers (IC/OC/PWM)	Serial interfaces	I/0s wakeup pins
STM8AF61AAT	LQFP80 (14x14)	128 K	6 K	2 K	16	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, USART, I²C	72/38
STM8AF619AT		96 K		2 K				
STM8AF61A9T	LQFP64 (10x10)	128 K		2 K				56/37
STM8AF6199T		96 K		2 K				
STM8AF6189T		64 K	4 K	1.5 K				
STM8AF6179T		48 K	3 K	1.5 K				
STM8AF6169T		32 K	2 K	1 K				
STM8AF61A8T	LQFP48 (7x7)[1]	128 K	6 K	2 K	10			40/36
STM8AF6198T		96 K		2 K				
STM8AF6188T		64 K	4 K	1.5 K				
STM8AF6178T		48 K	3 K	1.5 K				
STM8AF6168T		32 K	2 K	1 K			LIN(UART), SPI, I²C	
STM8AF6148T		16 K	1 K	0.5 K				
STM8AF6186T	LQFP32 (7x7)	64 K	4 K	1.5 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)		25/24
STM8AF6176T		48 K	3 K	1.5 K				
STM8AF6166T		32 K	2 K	1 K				
STM8AF6146T		16 K	1 K	0.5 K		1x8-bit: TIM4 2x16-bit: TIM1, TIM3 (6/6/6)	LIN(UART), SPI	

1. Also QFN package available

4 Block diagram

Figure 1. STM8 device block diagram



5 Product overview

The following section intends to give an overview of the basic features of the STM8A functional modules and peripherals.

For more detailed information please refer to the STM8 hardware reference manual RM0009.

5.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 21 internal registers (6 directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

5.1.1 Single wire data interface (SWIM) debug module

The debug module with its single wire data interface SWIM permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes. There is a maximum data transmission speed of 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints)
- 2 advanced breakpoints, 23 predefined configurations

5.2 Interrupt controller

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 38 external interrupts on 4 vectors
- Trap and reset interrupts

5.3 Non-volatile memory

- Up to 128 Kbytes of program single voltage Flash memory
- Up to 2 Kbytes true data EEPROM
- Read while write: Writing in data memory possible while executing code in program memory
- 128 user option bytes

Architecture

- Array: Up to 128 Kbytes of Flash program memory organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes)

Writing, erasing, word and block register management is handled automatically by the memory interface.

Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory in case of user software malfunction. The implemented WP scheme enables

- Write protection of the program memory in user mode
- Code update in user mode

The program memory is divided into two areas:

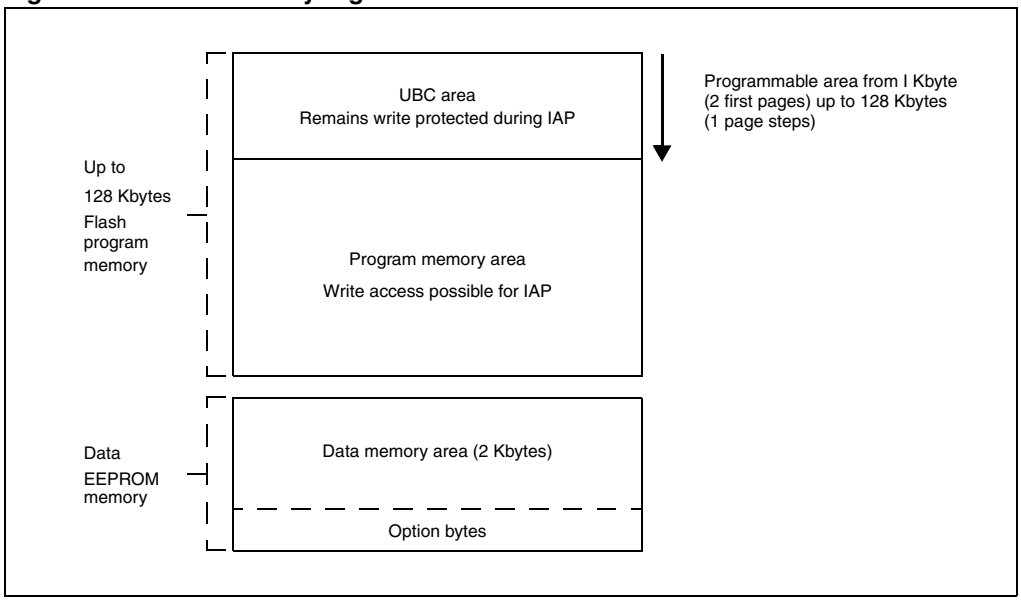
- Main program memory: Up to 128 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 128 Kbytes

The UBC area remains write-protected during in-application programming. It permits storage of the boot program or specific code libraries.

The boot area is a part of the program memory that contains the reset and interrupt vectors, the reset routine and usually the IAP and communication routines. The UBC area has a second level of protection to prevent unintentional erasing or modification during IAP programming. This means that the mass keys do not unlock the UBC area.

The size of the UBC is programmable through the UBC option byte, in increments of 512 bytes, by programming the UBC option byte in ICP mode.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the program memory, data memory and RAM in debug mode. Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory.

Speed

- Operation at up to 16 MHz CPU clock frequency without wait-states
- Programming time (same for word or block):
  - Fast programming (without erase): < 3 ms
  - Standard programming (erase + program): < 6 ms
  - Erase time: < 3 ms
  - Total code write time for 128 Kbyte: (1024) pages * 3 ms = 3.7 s (fast write)

5.4 Low-power operating modes

The product features various low-power modes:

- Slow mode: prescaled CPU clock, selected peripherals at full clock speed
- Active halt mode: CPU and peripheral clock stopped. The programmable wake-up time is controlled by the AWU unit using the internal low-power 128 kHz oscillator clock.
- Halt mode: CPU and peripheral clock stopped, the device remains powered. Wake-up by external interrupt.

In all modes the CPU and peripherals remain permanently powered, the system clock is applied only to selected modules.

The RAM content is guaranteed. Also, the brown-out reset circuit remains activated.

5.5 Clock and clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and insures clock robustness.

Features

- **Clock sources:** Internal 16 MHz and 128 kHz RC oscillators, intrapad crystal oscillator and input for external clock signal
- **Reset:** After reset the microcontroller restarts by default with an internal 2 MHz clock (16 MHz/8). The prescaler ratio and the clock source can be changed by the application program as soon as the code execution starts.
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Wake-up:** The recovery from halt and AWU (auto wake-up) low power modes uses the internal 16 MHz/8 RC oscillator for quick start-up and then switches to the last selected clock source before halt mode is entered.
- **Clock security system (CSS):** This feature is automatically is automatically activated if the external clock is selected. In case of a clock failure, the internal RC (16 MHz/8) is automatically selected and an interrupt is generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application. Available frequencies are 8 MHz, 4 MHz or 1 MHz.

5.5.1 Internal 16 MHz RC oscillator

- Default clock after reset 2 MHz (16 MHz/8)
- Wake-up time: < 2 µs

Precision:

- Calibration during final test at room-temperature to ±1 %
- ±3 % at 4.5 to 5.5 V (0 °C to 90 °C)
- ±5 % for the full supply voltage and temperature range (3.0 to 5.5 V, -40 °C to 125 °C)

Trimming

A trimming register permits frequency readjustment to a precision of 1.5 % by the application program. The initial final-test setting remains unchanged.

5.5.2 Internal 128 kHz RC oscillator

Frequency: 128 kHz, independent from the main clock

Precision: 12.5 % over full voltage and frequency range, minimum frequency 100 kHz

This clock drives the watchdog or the wake-up timer also automatically activates the internal 128 kHz oscillator.

5.5.3 Internal high-speed crystal oscillator

The internal high-speed crystal oscillator delivers the main clock in normal run mode. It operates with quartz and ceramic resonators.

- Frequency range: 1 to 24 MHz
- Wake-up time: < 2 ms @ 24 MHz
- Oscillation mode: preferred fundamental
- Output duty cycle: max 55/45 %
- I/Os: Standard I/O pins multiplexed with OSCin, OSCout

Optionally, an external clock signal can be injected into the OSCIN input pin.

Resonators (quartz or ceramic)

- Load capacitors: 10 to 20 pF
- Serial resistance: 50 to 80 Ω
- Maximum crystal power: 100 µW

5.5.4 External clock input

- Comparator hysteresis: 0.1 * V_{DD}
- Frequency: 32 kHz to 24 MHz

5.5.5 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

5.6 Timers

5.6.1 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

The WDG timer activity is controlled by option bytes. Once activated the watchdog can not be disabled by the user program without reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out periode can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower then the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHZ LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

5.6.2 Auto wake-up counter

- Used for auto wake-up from active halt mode
- Clock source: internal 128 kHz internal low frequency RC oscillator or external clock
- Programmable interrupt time from 5 ms up to 1 s (TBD)

5.6.3 Multipurpose and PWM timers

The STM8 devices contain up to three 16-bit multipurpose and PWM timers providing 9 CAPCOM channels in total.

Table 5. STM8 timer configuration

Timer	Counter	Pre-scaler	Type	CAPCOM	Complem. outputs	Trigger unit
Timer1	16	16	Up/down	4	3	Yes
Timer2		15-bit fixed power of 2 ratios	Up	3	0	No
Timer3				2		
Timer4	8	7-bit fixed power of 2 ratios		0		

16-bit PWM timers

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable CAPCOM channels
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

Timer 1 - multipurpose PWM timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down AR counter with 16-bit prescaler
- 4 independent CAPCOM channels configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signal
- Break input to force the timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

5.6.4 System timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

5.7 ADC

All STM8 products contain one 10-bit successive approximation ADC with up to 16 multiplexed input channels.

General features:

- Input voltage range: 0 to V_{DDA}
- Conversion time: 14 clock cycles (7 µs @ 2 MHz ADC clock)
- Acqusition modes:
  - Single conversion
  - Continous acquisition - Up to 100 Ksamples/s effective sampling rate
  - Analog watchdog with 2 trigger levels (not on 128 K and 96 K products)
- Trigger
  - Trigger register and external trigger input
- Interrupts
  - End of conversion (EOC) - can be masked
- Electrical parameters:
  - TUE ≤ 3 LSB max.
  - Wake-up time from power-down < 7µs
  - Maximum source impedance: 15 kΩ
  - Input capacitance 3 pF

5.8 Communication interfaces

The following communication interfaces are implemented on STM8 products:

- USART: Full feature UART, SPI emulation, LIN master capability
- LIN-UART: LIN2.1 master/slave capability, full feature UART
- SPI - full and half-duplex, 8 Mbit/s
- I²C - up to 400 Kbit/s
- CAN (rev. 2.0A,B) - 3 Tx mailboxes - up to 1 Mbit/s
- SWIM - single wire interface for debugging and device programming

5.8.1 USART

Main features

- 1 Mbit/s full duplex SCI
- LIN master capable
- SPI emulation
- Baud rate prescaler size: 12-bit mantissa/4-bit fractional

Asynchronous communication (SCI)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- 2 receiver wake-up modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit synch break frame
- Reception: Detects 11-bit break frame

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Max. speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

5.8.2 LIN-UART

Main features

- LIN master/slave rev. 2.1 compliant
- Auto-synchronization in LIN slave mode
- Baud rate prescaler size 12-bit mantissa/4-bit fractional
- 1 Mbit full duplex SCI

LIN master

- Autonomous header handling
- 13-bit LIN synch break generation

LIN slave

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ±15 %
- Synch delimiter checking
- 11-bit LIN synch break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

Asynchronous communication (SCI)

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- Independently programmable transmit and receive baud rates up to 500 Kbit/s
- Programmable data word length (8 or 9 bits)
- Low-power standby mode - 2 receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Overrun, noise and frame error detection
- 6 interrupt sources
- Tx, Rx parity control

5.8.3 SPI

- Maximum speed: 8 Mbit/s ($f_{CPU}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

5.8.4 I^2C

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)
- 3 interrupt vectors:
  - 1 interrupt for successful address/data communication
  - 1 interrupt for error condition
  - 1 interrupt for wake-up from halt
- Wake-up

5.8.5 CAN

The beCAN3 controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It has been designed to manage a high number of incoming messages efficiently with a minimum CPU load.

For safety-critical applications the CAN controller provides all hardware functions to support the CAN time triggered communication option (TTCAN).

The maximum transmission speed is 1 Mbit.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request
- Time stamp on SOF transmission

Reception

- 8-, 11- and 29-bit ID
- 1 receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message
- Configurable FIFO overrun
- Time stamp on SOF reception
- 6 filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID
- Filtering modes:
  - Mask mode permitting ID range filtering
  - ID list mode
- Time triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Configurable timer resolution
  - Time stamp sent in last two data bytes

Interrupt management

- Maskable interrupt
- Software-efficient mailbox mapping at a unique address space

5.9 Input/output specifications

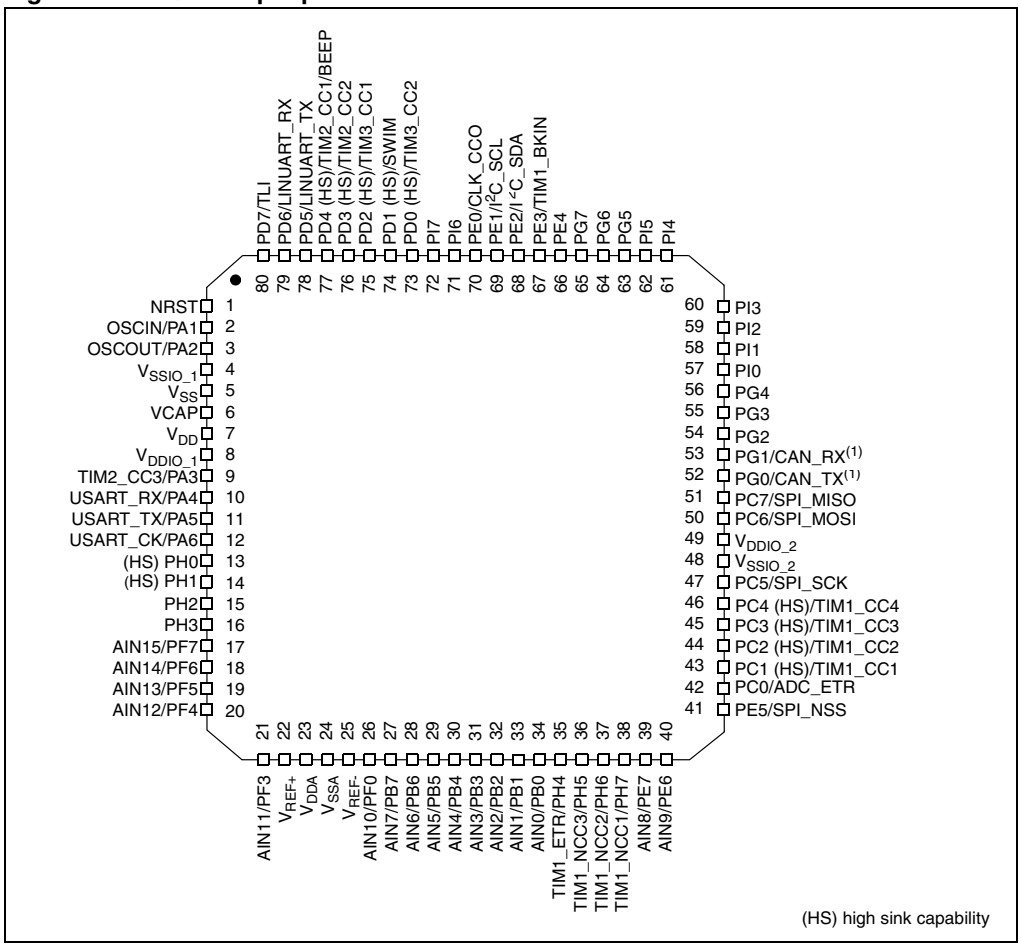
The product features four different I/O types:

- Standard I/O 1.5 mA, rise/fall time 120 ns at 5 V, 50 pF load, 2 MHz
- Fast I/O 3 mA, rise/fall time 20 ns at 5 V, 50 pF load, 10 MHz
- High sink 8 mA @ V_{OL} = 0.6 V, speed similar to standard I/O
- True open drain (I^2C interface)
- In order to decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

6 Pinouts and pin description

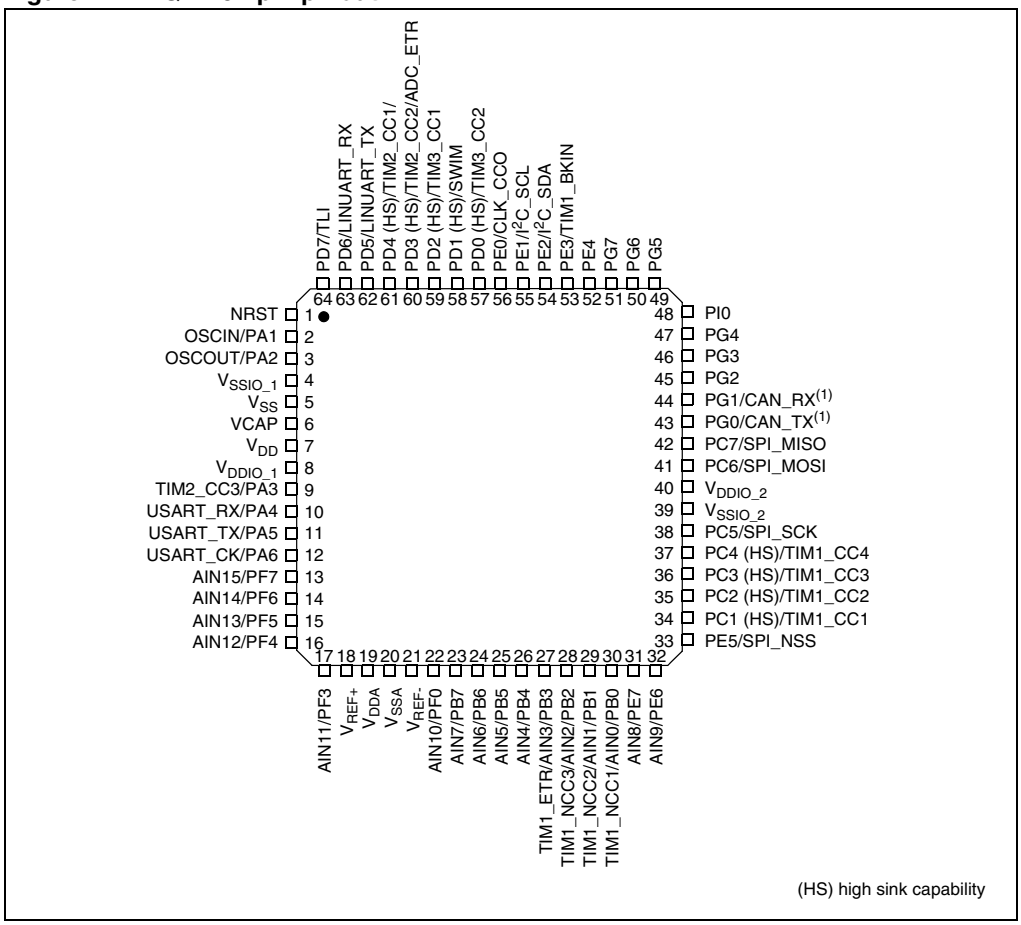
6.1 LQFP package pinouts

Figure 3. LQFP 80-pin pinout



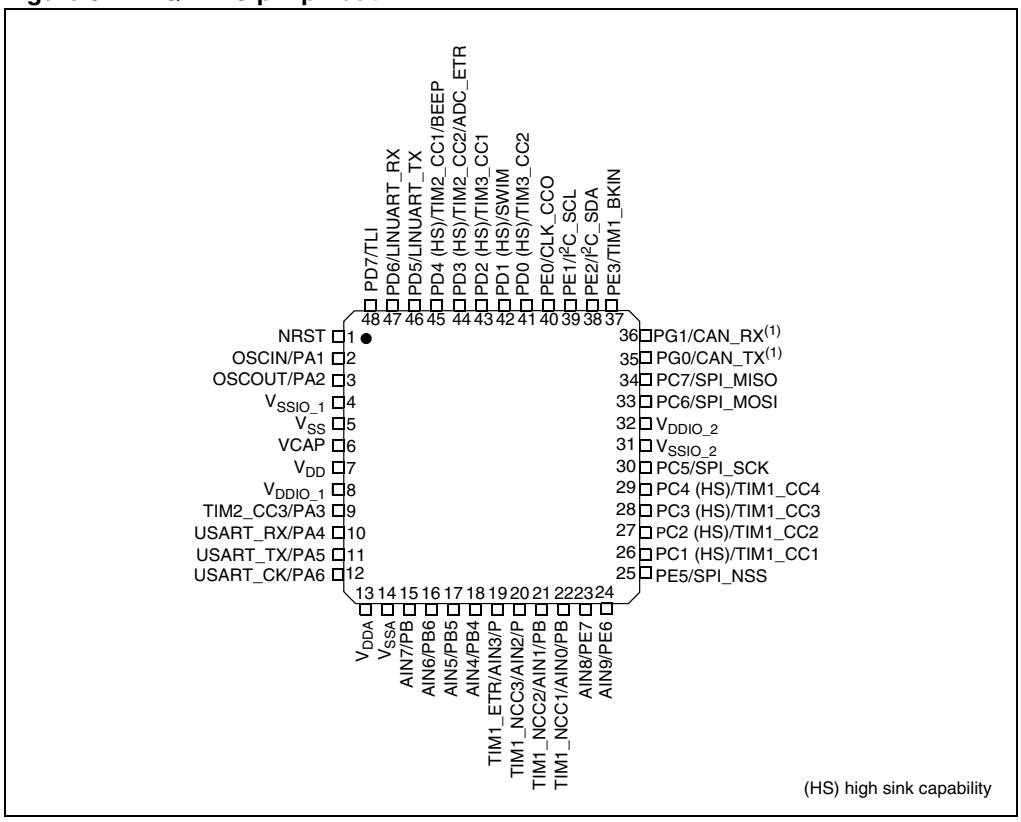
1. Only available on the STM8AF51xx product line

Figure 4. LQFP 64-pin pinout



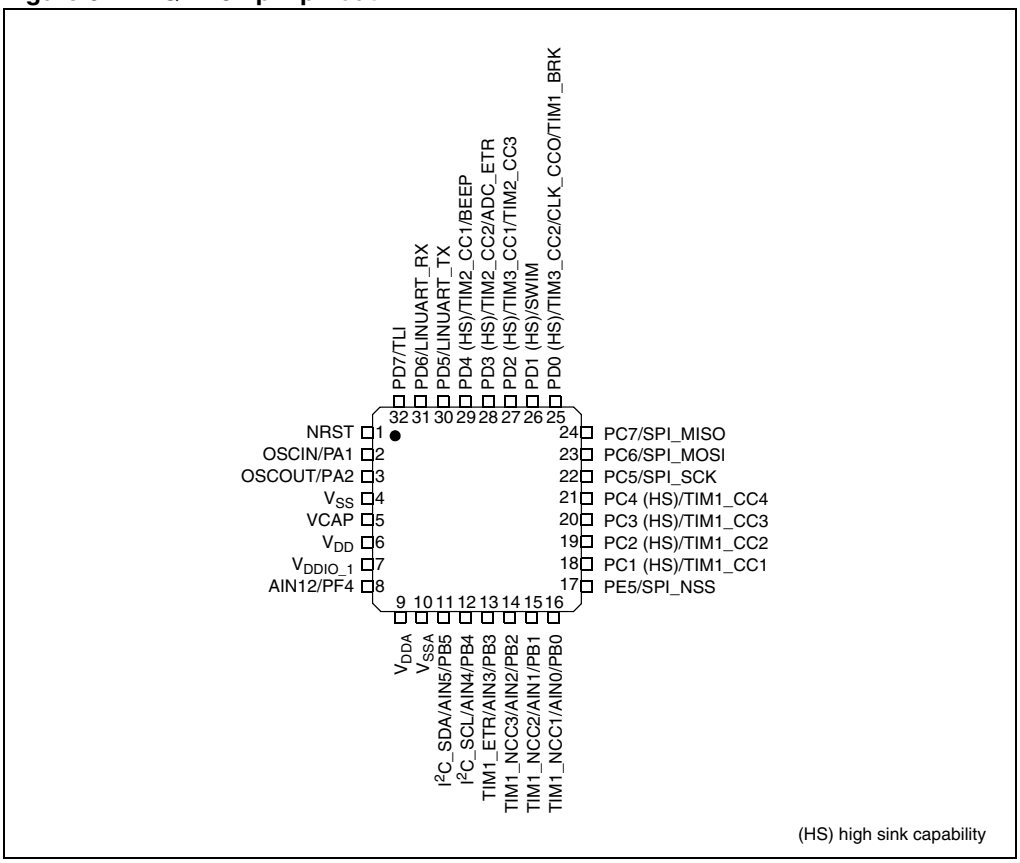
1. Only available on the STM8AF51xx product line

Figure 5. LQFP 48-pin pinout



1. Only available on the STM8AF51xx product line

Figure 6. LQFP 32-pin pinout



6.2 Pin description

Table 6. Legend/abbreviation for *Table 7*

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS
	Output	HS = High sink (20 mA)
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull

Reset state is shown in **bold**.

Table 7. STM8A MCU family pin description

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	1	NRST	I/O		**X**						Reset		
2	2	2	2	PA1/OSCIN	I/O	**X**	X	X		O1	X	X	**Port A1**	Resonator/crystal in	
3	3	3	3	PA2/OSCOUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/crystal out	
4	4	4	-	V_{SSIO_1}	S								I/O ground		
5	5	5	4	V_{SS}	S								Digital ground		
6	6	6	5	VCAP	S								1.8 V regulator capacitor		
7	7	7	6	V_{DD}	S								Digital power supply		
8	8	8	7	V_{DDIO_1}	S								I/O power supply		
9	9	9	-	PA3/TIM2_CC3	I/O	**X**	X	X		O1	X	X	**Port A3**	Timer 2 - channel3	TIM3_CC1 [AFR1]
10	10	10	-	PA4/USART_RX	I/O	**X**	X	X		O3	X	X	**Port A4**	USART receive	
11	11	11	-	PA5/USART_TX	I/O	**X**	X	X		O3	X	X	**Port A5**	USART transmit	
12	12	12	-	PA6/USART_CK	I/O	**X**	X	X		O3	X	X	**Port A6**	USART synchronous clock	
13	-	-	-	PH0	I/O	**X**	X		HS	O3	X	X	**Port H0**		
14	-	-	-	PH1	I/O	**X**	X		HS	O3	X	X	**Port H1**		
15	-	-	-	PH2	I/O	**X**	X			O1	X	X	**Port H2**		
16	-	-	-	PH3	I/O	**X**	X			O1	X	X	**Port H3**		
17	13	-	-	PF7/AIN15	I/O	**X**	X			O1	X	X	**Port F7**	Analog input 15	
18	14	-	-	PF6/AIN14	I/O	**X**	X			O1	X	X	**Port F6**	Analog input 14	
19	15	-	-	PF5/AIN13	I/O	**X**	X			O1	X	X	**Port F5**	Analog input 13	
20	16	-	8	PF4/AIN12	I/O	**X**	X			O1	X	X	**Port F4**	Analog input 12	
21	17	-	-	PF3/AIN11	I/O	**X**	X			O1	X	X	**Port F3**	Analog input 11	
22	18	-	-	V_{REF+}	S								ADC positive reference voltage		
23	19	13	9	V_{DDA}	S								Analog power supply		
24	20	14	10	V_{SSA}	S								Analog ground		
25	21	-	-	V_{REF-}	S								ADC negative reference voltage		
26	22	-	-	PF0/AIN10	I/O	**X**	X			O1	X	X	**Port F0**	Analog input 10	

Table 7. STM8A MCU family pin description (continued)

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
27	23	15	-	PB7/AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	
28	24	16	-	PB6/AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
29	25	17	11	PB5/AIN5	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	12	PB4/AIN4	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
31	27	19	13	PB3/AIN3	I/O	**X**	X	X		O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
32	28	20	14	PB2/AIN2	I/O	**X**	X	X		O1	X	X	**Port B2**	Analog input	TIM1_ NCC3 [AFR5]
33	29	21	15	PB1/AIN1	I/O	**X**	X	X		O1	X	X	**Port B1**	Analog input 1	TIM1_ NCC2 [AFR5]
34	30	22	16	PB0/AIN0	I/O	**X**	X	X		O1	X	X	**Port B0**	Analog input 0	TIM1_ NCC1 [AFR5]
35	-	-	-	PH4/TIM1_ETR	I/O	**X**	X			O1	X	X	**Port H4**	Timer 1 - trigger input	
36	-	-	-	PH5/ TIM1_NCC3	I/O	**X**	X			O1	X	X	**Port H5**	Timer 1 - inverted channel 3	
37	-	-	-	PH6/TIM1_NCC2	I/O	**X**	X			O1	X	X	**Port H6**	Timer 1 - inverted channel 2	
38	-	-	-	PH7/TIM1_NCC1	I/O	**X**	X			O1	X	X	**Port H7**	Timer 1 - inverted channel 2	
39	31	23	-	PE7/AIN8	I/O	**X**	X			O1	X	X	**Port E7**	Analog input 8	
40	32	24		PE6/AIN9	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 9	
41	33	25	17	PE5/SPI_NSS	I/O	**X**	X	X		O1	X	X	**Port E5**	SPI master/slave select	
42	-	-	-	PC0/ADC_ETR	I/O	**X**	X	X		O1	X	X	**Port C0**	ADC trigger input	
43	34	26	18	PC1/TIM1_CC1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	
44	35	27	19	PC2/TIM1_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	
45	36	28	20	PC3/TIM1_CC3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	

Table 7. STM8A MCU family pin description (continued)

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
46	37	29	21	PC4/TIM1_CC4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	
47	38	30	22	PC5/SPI_SCK	I/O	**X**	X	X		O3	X	X	**Port C5**	SPI clock	
48	39	31	-	V_{SSIO_2}	S								I/O ground		
49	40	32	-	V_{DDIO_2}	S								I/O power supply		
50	41	33	23	PC6/SPI_MOSI	I/O	**X**	X	X		O3	X	X	**Port C6**	SPI master out/ slave in	
51	42	34	24	PC7/SPI_MISO	I/O	**X**	X	X		O3	X	X	**Port C7**	SPI master in/ slave out	
52	43	35	-	PG0/CAN_TX	I/O	**X**	X			O1	X	X	**Port G0**	CAN transmit	
53	44	36	-	PG1/CAN_RX	I/O	**X**	X			O1	X	X	**Port G1**	CAN receive	
54	45	-	-	PG2	I/O	**X**	X			O1	X	X	**Port G2**		
55	46	-	-	PG3	I/O	**X**	X			O1	X	X	**Port G3**		
56	47	-	-	PG4	I/O	**X**	X			O1	X	X	**Port G4**		
57	48	-	-	PI0	I/O	**X**	X			O1	X	X	**Port I0**		
58	-	-	-	PI1	I/O	**X**	X			O1	X	X	**Port I1**		
59	-	-	-	PI2	I/O	**X**	X			O1	X	X	**Port I2**		
60	-	-	-	PI3	I/O	**X**	X			O1	X	X	**Port I3**		
61	-	-	-	PI4	I/O	**X**	X			O1	X	X	**Port I4**		
62	-	-	-	PI5	I/O	**X**	X			O1	X	X	**Port I5**		
63	49	-	-	PG5	I/O	**X**	X			O1	X	X	**Port G5**		
64	50	-	-	PG6	I/O	**X**	X			O1	X	X	**Port G6**		
65	51	-	-	PG7	I/O	**X**	X			O1	X	X	**Port G7**		
66	52	-	-	PE4	I/O	**X**	X	X		O1	X	X	**Port E4**		
67	53	37	-	PE3/TIM1_BKIN	I/O	**X**	X	X		O1	X	X	**Port E3**	Timer 1 - break input	
68	54	38	-	PE2/I^2C_SDA	I/O	**X**	X	X		O1	T(1)	X	**Port E2**	I^2C data	
69	55	39	-	PE1/I^2C_SCL	I/O	**X**	X	X		O1	T(1)	X	**Port E1**	I^2C clock	
70	56	40	-	PE0/CLK_CCO	I/O	**X**	X	X		O3	X	X	**Port E0**	Configurable clock output	
71	-	-	-	PI6	I/O	**X**	X			O1	X	X	**Port I6**		
72	-	-	-	PI7	I/O	**X**	X			O1	X	X	**Port I7**		

Table 7. STM8A MCU family pin description (continued)

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
73	57	41	25	PD0/TIM3_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
74	58	42	26	PD1/SWIM	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
75	59	43	27	PD2/TIM3_CC1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CC3 [AFR1]
76	60	44	28	PD3/TIM2_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
77	61	45	29	PD4/TIM2_CC1/BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
78	62	46	30	PD5/ LINUART_TX	I/O	**X**	X	X		O1	X	X	**Port D5**	LINUART data transmit	
79	63	47	31	PD6/ LINUART_RX	I/O	**X**	X	X		O1	X	X	**Port D6**	LINUART data receive	
													Caution: This pin must be held low during power on		
80	64	48	32	PD7/TLI	I/O	**X**	X	X		O1	X	X	**Port D7**	Top level interrupt	TIM1_CC4 [AFR4]

1. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented)

6.2.1 Alternate function remapping

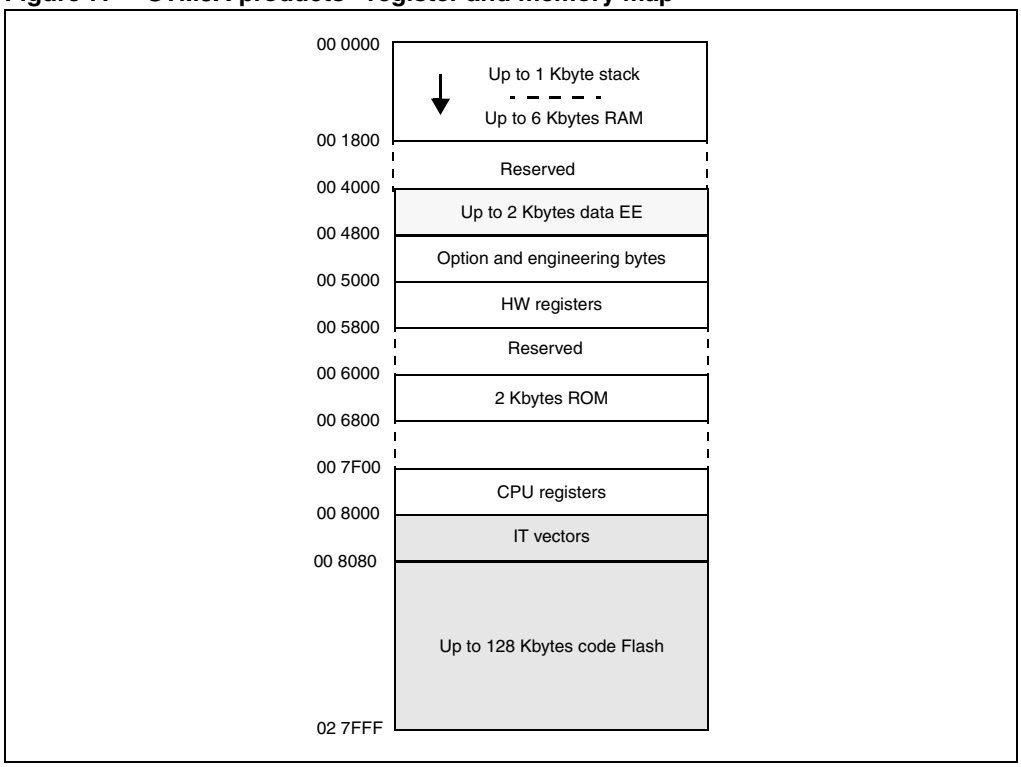
As show in the rightmost column of *Table 7*, some alternate functions can be remapped at different I/O ports by programming one of 8 AFR (alternate function remap) option bits. Refer to *Section 10: Option bytes on page 48*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see GPIO section of the STM8S/STM8A Reference manual).

7 Memory map

Figure 7. STM8A products - register and memory map



0000h - 17FFh Up to 6 Kbytes RAM

1800h - 3FFFh Reserved

4000h - 47FFh Up to 2 Kbytes data EE

4800h - 487Fh 128 user option bytes

4880h - 48FFh 128 engineering bytes

4900h - 4FFFh Reserved

5000h - 57FFh HW registers 2 Kbytes

5800h - 5FFFh Reserved

6000h - 67FFh 2 Kbytes boot ROM

6800h - 7EFFh Reserved

7F00h - 7FFFh CPU registers

8000h - 807Fh Interrupt vectors

8080h - 27FFFh Program EE

8 Interrupt table

Table 8. Interrupt table

Priority	Source block	Description	Interrupt vector address	Wake-up from halt	Comments
-	Reset	Reset	6000h	Yes	Reset vector in ROM
-	TRAP	SW interrupt	8004h		
0	TLI	External top level interrupt	8008h		
1	AWU	Auto wake up from halt	800Ch	Yes	
2	Clock controller	Main clock controller	8010h		
3	MISC	Ext interrupt E0	8014h	Yes	Port A interrupts
4	MISC	Ext interrupt E1	8018h	Yes	Port B interrupts
5	MISC	Ext interrupt E2	801Ch	Yes	Port C interrupts
6	MISC	Ext interrupt E3	8020h	Yes	Port D interrupts
7	MISC	Ext interrupt E4	8024h	Yes	Port E interrupts
8	CAN	CAN interrupt Rx	8028h	Yes	
9	CAN	CAN interrupt TX/ER/SC	802Ch		
10	SPI	End of transfer	8030h	Yes	
11	Timer 1	Update/overflow/ trigger/break	8034h		
12	Timer 1	Capture/compare	8038h		
13	Timer 2	Update/overflow/ break	803Ch		Trigger not available on medium end timer
14	Timer 2	Capture/compare	8040h		
15	Timer 3	Update/overflow/ break	8044h		Trigger not available on medium end timer
16	Timer 3	Capture/compare	8048h		
17	USART (SCI1)	Tx complete/ ER/SPI EOT/SPI Error	804Ch		
18	USART (SCI1)	Receive data full reg.	8050h		
19	I^2C	I^2C interrupts	8054h	Yes	
20	Simple USART (SCI2)	Tx complete/error/ SPI EOT/SPI error	8058h		

Table 8. Interrupt table (continued)

Priority	Source block	Description	Interrupt vector address	Wake-up from halt	Comments
21	Simple USART (SCI2)	Receive data full reg.	805Ch		
22	ADC	End of conversion	8060h		
23	Very-low-end timer (timer 4)	Update/overflow	8064h		
24	EEPROM	ECC correction	8068h		Single bit error correction interrupt is available for engineering mode only
25			806Ch		Available for future expansion
26			8070h		Available for future expansion
27			8074h		Available for future expansion
28			8078h		Available for future expansion
29			807Ch		Available for future expansion

9 Register mapping

Table 9. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
00 5000h	Port A	PA_ODR	Port A data output latch register	00h
00 5001h		PA_IDR	Port A input pin value register	00h
00 5002h		PA_DDR	Port A data direction register	00h
00 5003h		PA_CR1	Port A control register 1	00h
00 5004h		PA_CR2	Port A control register 2	00h
00 5005h	Port B	PB_ODR	Port B data output latch register	00h
00 5006h		PB_IDR	Port B input pin value register	00h
00 5007h		PB_DDR	Port B data direction register	00h
00 5008h		PB_CR1	Port B control register 1	00h
00 5009h		PB_CR2	Port B control register 2	00h
00 500Ah	Port C	PC_ODR	Port C data output latch register	00h
00 500Bh		PB_IDR	Port C input pin value register	00h
00 500Ch		PC_DDR	Port C data direction register	00h
00 500Dh		PC_CR1	Port C control register 1	00h
00 500Eh		PC_CR2	Port C control register 2	00h
00 500Fh	Port D	PD_ODR	Port D data output latch register	00h
00 5010h		PD_IDR	Port D input pin value register	00h
00 5011h		PD_DDR	Port D data direction register	00h
00 5012h		PD_CR1	Port D control register 1	00h
00 5013h		PD_CR2	Port D control register 2	00h
00 5014h	Port E	PE_ODR	Port E data output latch register	00h
00 5015h		PE_IDR	Port E input pin value register	00h
00 5016h		PE_DDR	Port E data direction register	00h
00 5017h		PE_CR1	Port E control register 1	00h
00 5018h		PE_CR2	Port E control register 2	00h
00 5019h	Port F	PF_ODR	Port F data output latch register	00h
00 501Ah		PF_IDR	Port F input pin value register	00h
00 501Bh		PF_DDR	Port F data direction register	00h
00 501Ch		PF_CR1	Port F control register 1	00h
00 501Dh		PF_CR2	Port F control register 2	00h

Table 9. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 501Eh	Port G	PG_ODR	Port G data output latch register	00h
00 501Fh		PG_IDR	Port G input pin value register	00h
00 5020h		PG_DDR	Port G data direction register	00h
00 5021h		PG_CR1	Port G control register 1	00h
00 5022h		PG_CR2	Port G control register 2	00h
00 5023h	Port H	PH_ODR	Port H data output latch register	00h
00 5024h		PH_IDR	Port H input pin value register	00h
00 5025h		PH_DDR	Port H data direction register	00h
00 5026h		PH_CR1	Port H control register 1	00h
00 5027h		PH_CR2	Port H control register 2	00h
00 5028h	Port I	PI_ODR	Port I data output latch register	00h
00 5029h		PI_IDR	Port I input pin value register	00h
00 502Ah		PI_DDR	Port I data direction register	00h
00 502Bh		PI_CR1	Port I control register 1	00h
00 502Ch		PI_CR2	Port I control register 2	00h

Table 10. General hardware register map

Address	Block	Register label	Register name	Reset status
00 5050h to 00 5059h	Reserved area (10 bytes)			
00 505Ah	Flash	FLASH_CR1	Flash control register 1	00h
00 505Bh		FLASH_CR2	Flash control register 2	00h
00 505Ch		FLASH_NCR2	Flash complementary control register 2	FFh
00 505Dh		FLASH _FPR	Flash protection register	00h
00 505Eh		FLASH _NFPR	Flash complementary protection register	FFh
00 505Fh		FLASH _IAPSR	Flash in-application programming status register	00h
00 5060h to 00 5061h	Reserved area (2 bytes)			
00 5062h	Flash	FLASH _PUKR	Flash program memory unprotection register	00h
00 5063h	Reserved area (1 byte)			
00 5064h	Flash	FLASH _DUKR	Data EEPROM unprotection register	00h
00 5065h to 00 509Fh	Reserved area (59 bytes)			
00 50A0h	ITC	EXTI_CR1	External interrupt control register 1	00h
00 50A1h		EXTI_CR2	External interrupt control register 2	00h
00 50A2h to 00 50B2h	Reserved area (17 bytes)			
00 50B3h	RST	RST_SR	Reset status register	xxh
00 50B4h to 00 50BFh	Reserved area (12 bytes)			
00 50C0h	CLK	CLK_ICKR	Internal clock control register	01h
00 50C1h		CLK_ECKR	External clock control register	00h
00 50C2h	Reserved area (1 byte)			

Table 10. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 50C3h	CLK	CLK_CMSR	Clock master status register	E1h
00 50C4h		CLK_SWR	Clock master switch register	E1h
00 50C5h		CLK_SWCR	Clock switch control register	xxxx 0000b
00 50C6h		CLK_CKDIVR	Clock divider register	18h
00 50C7h		CLK_PCKENR1	Peripheral clock gating register 1	FFh
00 50C8h		CLK_CSSR	Clock security system register	00h
00 50C9h		CLK_CCOR	Configurable clock control register	00h
00 50CAh		CLK_PCKENR2	Peripheral clock gating register 2	FFh
00 50CBh		CLK_CANCCR	CAN clock control register	00h
00 50CCh		CLK_HSITRIMR	HSI clock calibration trimming register	xxh
00 50CDh		CLK_SWIMCCR	SWIM clock control register	x0h
00 50CEh to 00 50D0h	Reserved area (3 bytes)			
00 50D1h	WWDG	WWDG_CR	WWDG control register	7Fh
00 50D2h		WWDG_WR	WWDR window register	7Fh
00 50D3h to 00 50DFh	Reserved area (13 bytes)			
00 50E0h	IWDG	IWDG_KR	IWDG key register	-
00 50E1h		IWDG_PR	IWDG prescaler register	00h
00 50E2h		IWDG_RLR	IWDG reload register	FFh
00 50E3h to 00 50EFh	Reserved area (13 bytes)			
00 50F0h	AWU	AWU_CSR1	AWU control/status register 1	00h
00 50F1h		AWU_APR	AWU asynchronous prescaler buffer register	3Fh
00 50F2h		AWU_TBR	AWU timebase selection register	00h
00 50F3h	BEEP	BEEP_CSR	BEEP control/status register	1Fh
00 50F4h to 00 50FFh	Reserved area (12 bytes)			

Table 10. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5200h	SPI	SPI_CR1	SPI control register 1	00h
00 5201h		SPI_CR2	SPI control register 2	00h
00 5202h		SPI_ICR	SPI interrupt control register	00h
00 5203h		SPI_SR	SPI status register	02h
00 5204h		SPI_DR	SPI data register	00h
00 5205h		SPI_CRCPR	SPI CRC polynomial register	07h
00 5206h		SPI_RXCRCR	SPI Rx CRC register	FFh
00 5207h		SPI_TXCRCR	SPI Tx CRC register	FFh
00 5208h to 00 520Fh	Reserved area (8 bytes)			
00 5210h	I2C	I2C_CR1	I^2C control register 1	00h
00 5211h		I2C_CR2	I^2C control register 2	00h
00 5212h		I2C_FREQR	I^2C frequency register	00h
00 5213h		I2C_OARL	I^2C own address register low	00h
00 5214h		I2C_OARH	I^2C own address register high	00h
00 5215h		Reserved		
00 5216h		I2C_DR	I^2C data register	00h
00 5217h		I2C_SR1	I^2C status register 1	00h
00 5218h		I2C_SR2	I^2C status register 2	00h
00 5219h		I2C_SR3	I^2C status register 3	00h
00 521Ah		I2C_ITR	I^2C interrupt control register	00h
00 521Bh		I2C_CCRL	I^2C clock control register low	00h
00 521Ch		I2C_CCRH	I^2C clock control register high	00h
00 521Dh		I2C_TRISER	I^2C TRISE register	02h
00 521Eh		I2C_PECR	I^2C packet error checking register	00h
00 521Fh to 00 522Fh	Reserved area (17 bytes)			

Table 10. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5230h	USART	USART_SR	USART status register	C0h
00 5231h		USART_DR	USART data register	xxh
00 5232h		USART_BRR1	USART baud rate register 1	00h
00 5233h		USART_BRR2	USART baud rate register 2	00h
00 5234h		USART_CR1	USART control register 1	00h
00 5235h		USART_CR2	USART control register 2	00h
00 5236h		USART_CR3	USART control register 3	00h
00 5237h		USART_CR4	USART control register 4	00h
00 5238h		USART_CR5	USART control register 5	00h
00 5239h		USART_GTR	USART guard time register	00h
00 523Ah		USART_PSCR	USART prescaler register	00h
00 523Bh to 00 523Fh	Reserved area (5 bytes)			
00 5240h	LINUART	LINUART_SR	LINUART status register	C0h
00 5241h		LINUART_DR	LINUART data register	xxh
00 5242h		LINUART_BRR1	LINUART baud rate register 1	00h
00 5243h		LINUART_BRR2	LINUART baud rate register 2	00h
00 5244h		LINUART_CR1	LINUART control register 1	00h
00 5245h		LINUART_CR2	LINUART control register 2	00h
00 5246h		LINUART_CR3	LINUART control register 3	00h
005247h		LINUART_CR4	LINUART control register 4	00h
00 5248h		Reserved		
00 5249h		LINUART_CR6	LINUART control register 6	00h
00 524Ah to 00 524Fh	Reserved area (6 bytes)			

Table 10. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5250h	TIM1	TIM1_CR1	TIM1 control register 1	00h
00 5251h		TIM1_CR2	TIM1 control register 2	00h
00 5252h		TIM1_SMCR	TIM1 slave mode control register	00h
00 5253h		TIM1_ETR	TIM1 external trigger register	00h
00 5254h		TIM1_IER	TIM1 Interrupt enable register	00h
00 5255h		TIM1_SR1	TIM1 status register 1	00h
00 5256h		TIM1_SR2	TIM1 status register 2	00h
00 5257h		TIM1_EGR	TIM1 event generation register	00h
00 5258h		TIM1_CCMR1	TIM1 capture/compare mode register 1	00h
00 5259h		TIM1_CCMR2	TIM1 capture/compare mode register 2	00h
00 525Ah		TIM1_CCMR3	TIM1 capture/compare mode register 3	00h
00 525Bh		TIM1_CCMR4	TIM1 capture/compare mode register 4	00h
00 525Ch		TIM1_CCER1	TIM1 capture/compare enable register 1	00h
00 525Dh		TIM1_CCER2	TIM1 capture/compare enable register 2	00h
00 525Eh		TIM1_CNTRH	TIM1 counter high	00h
00 525Fh		TIM1_CNTRL	TIM1 counter low	00h
00 5260h		TIM1_PSCRH	TIM1 prescaler register high	00h
00 5261h		TIM1_PSCRL	TIM1 prescaler register low	00h
00 5262h		TIM1_ARRH	TIM1 auto-reload register high	FFh
00 5263h		TIM1_ARRL	TIM1 auto-reload register low	FFh
00 5264h		TIM1_RCR	TIM1 repetition counter register	00h
00 5265h		TIM1_CCR1H	TIM1 capture/compare register 1 high	00h
00 5266h		TIM1_CCR1L	TIM1 capture/compare register 1 low	00h
00 5267h		TIM1_CCR2H	TIM1 capture/compare register 2 high	00h
00 5268h		TIM1_CCR2L	TIM1 capture/compare register 2 low	00h
00 5269h		TIM1_CCR3H	TIM1 capture/compare register 3 high	00h
00 526Ah		TIM1_CCR3L	TIM1 capture/compare register 3 low	00h
00 526Bh		TIM1_CCR4H	TIM1 capture/compare register 4 high	00h
00 526Ch		TIM1_CCR4L	TIM1 capture/compare register 4 low	00h
00 526Dh		TIM1_BKR	TIM1 break register	00h
00 526Eh	TIM1	TIM1_DTR	TIM1 dead-time register	00h
00 526Fh		TIM1_OISR	TIM1 output idle state register	00h
00 5270h to 00 52FFh	Reserved area (147 bytes)			

Table 10. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5300h	TIM2	TIM2_CR1	TIM2 control register 1	00h
00 5301h		TIM2_IER	TIM2 Interrupt enable register	00h
00 5302h		TIM2_SR1	TIM2 status register 1	00h
00 5303h		TIM2_SR2	TIM2 status register 2	00h
00 5304h		TIM2_EGR	TIM2 event generation register	00h
00 5305h		TIM2_CCMR1	TIM2 capture/compare mode register 1	00h
00 5306h		TIM2_CCMR2	TIM2 capture/compare mode register 2	00h
00 5307h		TIM2_CCMR3	TIM2 capture/compare mode register 3	00h
00 5308h		TIM2_CCER1	TIM2 capture/compare enable register 1	00h
00 5309h		TIM2_CCER2	TIM2 capture/compare enable register 2	00h
00 530Ah		TIM2_CNTRH	TIM2 counter high	00h
00 530Bh		TIM2_CNTRL	TIM2 counter low	00h
00 530Ch		TIM2_PSCR	TIM2 prescaler register	00h
00 530Dh		TIM2_ARRH	TIM2 auto-reload register high	FFh
00 530Eh		TIM2_ARRL	TIM2 auto-reload register low	FFh
00 530Fh		TIM2_CCR1H	TIM2 capture/compare register 1 high	00h
00 5310h		TIM2_CCR1L	TIM2 capture/compare register 1 low	00h
00 5311h		TIM2_CCR2H	TIM2 capture/compare register 2 high	00h
00 5312h		TIM2_CCR2L	TIM2 capture/compare register 2 low	00h
00 5313h		TIM2_CCR3H	TIM2 capture/compare register 3 high	00h
00 5314h		TIM2_CCR3L	TIM2 capture/compare register 3 low	00h
00 5315h to 00 531Fh	Reserved area (11 bytes)			

Table 10. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5320h	TIM3	TIM3_CR1	TIM3 control register 1	00h
00 5321h		TIM3_IER	TIM3 interrupt enable register	00h
00 5322h		TIM3_SR1	TIM3 status register 1	00h
00 5323h		TIM3_SR2	TIM3 status register 2	00h
00 5324h		TIM3_EGR	TIM3 event generation register	00h
00 5325h		TIM3_CCMR1	TIM3 capture/compare mode register 1	00h
00 5326h		TIM3_CCMR2	TIM3 capture/compare mode register 2	00h
00 5327h		TIM3_CCER1	TIM3 capture/compare enable register 1	00h
00 5328h		TIM3_CNTRH	TIM3 counter high	00h
00 5329h		TIM3_CNTRL	TIM3 counter low	00h
00 532Ah		TIM3_PSCR	TIM3 prescaler register	00h
00 532Bh		TIM3_ARRH	TIM3 auto-reload register high	FFh
00 532Ch		TIM3_ARRL	TIM3 auto-reload register low	FFh
00 532Dh		TIM3_CCR1H	TIM3 capture/compare register 1 high	00h
00 532Eh		TIM3_CCR1L	TIM3 capture/compare register 1 low	00h
00 532Fh		TIM3_CCR2H	TIM3 capture/compare register 2 high	00h
00 5330h		TIM3_CCR2L	TIM3 capture/compare register 2 low	00h
00 5331h to 00 533Fh	Reserved area (15 bytes)			
00 5340h	TIM4	TIM4_CR1	TIM4 control register 1	00h
00 5341h		TIM4_IER	TIM4 interrupt enable register	00h
00 5342h		TIM4_SR	TIM4 status register	00h
00 5343h		TIM4_EGR	TIM4 event generation register	00h
00 5344h		TIM4_CNTR	TIM4 counter	00h
00 5345h		TIM4_PSCR	TIM4 prescaler register	00h
00 5346h		TIM4_ARR	TIM4 auto-reload register	FFh
00 5347h to 00 53FFh	Reserved area (184 bytes)			

Table 10. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5400h	ADC	ADC _CSR	ADC control/status register	00h
00 5401h		ADC_CR1	ADC configuration register 1	00h
00 5402h		ADC_CR2	ADC configuration register 2	00h
00 5403h		ADC_CR3	ADC configuration register 3	00h
00 5404h		ADC_DRH	ADC data register high	00h
00 5405h		ADC_DRL	ADC data register low	00h
00 5406h		ADC_TDRH	ADC Schmitt trigger disable register high	00h
00 5407h		ADC_TDRL	ADC Schmitt trigger disable register low	00h
00 5408h to 00 541Fh	Reserved area (24 bytes)			
00 5420h	CAN	CAN_MCR	CAN master control register	02h
00 5421h		CAN_MSR	CAN master status register	02h
00 5422h		CAN_TSR	CAN transmit status register	00h
00 5423h		CAN_TPR	CAN transmit priority register	0Ch
00 5424h		CAN_RFR	CAN receive FIFO register	00h
00 5425h		CAN_IER	CAN interrupt enable register	00h
00 5426h		CAN_DGR	CAN diagnosis register	0Ch
00 5427h		CAN_FPSR	CAN page selection register	00h
00 5428h		CAN_P0	CAN paged register 0	
00 5429h		CAN_P1	CAN paged register 1	
00 542Ah		CAN_P2	CAN paged register 2	
00 542Bh		CAN_P3	CAN paged register 3	

Table 10. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 542Ch	CAN	CAN_P4	CAN paged register 4	
00 542Dh		CAN_P5	CAN paged register 5	
00 542Eh		CAN_P6	CAN paged register 6	
00 542Fh		CAN_P7	CAN paged register 7	
00 5430h		CAN_P8	CAN paged register 8	
00 5431h		CAN_P9	CAN paged register 9	
00 5432h		CAN_PA	CAN paged register A	
00 5433h		CAN_PB	CAN paged register B	
00 5434h		CAN_PC	CAN paged register C	
00 5435h		CAN_PD	CAN paged register D	
00 5436h		CAN_PE	CAN paged register E	
00 5437h		CAN_PF	CAN paged register F	
00 5438h to 00 57FFh	Reserved area (968 bytes)			

Table 11. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
00 7F00h	CPU	A	Accumulator	00h
00 7F01h		PCE	Program counter extended	00h
00 7F02h		PCH	Program counter high	80h
00 7F03h		PCL	Program counter low	00h
00 7F04h		XH	X index register high	00h
00 7F05h		XL	X index register low	00h
00 7F06h		YH	Y index register high	00h
00 7F07h		YL	Y index register low	00h
00 7F08h		SPH	Stack pointer high	17h
00 7F09h		SPL	Stack pointer low	FFh
00 7F0Ah		CCR	Condition code register	28h
00 7F0Bh to 00 7F5Fh	Reserved area (85 bytes)			
00 7F60h	CFG	CFG_GCR	Global configuration register	00h
00 7F70h	ITC	ITC_SPR1	Interrupt software priority register 1	FFh
00 7F71h		ITC_SPR2	Interrupt software priority register 2	FFh
00 7F72h		ITC_SPR3	Interrupt software priority register 3	FFh
00 7F73h		ITC_SPR4	Interrupt software priority register 4	FFh
00 7F74h		ITC_SPR5	Interrupt software priority register 5	FFh
00 7F75h		ITC_SPR6	Interrupt software priority register 6	FFh
00 7F76h		ITC_SPR7	Interrupt software priority register 7	FFh
00 7F77h to 00 7F79h	Reserved area (3 bytes)			
00 7F80h	SWIM	SWIM_CSR	SWIM control status register	00h
00 7F81h to 00 7F8Fh	Reserved area (15 bytes)			

Table 11. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
00 7F90h	DM	DM_BK1RE	Breakpoint 1 register extended byte	FFh
00 7F91h		DM_BK1RH	Breakpoint 1 register high byte	FFh
00 7F92h		DM_BK1RL	Breakpoint 1 register low byte	FFh
00 7F93h		DM_BK2RE	Breakpoint 2 register extended byte	FFh
00 7F94h		DM_BK2RH	Breakpoint 2 register high byte	FFh
00 7F95h		DM_BK2RL	Breakpoint 2 register low byte	FFh
00 7F96h		DM_CR1	Debug module control register 1	00h
00 7F97h		DM_CR2	Debug module control register 2	00h
00 7F98h		DM_CSR1	Debug module control/status register 1	10h
00 7F99h		DM_CSR2	Debug module control/status register 2	00h
00 7F9Ah		DM_ENFCTR	Enable function register	FFh
00 7F9Bh to 00 7F9Fh	Reserved area (5 bytes)			

10 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 12: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be toggled in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (UM0316) and STM8 SWIM and debug manual (UM0320) for information on SWIM programming procedures.

Table 12. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
4800h	Read-out protection (ROP)	OPT0	ROP[7:0]								00h
4801h	User boot code(UBC)	OPT1	UBC[7:0]								00h
4802h		NOPT1	NUBC[7:0]								FFh
4803h	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	00h
4804h		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	FFh
4805h	Watchdog option	OPT3	Reserved				LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	00h
4806h		NOPT3	Reserved				NLSI_EN	NIWDG_HW	NWWDG_HW	NWWG_HALT	FFh
4807h	Clock option	OPT4	Reserved				EXTCLK	CKAWUSEL	PRSC1	PRSC0	00h
4808h		NOPT4	Reserved				NEXTCLK	NCKAWUSEL	NPRSC1	NPRSC0	FFh
4809h	HSE clock startup	OPT5	HSECNT[7:0]								00h
480Ah		NOPT5	NHSECNT[7:0]								FFh
480Bh	Reserved	OPT6	Reserved								00h
480Ch		NOPT6	Reserved								FFh
480Dh	Flash wait states	OPT7	Reserved							Wait state	00h
480Eh		NOPT7	Reserved							Nwait state	FFh

Table 13. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** *Memory readout protection (ROP)* AAh: Enable readout protection (write access via SWIM protocol) *Note: Refer to the STM8S/STM8A Reference manual RM0009 section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** *User boot code area* 00h: no UBC, no write-protection 01h: Page 0 and 1 defined as UBC, memory write-protected 02h to FFh: Pages 2 to 255 defined as UBC, memory write-protected *Note: Refer to the STM8S/STM8A Reference manual RM0009 section on Flash/EEPROM write protection and the Flash_fpr register for more details.*
OPT2	**AFR7***Alternate function remapping option 7* 0: Port D4 alternate function = TIM2_CC1 1: Port D4 alternate function = BEEP **AFR6** *Alternate function remapping option 6* 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL **AFR5** *Alternate function remapping option 5* 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_NCC3, port B1 alternate function = TIM1_NCC2, port B0 alternate function = TIM1_NCC1 **AFR4** *Alternate function remapping option 4* 0: Port D7 alternate function = TLI 1: Port D7 alternate function = TIM1_CC4 **AFR3** *Alternate function remapping option 3* 0: Port D0 alternate function = TIM3_CC2 1: Port D0 alternate function = TIM1_BKIN **AFR2** *Alternate function remapping option 2* 0: Port D0 alternate function = TIM3_CC2 1: Port D0 alternate function = CLK_CCO Note: AFR2 option has priority over AFR3 if both are activated **AFR1** *Alternate function remapping option 1* 0: Port A3 alternate function = TIM2_CC3, port D2 alternate function TIM3_CC1 1: Port A3 alternate function = TIM3_CC1, port D2 alternate function TIM2_CC3 **AFR0** *Alternate function remapping option 0* 0: Port D3 alternate function = TIM2_CC2 1: Port D3 alternate function = ADC_ETR

Table 13. Option byte description (continued)

Option byte no.	Description
OPT3	**LSI_EN:** *Low speed internal clock enable* 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: *Independent watchdog* 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: *Window watchdog activation* 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: *Window watchdog reset on halt* 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK:** *External clock selection* 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: *Auto wake-up unit/Independent watchdog clock* 0: LSI clock source selected for AWU and IWDG 1: HSE clock with prescaler selected as clock source for for AWU and IWDG
	PRSC[1:0] AWU/IWDG clock prescaler 00: 24 MHz to 128 kHz prescaler 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** *HSE crystal oscillator stabilization time* This configures the stabilisation time to 0, 16, 256, 4096 HSE cycles.
OPT6	Reserved
OPT7	**WAITSTATE** *Wait state configuration* This option configures the number of wait states inserted when reading from the Flash/data EEPROM memory. 0: No wait states 1: 1 wait states

11 Electrical characteristics

11.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

11.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

11.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

11.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

11.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

11.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

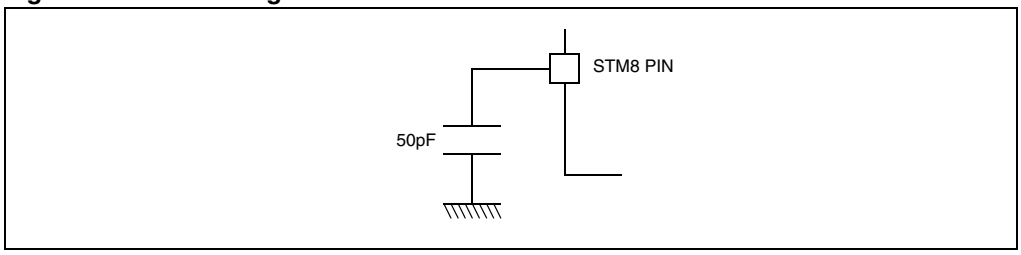
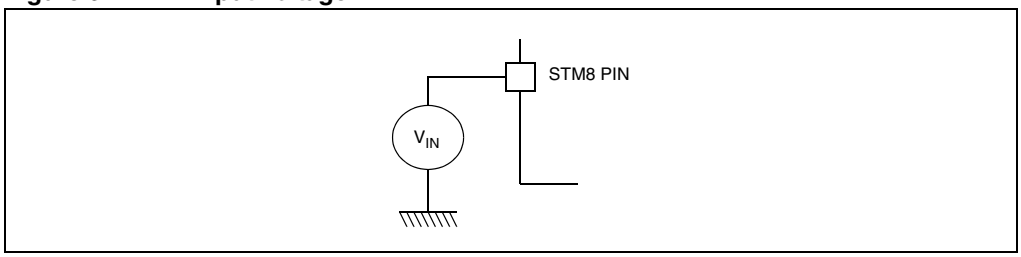


Figure 9. Pin input voltage



11.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{SS} \rvert$	Variations between different power pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins		50	
V_{ESD}	Electro-static discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 61*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	60	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	60	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	- 20	
$I_{INJ(PIN)}$(2)(3)	Injected current on NRST pin	± 4	
	Injected current on OSC_IN pin	± 4	
	Injected current on any other pin(4)	± 4	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(4)	± 20	

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
3. Negative injection disturbs the analog performance of the device. See note in *Section 11.3.8: 10-bit ADC characteristics on page 71*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	

11.3 Operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency		0	24	MHz
V_{DD}/V_{DD_IO}	Standard operating voltage		3.0	5.5	V
T_A	Ambient temperature	Suffix A	-40	85	°C
		Suffix B	-40	105	°C
		Suffix C	-40	125	°C
		Suffix D	-40	145	°C
T_J	Junction temperature range	A suffix version	-40	90	°C
		B suffix version	-40	110	°C
		C suffix version	-40	130	°C
		D suffix version	-40	150	°C

Table 18. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate		20		∞	µs/V
	V_{DD} fall time rate(1)		20		∞	
t_{TEMP}	Reset release delay	V_{DD} rising	TBD	3		ms
	Reset generation delay(1)	V_{DD} falling	TBD	3		µs
V_{IT+}	Power-on reset threshold		TBD	2.8	TBD	V
V_{IT-}	Brown-out reset threshold		TBD	2.7	TBD	V
$V_{HYS(BOR)}$	Brown-out reset hysteresis		TBD	70	TBD	V

1. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.

11.3.1 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are enabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 19. Total current consumption in run and wait modes at V_{DD} = 5.0 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode	CPU and all peripherals running	External/internal HS clock	1 mA + 0.6 mA/MHz	TBD	mA
$I_{DD(WFI)}$	Supply current in wait mode	CPU not clocked, all peripherals running	Peripheral clock 16 MHz	1.6 mA	TBD	mA

Table 20. Total current consumption and timing in halt, fast active halt and slow active halt modes at V_{DD} = 5.0 V

Symbol	Parameter	Conditions		Typ(1)	Max(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash/EEPROM in standby mode, RAM contents guaranteed, oscillators stopped		10	25	µA
$I_{DD(FAH)}$	Supply current in fast active halt mode	Flash/EEPROM in standby mode, RAM contents guaranteed, auto wake-up unit (AWU) and 128 kHz LSI oscillator active	HSE osc 16 MHz	660	700	
			LSI RC 128 kHz	160	200	
$I_{DD(SAH)}$	Supply current in slow active halt mode		LSI RC 128 kHz/100 kHz ext. clock	13	30	
$t_{WU(FAH)}$	Wake-up time from fast active halt mode to run mode			15	TBD	µs
$t_{WU(SAH)}$	Wake-up time from slow active halt mode to run mode			55	100	µs

1. T_A = 55°C, V_{DD} = 5 V, worst case process corner . Data based on characterization results, not tested in production

Table 21. Total current consumption in run and wait modes at V_{DD} = 3.0 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode	CPU and all peripherals running	External/internal HS clock	1 mA + 0.4 mA/MHz	TBD	mA
$I_{DD(WFI)}$	Supply current in wait mode	CPU not clocked, all peripherals running	Peripheral clock 16 MHz	1.5 mA	TBD	mA

Table 22. Total current consumption and timing in halt, fast active halt and slow active halt modes at V_{DD} = 3.0 V(1)

Symbol	Parameter	Conditions		Typ	Max (2)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash/EEPROM in standby mode, RAM contents guaranteed, oscillators stopped		6	25	µA
$I_{DD(FAH)}$	Supply current in fast active halt mode	Flash/EEPROM in standby mode, RAM contents guaranteed, auto wake-up unit (AWU) and 128 kHz LSI oscillator active	HSE osc 16 MHz	750	TBD	
			LSI RC 128 kHz	250	TBD	
$I_{DD(SAH)}$	Supply current in slow active halt mode		LSI RC 128 kHz/100 kHz ext. clock	7	30	
$t_{WU(FAH)}$	Wake-up time from fast active halt mode to run mode			15	TBD	µs
$t_{WU(SAH)}$	Wake-up time from slow active halt mode to run mode			55	100	µs

1. Data based on characterization results, not tested in production
2. Worst-case process corner, T_A = 55 °C

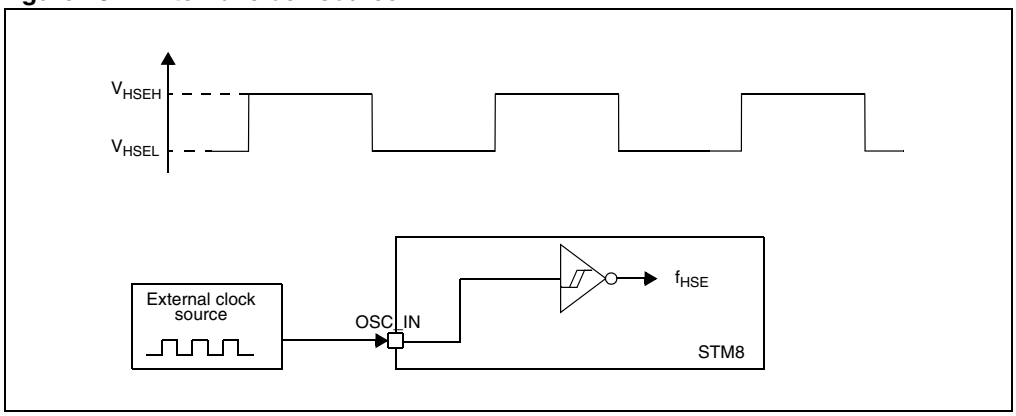
11.3.2 Clock and timing characteristics

External clock sources

Table 23. External clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency		0		24	MHz
V_{HSEH}	OSCIN input pin high level voltage		0.7 x V_{DD}		V_{DD}	V
V_{HSEL}	OSCIN input pin low level voltage		V_{SS}		0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1		+1	µA

Figure 10. External clock source



HSE crystal/ceramic resonator oscillator

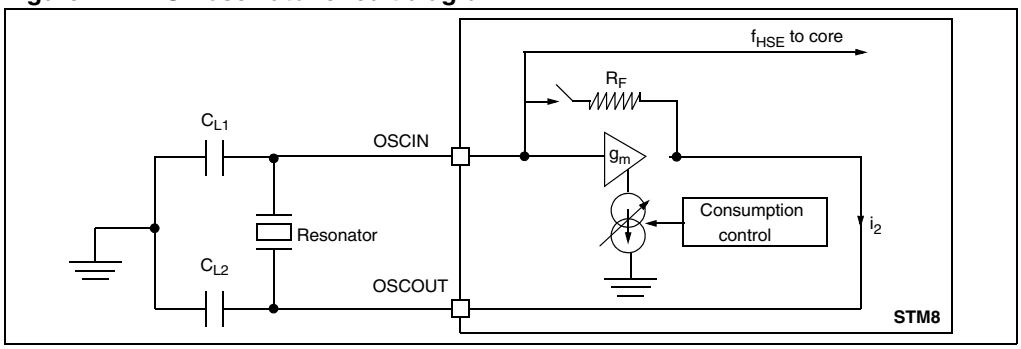
The HSE clock oscillator can be supplied with a 1-24 MHz crystal/ceramic resonator oscillator.All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 24. HSE oscillator characteristics

Symbol	Parameter	Conditions	Typ	Unit
R_F	Feedback resistor		220	kΩ
C_L (1)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(2)	R_M = 30 Ω (typ)	30	pF
i_2	HSE driving current	V_{DD} = 5.0 V V_{IN} = V_{SS}	3 (startup) 1 (stabilized)	mA
g_m	Oscillator transconductance		3.5	mA/V
$t_{SU(HSE)}$ (3)	Startup time	V_{SS} is stabilized	1	ms
$I_{DD(HSE)}$	HSE oscillator power consumption		500	µA

1. C_{L1} and C_{L2} are approximately equivalent to 2 C_L
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
3. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturerg_{mcrit}

Figure 11. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$

R_m: Notional resistance (see crystal specification)

Co: Shunt capacitance (see crystal specification)

C: Grounded external capacitance

$g_m >> g_{mcrit}$

Internal clock sources

High speed internal RC oscillator (HSI)

Table 25. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency		14	16	18	MHz
ACC_{HSI}	Accuracy of HSI oscillator when calibrated	V_{DD} = 5.0 V, T_A = 25°C	-1.0	1.0	1.0	%
		V_{DD} = 5.0 V, 0 °C ≤T_A ≤85 °C	-3.0(1)	1.0	+3.0(1)	%
		V_{DD} = 3.0 V ≤V_{DD} ≤ 5.5 V, 40 °C ≤T_A ≤125 °C	-5.0(1)	1.0	+5.0(1)	%
$t_{su(HSI)}$	HSI oscillator wake-up time including calibration			2(1)	TBD	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			170	250(1)	µA

1. Data based on characterization results, not tested in production

Low speed internal RC oscillator (LSI)

V_{DD} = 5.0 V and T_A = -40 to 145 °C unless otherwise specified.

Table 26. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency		110	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wake-up time			7	TBD(1)	µs
$I_{DD(LSI)}$	LSI oscillator power consumption			5	TBD(1)	µA

1. Data based on characterization results, not tested in production.

11.3.3 Memory characteristics

RAM and hardware registers

Table 27. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	2.7			V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.

Flash program memory/data EEPROM memory

General conditions

T_A = -40 to 125 °C when programming/erasing Flashprogram memory.

T_A = -40 to 145 °C when programming/erasing data EEPROM.

Table 28. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}(2)	Operating voltage (in execution mode)	$f_{CPU} \leq 24$ MHz	3.0		5.5	V
	Operating voltage (in write/erase mode)		3.0		5.5	
	Operating voltage (in global erase mode for ROP reset)		3.0		5.5	
t_{prog}	Standard programming time (including erase) for word/block (4 bytes/128 bytes)			6	6.6	ms
	Fast programming time for word/block (4 bytes / 128 bytes)			3	3.3	ms
t_{erase}	Erase time for 128 bytes (block)			3	3.3	ms
t_{RET}	Intrinsic data retention	T_A = +25 °C	40			years
		T_A = +55 °C	20			
		T_A = +85 °C	10			

Table 28. Flash program memory/data EEPROM memory (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
N_{RW}	Erase/write cycles (program memory)	T_A = -40 to +125 °C			1 k	cycles
	Erase/write cycles (data memory)	T_A = +25 °C			300 k	
		T_A = +125 °C			100 k	
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 bytes (block)	V_{DD} = 3.3 V		TBD	TBD	mA
		V_{DD} = 5.0 V		TBD	TBD	
I_{DD}	Supply current (standby mode)	V_{DD} = 5.0 V		2	TBD	µA
t_{WU}(3)	Wake-up time from off mode to run mode	V_{DD} = 5.0 V		25		µs
	Wake-up time from standby mode to run mode	V_{DD} = 5.0 V		2		µs

1. Guaranteed by characterization, not tested in production.
2. For applications using EEPROM, the read/write conditions must be taken into account.
3. Guaranteed by design

11.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-static discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

Table 29. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 5 V, T_A = +25 °C, f_{MASTER} = 16 MHz conforms to IEC 1000-4-2	1.5 kV class A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 5 V, T_A=+25 °C, f_{MASTER} = 16 MHz conforms to IEC 1000-4-4	2 kV class A

Electro magnetic interference (EMI)

Emission tests conform to the SAE J 1752/3 standard for test software, board layout and pin loading.

Table 30. EMI data

Symbol	Parameter	Conditions	Monitored frequency band	Max f_{CPU}(1)	Unit
				16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = +25 °C, LQFP80, 64, 48, 32 packages conforming to SAE J 1752/3	0.15 MHz to 1GHz	24	dBµV
			SAE EMI level	2.5	-

1. Data based on characterization results, not tested in production

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-static discharge (ESD)

Electro-static discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard.

Table 31. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human body model)	T_A = +25°C, conforming to JESD22-A114	II	2000	V
$V_{ESD(HBM)}$	Electro-static discharge voltage (Machine model)	T_A = +25°C, conforming to JESD22-A115	B	TBD	V
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge device model)	T_A=+25°C, conforming to JESD22-C101	III	500	V

1. Data based on characterization results, not tested in production

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-static discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 32. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = +25 °C	A
		T_A = +85 °C	A
		T_A = +125 °C	A
DLU	Dynamic latch-up class	V_{DD} = 5 V, f_{CPU} = 16 MHz, T_A= +25 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

11.3.5 I/O port pin characteristics

General characteristics

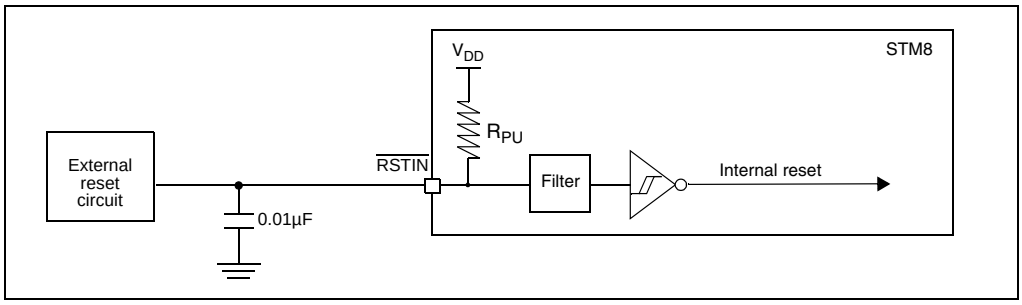
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 33. I/O electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max
V_{IL}	Input low level voltage	V_{DD} = 3 V to 5.5 V	-0.3 V		0.3 x V_{DD}
V_{IH}	Input high level voltage		0.7 x V_{DD}		V_{DD} + 0.3 V
V_{hys}	Hysteresis(1)		0.1 x V_{DD}		
V_{OH}	I = 3 mA	V_{DD} = 5 V	V_{DD} - 0.5 V		
	I = 1.5mA	V_{DD} = 3 V	V_{DD} - 0.4 V(2)		
V_{OL}	I = 3 mA	V_{DD} = 5 V			0.5 V
	I = 8 mA	V_{DD} = 5 V			0.6 V(3)
	I = 1.5 mA	V_{DD} = 3 V			0.4 V(2)
R_{pu}(4)	Pull-up resistor	V_{DD} = 3 V to 5.5 V	TBD	45 kΩ	TBD
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os V_{DD} = 3 V to 5.5 V Load = 50 pF			20 ns
		Standard and high sink I/Os V_{DD} = 3 V to 5.5 V Load = 50 pF			125 ns
I_{lkg}	Input leakage current, analog and digital	V_{DD} = 3 V to 5.5 V T_A = 125 °C			±1 µA
$I_{lkg\ ana}$	Analog input leakage current	V_{DD} = 3 V to 5.5 V T_A = 85 °C			±250 nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O(5)	Injection current ±4 mA V_{DD} = 3 V to 5.5 V(6)			±1 µA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
2. Target specification
3. High sink I/O
4. If selected
5. Leakage could be higher than max. if negative current is injected on adjacent pins.
6. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 11.2 on page 52* for more details.

Figure 12. Recommended NRST pin protection(1)(2)



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 33*. Otherwise the reset is not taken into account internally.

Figure 13. Typical V_{OL} vs. I_{IO} at V_{DD} = 3 V (standard)

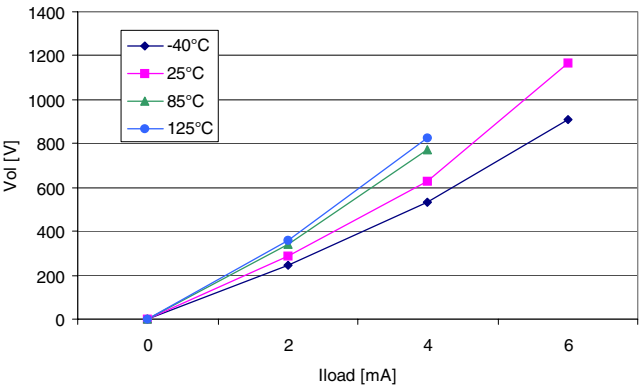


Figure 14. Typical V_{OL} vs. I_{IO} at V_{DD} = 5 V (standard)

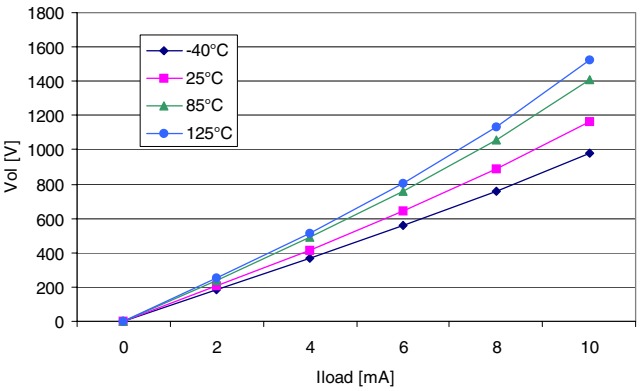


Figure 15. Typical V_{OL} vs. I_{IO} at V_{DD} = 3 V (high sink)

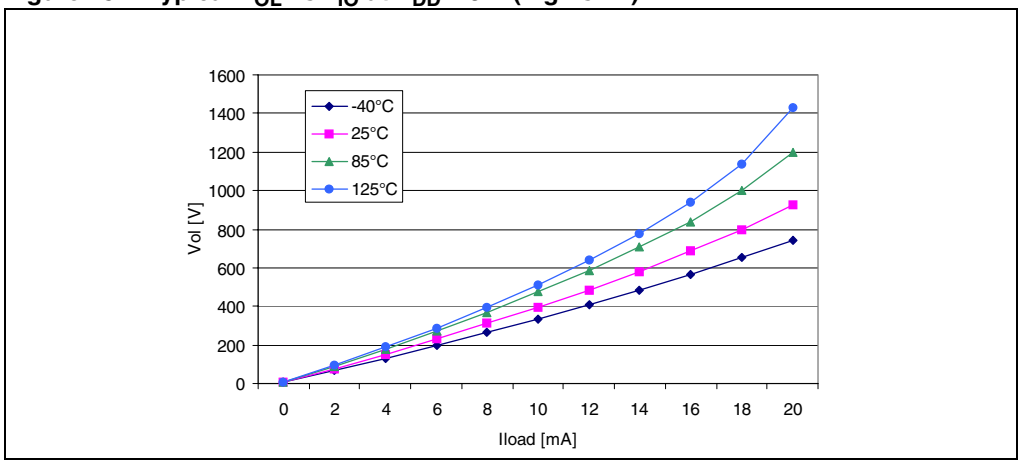
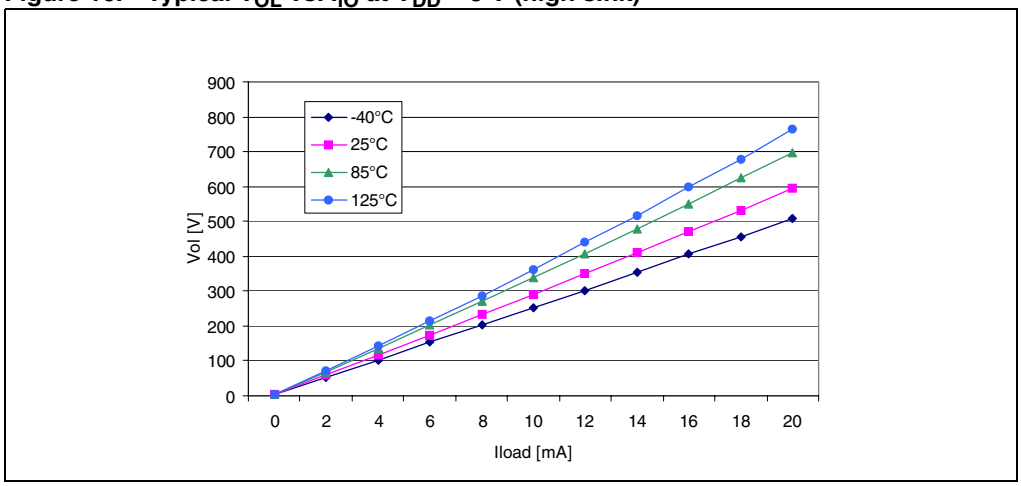


Figure 16. Typical V_{OL} vs. I_{IO} at V_{DD} = 5 V (high sink)



11.3.6 TIM timer characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 34. TIM 1, 2, 3 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time(1)		2			T_{MASTER}
$t_{res(TIM)}$	Timer resolution time(1)		1			T_{MASTER}
f_{EXT}	Timer external clock frequency(1)				24	MHz
Res_{TIM}	Timer resolution(1)			16		bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected(1)			1		T_{MASTER}
T_{MAX_COUNT}	Maximum possible count(1)				65,536	T_{MASTER}

1. Not tested in production

11.3.7 Communications interfaces

SPI serial peripheral interface (master mode)

General operating conditions: $C_L \approx$ 45 pF

Table 35. SSP master mode characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK}	SPI clock frequency(2)			20 MHz	MHz
$t_{r(SCK)}$	SPI clock rise time			20 ns	ns
$t_{f(SCK)}$	SPI clock fall time			20 ns	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time			TBD	
t_{NSSLQV}	NSS low to data output MOSI valid time			0.5 t_{SCK}+15 ns	
$t_{SCKNSSH}$	SCK last edge to NSS high	CPHA = 0		0.5 t_{SCK}+15 ns	
		CPHA = 1		t_{SCK}+15 ns	
t_{SCKQV}	SCK trigger edge to data output MOSI valid time			15	
t_{SCKQX}	SCK trigger edge to data output MOSI invalid time		0		
t_{su}	Data input (MISO) setup time w.r.t SCK sampling edge		25		
t_h	Data input (MISO) hold time w.r.t SCK sampling edge		0		

1. Data based on characterisation results, not tested in production
2. Max frequency is $f_{MASTER}/2$; f_{MASTER} max = 24 MHz. This takes into account the frequency limitation due to I/O speed capability.

Figure 17. SPI configuration - master mode, single transfer

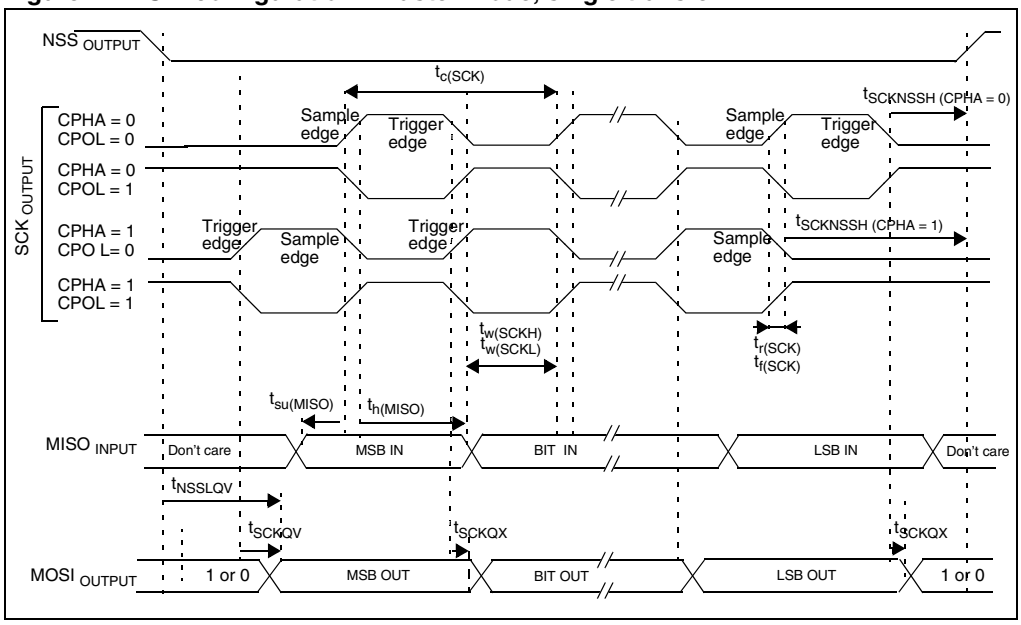


Figure 18. SPI configuration - master mode, continous transfer, CPHA = 0

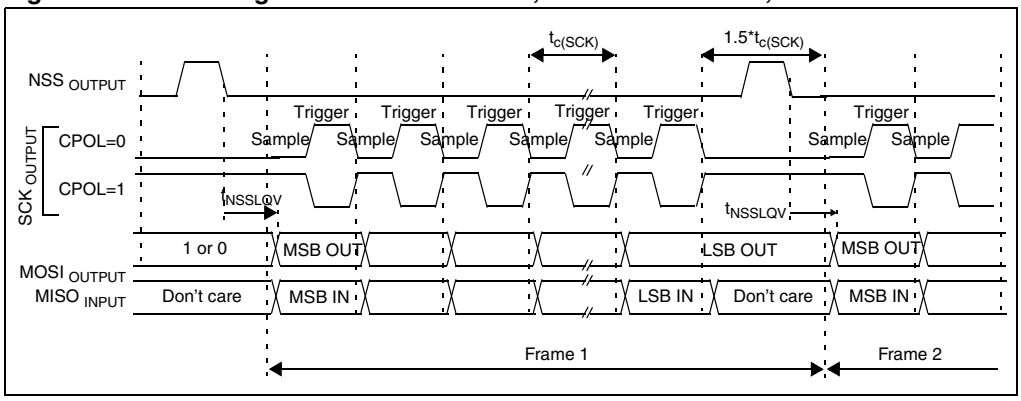
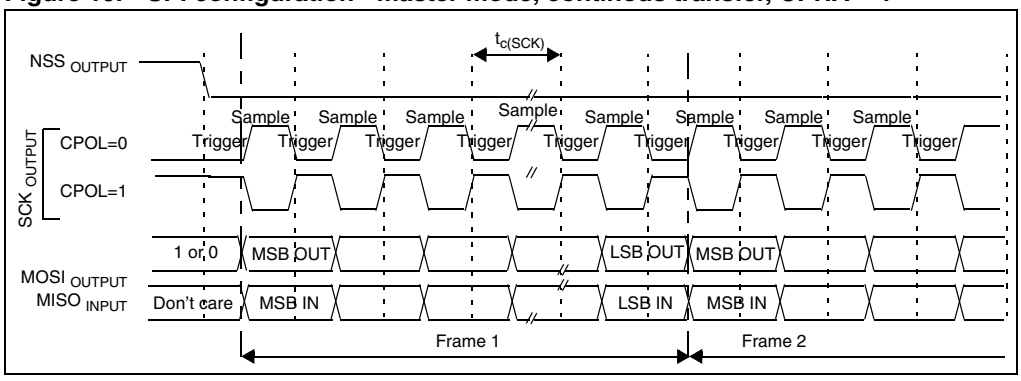


Figure 19. SPI configuration - master mode, continous transfer, CPHA = 1



SPI serial peripheral interface (slave mode)

Subject to general operating conditions with $C_L \approx$ 45 pF

Table 36. SPI slave mode characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK}	SPI clock frequency			20	MHz
$t_{su(NSS)}$	NSS input setup time w.r.t SCK first edge		0		ns
$t_{h(NSS)}$	NSS input hold time w.r.t SCK last edge		t_{MASTER} + 15 ns		
t_{NSSLQV}	NSS low to data output MISO valid time		2 t_{MASTER}	3 t_{MASTER} + 30 ns	
t_{NSSLQZ}	NSS low to data output MISO invalid time		2 t_{MASTER}	3 t_{MASTER} + 15 ns	
t_{SCKQV}	SCK trigger edge to data output MISO valid time				
t_{SCKQX}	SCK trigger edge to data output MISO invalid time		2 t_{MASTER}		
$t_{su(MOSI)}$	MOSI setup time w.r.t SCK sampling edge		0		
$t_{h(MOSI)}$	MOSI hold time w.r.t SCK sampling edge		3 t_{MASTER} + 15 ns		

1. Data based on characterisation results, not tested in production

Figure 20. SPI configuration, slave mode with CPHA = 0, single transfer

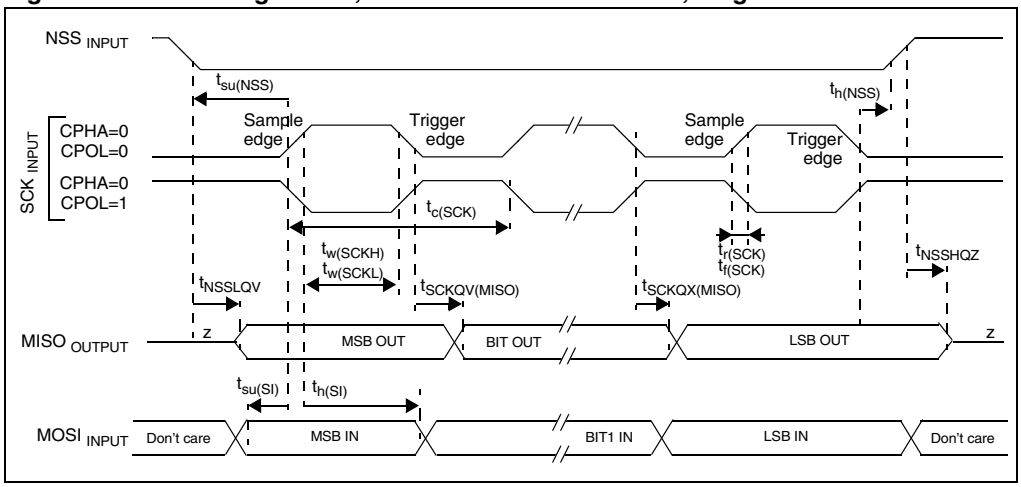


Figure 21. SPI configuration - slave mode with CPHA = 0, continous transfer

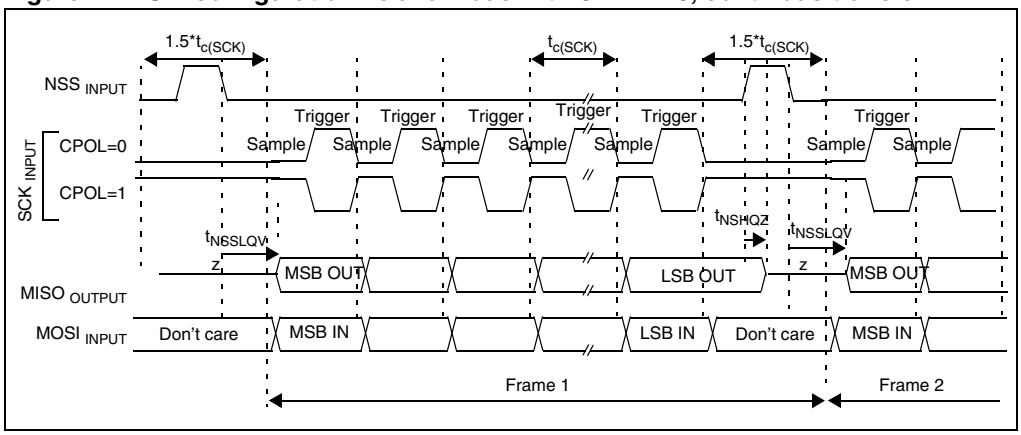


Figure 22. SPI configuration, slave mode with CPHA = 1, single transfer

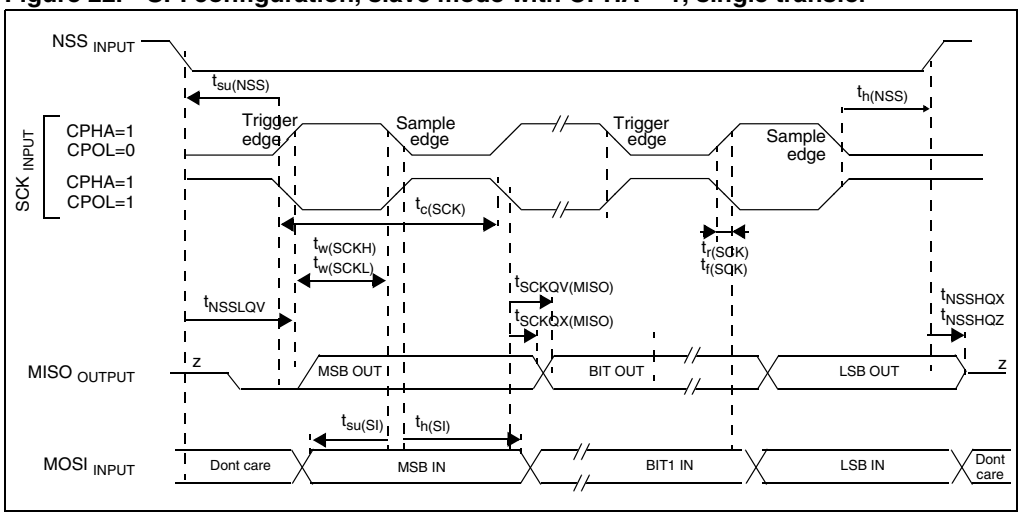


Figure 23. SPI configuration - slave mode with CPHA = 1, continous transfer

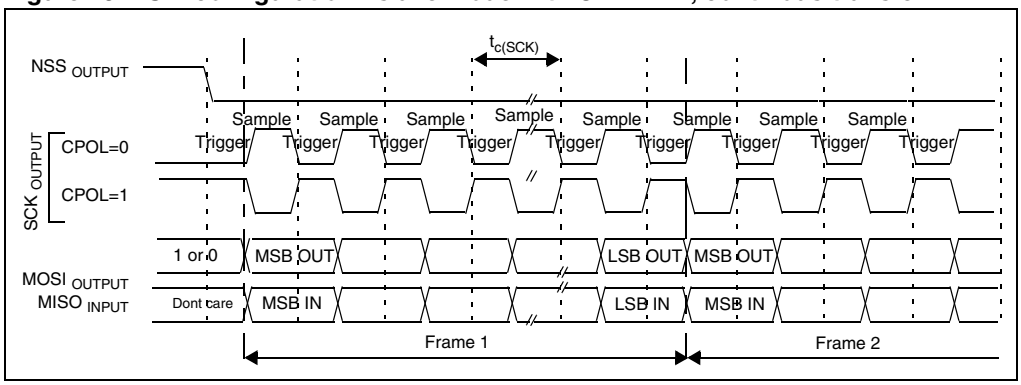


Table 37. I^2C characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I^2C speed (400kHz)
2. Data based on standard I^2C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

11.3.8 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 38. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency		1		2	MHz
V_{AIN}	Conversion voltage range(1)		V_{SSA}		V_{DDA}	V
C_{ADC}	Internal sample and hold capacitor			3		pF
t_S(1)	Minimum sampling time	f_{ADC} = 2 MHz		0.5		µs
t_{STAB}	Wake-up time from standby			7		µs
t_{CONV}	Minimum total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 2 MHz		7		µs
				14		$1/f_{ADC}$

1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 39. ADC accuracy with f_{ADC} = 2 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error (1)		1.5	3	LSB
$\|E_O\|$	Offset error (1)		1.5	2	
$\|E_G\|$	Gain error (1)		1.5	2	
$\|E_D\|$	Differential linearity error (1)		1	2	
$\|E_L\|$	Integral linearity error (1)		1	2	

1. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 11.3.5* does not affect the ADC accuracy.

Table 40. ADC accuracy with f_{ADC} = 2 MHz, R_{AIN} < 10 kΩ R_{AIN}, V_{DDA} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error(1)		2	4	LSB
$\|E_O\|$	Offset error(1)		2	2.5	
$\|E_G\|$	Gain error(1)		1.5	2	
$\|E_D\|$	Differential linearity error(1)		1	2	
$\|E_L\|$	Integral linearity error(1)		1.5	2	

1. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 11.3.5* does not affect the ADC accuracy.

Figure 24. ADC accuracy characteristics

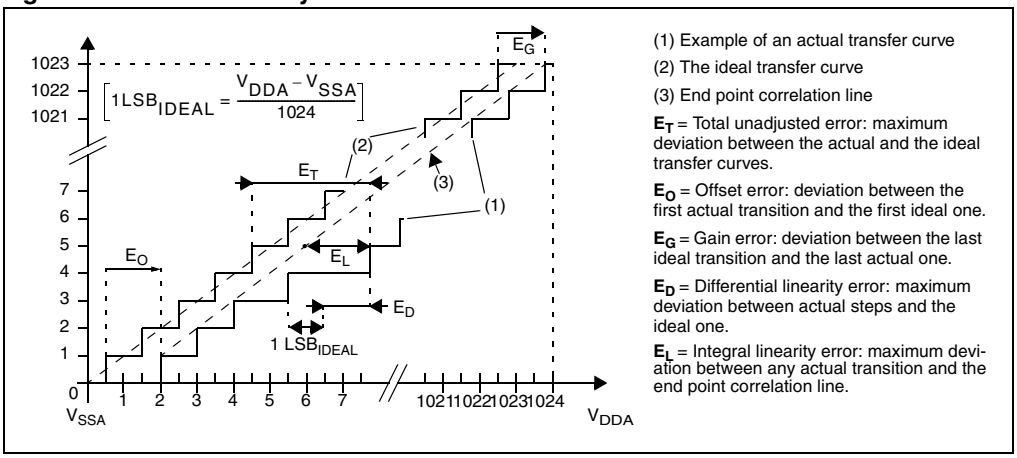
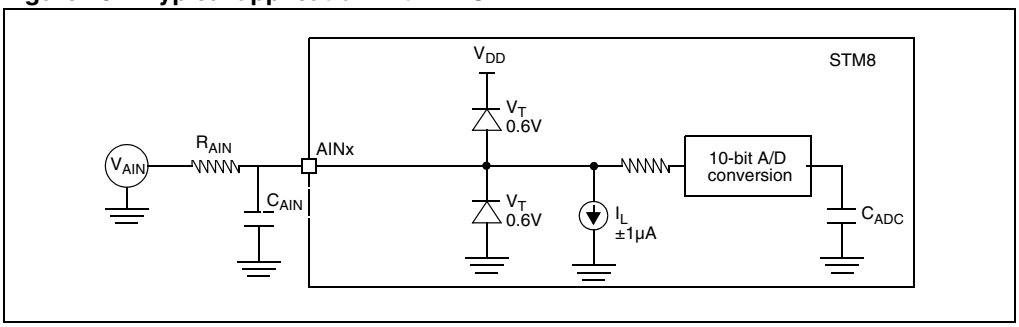


Figure 25. Typical application with ADC



11.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 17: General operating conditions on page 54*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 41. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.4.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

11.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order codes (see *Figure 30: STM8A order codes on page 80*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 82 °C (measured according to JESD51-2), I_{DDmax} = 8 mA, V_{DD} = 5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

$$P_{INTmax} = 8 \text{ mA} \times 5 \text{ V} = 400 \text{ mW}$$

$$P_{IOmax} = 20 \times 8 \text{ mA} \times 0.4 \text{ V} = 64 \text{ mW}$$

This gives: P_{INTmax} = 400 mW and P_{IOmax} 64 mW:

$$P_{Dmax} = 400 \text{ mW} + 64 \text{ mW}$$

Thus: P_{Dmax} = 464 mW

Using the values obtained in *Table 41: Thermal characteristics on page 73* T_{Jmax} is calculated as follows:

– For LQFP64 46°C/W

$$T_{Jmax} = 82° \text{ C} + (46° \text{ C/W} \times 464 \text{ mW}) = 82°\text{C} + 21°\text{C} = 103° \text{ C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105°$ C).

In this case, parts must be ordered at least with the temperature range suffix B (see *Figure 30: STM8A order codes on page 80*).

12 Package characteristics

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at *www.st.com*.

12.1 Package mechanical data

Figure 26. 80-pin low profile quad flat package (14 x 14)

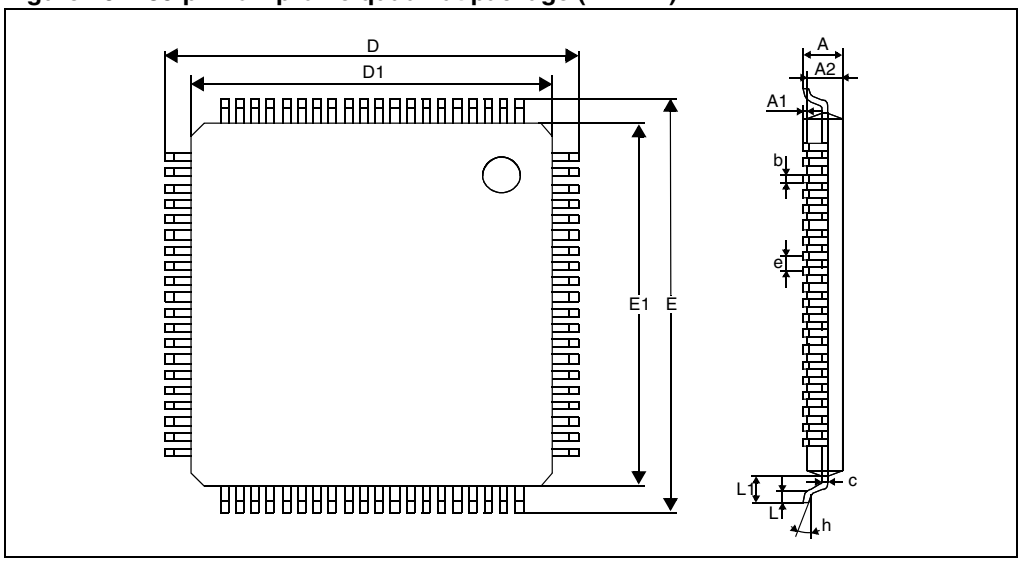


Table 42. 80-pin low profile quad flat package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.22	0.32	0.38	0.0087	0.0126	0.0150
C	0.09		0.20	0.0035		0.0079
D		16.00			0.6299	
D1		14.00			0.5512	
E		16.00			0.6299	
E1		14.00			0.5512	
e		0.65			0.0256	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 27. 64-pin low profile quad flat package (10 x 10)

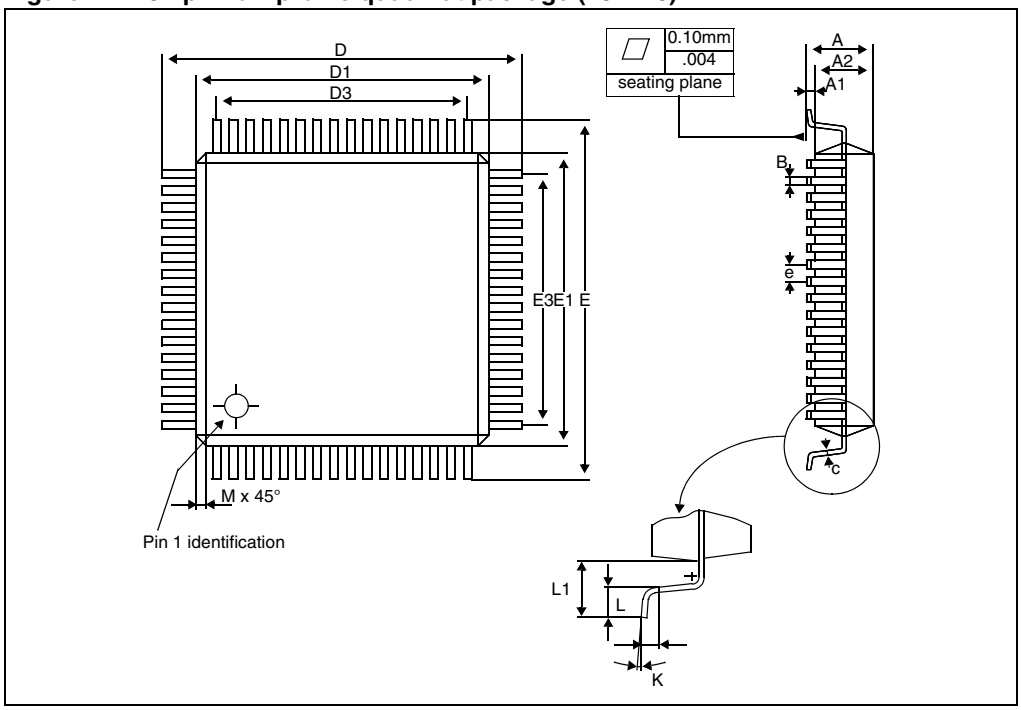


Table 43. 64-pin low profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 28. 48-pin low profile quad flat package (7 x 7)

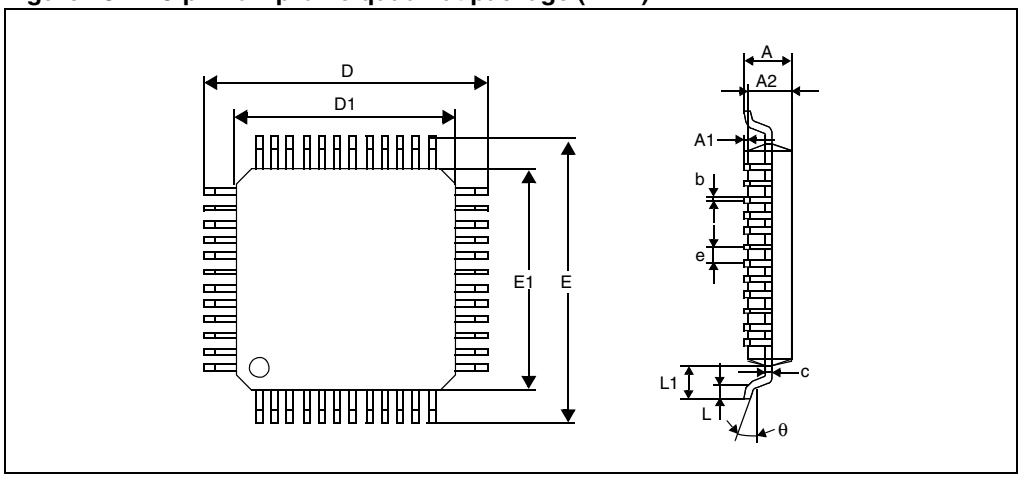
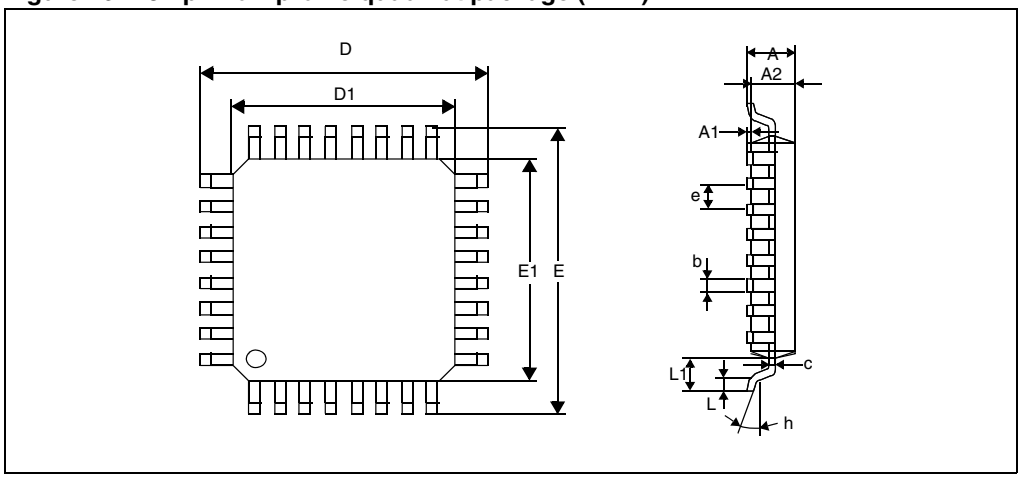


Table 44. 48-pin low profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.50			0.0197	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 29. 32-pin low profile quad flat package (7 x 7)



1. Available only for STM8A products with up to 64 Kbytes Flash

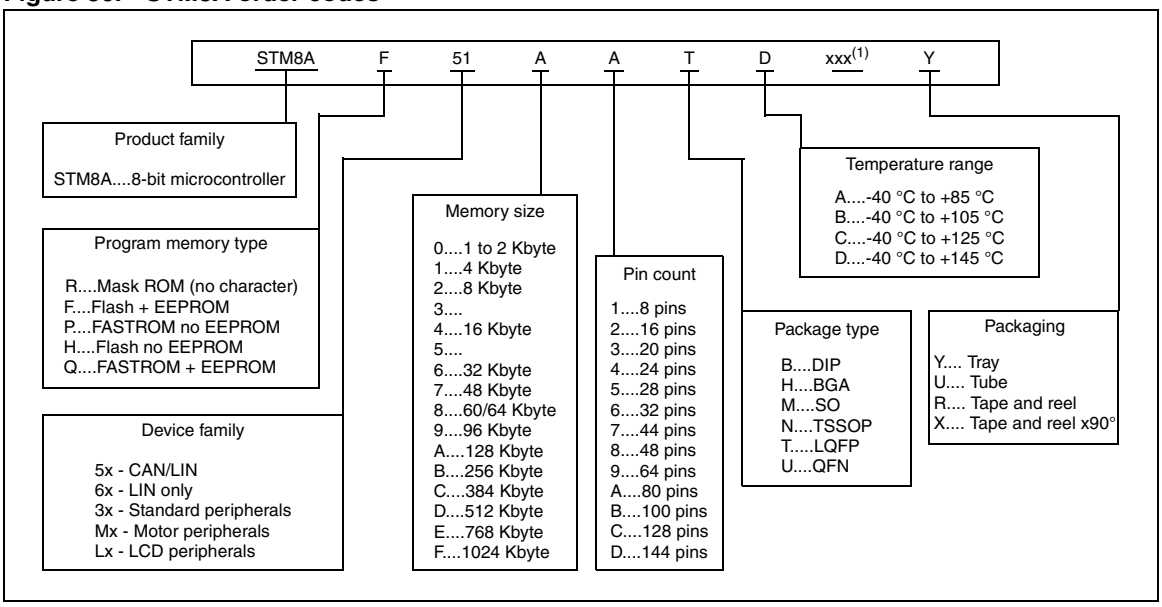
Table 45. 32-pin low profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.80			0.0315	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

13 Ordering information

Figure 30. STM8A order codes



1. Customer specific ROM code

14 STM8 development tools

Development tools for the STM8 microcontrollers include the

- STice emulation system offering tracing and code profiling
- STVD high-level language debugger including C compiler, assembler and integrated development environment
- STVP Flash programming software

In addition, the STM8 comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

14.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full-featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including tracing, profiling and code coverage analysis to help detect execution bottlenecks and dead code.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

STice key features

- Program and data trace recording up to 128 K records
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Real-time read/write of all device ressources during emulation
- Occurrence and time profiling and code coverage analysis (new features)
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- USB 2.0 high speed interface to host PC
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8

14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST7/STM8 visual develop (STVD7) IDE and the ST7/STM8 visual programmer (STVP) software interface. STVD provides seamless integration of the cosmic C compiler for STM8, which is available in a free version that outputs up to 16 Kbytes of code.

14.2.1 ST7/STM8 toolset

ST7/STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com/mcu. This package includes:

ST visual develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST7 visual programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of your STM8 microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD7 integrated development environment, making it possible to configure and control the building of your application directly from an easy-to-use graphical interface.

Available toolchains include:

- **Cosmic C compiler for STM8** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.
- **ST7/STM8 assembler linker** – Free assembly toolchain included in the ST7/STM8 toolset, which allows you to assemble and link your application source code.

14.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on your application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming your STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

15 Revision history

Table 46. Document revision history

Date	Revision	Changes
31-Jan-2008	Rev 1	Initial release

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