Motion-JPEG

Real Time Video CODEC LSI

Product Specification

1. OUTLINE

Real Time Video Codec LSI is a LSI chip which can compress/decompress high performace still image and motion picture data. The method of Encode/Decode is based on JPEG, an international standard encode/decode method for color still image.

Features:

• Compression/Decompression of high performace still image & motion picture data. (High Speed)

* for color image, 14.3MHz/Pixel high speed
* for grey level image, 28.6MHz/Pixel high speed
* real time process for color image and grey level image (full frame [30 frames/sec], full screen [768x480 : NTSC] in case of DMA mode) (High Quality Image)
* block distortion detection function
* real time process even in high quality mode. (full frame [30 frames/sec], full screen [768x480 : NTSC] in case of DMA mode)

• Total cost down for the system

(Minimize external circuit & packaging area)
* can directly connect with NTSC signal encoder/decoder without frame memory.
* comprssion/decompression functions in one chip
* color space conversion function
* control function of buffer memory for raster block conversion
* For the system without cpu, it provides independent board and separated cpu I/F and compression data I/ F.

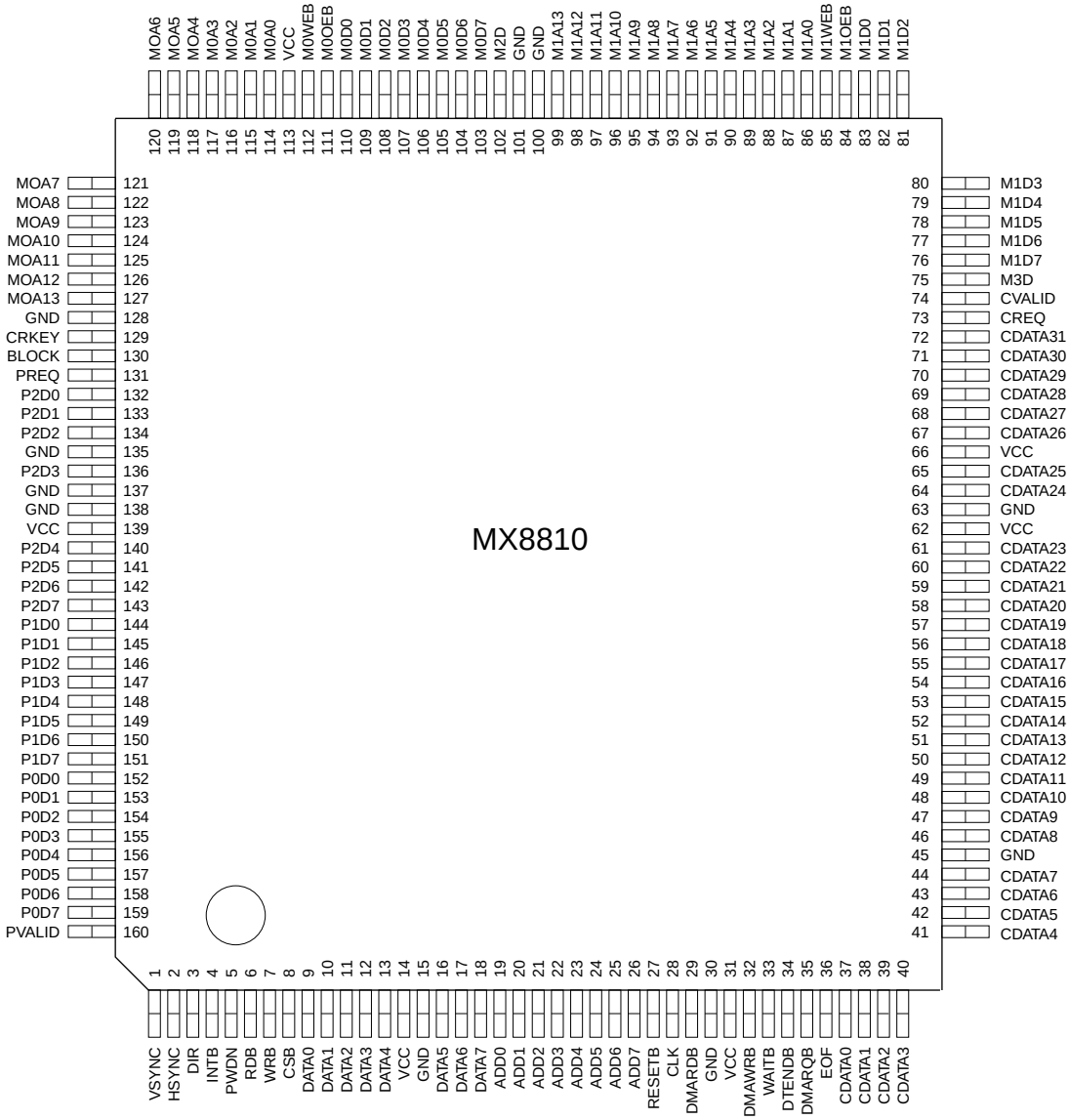
• Others

* field decision function
* power down function
* standard Y quantization table/ standard C quantization table (user definable)
* quantization table scale function
* standard Y huffman table/ standard C huffman table
* 32bits/16bits DMA mode or synchronous mode can be used in data compression I/O.
* chroma-key detection
* maximum system clock = 28.6MHz
* 160 pins QFP
* 5V single power supply

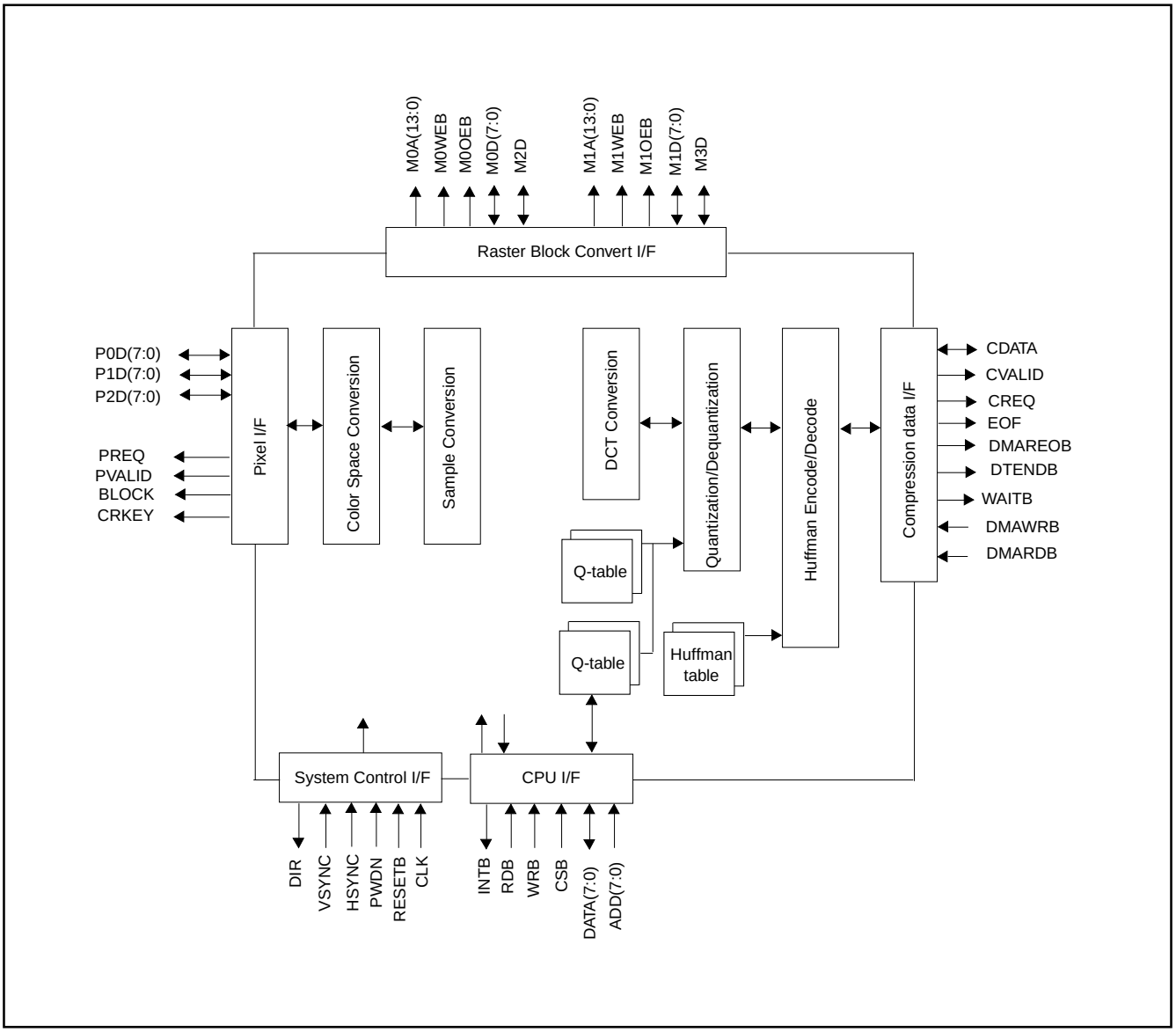
Application:

- CATV
- High-Speed Video Camera
- Animation process board for PC
- TV
- Security Camera
- Digital Still Video Camera
- Image Editor

2.PIN CONFIGURATION



3.BLOCK DIAGRAM



4.PIN DESCRIPTION

4-1 Pin Definition Table

PIN NO	SYMBOL	I/O	OUT TYPE
1	VSYNC	IN	
2	HSYNC	IN	
3	DIR	OUT	4
4	INTB	OD	4
5	PWDN	IN	
6	RDB	IN	
7	WRB	IN	
8	CSB	IN	
9~13,16~18	DATA0~DATA7	IO	4
19~26	ADD0~ADD7	IN	
27	RESETB	IN	
28	CLK	IN	
29	DMARDB	IN	
32	DMAWRB	IN	
33	WAITB	OUT	4
34	DTENDB	OD	4
35	DMAREQB	OUT	4
36	EOF	OUT	4
37~44,46~61,64~65,67~72	CDATA0~CDATA31	I/O	4
73	CREQ	OUT	4
74	CVALID	OUT	4
75	M3D	IO	2
76~83	M1D0~M1D7	IO	2
84	M1OEB	OUT	2
85	M1WEB	OUT	2
86~99	M1A0~M1A13	OUT	2
102	M2D	IO	2
103~110	M0D0~M0D7	IO	2
111	M0OEB	OUT	2
112	M0WEB	OUT	2
114~127	M0A0~M0A13	OUT	2
129	CRKEY	OUT	2
130	BLOCK	OUT	2

PIN NO	SYMBOL	I/O	OUT TYPE
131	PREQ	OUT	2
132~134,136,140~143	P2D0~P2D7	IO	2
144~151	P1D0~P1D7	IO	2
152~159	P0D0~P0D7	IO	2
160	PVALID	OUT	2
14,31,62,66,113,139	VCC	POWER	
15,30,45,63,100,101,128,135, 137,138	GND	POWER	

I/O:
IN:TTL level input
OUT:output
IO:TTL level I/O
OD:open dr

OUTPUT TYPE:
2:Iol = 2mA/Ioh = -1mA
4:Iol = 4mA/Ioh = -2mA

4-2. Pin Function Description

<Pixel I/F>

- P0D7~0 [IO] (Pixel data 0 signal)
  Pixel data 0's Input/Ouput

- P1D7~0 [IO] (Pixel data 1 signal)
  Pixel data 1's Input/Ouput

- P2D7~0 [IO] (Pixel data 2 signal)
  Pixel data 2's Input/Ouput

- PREQ [OUT] Pixel data access busy signal)
  If it is "H", pixel data access busy when CLK is active.

- PVALID [OUT] (Pixel data valid signal)
  If it is "H", pixel data output is valid when CLK is active.

- BLOCK [OUT] (Block distortion detection signal)
  If it is "H", block distortion is predictable for pixel data when CLK is active.

- CRKEY [OUT] (Chroma-key signal)
  If it is "H", chroma-key is detected for pixel data when CLK is active.

<Raster Block Convert I/F>

- M0A13~0 [OUT] (External memory 0 address signal)
  Address output to external memory 0 for raster block conversion.

- M1A13~0 [OUT] (External memory 1 address signal)
  Address output to external memory 1 for raster block conversion.

- M0WEB [OUT] (External memory 0 write enable signal)
  Write enable output to external memory 0 for raster block conversion. (negative)

- M1WEB [OUT] (External memory 1 write enable signal)
  Write enable output to external memory 1 for raster block conversion. (negative)

- M0OEB [OUT] (External memory 0 output enable signal)
  Output enable output to external memory 0 for raster block conversion.(negative)

M1OEB [OUT] (External memory 1 output enable signal)
Output enable output to external memory 1 for raster block conversion. (negative)

M0D7~0 [IO] (External memory 0 data signal)
Data I/O to external memory 0 for raster block conversion.

M1D7~0 [IO] (External memory 1 data signal)
Data I/O to external memory 1 for raster block conversion.

M2D [IO] (External memory data signal for block distortion detection)
Data I/O to external memory for block distortion detection .

M3D [IO] (External memory data signal for block distortion detection)
Data I/O to external memory for block distortion detection .

<Compression Data I/F>

- CDATA31~0 [IO] (Compression data signal)
  Compression data I/O. In case of 16bits DMA, CDATA15~0 is valid.

- CVALID [OUT] (Compression data valid signal)
  In case of synchronous mode compression, "H" means compression data output is valid when CLK is active.

- CREQ [OUT] (Compression data access busy signal)
  In case of synchronous mode decompression, "H" means compression data access busy when CLK is active.
  P.S.) It is a level signal. Do not use in "canging edge (edge trigger)".

- EOF [OUT] (Last process image's last compression data signal)
  In case of DMA mode compression, "H" means that the compression data being read out is the last image's last compression data.
  In case of synchronous mode compression, "H" means that the compression data is the last image's last compres sion data while CLK is active.

- DMAREQB [OUT] (DMA request signal)
  If it is "L", DMA transfer is requested.

- DTENDB [OD] (Image's last compression data signal)
  In case of DMA mode compression, "L" means that the compression data being read out is each image's last compression data.
  In case of synchronous mode compression, "L" means that the compression data is each image's last compression data while CLK is active.

- WAITB [OUT] (Compression data bus wait signal)
  If it is "L", read/write wait request from internal compression data FIFO.

- DMAWRB [IN] (Compression data write enable signal)
  Write enable input to internal compression data FIFO. (negative)

- DMARDB [IN] (Compression data read enable signal)
  Read enable input to internal compression data FIFO. (negative)

<CPU I/F>

- ADD7~0 [IN] (CPU address signal)
  8 bits CPU address bus for selection of parameter setting internal register.

- DATA7~0 [IO] (CPU data signal)
  8 bits CPU data bus for parameter data's I/O.

- CSB [IN] (CPU chip select signal)
  Chip select input of CPU bus. (negative)

- WRB [IN] (CPU data write enable signal)
  Write enable input to parameter setting internal register. (negative)

- RDB [IN] (CPU data read enable signal)
  Read enable input to parameter setting internal register. (negative)

- INTB [OD] (Interrupt request signal)
  If it is "L", interrupt request to CPU. (negative)

<System Control I/F>

- CLK [IN] (Clock signal)
  Clock input.

- RESETB [IN] (Hardware reset signal)
  If it is "L", hardware reset will be executed. Internal circuit will be initialized and internal register will be set by default value.
  In the period of hardware reset, all I/O pins will be changed to input mode.

- PWDN [IN] (Power down signal)
  If it is "H", change to the power down mode.

- HSYNC [IN] (Horizontal synchronous signal)
  Horizontal synchronous signal input. (positive)

- VSYNC [IN] (Vertical synchronous signal)
  Vertical synchronous signal input. (positive)

- DIR [OUT] (Interface direction signal)
  If it is "H", pixel I/F is input mode and compression data I/F is output mode.
  If it is "L", pixel I/F is output mode and compression data I/F is input mode.

<Power Supply>

- VCC [power] (Power supply)

- GND [power] (Ground)

5. FUNCTION DISCRIPTION

5-1.FUNCTIONS

5-1-1. Pixel I/F

Data input/output, based on HSYNC/VSYNC valid data area.
Corresponding formats are
o RGB format o YCrCb format o YC format o Y0Y1 format

5-1-2. Color Space Conversion

RGB space <---> YCrCb space conversion

5-1-3. Sample Conversion

In compression, 1/2 thin out Cr and Cb in horizontal direction then multiplex it.
In decompression, demultiplex Cr and Cb then execute previous value interpolation in horizontal direction.

5-1-4. Raster Block Convert I/F

Interface to external memory for the conversion of raster order <---> 8x8 block order.

5-1-5. Quantization Table

Standard Y table and Standard C table is equipped for the quantization table. User can also select his own user-define Y table/ user-define C table.

5-1-6. Quantization Table Scale

In standard quantization table and user define quantization table, each value is uniformly scalable.

5-1-7. Huffman Table

Standard Y table/ Standard C table is equipped.

5-1-8. Compression Data I/F

Compression data I/O in synchronous mode or DMA mode.
In synchronous mode, it operates at all compression rate in case of no processing enor.
But, in decompression, the frequency of clock is limited by the AC characterization.
In case of DMA mode, 16 bits or 32 bits bus width for selection.
And 28.6MHz is the upper limit of operation, but in case of processing error, the compression rate will be limited.

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5-1-9. Power Down

Stop providing clock to internal circuit in order to save power consumption.

5-1-10. Field Decision

Interlace/nointerlace decision from horizontal synchronous signal and vertical synchronous signal.
In case of interlace, first field is the beginning of compression / decompression.

5-1-11. Block Distortion Detection

It can detect the block which is possibly a distorted block in decompression. From detected result, block distortion could be amended by external filter control.

5-1-12. Chroma-key Detection

In case of decompression, chroma-key could be detected.

5-2. Block Functions

5-2-1. Pixel I/F

Pixel I/F provides Input/Output for the data based on HSYNC/VSYNC valid data area on defined pixel format.
In case of compression, set PERQ "H" and access pixel data when CLK is active.
In case of decompression, if set PVAILD "H" vaild pixel data is exported.
The corresponding formats are

• RGB format • YCrCb format • YC format • Y0Y1 format

5-2-2. Color Space Conversion

In case that RGB format is selected to be pixel format, RGB space <--->YCrCb space conversion will be executed. In case of other pixel formats, there is no conversion.

R0 R1 R2 R3 ... <---> Y0 Y1 Y2 Y3...
G0 G1 G2 G3 ... <---> Cr0 Cr1 Cr2 Cr3...
B0 B1 B2 B3 ... <---> Cb0 Cb1 Cb2 Cb3...

Moreover, In case of decompression, chroma-key detection is executed.

5-2-3. Sample Conversion

When RGB format and YCrCb format are selected to be a pixel format, in compression, 1/2 thin out Cr and Cb in horizontal direction then multiplex it. In decompression, demultiplex Cr and Cb then execute previous value interpolation. There is no conversion in other pixel formats.

Compression: Y0 Y1 Y2 Y3.... --- > Y0 Y1 Y2 Y3 ... .
Cr0 Cr1 Cr2 Cr3.... ---> — Cr0 Cb0 Cr2 Cb2...
Cb0 Cb1 Cb2 Cb3....---- ----> — —>

Deompression: Y0 Y1 Y2 Y3.... <--- Y0 Y1 Y2 Y3...
Cr0 Cr0 Cr2 Cr2.... <--- Cr0 Cb0 Cr2 Cb2....
Cb0 Cb0 Cb2 Cb2.... <---

5-2-4. Raster Block Convert I/F

Interface to external memory for raster order <---> 8x8 block order conversion.

5-2-5. DCT Conversion

8x8 image block <---> DCT factor 2-dimension DCT conversion.

5-2-6. Quantization / Dequantization

ZIGZAG conversion and quantization / dequantization are executed here. We can select ROM's standard Y table / standard C table or RAM's user Y table / user C table to be quantization table.
Each value of selected table is scalable uniformly by the scale factor setting.
Moreover, in case of decompression, the block which is possibly a distorted block will be detected.
From the detected result, block distortion could be amended by external filter control.

5-2-7. Huffman Encode/Decode

In case of compression, huffman encode the quantized DCT factor to compression data. In case of decompression, huffman decode the compressed data. Huffman table is equipped as standard Y table / standard C table.

5-2-8. Compression Data I/F

Compression data' I/O in synchronous mode or DMA mode.

- Synchronous mode

  32 bits bus width.
  In case of compression, if CVALID = "H", valid compression data is exported.
  In case of decompression, if CREQ = "H" and CLK is active, access compression data.

- DMA mode

  16 bits or 32 bits bus width.
  2k bytes compression data FIFO.

Compression:

If compression data FIFO is not empty, set DMAREQB "L".
If compression data FIFO is empty, set DMAREQB "H".
When compression data FIFO is not empty, if DMARDB = "L", valid compression data is exported.
When compression data FIFO is empty, if DMARDB = "L", WAITB will be "L".
When changing to nonempty, WAITB will change to "H" and valid compression data is exported.
For each image's last compression data, if DMARDB = "L", DTENDB change to "L".
(If DMARDB change to "H" DTENDB will be "Z")

Decompression:

If compression data FIFO is not full, set DMAREQB "L".
If compression data FIFO is full, set DMAREQB "H".
When compression data FIFO is not full, if DMAWRB = "L", access compression data when DMAWRB is active.
When compression data FIFO is full, if DMAWRB = "L", WAITB will be "L".
When changing to "H" not full, WAITB change to access compression data when DMARDB is active.

5-2-9. CPU I/F

Parameters' setting.
Set values to the internal registers using 8 bits address bus and 8 bits data bus.

5-2-10. System Control I/F

Control hardware reset, power down and field decision functions.
Field decision function is executed in 7th line's HSYNC from VSYNC.
Output of I/O direction of Pixel I/F and compression data I/F.

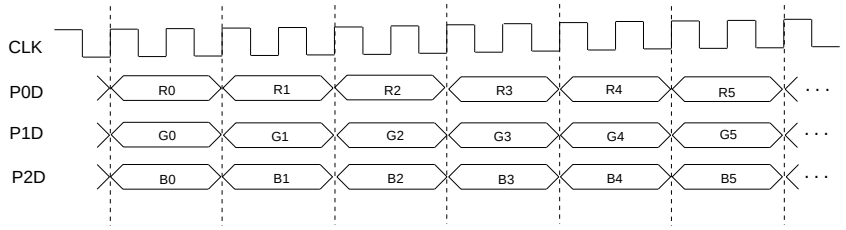
5-3. External Interface

5-3-1. Pixel I/F

Pixel I/F provides Input/Output for the data based on HSYNC/VSYNC valid data area on defined pixel format. I/O rate is 1/2 of system clock's frequency.
Compression: export "H" to PREQ, access pixel data while CLK is active.
Decompression: If PVALID = "H", valid pixel data is exported. Refer when CLK is active.
Moreover, detection result output to BLOCK and the result of chroma-key detection output to CRKEY.

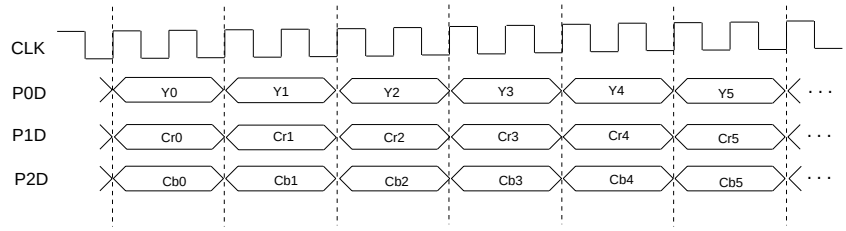
RGB format

R,G,B=raster order data , 8bits positive number



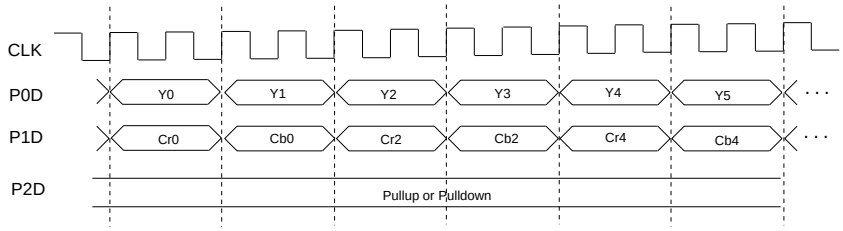
YCrCb format

Y=raster order data , 8bits positive number
Cr,Cb=raster order data , 8bits 2'complement



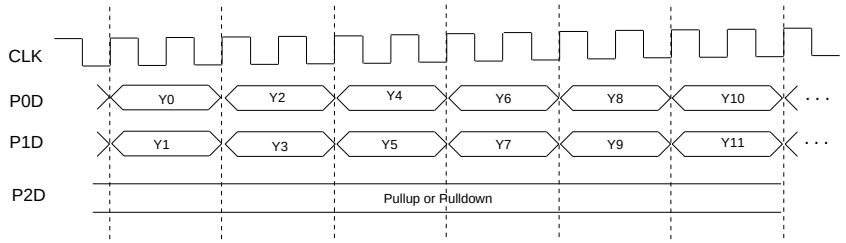
YC format

Y=raster order data , 8bits positive number
C=raster order data with Cr,Cb half-and-half, 8bits 2'complement



Y0Y1 format

Y0=raster order even number data , 8bits positive number
Y1=raster order O&D data , 8bits 2'complement



5-3-2. Raster Block Convert I/F

The I/O of control signal (address, write enable, output enable) and bidirection data to external memory. Use SRAM to be an external memory, the direct connection is possible. (e.g. refer " 6-1, External memory for raster block")

5-3-3. Compression Data I/F

The Input/Output of compression data in synchronous mode or DMA mode.

• Synchronous mode

32 bits bus width.
Compression: If CVALID = "H", compression data is exported. Refer when CLK is active.
Moreover, DTENDB and each image's last compression data will be exported at the same time.
Decompression: When CREQ = "H" and CLK is active, compression data access busy.

• DMA mode

16 bits bus width or 32 bits bus width.
In case of 16 bits, CDATA15 ~ CDATA0 are I/O of compression data.
(CDATA31 ~ CDATA16 are used as pull up or pull down)
Compression:
1) Read access
No matter DMAREQB is L or H, Set DMARDB "L" and confirm
WAITB = "H", then refer to valid compression data while DMARDB is active.
2) DMA demand
Set DMARDB "L" when DMAREQB = "L", then refer valid compression data while DMARDB is active.
When DMAREQB = "H", read will not be executed.
3) DMA burst
Begin to read when DMAREQB = "L", if WAITB = "L" DMARDB keeps "L" untill WAITB changes to "H".
When DTENDB change to "L", reading stop.

Deompression:
1) Write access
No matter DMAREQB is L or H, Set DMAWRB "L" and confirm WAITB = "H", then write compression data while DMAWRB is active.
2) DMA demand
Set DMAWRB "L" when DMAREQB = "L", then write compression data while DMAWRB is active.
When DMAREQB = "H", write will not be executed.
3) DMA burst
Begin to write when DMAREQB = "L", if WAITB = "L"
DMAWRB keeps "L" untill WAITB changes to "H".

- **I/O format of compression data**

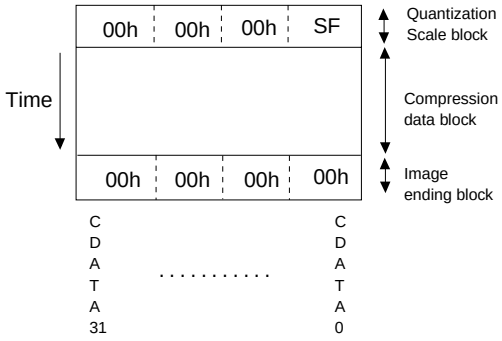
  Each image's I/O compression data are constructed by quantization table scale block, compression data block and image ending block.

  o Quantization table scale block
  constructed by 24 bits data (00h,00h,00h) and 8 bits quanttization table scale factor (SF).

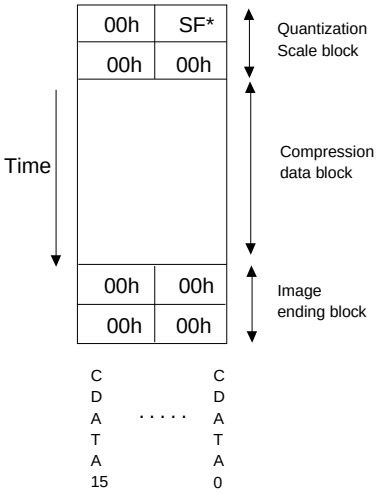
  o Compression data block
  constructed by compression data which the marker is deleted (byte strip) from JPEG data.

  o Image ending block
  constructed by 32 bits data (00h,00h,00h,00h).

Synchronous and 32bits DMA mode



16bits DMA mode



SF:8bits' quantization table scalefacton

5-3-4. CPU I/F

Parameters' setting is executed here.

Set values to the internal registers using 8 bits address bus and 8 bits data bus.

• Address Map

REGISTER	Address MAP	R/W	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
Command	00	R/W	STA	-	-	-	-	-	-	SRB
Mode	01	R/W	DET	DMA	-	WID		PFM		ENC
Scale factor	02	R/W			ESC	(7:0)				
Horizontal dot cycle	04	R/W	-	-	-	-		HCY	(11:8)	
	05	R/W				HCY	(7:0)			
Horizontal valid dot delay	06	R/W	-	-	-	-		HDL	(18:8)	
	07	R/W				HDL	(7:0)			
Horizontal valid dot width	08	R/W	-	-	-	-		HWD	(10:8)	
	09	R/W				VCY	(7:0)			
Vertical line cycle	0A	R/W	-	-	-	-		VCY	(11:8)	
	0B	R/W				VCY	(7:0)			
Vertical valid line delay	0C	R/W	-	-	-	-		VDL	(10:8)	
	0D	R/W				VDL	(7:0)			
Vertical valid line width	0E	R/W	-	-	-	-	-	VWD	(10:8)	
	0F	R/W				VWD	(7:0)			
Status	10	R	FIN	FUL	EMP	ERR	-	-	-	-
Interrupt mask	11	R/W	MFI	MFU	MEM	MER	-	-	-	-
Y detection	12	R/W	YDT	(7:5)		-	-	-	-	-
Cr detection	13	R/W	CRD	(7:5)		-	-	-	-	-
Cb detection	14	R/W	CBT	(7:5)		-	-	-	-	-
Y detect mask	15	R/W	MYD	(7:5)		-	-	-	-	-
Cr detect mask	16	R/W	MCR	(7:5)		-	-	-	-	-
Cb detect mask	17	R/W	MCB	(7:5)		-	-	-	-	-
Y quantization table	80 ↓ BF	R/W ↓ R/W				YQ00 ↓ YQ63	(7:0) ↓ (7:0)			
C quantization	C0 ↓ FF	R/W ↓ R/W				CQ00 ↓ CQ63	(7:0) ↓ (7:0)			

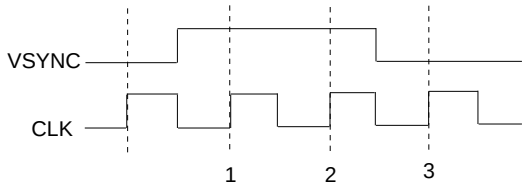
Note: When address="03" or "18-7F" please don't read and write.

• Command register

Control start/finish of compression/decompression and software reset process.

	Function	H	L	S/W reset	H/W reset
STArt	Start	Start	Stop	Previous value	L
Soft ReseT_B	S/W reset	release	reset	/	H

STA(bit7): refer STA while VSYNC rises to "H" when CLK is active. (refer the following figure)
If it is 1, wait for first field then start the process.
If it is 0, process current field then finish.



1) VSYNC rises to "H" when CLK is active, refer STA.
2) Because VSYNC do not change from "H" when CLK is active, do not refer STA.
3) Because VSYNC is "L" when CLK is active, do not refer STA .

SRB(bit0): If set it to 0, software reset process starts.
Set it to 1 when software reset process is over.
Software reset will cause process compulsory interrupt,releasing process error and clearing internal compression data FIFO.

• Mode Register

Mode control for Compression / Decompression, Pixel I/F, Compression data I/F and Quantization table(Q-table).

	Function	H	L	S/W reset	H/W reset
Default -Table	Q-Table	ROM	RAM	Previous Value	H
DMA	DMA/Sync	DMA	Sync	Previous Value	H
WIDe bus	DMA pulse width	32bit	16bit	Previous Value	L
Pix ForMat	Pixel I/F Format	Data		Previous Value	6h
EnCode/ decode	Compression/ Decompression	Compression	DCcompression	Previous Value	H

DFT(bit7): If set it to 1, standard Q-table will be selected.
If set it to 0, user define Q-table will be selected.
When user define Q-table is selected, you must setup values to the table.

DMA(bit6): If set it to 1, DMA mode of compression data I/F will be selected.
If set it to 0, synchronous mode of compression data I/F will be selected.

WID(bit4): It is valid while DMA mode of compression data I/F is selected.
If set it to 1, 32 bits DMA will be selected.
If set it to 0, 16 bits DMA will be selected.

PFM(bit3-0): Use the following value to select pixel I/F format.
RGB format = 7h
YCrCb format= 6h
YC format = 4h
Y0Y1 format = 0h
P.S.) please do not use the other values.

ENC(bit0): If set it to 1, Compression mode will be selected.
If set it to 0, Decompression mode will be selected.

• Scale Factor Register

Control the scale factor of Q-table.

	Function	H	L	S/W reset	H/W reset
E-SCale factor(7:0)	Quantization table scale factor	Data		Previous Value	04h

ESC(bit7-0): In compression, please setup Q-table scale factor.
Q-table each value is divided by this scale factor while quantization is executing.
bit7-2 are integer part and bit1-0 are decimal fraction.

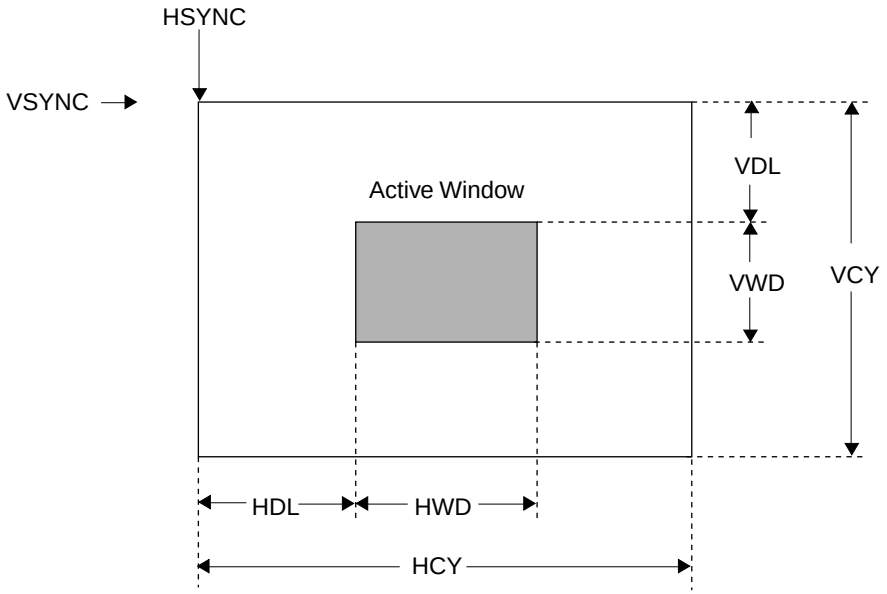
- Horizontal Dot Cycle Register
  Horizontal Valid Dot Delay Register
  Horizontal Valid Dot Width Register
  Vertical Line Cycle Register
  Vertical Valid Line Delay Register
  Vertical Valid Line Width Register

  Control the valid area which based on image's size and HSYNC /VSYNC.

	Function	H	L	S/W reset	H/W reset
H_CYcle(11:0)	Horizontal Dot Cycle	Data		Previous Value	-
H_DeLay(10:0)	Horizontal Effective Delay	Data		Previous Value	-
H_WiDth(10:0)	Horizontal Effective width	Data		Previous Value	-
V_CYcle(11:0)	Horizontal live cycle	Data		Previous Value	-
V_DeLay(10:0)	Horizontal Effective Delay	Data		Previous Value	-
V_WiDth(10:0)	Horizontal Effective Width	Data		Previous Value	-

HCY, HDL, HWD's unit are dot (pixel). Please setup the values from HSYNC.
VCY, VDL, VWD's unit are line. From VSYNC, Please set up the values at the intervals of HSYNC.

About each value, please refer to the following figure.



P.S.) Please precisely set
(CLK frequency)/(Horizontal sync frequency)/2-1 to HCY.

Set -1 of the value to each register.
In case of interlace, please set field size related value.
The following table shows the other limitation.

Y0Y1 format selected

	MIN	MAX	OTHERS
HCY	.(HWD+1)¸ 2+99 .HDL+HWD+5 bigger value of two	7FFh	
HDL	001h	3FFh	
HWD	01Fh	3FFh	64X-1
VCY	VDL+VWD+2	FFFh	
VDL	010h	7FFh	
VWD	007h	7FFh	8X-1

Other pixel formats selected

	MIN	MAX	OTHERS
HCY	.(HWD+1)¸ 2+49 .HDL+HWD+2 bigger value of two	7FFh	
HDL	001h	3FFh	
HWD	01Fh	3FFh	32X-1
VCY	VDL+VWD+2	FFFh	
VDL	010h	7FFh	
VWD	007h	7FFh	8X-1

• Status Register
Presents Internal Operating Status

	Function	H	L	S/W reset	H/W reset
FINish	End	End	Processing	H	H
FULl	FIFO full	Full	not full	L	L
EMPty	FIFO empty	Empty	not empty	H	H
ERRor	Error	Error	not error	L	L

FIN(bit7): If 1, means compression data I/F's process is over.
If 0, means compression data I/F is in processing.

FUL(bit6):If 1, means compression data FIFO is full.
If 0, means compression data FIFO is not full.

EMP(bit5):If 1, means compression data FIFO is empty.
If 0, means compression data FIFO is not empty.

ERR(bit4):If 1, means process error.
If 0, means it is not process error.
Error when compression data FIFO is full in compression and compression data FIFO is empty in decompression.
For releasing from error condition, please do compulsorily interrupt the process of hardware reset or software reset.

• Interrupt Mask Register
Control the interrupt conditions.

	Function	H	L	S/W reset	H/W reset
MaskFInish	Finish mask	Output	Mask	Previous Value	L
MaskFUll	Full mask	Output	Mask	Previous Value	L
MaskEMpty	Empty mask	Output	Mask	Previous Value	L
MaskERro	Error mask	Output	Mask	Previous Value	L

MFI(bit7):If 1, interrupt when compression data I/F's process is over.
If 0, do not interrupt when compression data I/F's process is over.

MFU(bit6):If 1, interrupt when compression data FIFO is full.
If 0, do not interrupt when compression data FIFO is full.

MEM(bit5): If 1, interrupt when compression data FIFO is empty.
If 0, do not interrupt when compression data FIFO is empty.

MER(bit4):If 1, interrupt when process error.
If 0, do not interrupt when process error.

• Y detect Register
Cr detect Register
Cb detect Register
Y detect Mask Register
Cr detect Mask Register
Cb detect Mask Register

Control the chroma-key detection conditions.

	Function	H	L	S/W reset	H/W reset
Y-Detect(7:5)	Y detect value	Data	Data	Previous Value	00h
CR-Detect(7:5)	Cr detect value	Data	Data	Previous Value	00h
CB-Detect(7:5)	Cb detect value	Data	Data	Previous Value	00h
MaskY-Detect(7:5)	Y detect mask	Detect	Mask	Previous Value	00h
MaskCR-detect(7:5)	Cr detect mask	Detect	Mask	Previous Value	00h
MaskCB-Detect(7:5)	Cb detect mask	Detect	Mask	Previous Value	00h

YDT(bit7-5): Setup chroma-key detection Y component.
CRD(bit7-5): Setup chroma-key detection Cr component.
CBD(bit7-5): Setup chroma-key detection Cb component.
MYD(bit7-5): Setup "H" at chroma-key detection Y component's bit position.
MCR(bit7-5): Setup "H" at chroma-key detection Cr component's bit position.
MCB(bit7-5): Setup "H" at chroma-key detection Cb component's bit position.

• Y Quantization table
C Quantization table

	Function	H	L	S/W reset	H/W reset
Y_Q00(7:0)	Y quantization coefficient 00	Data	Data	Previous Value	Initial Value
↓	↓	↓	↓	↓	↓
Y_Q63(7:0)	Y quantization coefficient 63	Data	Data	Previous Value	Initial Value
C_Q00(7:0)	C quantization coefficient 00	Data	Data	Previous Value	Initial Value
↓	↓	↓	↓	↓	↓
C_Q63(7:0)	C quantization coefficient 63	Data	Data	Previous Value	Initial Value

When standard Q-table is selected, read only.
When user define Q-table is selected, read / write both work.
The format is 8 bits integer without sign.

5-3-5. System Control I/F

- Hardware reset

  When internal circuit is initialized, internal register will be set by default value.
  When internal circuit is initialized, process compulsory interrupt, releasing process error and clearing internal compression data FIFO will be executed.
  In the period of hardware reset, all I/O pins will be changed to input mode.

- Power down

  After hardware reset, please power down. Moreover, after releasing from power down, please execute the hardware reset.

- Field decision

  Interlace/Noninterlace is decided by position of 7th line's HSYNC counted from VSYNC.
  (There is no relationship with equivalent pulse and cut-in pulse of 1st~6th line)
  In case of interlace, compression/decompression starts from 1st field.

- I/O direction

  Export signal DIR for bus control of pixel I/F and compression data I/F.
  If "H", Pixel I/F is input and compression data I/F is output.
  If "L", Pixel I/F is output and compression data I/F is input.

5-4. Operations

5-4-1. General Operation

Please follow the following steps.

1.Turn on the power.

2. Hardware reset. (Set RESETB "L")

3.Set up the internal registers except command register (address = 00) if the change is necessary.

P.S.)In case of changing to DMA compression mode or changing to DMA decompression mode, please set up when the compression data FIFO is empty.
In case of EMP in status register (address = 10), the status of compression data FIFO could be investigated.
Compression data FIFO could be cleared by hardware reset or software reset.

4.Set "start process (81h)" to command register (address = 00).

5.Refer command register by VSYNC and start the process from 1st field.

6.Set "stop process (01h)" to command register (address = 00).

7.Refer command register by VSYNC and stop after the field processed.

8.If it is necessary, back to step 3.

5-4-2. Process compulsory interrupt, Releasing process error and the clearing operation of compression data FIFO

Please follow the following steps.

In case of hardware reset:

1. Execute the hardware reset. (set RESETB "L")
P.S.1) the value of CPU I/F's internal register will be changed to default value.
P.S.2) In the period of input/output of a image compression data, the image's compression data will be invalid if this operation is executed.
2. Back to general operation (5-4-1) step 3.

In case of software reset:

1. Set"stop process & software reset (00h)" to command register (address = 00).
P.S.1) In the period of input/output of a image compression data, the image's compression data will be invalid if this operation is executed.
2. Set "release software reset (01h)" to command register (address = 00).
3. Back to general operation (5-4-1) step 3.

5-4-3. Power Down Operation

The following shows power down operation.

1. Execute hardware reset. (set RESETB "L")
P.S.1) CPU I/F's internal register will be set by default value.
P.S.2) Execute process compulsory interrupt, realeasing process error and clearing compression data FIFO.
2. Start power down. (set PWDN "H")")
3. Release power down (set PWDN "L")"L")
4. Execute hardware reset. (set RESETB "L")"L")
5. Back to the general operation (5-4-1) step 3.
P.S.) The value of CPU I/F's internal register is default value.

6. External Circuit

6-1. External Memory for Raster Block Conversion

Raster block convert I/F is the interface which connects with external memory for raster order <—> 8x8 block order conversion.

he following table shows example of necessary external memory.

Selected YOYI Format

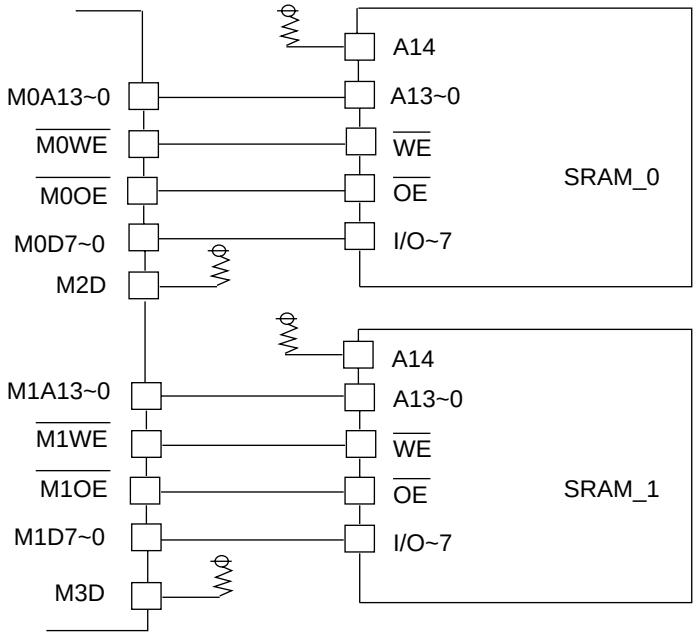
Horizontal valid dot width	Memory capacity	Data width	Pcs
64~256	16 k bits	8 bits	2
320~1024	64 k bits	8 bits	2

Selected other Format

Horizontal valid dot width	Memory capacity	Data width	Pcs
32~128	16 k bits	8 bits	2
160~512	64 k bits	8 bits	2
544~1024	256 k bits	8 bits	2

* When block distortion detecting function is used, data width should extend to 9 bits from 8 bits. (expend the memory capacity)

The following diagram shows no block distortion detecting function.



P.S.1) To meet the SRAM's write recovery and data hold, please notice each signal's delay skew caused by connection capacity.
P.S.2) Set pull up or pull down in unused M2D and M3D passing through a resister.(Please do not directly connect with VCC or GND.)
P.S.3) In case that unused signals happened in M0A13~0 and M1A13~0, open it.

6-2 Clock Generation Circuit

The circuit method for clock generation from NTSC signal is as following:

1.In case of standand NTSC signal (TV broad cast signal, LD playback signal) please use clock generation of line-lock method or burstlock method.

2.In case of non-standard NTSC signal, please use clock generation circuit of line lock method.

7.Electricity Characteritics

7-1.Absolute Maximum Rating Recommended operating condition

Absolute Maximum Rating (GND=0V)

Item	Symbol	Ratings	Units
Supply Voltage	VCC	-0.3~7.0	V
Input Voltage	Vi	-0.3~VCC+0.3	V
Output Voltage	Vo	-0.3~VCC+0.3	V
Operating Temperature	Topr	0~70	℃
Storage Temperature	Tstg	-55~-150	℃

Recommended Operating Condition

		Ratings			
Item	Symbol	MIN	TYP	MAX	Units
Supply Voltage	VCC	4.75	5.0	5.25	V
Input Low Voltage	Vil	0		0.8	V
Input High Voltage	Vih	2.0		VCC	V
Temperature around	Ta	0	25	70	℃

7-2 D.C. Characteristics

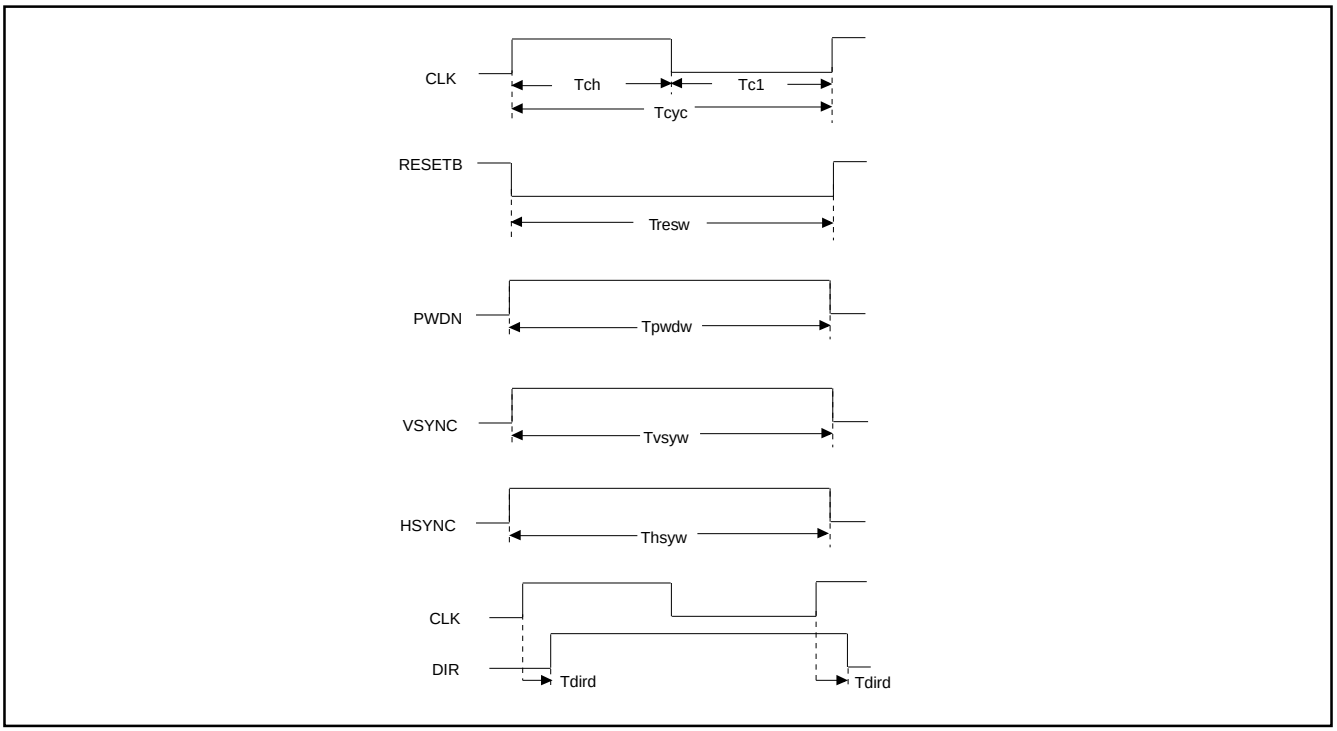
DC Characteristics (VCC=5V±5%,GND=0V,Ta=0~70℃)

			Ratings			
Item	Symbol	Conditions	MIN	TYP	MAX	Units
Static Consumption Current	Ist	Io=0mA			1	mA
Operating Consumption Current	Iop	CLK=28.6MHz,Io=0mA			360	mA
Input Leakage Current	Iil	Vi=VCC~0v	-1		1	uA
Output Leakage Current	Ioz	High-impedance	-10		10	uA
Output High Voltage	Voh	Ioh=1mA or -2mA	2.4			V
Output Low Voltage	Vol	Iol=2mA or 4mA			0.4	V
Input High Voltage	Vih	TTL level input	2.0			V
Input Loww Voltage	Vih	TTL level Output			0.8	V

Capacitance (Ta=25℃,f=1MHz)

			Ratings			
Item	Symbol	Conditions	MIN	TYP	MAX	Units
Input Capacitance	Cin	Vin=0V			10	pF
Output Capacitance	Cout	Vout=0V			10	pF
I/O Capacitance	Cio	Vi0=0V			10	pF

7-3 A.C. Characteristics
System Control I/F Timing



	Symbol	MIN	TYP	MAX	Units	Conditions
CLK Cycle	Tcyc	35			ns	
CLK "H" time	Tch	16			ns	
CLK "L" time	Tcl	16			ns	

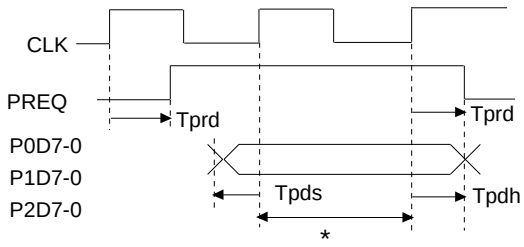
	Symbol	MIN	TYP	MAX	Units	Conditions
RESETB pulse width	Tresw	2xTcyc			ns	
PWDN pulse width	Tpwdw	2xTcyc			ns	
VSYNC pulse width	Tvsyw	2xTcyc		*1	ns	
HSYNC pulse width	Thsyw	2xTcyc		*2	ns	

	Symbol	MIN	TYP	MAX	Units	Conditions
DIR Output Delay	Tdird	3		25	ns	50pF

*1:12 x Tcyc x (HCY+1)
*2:0.5 x Tcyc x (HCY+1)
HCY is the value of interual register

Pixel I/F Timing

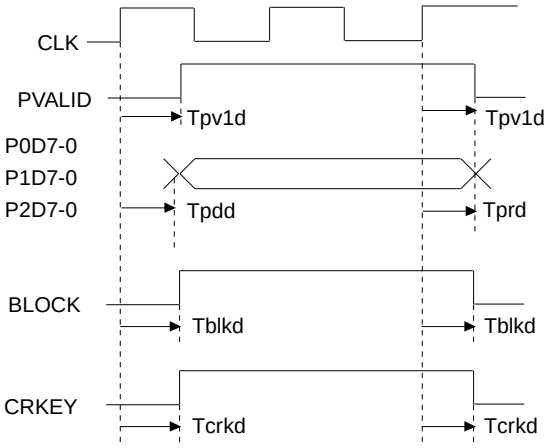
Compression



	Symbol	MIN	TYP	MAX	Units	Conditions
PREQ Output Delay	Tprd	3		22	ns	30pF
PXD Setup	Tpds	10			ns	
PXD hold	Tpdh	0			ns	

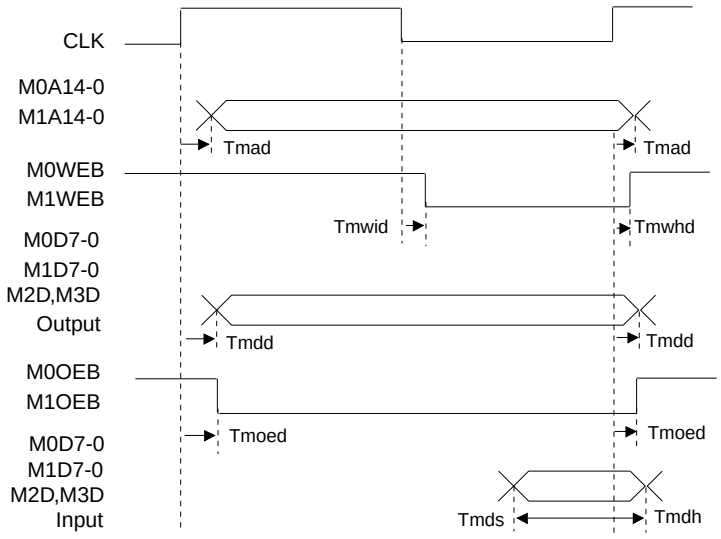
* Please do not change the Input data in this period.

Decompression



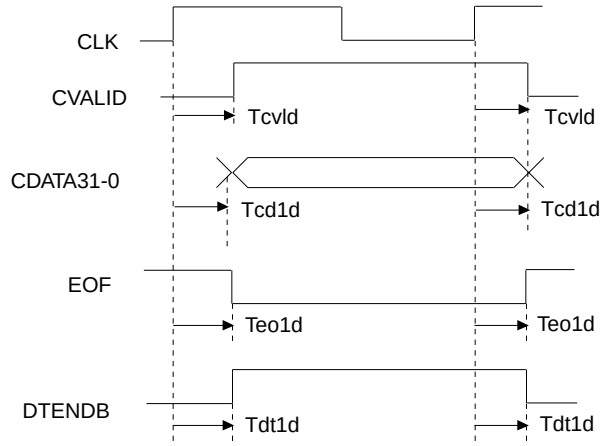
	Symbol	MIN	TYP	MAX	Units	Conditions
PVALID Output Delay	Tpv1d	3		22	ns	30pF
PXD Output Delay	Tpdd	3		22	ns	30pF
BLOCK Output Delay	Tblkd	3		22	ns	30pF
CRKEY Output Delay	Tcrkd	3		22	ns	30pF

Raster Block Convert I/F Timing



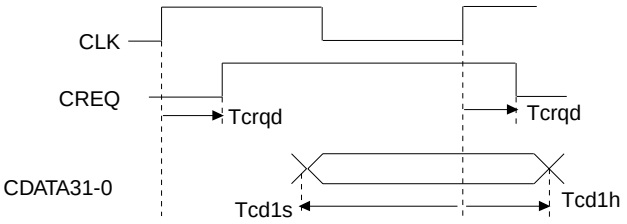
	Symbol	MIN	TYP	MAX	Units	Conditions
MAX Output Delay	Tmad	3		18	ns	30pF
MXWEB Falling Delay	Tmw1d	3		15	ns	30pF
MXWEB Rising Delay	Tmwhd	3		15	ns	30pF
MXD Output Delay	Tmdd	3		37	ns	30pF
MXOEB Output Delay	Tmoed	3		25	ns	30pF
MXD Setup	Tmds	2			ns	
MXD Hold	Tmdh	3			ns	

Compression Data I/F Timing
Compression in Synchronous Mode



Symbol	MIN	TYP	MAX	Units	Conditions	
CVALID Output Delay	Tcrld	3		22	ns	50pF
CDATA Output Delay	Tcd1d	3		22	ns	50pF
EOF Output Delay	Teo1d	3		22	ns	50pF
DTENDB Output Delay	Tdt1d	3		22	ns	50pF

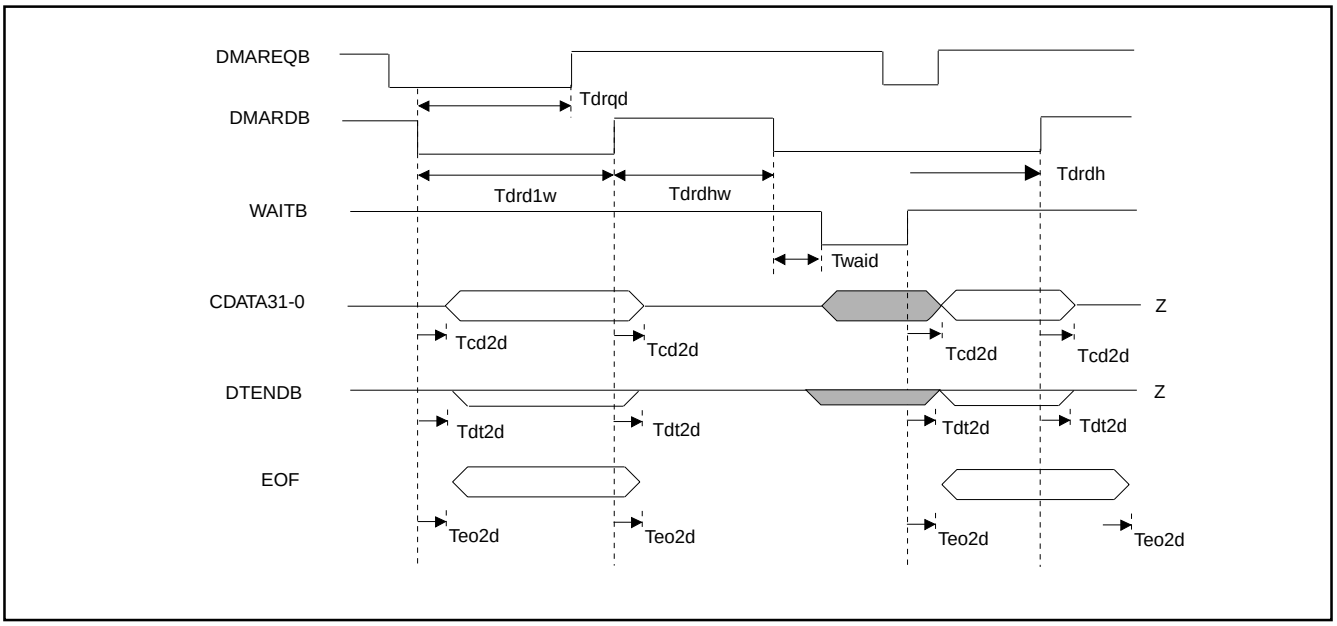
Decompression in Synchronous Mode



Symbol	MIN	TYP	MAX	Units	Conditions	
CREQ Output Delay	Tcrqd	3		50	ns	30pF
CDATA Setup	Tcd1s	10			ns	
CDATA Hold	Tcd1h	0			ns	

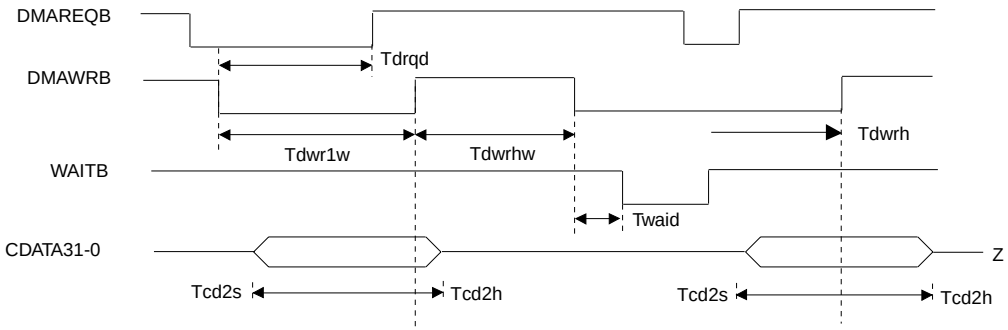
P.S:CREQ is a level signal.
Do not use edge trigger.

Compression in DMA Mode



	Symbol	MIN	TYP	MAX	Units	Conditions
DMAREQB Output Delay	Tdrqd	3		2XTcyc+22	ns	
DMARDB "L" time	Tdrdlw	2XTcyc+3			ns	
DMARDB "H" time	Tdrdhw	2XTcyc+3			ns	
DMARDB	Tdrdh	2XTcyc+3			ns	
CDTAT Output Delay	Tcd2d	3		22	ns	50pF
DTENDB Output Delay	Tdt2d	3		2XTcyc+22	ns	50pF
EOF Output Delay	Teo2d	3		22	ns	50pF
WAITB Output Delay	Twaid	3		22	ns	50pF

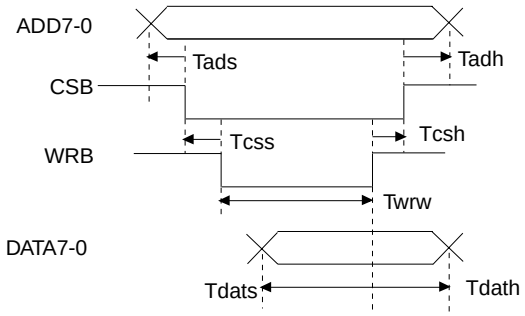
Decompression in DMA Mode



	Symbol	MIN	TYP	MAX	Units	Conditions
DMAREQB Output Delay	Tdrqd	3		2XTcyc+22	ns	50pF
DMAWRB "L" time	Tdwrlw	2XTcyc+3			ns	
DMAWRB "H" time	Tdwrhw	2XTcyc+3			ns	
DMARDB	Tdwrh	2XTcyc+3			ns	
CDTAT	Tcd2s	10			ns	
CDATA	Tcd2h	0			ns	
WAITB Output Delay	Twaid	3		22	ns	50pF

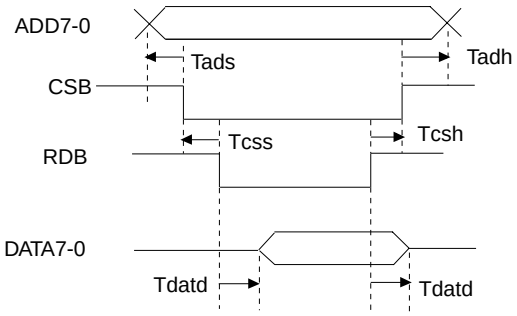
CPU I/F Timing

WRITE



	Symbol	MIN	TYP	MAX	Units	Conditions
ADD setup	Tads	0			ns	
ADD hold	Tadh	0			ns	
CSB setup	Tcss	10			ns	
CSB hold	Tcsh	0			ns	
WRB pulse width	Twrw	20			ns	
DATA setup	Tdats	20			ns	
DATA hold	Tdath	0			ns	

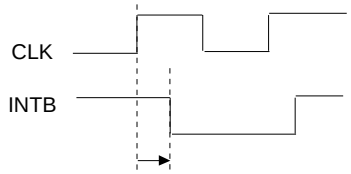
READ



	Symbol	MIN	TYP	MAX	Units	Conditions
ADD setup	Tads	0			ns	
ADD hold	Tadh	0			ns	
CSB setup	Tcss	35			ns	*1
		10			ns	*2
CBS hold	Tcsh	0			ns	
DATA Output	Tdatd	3		22	ns	50pF

*1:When Reading Quantization Table
*2:When Reading Registers which is not Quantization Table

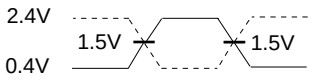
Interrupt Request



	Symbol	MIN	TYP	MAX	Units	Conditions
INTB output delay	Tintd			22	ns	50pF

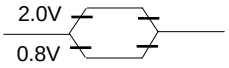
AC test condition

Input voltage timing



Tr=5ns, Tf=5ns

Output judgenent voltage

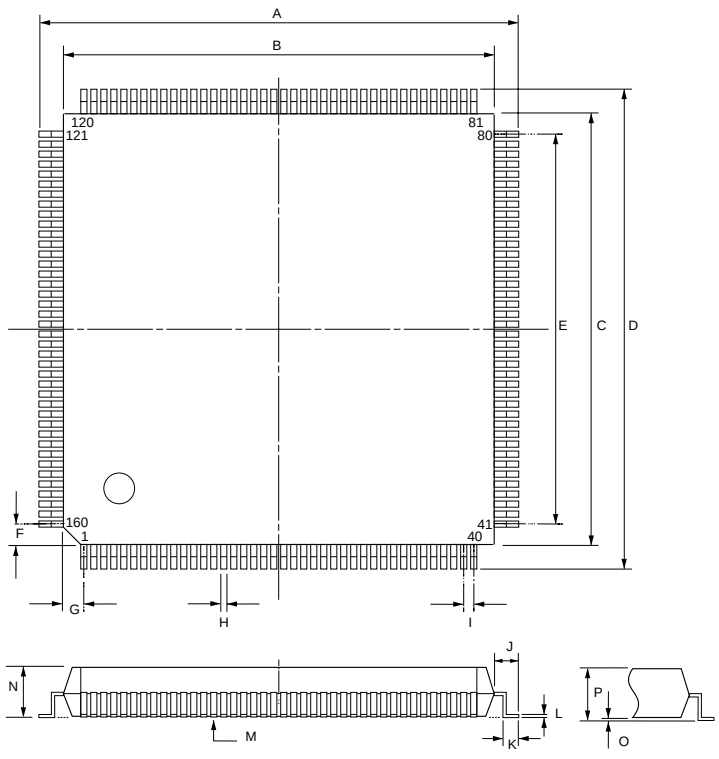


8.Package Appearance

The following figure is Package's Appearance

ITEM	MILLIMETERS	INCHES
A	31.20 ±.30	1.228 ±.012
B	28.00 ± .10	1.102 ±.004
C	28.00 ±.10	1.102 ±.004
D	31.20 ±.30	1.228 ±.012
E	25.35	.999
F	1.33 [REF.]	.052 [REF.]
G	1.33 [REF.]	.052 [REF.]
H	.30 [Typ.]	.012 [Typ.]
I	.65 [Typ.]	.026 [Typ.]
J	1.60 [REF.]	.063 [REF.]
K	.80 ± 2.0	.031 ±.008
L	.15 [Typ.]	.006 [Typ.]
M	.10 max.	.004 max.
N	3.35 max.	.132 max.
O	.10 min.	.004 min.
P	3.68 max.	.145 max.

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



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