MX8830B/MX8830R/MX8830X
Synchronous Buck MOSFET Driver

Features:

- Logic Level Gate Drive Compatible
- 1A Source, 1A Sink Peak Drive Current
- Programmable High-Side Driver Turn-on Delay
- Supports Floating Voltage for Top Driver Up to 24V
- MX8830B/MX8803R/MX8830X: Undervoltage Lockout
- MX8830R/MX8830X: Output Shutdown, Low Side Shutdown Inputs
- 10µA Shut Down Current
- 2mA Quiescent Current (Non- Switching)
- Bootstrapped High Side Driver
- Cross-Conduction Protection

Applications:

- Multiphase Desktop CPU Supplies
- Mobile CPU Core Voltage supplies
- High Current / Low Voltage DC/DC Synchronous Buck Converters

General Description

The MX8830 family are 1A Source / 1A Sink Synchronous Buck MOSFET Drivers. These Synchronous Buck MOSFET Drivers are specifically designed to drive two N-channel power MOSFETs in a synchronous buck converter. The High-Side driver is powered via a bootstrapped power connection. The driver is capable of 13ns High-Side output, and 12ns Low-Side output transition times driving a 3000pF load.

The MX8830B, MX8830R, and MX8830X incorporate an undervoltage lockout to prevent unintentional gate drive output during low voltage conditions. The MX8830R/X include External Shutdown, and the MX8830X Low-Side Drive Shutdown features. Simultaneous shutdown of both outputs prevents rapid output capacitor discharge. The high-side turn-on delay is adjustable with an external capacitor added at the DLY pin.

The MX8830B/MX8830R/MX8830X are designed to operate over a temperature range of -40°C to +85°C. The MX8830B is available in an 8-Lead SOIC, and the MX8830R in a 10-lead DFN.

Figure 1. MX8830B Functional Block Diagram and General Application Circuit

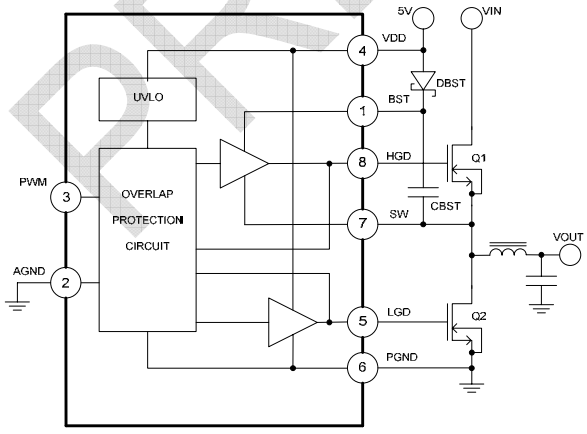


Figure 2. MX8830R Functional Block Diagram and General Application Circuit

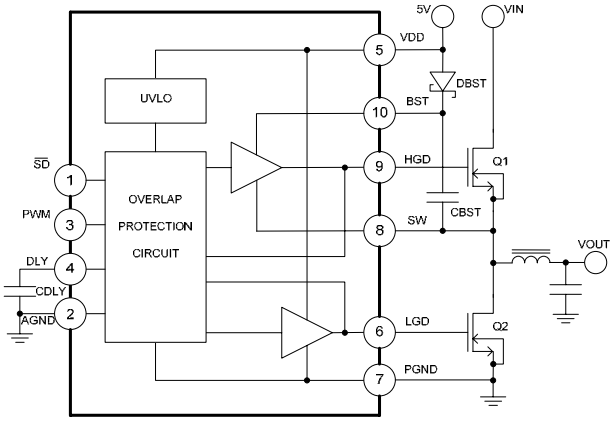
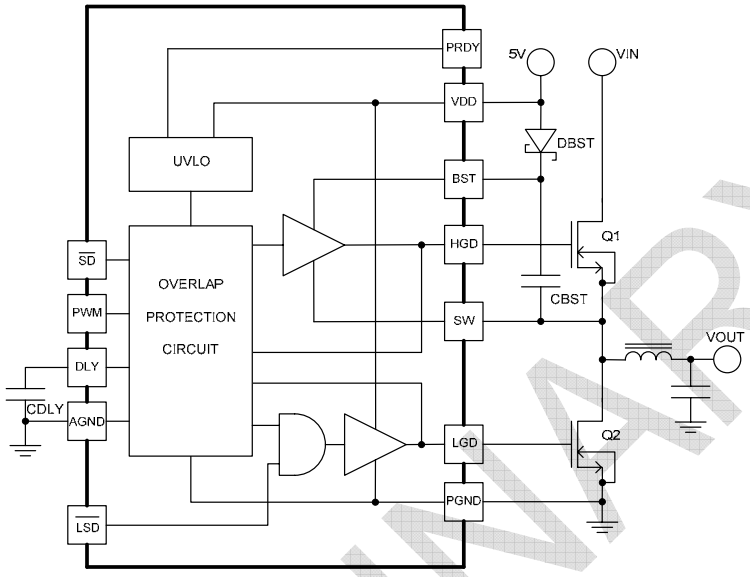


Figure 3. MX8830X Functional Block Diagram and General Application Circuit



Ordering Information

Part No.	Description	Package	Pack Quantity
MX8830B	Under Voltage Lockout	SOIC-8	98 (Tube)
MX8830BTR	Under Voltage Lockout	SOIC-8	2500 (Tape&Reel)
MX8830R10	Under Voltage Lockout , Power Down, External Delay Cap	DFN-10	121 (Tube)
MX8830R10TR	Under Voltage Lockout , Power Down, External Delay Cap	DFN-10	2000 (Tape&Reel)
MX8830X	UVLO , Power Ready, Power Down, Low Side Shutdown, Ext Dly Cap	Die	Waffle Pack

Absolute Maximum Ratings

Parameter	Rating
V_{DD}	-0.3V to +7V
BST	-0.3V to +30V
BST to SW	-0.3V to +7V
SW	-0.2V to +24V
PWM	-0.3V to +7V
Operating Ambient Temp Range	-40°C to +85°C
Operating Junction Temp Range	-40°C to +125°C
θJA	150°C/W
θJC	40°C/W
Storage Temp Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

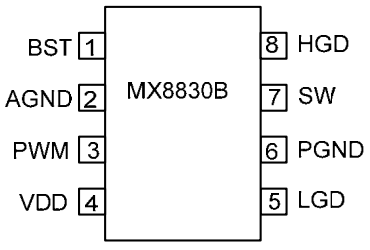
ESD Warning

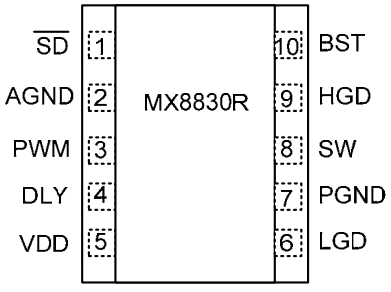
ESD (electrostatic discharge) sensitive device. Although the MX8830B/MX8830R/MX8830X feature proprietary ESD protection circuitry, permanent damage may be sustained if subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Lead / Signal Description and Configurations

MX8830B	MX8830R	MX8830X	Name	Description
1	10	Bonding Pad	BST	Upper Gate Driver Floating DC Power Terminal for Bootstrap Capacitor Connection.
2	2	Bonding Pad	AGND	Analog Ground
3	3	Bonding Pad	PWM	Three State PWM Input. PWM input to the Gate Drivers.
4	5	Bonding Pad	VDD	Positive Supply Terminal for Logic and Lower Gate Driver. A ceramic bypass capacitor of 1uF should be connected from VDD to PGND.
5	6	Bonding Pad	LGD	Lower Gate Driver Output Terminal
6	7	Bonding Pad	PGND	Lower Gate Driver DC Power Return Terminal
7	8	Bonding Pad	SW	Upper Gate Driver Floating DC Power Return Terminal
8	9	Bonding Pad	HGD	Upper Gate Driver Output Terminal
N/A	4	Bonding Pad	DLY	Terminal for External Delay Capacitor Connection. Capacitor to Ground at this pin adds propagation delay from Lower Gate Driver going Low to the Upper Gate Driver going High. t_{DLY} (nS) = C_{DLY} (pF) x (0.5nS/pF)
N/A	1	Bonding Pad	$\overline{SD}$	TTL-level Shut Down Input Signal with active pull-up. $\overline{SD}$ enables normal operation when high. When $\overline{SD}$ is low, the driver outputs are forced low and I_{DD} is at its minimum.
N/A	N/A	Bonding Pad	$\overline{LSD}$	TTL-level Low Side Shut Down Input Signal with active pull-up. $\overline{LSD}$, when low forces the Lower Gate Driver output low. When $\overline{LSD}$ is high, the lower Gate Driver output is enabled.
N/A	N/A	Bonding Pad	PRDY	Power Good Output Terminal. Logic high at this terminal indicates VDD is above the UVLO Threshold.

SOIC and DFN Top View Lead Configurations





Electrical Characteristics

Power Supply Terminals

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Analog Supply Voltage Range	V_{DD}	V_{DD}		4.5		5.5	V
High Gate Driver Supply Voltage Range		V_{BST} - V_{SW}		4.5		5.5	V
Low Gate Driver Supply Voltage Range		V_{DD} - V_{PGND}		4.5		5.5	V
Floating Supply Voltage Range		V_{SW} - V_{PGDN}		0.0		24.0	V
Analog Supply Current	I_{DD}	Normal Mode PWM = V_{PGND}			2	4	mA
High Gate Driver Supply Current	I_{BST}	Normal Mode PWM = V_{PGND}			0.5	1	mA
Analog Supply Current	$I_{DD\_Shutdown}$	Shut Down Mode, $\overline{LSD}$ = V_{DD}, $\overline{SD}$ = PWM = V_{PGND}			10		µA
High Gate Driver Supply Current	$I_{BST\_Shutdown}$	Shut Down Mode $\overline{LSD}$ = PWM = V_{PGND}			<1	10	µA

Digital Input Terminals

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{IN}	$\overline{LSD}$ = $\overline{SD}$ = V_{DD}	-1		1	µA
Input pull-down Current			2	10	100	µA
Input pull-up Current		$\overline{SD}$ = V_{PGND}	-2	-10	-100	µA
Input pull-up Current		$\overline{LSD}$ = V_{PGND}	-2	-10	-100	µA
Minimum High Level Input Voltage	V_{IH}		2.0			V
Maximum Low Level Input Voltage	V_{IL}				0.8	V

PWM Input

(See Timing Diagram)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Current	I_{PWM}	V_{PWM} = 5V		250		µA
		V_{PWM} = 0V		-250		µA
PWM Rising Threshold		V_{DD} = 5V		3.7		V
PWM Falling Threshold		V_{DD} = 5V		1.3		V
Typical Three-State Shutdown Window			1.5		3.6	V

UVLO Circuit

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{DD} Rising Threshold	$UVOL_{RISE}$		4.2	4.4	4.5	V
V_{DD} Falling Threshold	$UVOL_{FALL}$		3.9	4.25	4.5	V
PRDY Source Current	$PRDY_{SOURCE}$	V_{DD} -100mV		10		mA
PRDY Sink Current	$PRDY_{SINK}$	V_{SS} + 200mV		5		mA

Delay Circuit

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Upper Gate-Driver Turn on Delay Time with respect to external delay capacitor	t_{DLY}	Capacitor C_{DLY}(pF) from DLY pin to PGND		0.5		nS/pF

High Side Gate Driver Circuit

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Side Gate-Driver On-Resistance, Sourcing Current	R_{HGD_SRC}	$V_{BST} - V_{SW}$ = 4.6V			2.2	Ω
High Side Gate-Driver On-Resistance, Sinking Current	R_{HGD_SNK}	$V_{BST} - V_{SW}$ = 4.6V			1.2	Ω
High Side Gate-Driver(1) Rise-Time	t_{R_HGD}	C_{LOAD} = 3nF T_{R_HGD} measured from 10% to 90% of (V_{HGD} - V_{SW})		13	20	nS
High Side Gate-Driver(1) Fall-Time	t_{F_HGD}	C_{LOAD} = 3nF T_{F_HGD} measured from 90% to 10% of (V_{HGD} - V_{SW})		10	15	nS
High Side Gate-Driver(1) Source Current	I_{SOURCE}	C_{LOAD} = 3nF T_{R_HGD} measured from 10% to 90% of (V_{HGD} - V_{SW})	0.6	0.9		A
High Side Gate-Driver(1) Sink Current	I_{SINK}	C_{LOAD} = 3nF T_{F_HGD} measured from 90% to 10% of (V_{HGD} - V_{SW})	0.8	1.2		A
Propagation Delay(1)	t_{PD_HGD1} t_{PD_HGD2}	C_{LOAD_HGD} = C_{LOAD_LGD} = 3nF C_{DLY} = 0pF			35 50	nS nS

Low Side Gate Driver Circuit

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low Side Gate-Driver On-Resistance, Sourcing Current	R_{LGD_SRC}	$V_{DD} – V_{PGND}$ = 4.6V			2	Ω
Low Side Gate-Driver On-Resistance, Sinking Current	R_{LGD_SNK}	$V_{DD} – V_{PGND}$ = 4.6V			1	Ω
Low Side Gate-Driver(1) Rise-Time	t_{R_LGD}	C_{LOAD} = 3nF T_{R_LGD} measured from 10% to 90% of ($V_{LGD} – V_{PGND}$)		12	18	nS
Low Side Gate-Driver(1) Fall-Time	t_{F_LGD}	C_{LOAD} = 3nF T_{F_LGD} measured from 90% to 10% of (V_{LGD} - V_{SW})		9	12	nS
Low Side Gate-Driver(1) Source Current	ISOURCE	C_{LOAD} = 3nF T_{R_LGD} measured from 10% to 90% of ($V_{LGD} – V_{PGND}$)	0.67	1.0		A
Low Side Gate-Driver(1) Sink Current	ISINK	C_{LOAD} = 3nF T_{F_LGD} measured from 90% to 10% of (V_{LGD} - V_{SW})	1.0	1.3		A
Propagation Delay(1)	t_{PD_LGD1} t_{PD_LGD2}	C_{LOAD_HGD} = C_{LOAD_LGD} = 3nF C_{DLY} = 0pF			60 20	nS nS

Shut Down Circuit Characteristics

T_A = -40°C to 85°C, V_{DD} = 5V, 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Propagation Delay(2)	t_{PD_LGDSD1}			25		nS
Propagation Delay(2)	t_{PD_LGDSD2}			10		nS
Propagation Delay(3)	t_{PD_GDSD1}			400		nS
Propagation Delay(3)	t_{PD_GDSD2}			800		nS
PWM Tri-State	T_{pd_tri1}	Turn On Delay		500		nS
PWM Tri-State	T_{pd_tri2}	Turn Off Delay		500		nS

*Notes:
(1) See Timing Diagram in Figure 4
(2) See Timing Diagram in Figure 5
(3) See Timing Diagram in Figure 6

Figure 4. Non-Overlap Timing Diagram for MX8830B/8830B/8830X

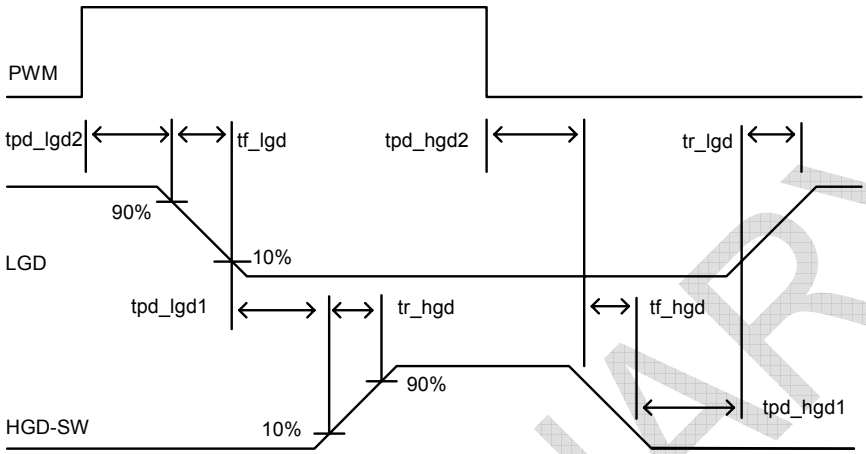


Figure 5. $\overline{\text{LSD}}$ Propagation Delay Timing for MX8830R/X

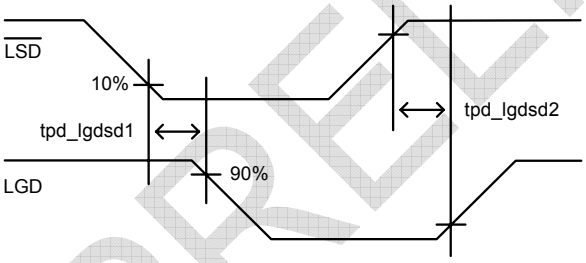
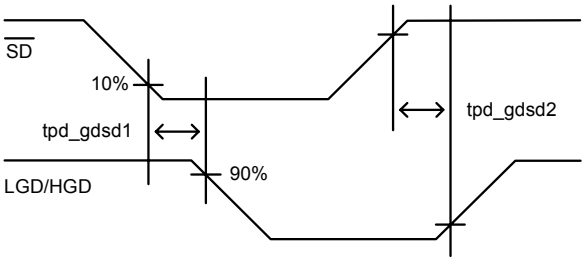
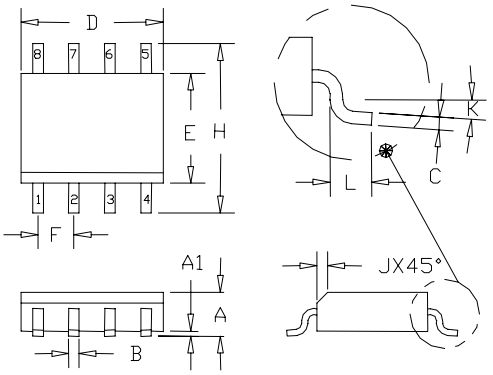


Figure 6. $\overline{\text{SD}}$ Propagation Delay Timing for MX8830R/X



Package Outlines

SOIC – 8



DIM.	DIMENSIONS (1) INCH MIN.	INCH MAX.	MM. MIN.	MM. MAX.	NOTE
A	.0532	.0688	1.35	1.75	----
A1	.0040	.0098	.10	.25	----
B	.013	.020	.33	.51	----
C	.0075	.0098	.19	.25	----
D	.1890	.1968	4.80	5.00	(2)
E	.1497	.1574	3.80	4.00	(2)
F	.050 BSC		1.27 BSC		----
H	.2284	.2440	5.80	6.20	----
J	.0099	.0196	.25	.50	----
K	0°	8°	0°	8°	----
L	.016	.050	.40	1.27	----

3. MOLDED PACKAGE SHALL CONFORM TO JEDEC STANDARD CONFIGURATION MS-012 VARIATION AA.

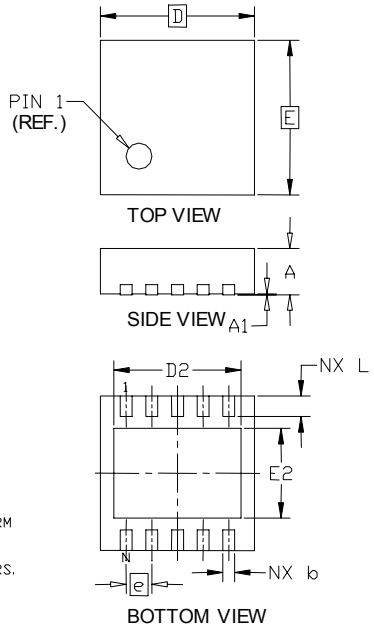
(2) DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

NOTES: (UNLESS OTHERWISE SPECIFIED)

DFN – 10

DIM.	DIMENSIONS (1) INCH MIN.	INCH MAX.	MM. MIN.	MM. MAX.
A	.0315	.0394	.80	1.00
A1	0	.0020	0	.05
b	.007	.012	.18	.30
D	.118 BSC		3.00 BSC	
D2	.0866	.1063	2.20	2.70
E	.118 BSC		3.00 BSC	
E2	.055	.069	1.40	1.75
e	.0197 BSC		.50 BSC	
L	.0118	.0197	.30	.50
N	10		10	



3. MOLDED PACKAGE SHALL CONFORM TO JEDEC STANDARD CONFIGURATION MO-229 VARIATION VEED-5.

2. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5M-1994.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

NOTES: (UNLESS OTHERWISE SPECIFIED)

Theory of Operation

The MX8830 family are dual MOSFET drivers, designed to drive two external N-channel power MOSFETs. The low-side driver is designed to drive a non-floating N-channel power MOSFET and its output is out of phase with the PWM input. The high-side driver is designed to drive a floating N-channel power MOSFET and its output is in phase with the PWM input. An external bootstrap circuit provides the floating power supply to the high-side driver.

The bootstrap circuit consists of a Schottky diode and a boost capacitor. When the PWM input transitions to a logic low, the low-side power MOSFET turns ON, the SW node is pulled to ground, and the bootstrap capacitor is charged to VDD through the Schottky diode. When the PWM transitions to a logic high, the high side power MOSFET begins to turn on and the SW node rises up to the input supply, VIN. In turn the boost capacitor raises the BST node voltage to a level equal to the input supply plus the boost capacitor voltage, providing sufficient voltage to the BST node to turn on the High-Side Power MOSFET. An internal cross-conduction prevention circuit monitors both gate driver outputs and allows each driver output to turn ON only when the other output driver turns OFF and falls below 1V.

Three-State PWM Input

A unique feature of these drivers and other Micronix drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the driver outputs are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the Electrical Specifications determine when the lower and upper gates are enabled.

This feature helps prevent a negative transient on the output voltage when the output is shut down, eliminating the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

Detailed Circuit Description

(Refer to the Application Diagrams)

The PMW input signal controls both the High Side and Low Side power MOSFET drivers. The Power MOSFETs are driven so that the SW node follows the polarity of the PWM signal.

Low-Side Gate Driver

The Low-Side Gate Driver is designed to drive a ground referenced N-Channel Power MOSFET. In a synchronous buck converter application, it drives the gate of the synchronous rectifier FET, (Q2). When the driver is enabled, (MX8830R/X SD=LSD=VDD), the driver output is 180˚ out of phase with the PWM input. The internal overlap protection circuit monitors the High-Side Gate Driver, and allows the Low-Side Gate Driver to turn on only when the High-Side Gate Driver output falls below 1.0 Volt. The supply rails for the Low-Side Gate Driver are VDD and PGND.

High-Side Gate Driver

The High-Side Gate Driver is designed to drive a floating N-Channel Power MOSFET referenced to SW. In a synchronous buck converter application, it drives the gate of the high side power MOSFET, (Q1). When the driver is enabled (MX8830R/X SD=VDD), the driver output is in phase with the PWM input. The bootstrap supply rails for the High-Side Gate Driver are BST and SW, and are generated by an external bootstrap circuit. The bootstrap circuit consists of a Schottky diode DBST, and a bootstrap capacitor CBST. During start up, the SW pin is at ground and the bootstrap capacitor CBST charges up to VDD through the Schottky diode DBST. When the PWM input transitions high the High-Side Gate Driver begins to turn Q1 ON by transferring charge from the bootstrap capacitor CBST to the gate of Q1. As Q1 turns on the SW pin will rise up to VIN, forcing the BST pin to VIN + VBOOSTCAP. This supplies the required gate to source voltage to Q1. When PWM transitions low the High-Side Driver and in turn Q1 switch off. When SW falls below 1 Volt the Low-Side Gate Driver turns on and recharges the bootstrap capacitor which completes the cycle.

Overlap Protection Circuit

The overlap protection circuit (OPC) monitors the High Side and Low Side Gate Driver Outputs and prevents both main power switches, Q1 and Q2, from being ON at the same time. This inhibits excessive shoot-through currents and minimizes the associated losses.

When the PWM input transitions low, Q1 begins to turn OFF, and Q2 turns ON only when the High-Side Gate Driver output falls below 1 volt. By waiting for the voltage on the High Side Gate Driver Output pin to reach 1 volt, the overlap protection circuit ensures that Q1 is OFF before Q2 turns on.

Similarly, when the PWM input transitions high, Q2 begins to turn OFF, and Q1 turns ON after the overlap protection circuit detects that the voltage at the Low-Side Gate Driver output has dropped below 1 volt. Once the driver output voltage falls below 1 volt, the overlap protection circuit initiates a delay timer that adds additional delay set by the external capacitor connected to the DLY pin. This programmable delay circuit allows adjustments to optimize performance based on the switching characteristics of the external power MOSFET.

Additionally, after PWM input transitions low and if SW node voltage does not fall below the non-overlap protection circuit threshold within 100nS, the low side driver turns ON automatically.

Low-Side Driver Shutdown

The MX8830R/X include a Low-Side Gate Driver shutdown feature. A logic low signal at the LSD input shuts down the Low Side Gate Driver, and in turn the synchronous rectifier FET. This signal can be used to achieve maximum battery life under light load conditions and maximum efficiency under heavy load conditions. Under heavy load conditions, LSD should be high so that the synchronous switch is controlled by the PWM signal for maximum efficiency. Under light load conditions the LSD can be low to disable the Low Side Gate Driver so the switching current can be minimized.

Shutdown

For optimal system power management, the MX8830R/X drivers can be shut down to conserve power. When the SD pin is high, the MX8830R/X are enabled for normal operation. Pulling the SD pin low forces the HGD and LGD outputs low, and reduces the supply current by disabling the internal reference.

Under Voltage Lockout

The Under Voltage Lockout (UVLO) circuit holds both driver outputs low during VDD supply ramp-up. The UVLO logic becomes active and in control of the driver outputs at a supply voltage of no greater than 1.5 V. When the supply voltage rises above the UVLO upper threshold the circuit allows the PWM input to control the drivers.

Application Information

Supply Capacitor Selection

A 1 uF ceramic bypass capacitor is recommended for the VDD input to provide noise suppression. The bypass capacitor should be located as close as possible to MX8830.

Bootstrap Circuit

The bootstrap circuit requires a charge storage capacitor CBST and a Schottky diode DBST, as shown in Figure 1. Selecting these components should be done with consideration of the electrical characteristics of the high-side FET chosen.

The bootstrap capacitor voltage rating must exceed the maximum input voltage, (VIN) + the maximum VDD voltage. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

Where, QGATE is the total gate charge of Q1, and ΔVBST is the allowable Q1 voltage droop.

To maximize the available drive for Q1 in the bootstrap circuit a Schottky diode is recommended. The bootstrap diode voltage rating must exceed the maximum input voltage, (VIN) + the maximum VDD voltage. The average forward current can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times F_{MAX}$$

where F_{MAX} is the maximum PWM input switching frequency. Peak surge current is dependent on the source impedance of the 5V supply and the ESR of CBST, and should be checked in-circuit.

Delay Capacitor Selection
A ceramic capacitor is recommended for the DLY input, and should be located as close a possible to the DLY pin.

Printed Circuit Board Layout Considerations
Use the following general guidelines when designing printed circuit boards:

1. Trace out the high current paths and use short, wide traces to make these connections.
2. Locate the VDD bypass capacitor as close as possible to the VDD and PGND pins.
3. Connect the source of the Lower MOSFET, (Q2) as close as possible the PGND.

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