EPSON

S1F78520

Charge-pump Step Down Regulator with Power Saving Mode

■ DESCRIPTION

The S1F78520 is a power IC which can generate two stabilized output voltages of 3.3 V (or 2.9 V or 2.5 V) and 2.5 V (or 2.0 V or 1.8 V) using the Li-ion battery. The 3.3 V range output is being generated through the LDO (series regulator). The 2.5 V range output is being generated through the charge pump type DC/DC converter consisting of built-in CMOS transistors. Since the voltages are being stabilized by adjustments of the charge pump DC/DC switching frequencies, higher conversion efficiencies as compared with the conventional series regulators can be acquired. Since the S1F78520 does not require external transistors, coils nor diodes, it is most suitable for the down sizing purpose and for reduction of the current consumption.

■ FEATURES

- Supply voltage ····· 3.6 V (2.7 V to 5.5 V) single power input
- Voltage conversion method ····· ① LDO (series regulator)
  ② Voltage dropping type charge pump
- Output voltages ····· ① 3.3 V or 2.9 V or 2.5 V ± 3%
  ② 2.5 V or 2.0 V or 1.8 V ± 4%
  (output voltage is external pin setting)
- Output current (Normal state/Standby state) ····· ① Max. (100 mA/1 mA)
  ② Max. (80 mA/100 µA)
- Conversion efficiency ····· ① 90% (the conversion from 3.6V to 3.3V)
  ② 85% (peak efficiency)
- Shut down current ····· µA· 1
- Self-consumption current ····· µA 75 (under no load state)
- Built-in self-consumption current suppressing function by use of standby (light load) signals
  Self-consumption current ····· µA 25 (under no load state)
- Output voltage② switching frequency ····· 450kHz
- Built-in power good detector (equipped with the delay setting function)
- Built-in low voltage detecting circuit (For setting of the detecting voltages, either of the internal setting fixed to the IC or the external pin setting is selectable.)
- Shipping state ····· SSOP3–24pin
- This IC is not of the radiation resistant design nor of the light resistance design.

■ BLOCK DIAGRAM

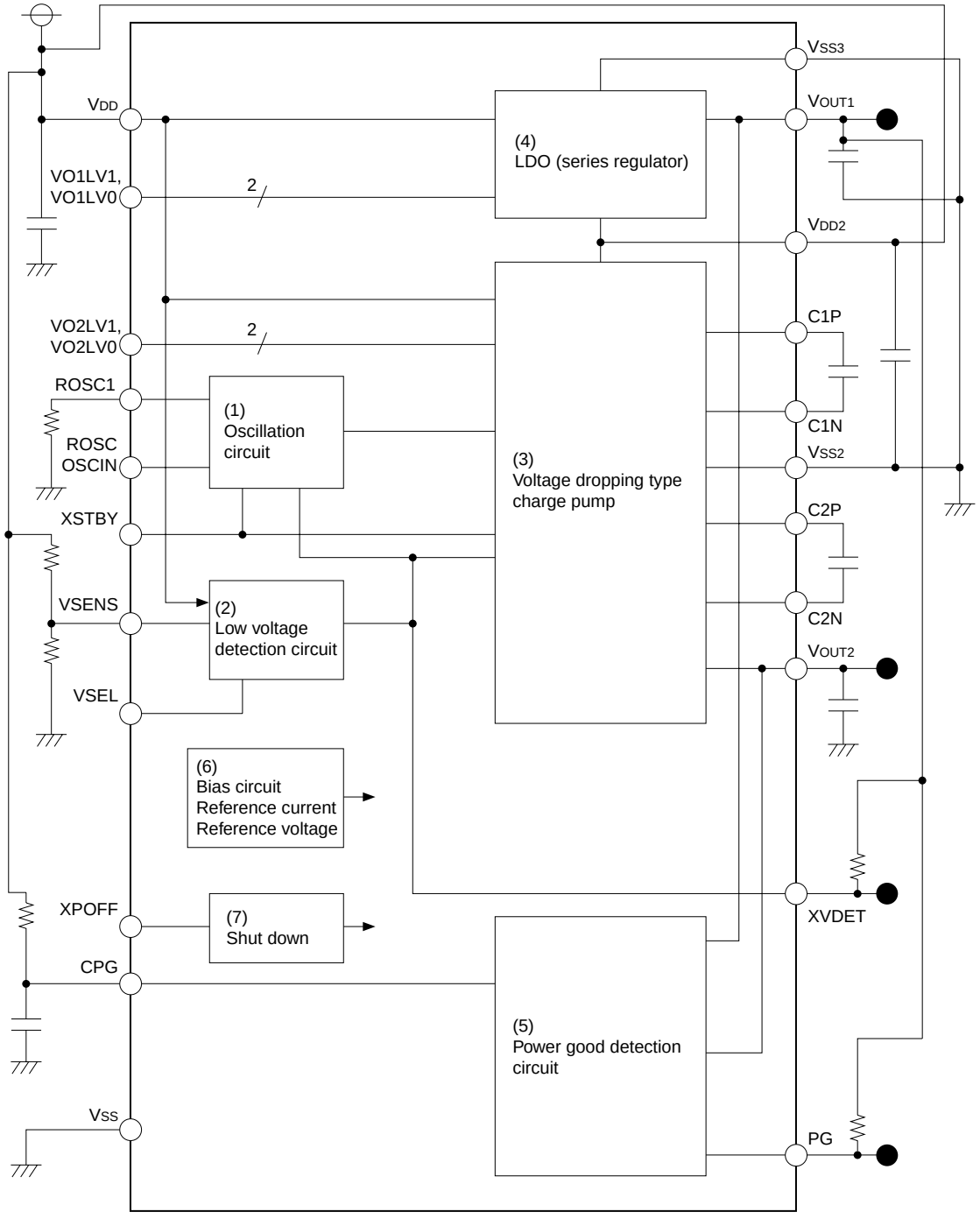


Fig. 1 Block diagram

■ DESCRIPTIONS FOR THE BLOCK DIAGRAM

(1) Oscillation circuit
This is the circuit to make oscillations by connecting a resistance to the ROSC1 pin and by supplying a constant current.

(2) Low voltage detection circuit
This circuit makes low voltage detections by monitoring the input voltage through the V_{DD} pin. Provision of a hysteresis width is effective to prevent occurrences of unstable outputs (causing oscillations) while performing low voltage detecting operations. For setting of the detecting voltages, use of either of the internal voltage setting fixed to the IC or the external voltage setting pin VSENS is selectable through the VSEL pin.

(3) Voltage dropping type charge pump
The specified voltage is being output by voltage drops effected by the charge pump upon the inputted supply voltage V_{DD}∗ - V_{SS}∗ and using the V_{SS}∗ potential as the reference voltage. The specified voltage is selectable (2.5 V or 2.0 V or 1.8 V) through the external pins VO2LV1, VO2LV0.
Also, the voltages are being stabilized by adjusting the switching frequencies of the charge pump. This circuit can drastically suppress the current consumption under the standby mode (light load).

(4) LDO (series regulator)
It stabilizes the voltage of the levels below the input supply voltage. The specified voltage is selectable (3.3 V or 2.9 V or 2.5 V) through the external pins VO1LV1, VO1LV0.

(5) Power good detection circuit
This circuit detects the power good signals when the output pins V_{OUT1} and V_{OUT2} are satisfying the specified voltage. Delay setting can be made for the power good signals by connecting a capacitor and a resistor to the external setting pin CPG.

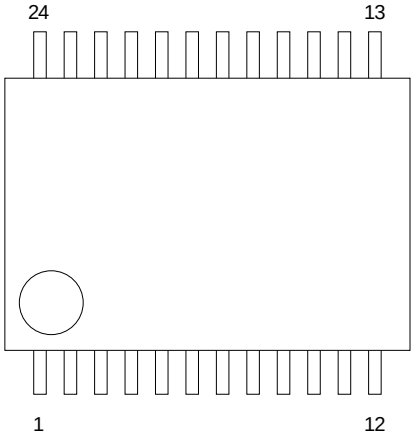
(6) Bias circuit
This circuit generates the reference voltage and reference current which are necessary for this IC.

(7) Shut down
Operations of all the circuits can be interrupted by setting the shut down pin XPOFF to the V_{SS}∗ level.

<Note> V_{DD}∗ = V_{DD}, V_{DD2}, V_{SS}∗ = V_{SS}, V_{SS2}, V_{SS3}

■ PIN ASSIGNMENT

SSOP3–24pin S1F78520M0A01



Pin No.	Pin name	Pin No.	Pin name
1	XPOFF	13	XVDET
2	VO2LV1	14	VSENS
3	VO2LV0	15	V_{DD}
4	C1N	16	VSEL
5	C1P	17	V_{SS3}
6	V_{OUT2}	18	V_{OUT1}
7	PG	19	V_{DD2}
8	CPG	20	C2P
9	ROSC1	21	C2N
10	V_{SS}	22	VO1LV0
11	OSCIN	23	VO1LV1
12	XSTBY	24	V_{SS2}

■ PIN DESCRIPTION

(1) Function pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>VO1LV1</td><td>I</td><td>23</td><td rowspan="2">VOUT1 Output voltage level designating pin.
<table>
<tr><th colspan="2">Pin setting</th><th rowspan="2">Output voltage</th></tr>
<tr><th>VO1LV1</th><th>VO1LV0</th></tr>
<tr><td>VSS∗ level</td><td>VSS∗ level</td><td>3.3V</td></tr>
<tr><td>VSS∗ level</td><td>VDD∗ level</td><td>2.9V</td></tr>
<tr><td>VDD∗ level</td><td>VSS∗ level</td><td>2.5V</td></tr>
<tr><td>VDD∗ level</td><td>VDD∗ level</td><td>Not for use</td></tr>
</table></td></tr>
<tr><td>VO1LV0</td><td>I</td><td>22</td></tr>
<tr><td>VO2LV1</td><td>I</td><td>2</td><td rowspan="2">VOUT2 Output voltage level designating pin.
<table>
<tr><th colspan="2">Pin setting</th><th rowspan="2">Output voltage</th></tr>
<tr><th>VO2LV1</th><th>VO2LV0</th></tr>
<tr><td>VSS∗ level</td><td>VSS∗ level</td><td>2.5V</td></tr>
<tr><td>VSS∗ level</td><td>VDD∗ level</td><td>2.0V</td></tr>
<tr><td>VDD∗ level</td><td>VSS∗ level</td><td>1.8V</td></tr>
<tr><td>VDD∗ level</td><td>VDD∗ level</td><td>Not for use</td></tr>
</table></td></tr>
<tr><td>VO2LV0</td><td>I</td><td>3</td></tr>
<tr><td>ROSC1</td><td>O</td><td>9</td><td>Pin to connect the external resistor for adjustment of the oscillating current.</td></tr>
<tr><td>XSTBY</td><td>I</td><td>12</td><td>This is the standby pin. Under the standby mode (light load), the internal structure of the IC can be operated by low current consumption when this signal is set to the VSS∗ level.</td></tr>
<tr><td>VSENS</td><td>I</td><td>14</td><td>Detecting voltage inputting pin for the low voltage detection circuit. This is effective only when the eternal setting is being selected.</td></tr>
<tr><td>VSEL</td><td>I</td><td>16</td><td>Detecting voltage selecting pin for the low voltage detection circuit.
The detecting voltage inputting pin VSENS becomes valid when this pin is set to the VSS∗ level. The detection voltage generated inside the IC becomes valid when this pin is set to the VDD∗ level.</td></tr>
<tr><td>XPOFF</td><td>I</td><td>1</td><td>This is the shut down pin. Set this pin to the VDD∗ level while the IC is in operation. Operations of all the circuits will be interrupted when this signal is set to the VSS∗ level, bringing the IC into the shut down state and making the output pins XVDET, PG to open state.</td></tr>
<tr><td>CPG</td><td>I</td><td>8</td><td>Delay time setting pin for the power good signals.</td></tr>
<tr><td>C1P</td><td>O</td><td>5</td><td>Positive side connection pin for the flying capacitor C1 for generation of the VOUT2 output voltage.</td></tr>
<tr><td>C1N</td><td>O</td><td>4</td><td>Negative side connection pin for the flying capacitor C1 for generation of the VOUT2 output voltage.</td></tr>
<tr><td>C2P</td><td>O</td><td>20</td><td>Positive side connection pin for the flying capacitor C2 for generation of the VOUT2 output voltage.</td></tr>
<tr><td>C2N</td><td>O</td><td>21</td><td>Negative side connection pin for the flying capacitor C2 for generation of the VOUT2 output voltage.</td></tr>
<tr><td>XVDET</td><td>O</td><td>13</td><td>This is the detection result output pin for the low voltage detection circuit. The output state is Nch open drain.
It outputs the VSS∗ level when the input power pin VDD is at the low voltage level.</td></tr>
<tr><td>PG</td><td>O</td><td>7</td><td>This is the power good signal pin for the output power pins VOUT1 and VOUT2. The output state is Nch open drain.
It goes open when both of the above output power pins are satisfying the specified voltage.</td></tr>
</table>

(2) Power pins

Pin name	I/O	Pin No.	Function
V_{DD}	I	15	Positive side input power pin.
V_{DD2}	I	19	Positive side input power pin.
V_{SS}	I	10	Negative side input power pin.
V_{SS2}	I	24	Negative side input power pin.
V_{SS3}	I	17	Negative side input power pin.
V_{OUT1}	O	18	LDO (series regulator) output power pin.
V_{OUT2}	O	6	Voltage dropping type charge pump output power pin.

<Note 1> Connect the V_{DD} and V_{DD2} each other externally and keep them at the same potential level.
<Note 2> Connect the V_{SS} < V_{SS2} and V_{SS3} each other externally and keep them at the same potential level.

(3) Testing pin

Pin name	I/O	Pin No.	Function
OSCIN	I	11	V_{DD}* level is normally fixed or open.

■ FUNCTIONAL DESCRIPTION

● Operational description

S1F78520 is a power supply IC which generates two output voltages, 3.3V (or 2.9V or 2.5V) and 2.5V (or 2.0V or 1.8V), stabilized from Li-ion batteries. High conversion efficiencies can be aquired under heavy loads by standby input signal. While low consuming current operations can be realized under light load state.

Generating voltage levels are:

- LDO (series regulator) output voltage [3.3 V or 2.9 V or 2.5 V]*1 (V_{OUT1})
- Voltage dropping type charge pump output voltage [2.5 V or 2.0 V or 1.8 V]*2 (V_{OUT2})

*1: Selection of 3.3 V or 2.9 V or 2.5 V is to be designated by use of the external pins VO1LV1, VO1LV0.
*2: Selection of 2.5 V or 2.0 V or 1.8 V is to be designated by use of the external pins VO2LV1, VO2LV0.

The V_{OUT1} output voltage is being generated by stabilizing the potential difference occurring between "V_{DD}∗ – V_{SS}∗" using the V_{SS}∗ potential as the reference voltage.

While the V_{OUT2} voltage is being generated after selection of the optimum voltage dropping ratio among different voltage dropping ratios for the voltage dropping type charge pump to let it work on the potential difference occurring between "V_{DD}∗ – V_{SS}∗" using the V_{SS}∗ potential as the reference voltage and stabilizing the voltage by fine adjustments of the switching frequencies. Since an extra voltage stabilizing circuit is not being used for the output, high conversion efficiencies can be acquired.

Indicated below is the system configuration diagram for the power circuit.

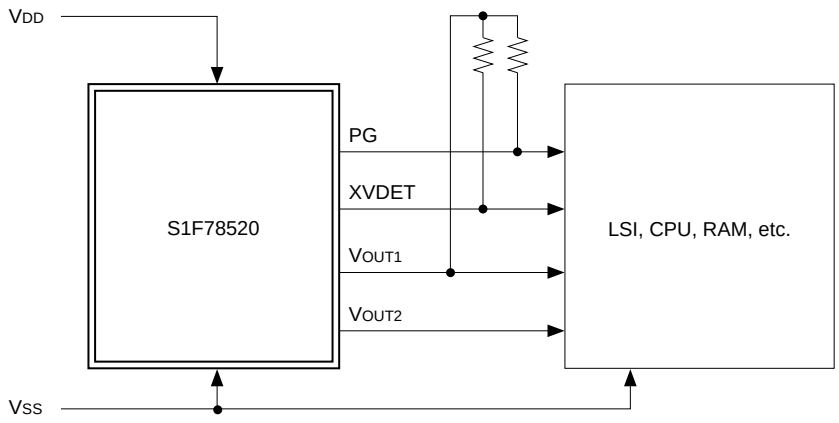


Fig. 2 System configuration diagram

● Oscillation circuit

The S1F78520 incorporates an oscillation circuit for the voltage dropping clock. This circuit is to be used connecting the oscillation current adjusting external resistor ROSC between the ROSC1 pin and the V_{SS}. The oscillation circuit will stop operation under shut down state (XPOFF = V_{SS}∗ level). Also, the oscillation will be interrupted by setting the ROSC1 pin to the V_{DD}∗ level or by making the pin into open state.
As the oscillation current adjusting external resistance, we recommend use of ROSC = 1MEG Ω.

● Standby mode

By setting the standby mode signal XSTBY externally, current consumption of this IC can be suppressed drastically.

The time required after the mode change is made with the standby pin until the internal mode of the IC is stabilized should be max. 10ms to min. 0s. Complete timing design should be effected when using the standby mode.

XSTBY pin	Mode name	Max. output current	Self-consumption current (Under no load state)
V_{DD}∗ level	Normal mode (Under heavy load state)	V_{OUT1} : 100 mA V_{OUT2} : 80 mA	75 µA
V_{SS}∗ level	Standby mode (Under light load state)	V_{OUT1} : 1 mA V_{OUT2} : 100 µA	25 µA

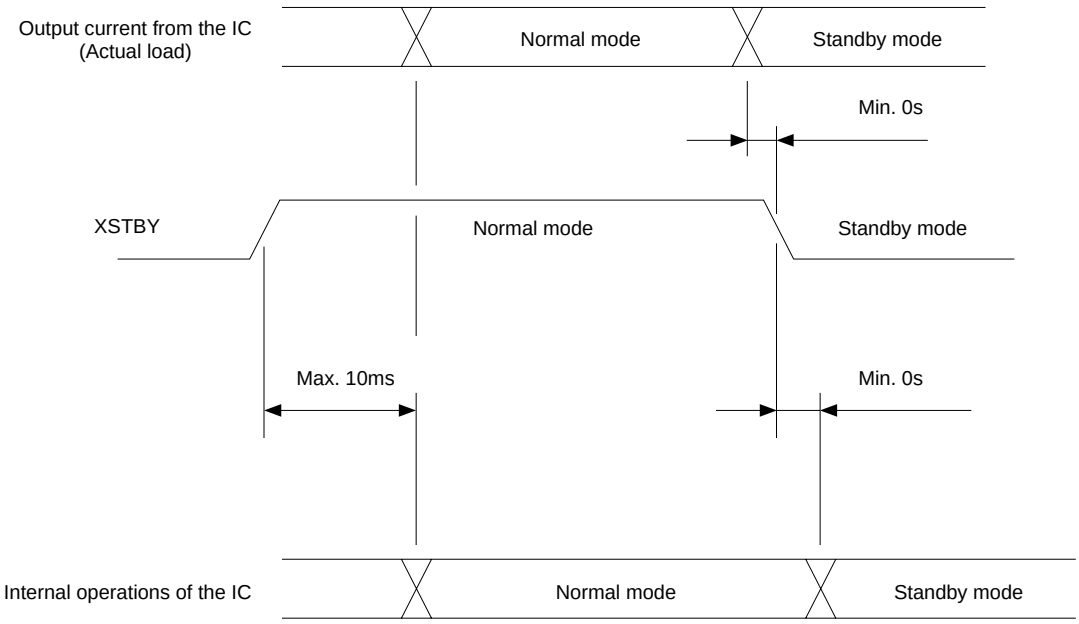


Fig. 3 below indicates a mode changing timing example.

● Low voltage detection circuit

This circuit makes low voltage detections by monitoring the input voltage through the V_{DD} pin. For setting of the detecting voltages, use of either of the internal voltage setting fixed to the IC or the external voltage setting pin VSENS is selectable through the external input pin VSEL.

VSEL pin	Detecting voltage selection	Detecting voltage value
V_{SS}∗ level	External pin VSENS	–VDET: (According to the formula 2) +VDET: (According to the formula 4)
V_{DD}∗ level	Internal voltage setting fixed to the IC	–VDET: 3.30 V +VDET: 3.39 V

The detecting voltage (–VDET) in case of external voltage setting will be the V_{DD} voltage value satisfying the following formulae.

$$V_{REF1} \geq V_{DD} \bullet (Rb)/(Ra + Rb) = VSENS \quad \text{.....(Formula 1)}$$

Consequently,

$$V_{DD} \leq V_{REF1} \bullet (Ra + Rb)/(Rb)\ [V] \quad \text{.....(Formula 2)}$$

can be established.

Also, the cancelling voltage (+VDET) in case of external voltage setting will be the VDD voltage value satisfying the following formulae.

$$V_{REF2} \leq V_{DD} \bullet (Rb)/(Ra + Rb) = VSENS \quad \text{.....(Formula 3)}$$

Consequently,

$$V_{DD} \geq V_{REF2} \bullet (Ra + Rb)/(Rb)\ [V] \quad \text{.....(Formula 4)}$$

can be established.

Fig. 4 below shows the block diagram for the external setting.

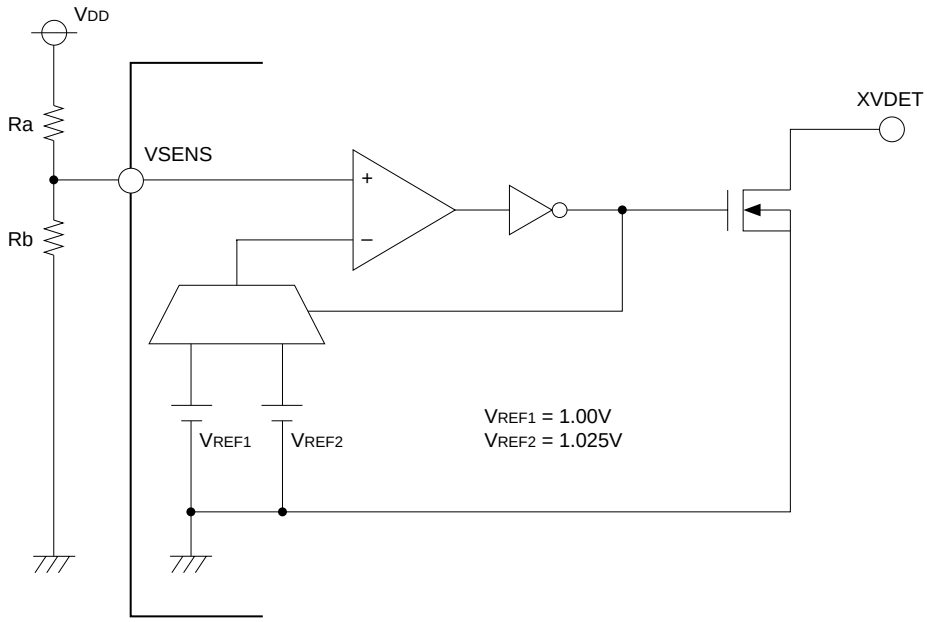


Fig. 4 Block diagram for the external setting

● Power good detection circuit

Power good signals are detected when both of the output pins V_{OUT1} and V_{OUT2} are satisfying the specified voltage.

As for the power good detection range, provision of a hysteresis width for the lower limit value of detection according to Fig. 5 indicated below is effective to prevent occurrences of unstable power good signal outputs in the neighborhood of the detection limit value range.

Also, delay setting can be made for the power good signals by use of the capacitor CDPG and the resistor RDPG. When the output voltage rises beyond the cancelling voltage, charge to the external capacitor will begin. When the capacitor voltage rises beyond the delaying threshold valve voltage, the power good signal changes from the V_{SS}∗ level to open state.

The delaying time can be calculated by formula 5.

Fig. 6 is an outline drawing for delay settings and Fig. 7 is the connection diagram in the neighborhood of the power good detection circuit.

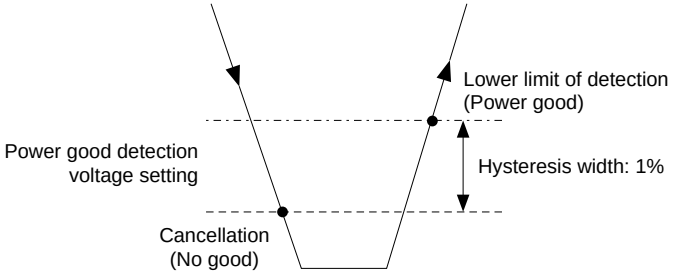


Fig. 5 Power good detecting range

Delay time (TDPG) can be calculated with the formula as below using external resistance (RDPG) and capacitor (CDPG).

$$TDPG\ (S) \fallingdotseq CDPG\ (F) \times RDPG\ (\Omega) \quad \text{(Formula 5)}$$

Example :

CDPG = 0.1µF, RDPG = 1MEGΩ

TDPG ≒ 0.1µF × 1MEGΩ = 0.1 (S)

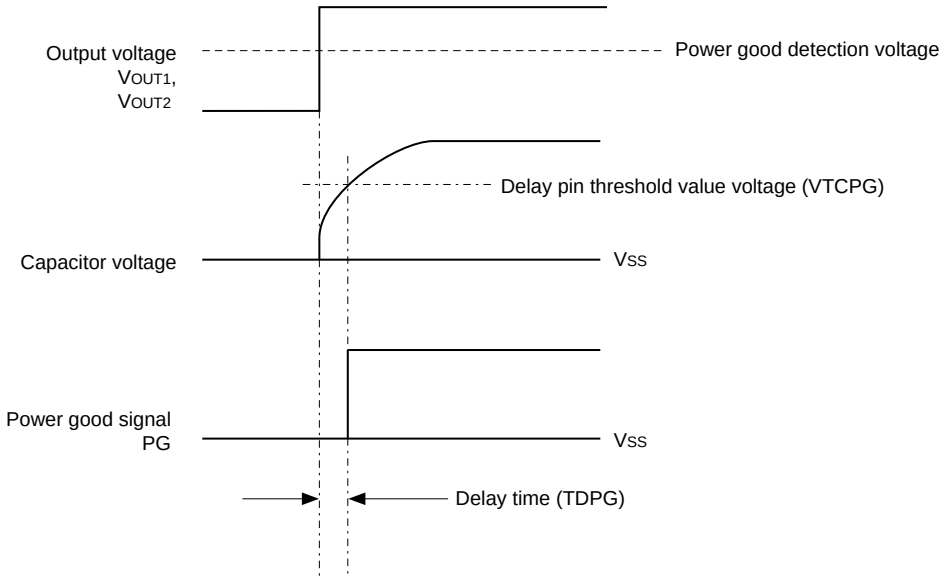


Fig. 6 Outline drawing for delay settings

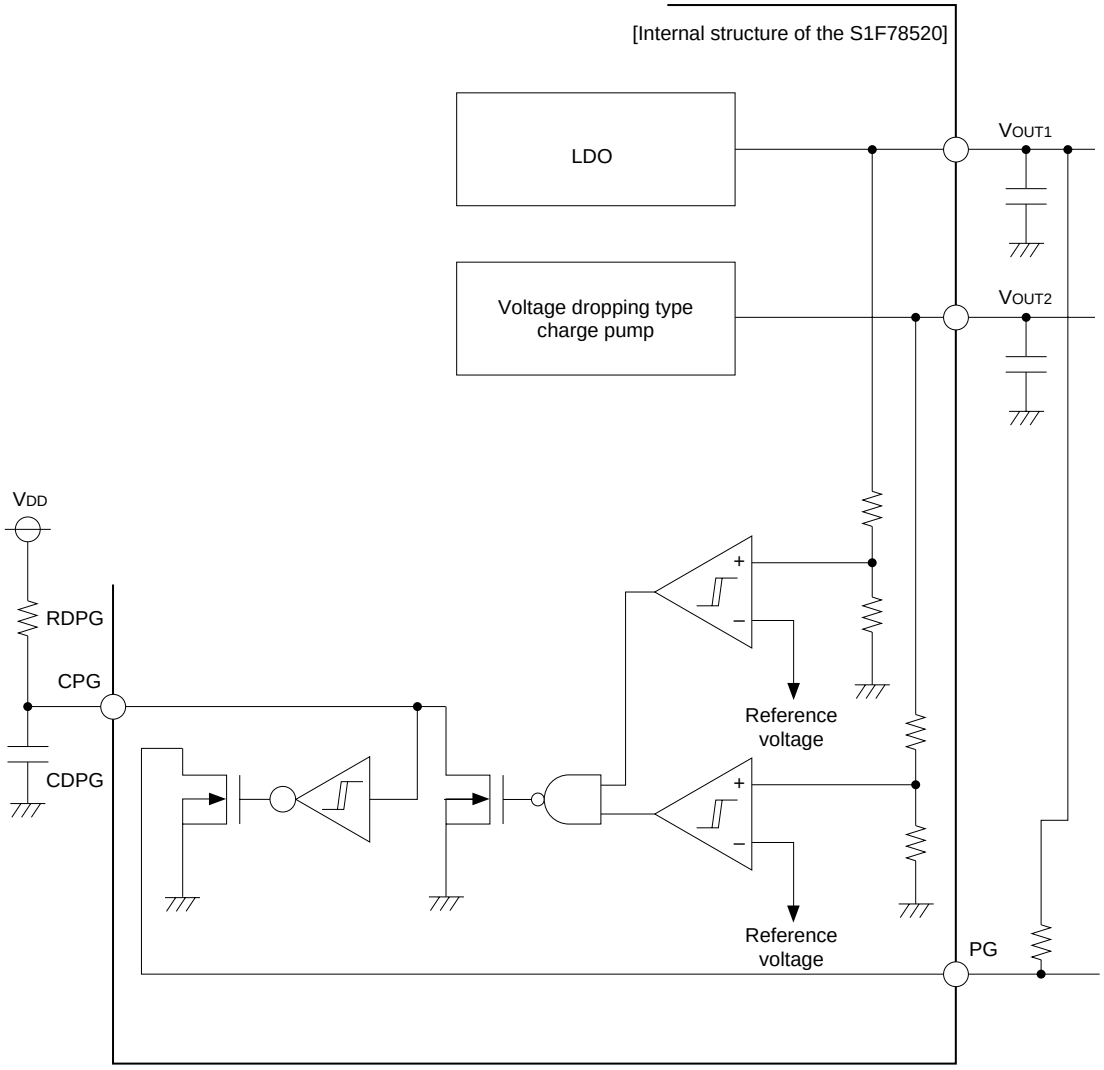


Fig. 7 Connection diagram in the neighborhood of the power good detection circuit

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating		Unit	Applicable pin	Remarks
		Min.	Max.			
Input supply voltage	V_{DD}	–0.3	7.0	V	V_{DD}, V_{DD2}	—
Output voltage 1	V_{OUT1}	–0.3	7.0	V	V_{OUT1},	—
Output voltage 2	V_{OUT2}	–0.3	7.0	V	V_{OUT2}	—
Input pin voltage	V_{IN}	–0.3	V_{DD}+0.3	V	<Note 1>	—
Input current	IV_{DD}	—	240	mA	V_{DD}, V_{DD2}	—
Output current 1	IV_{OUT1}	—	120	mA	V_{OUT1}	—
Output current 2	IV_{OUT2}	—	100	mA	V_{OUT2}	—
Allowable dissipation	P_D	—	520	mW	—	Ta = 25 °C
Operating temperature	Topr	–30	85	°C	—	—
Storage temperature	Tstg	–55	150	°C	—	—
Soldering temperature and time	Tsol	—	260 · 10	°C · s	—	At leads

<Note 1> The applicable pins are VO1LV1, VO1LV0, VO2LV1, VO2LV0, XSTBY, VSENS, VSEL, XPOFF, CPG and OSCIN.

<Note 2> Do not apply external voltage to the output pins and the pin connecting to the capacitor.

<Note 3> Use of the IC under any conditions exceeding the above absolute maximum ratings may cause malfunctioning or permanent breakdown. Or, even if the IC may operate normally temporarily, the reliability may greatly drop.

■ ELECTRICAL CHARACTERISTICS

● DC characteristics

❍ LDO (series regulator), voltage dropping type charge pump

In case particular designations are not made (Note 1): Ta = 25 °C

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Input supply voltage	V_{DD}	Applicable pin: V_{DD}	2.7	3.6	5.5	V	—
High level input voltage	V_{IH}	—	0.7*V_{DD}	—	V_{DD}	V	2
Low level input voltage	V_{IL}	—	0	—	0.3*V_{DD}	V	2
Input leak current	I_{LIN}	$V_{SS} \le V_I \le V_{DD}$ V_{DD} = 3.6 V	–0.5	—	0.5	µA	3
Output voltage 11	V_{OUT11}	Applicable pin: V_{OUT1} Output voltage setting: 3.3 V V_{DD} = 3.6 V IV_{OUT1} = 10 mA	3.20	3.30	3.40	V	—
Output voltage 12	V_{OUT12}	Applicable pin: V_{OUT1} Output voltage setting: 2.9 V V_{DD} = 3.6 V IV_{OUT1} = 10 mA	2.81	2.90	2.99	V	—
Output voltage 13	V_{OUT13}	Applicable pin: V_{OUT1} Output voltage setting: 2.5 V V_{DD} = 3.6 V IV_{OUT1} = 10 mA	2.42	2.50	2.58	V	—
Output voltage 21	V_{OUT21}	Applicable pin: V_{OUT2} Output voltage setting: 2.5 V V_{DD} = 3.6 V IV_{OUT2} = 10 mA	2.40	2.50	2.60	V	—
Output voltage 22	V_{OUT22}	Applicable pin: V_{OUT2} Output voltage setting: 2.0 V V_{DD} = 3.6 V IV_{OUT2} = 10 mA	1.92	2.00	2.08	V	—
Output voltage 23	V_{OUT23}	Applicable pin: V_{OUT2} Output voltage setting: 1.8 V V_{DD} = 3.6 V IV_{OUT2} = 10 mA	1.72	1.80	1.88	V	—
Output voltage 11	IV_{OUT11}	Applicable pin: V_{OUT1} Output voltage setting: 3.3 V V_{DD} = 3.6 V	—	—	100	mA	—
Output voltage 12	IV_{OUT12}	Applicable pin: V_{OUT1} Output voltage setting: 2.9 V V_{DD} = 3.6 V	—	—	100	mA	—
Output voltage 13	IV_{OUT13}	Applicable pin: V_{OUT1} Output voltage setting: 2.5 V V_{DD} = 3.6 V	—	—	100	mA	—

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Output voltage 21	IV_{OUT21}	Applicable pin: V_{OUT2} Output voltage setting: 2.5 V V_{DD} = 3.6 V	—	—	80	mA	—
Output voltage 22	IV_{OUT22}	Applicable pin: V_{OUT2} Output voltage setting: 2.0 V V_{DD} = 3.6 V	—	—	80	mA	—
Output voltage 23	IV_{OUT23}	Applicable pin: V_{OUT2} Output voltage setting: 1.8 V V_{DD} = 3.6 V	—	—	80	mA	—
Load stability 1	$\frac{\Delta V_{OUT1}}{\Delta I_{OUT1}}$	V_{DD} = 3.6 V Output voltage setting: 3.3 V 0 mA ≤ I_{OUT1} ≤ 50 mA	—	30	45	mV	—
Load stability 2	$\frac{\Delta V_{OUT2}}{\Delta I_{OUT2}}$	V_{DD} = 3.6 V Output voltage setting: 1.8 V 0 mA ≤ I_{OUT2} ≤ 25 mA	—	20	30	mV	—
I/O voltage difference	VDIF	V_{DD} = 3.0 V I_{OUT1} = 30 mA	—	80	150	mV	—
Output impedance	RV_{OUT2}	V_{DD} = 2.5 V I_{OUT2} = 10 mA	—	6.5	—	Ω	—
Current consumption 1	I_{OP1}	V_{DD} = 3.6 V, no load Normal mode	—	75	90	µA	—
Current consumption 2	I_{OP2}	V_{DD} = 3.6 V, no load Standby mode	—	25	40	µA	—
Resting current	IQ	V_{DD} = 3.6 V Shut down mode	—	—	1.0	µA	—
Input stability 1	$\frac{\Delta V_{OUT1}}{\Delta V_{DD}}$	3.6 V ≤ V_{DD} ≤ 4.6 V I_{OUT1} = 50 mA	—	0.4	0.8	%/ V	—
Input stability 2	$\frac{\Delta V_{OUT2}}{\Delta V_{DD}}$	3.6 V ≤ V_{DD} ≤ 4.6 V I_{OUT2} = 25 mA	—	0.3	0.6	%/ V	—
Power conversion efficiency (Charge pump)	Peff	Normal mode IV_{OUT2} = 40 mA	—	85	—	%	4
Output voltage / temperature coefficient 1	$\frac{\Delta V_{OUT1}}{\Delta Topr}$	IV_{OUT2} = 50 mA –30 °C ≤ Topr ≤ 85°C	—	±300	—	ppm/°C	—
Output voltage / temperature coefficient 2	$\frac{\Delta V_{OUT2}}{\Delta Topr}$	IV_{OUT2} = 0.05 mA –30 °C ≤ Topr ≤ 85°C	—	±300	—	ppm/°C	—

<Note 1> Conditions on the operation mode, external parts constant, pins, etc. in case particular designations are not made are as follows:
Connection and parts constant : Standard connection 1
XPOFF pin : XPOFF = HIGH (Normal mode)
XSTBY pin : XSTBY = HIGH (Normal mode)

<Note 2> The applicable pins are V01LV1, V01LV0, V02LV1, V02LV0, XSTBY, VSEL, XPOFF.

<Note 3> The applicable pins are V01LV1, V01LV0, V02LV1, V02LV0, CPG, XSTBY, VSENS, VSEL, XPOFF.

<Note 4> The power conversion efficiency of the voltage dropping type charge pump only.

❍Low voltage detection

In case particular designations are not made (Note 1): Ta = 25 °C

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Detection voltage	–VDET	VSEL pin = V_{DD}∗ level (Internal voltage setting fixed to the IC)	3.20	3.30	3.40	V	—
Hysteresis width	VHYS	VSEL pin = V_{DD}∗ level (Internal voltage setting fixed to the IC)	0.01	0.09	0.18	V	—
Reference detection voltage 1	V_{REF1}	VSEL pin = V_{SS}∗ level (External voltage setting to the VSENS pin)	0.97	1.00	1.03	V	—
Reference detection voltage 2	V_{REF2}	VSEL pin = V_{SS}∗ level (External voltage setting to the VSENS pin)	0.99	1.025	1.055	V	—
Min. operating voltage	VVDDL	Topr = 25 °C	—	—	1.5	V	2
		–30 °C ≤ Topr ≤ 85 °C	—	—	1.53		
Output current (Driver output pin)	IVDET	V_{DD} = 3.6 V XVDET = 0.1V	0.36	—	—	mA	—
Off leak current (Driver output pin)	IVDOFF	V_{DD} = XVDET = 5.5V	–150	—	150	nA	—
Transfer delay time	TPLH	—	—	—	100	µs	3
Detection voltage / temperature coefficient	$\frac{\Delta\text{-VDET}}{\Delta\text{Topr}}$	VSEL pin = V_{DD}∗ level (Internal voltage setting fixed to the IC) –30 °C ≤ Topr ≤ 85 °C	—	±300	—	ppm/°C	—

<Note 1> Conditions on the operation mode, external parts constant, pins, etc. in case particular designations are not made are as follows:
Connection and parts constant : Standard connection 1
XPOFF pin : XPOFF = HIGH (Normal mode)
XSTBY pin : XSTBY = HIGH (Normal mode)

<Note 2> The supply voltage value where the output voltage becomes 0.1V or less. (Pullup resistance : 470kΩ, Pullup voltage : 3.6V)

<Note 3> Time when the output voltage reaches 1.8V after applying the minimum operating voltage of → 3.6V pulse voltage to V_{DD} on the condition that pullup resistance is 470kΩ and pullup voltage is 3.6V.

❍Power good detection

In case particular designations are not made (Note 1): Ta = 25 °C

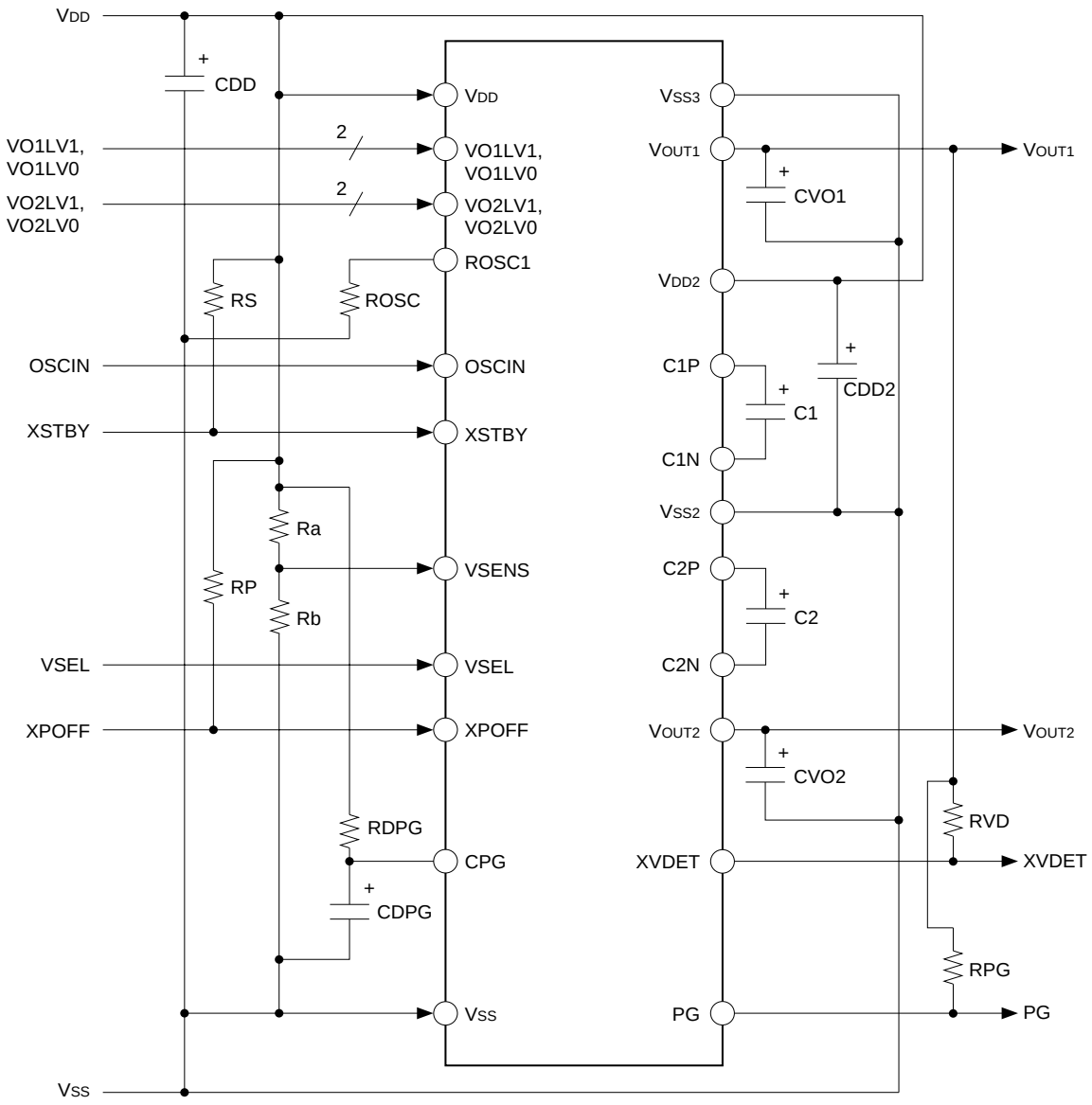
Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Lower limit detection voltage 11	VDLPG11	Applicable pin = VOUT1 Output voltage setting: 3.3 V Hysteresis width: 1%	2.82	2.91	3.00	V	—
Lower limit detection voltage 12	VDLPG12	Applicable pin = VOUT1 Output voltage setting: 2.9 V Hysteresis width: 1%	2.54	2.62	2.70	V	—
Lower limit detection voltage 13	VDLPG13	Applicable pin = VOUT1 Output voltage setting: 2.5 V Hysteresis width: 1%	2.16	2.23	2.30	V	—
Lower limit detection voltage 21	VDLPG21	Applicable pin = VOUT2 Output voltage setting: 2.5 V Hysteresis width: 1%	2.16	2.23	2.30	V	—
Lower limit detection voltage 22	VDLPG22	Applicable pin = VOUT2 Output voltage setting: 2.0 V Hysteresis width: 1%	1.68	1.74	1.80	V	—
Lower limit detection voltage 23	VDLPG23	Applicable pin = VOUT2 Output voltage setting: 1.8 V Hysteresis width: 1%	1.55	1.60	1.65	V	—
PG output current (Driver output pin)	IPG	VDD = 3.6V PG = 0.1V	0.36	—	—	mA	
PG off leak current (Driver output pin)	IPGOFF	VDD = PG = 5.5V	–150	—	150	nA	—
Delay pin Threshold value voltage	VTCPG	VDD = 3.6V	2.05	2.4	2.77	V	—
CPG output current (Delay pin)	ICPG	VDD = 3.6V CPG = 0.1V	0.06	—	—	mA	—
Lower limit detection voltage/ temperature coefficient 1	$\frac{\Delta VDLPG1}{\Delta Topr}$	Applicable pin: VOUT1 –30 °C ≤ Topr ≤ 85 °C	—	±300	—	ppm/°C	—
Lower limit detection voltage/ temperature coefficient 2	$\frac{\Delta VDLPG21}{\Delta Topr}$	Applicable pin: VOUT2 Output voltage setting: 2.0 V –30 °C ≤ Topr ≤ 85 °C	—	±300	—	ppm/°C	—

<Note 1> Conditions on the operation mode, external parts constant, pins, etc. in case particular designations are not made are as follows:

Connection and parts constant : Standard connection 1
XPOFF pin : XPOFF = HIGH (Normal mode)
XSTBY pin : XSTBY = HIGH (Normal mode)

■ REFERENCE EXTERNAL CONNECTION (AN EXAMPLE)

● Standard connection 1



Recommended values for the external parts

ROSC = 1MEGΩ

Ra = (Make the detection voltage setting according to the formulae 2 and 4.)

Rb = (Make the detection voltage setting according to the formulae 2 and 4.)

RS = RP = RVD = RPG = 470kΩ

CDD = CDD2 = 4.7µF

CDPG = 0.1µF [In case a delay time setting of 100ms is made.]

RDPG = 1MEGΩ [In case a delay time setting of 100ms is made.]

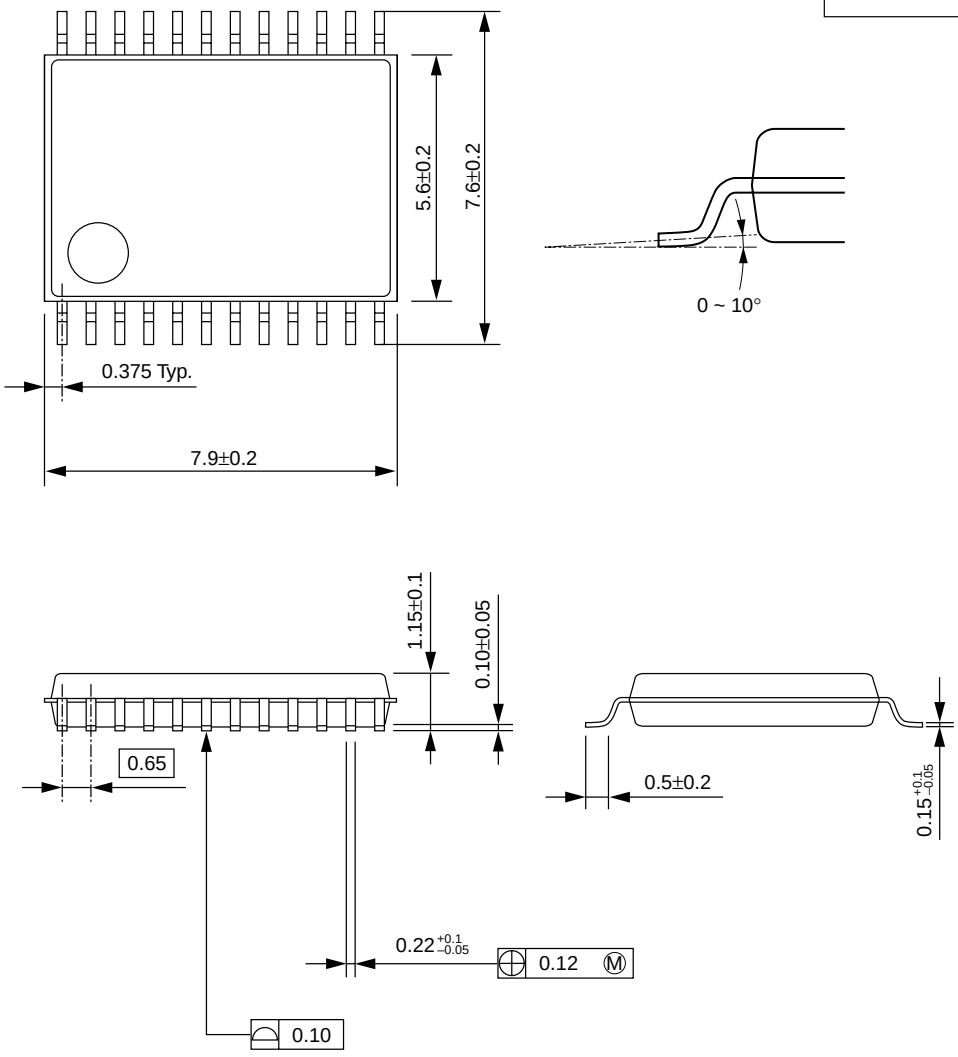
CV01 = CV02 = 22µF

C1 = C2 = 0.47µF

■ DIMENSIONAL OUTLINE DRAWING

SSOP3–24pin

EXAMPLE



Unit : mm

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