

# LM2685

## Dual Output Regulated Switched Capacitor Voltage Converter

### General Description

The LM2685 CMOS charge-pump voltage converter operates as an input voltage doubler, +5V regulator and inverter for an input voltage in the range of +2.85V to +6.5V. Five low cost capacitors are used in this circuit to provide up to 50mA of output current at +5V ( $\pm 5\%$ ), and 15mA at -5V. The LM2685 operates at a 130 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 800 $\mu$ A (operating efficiency greater than 80% with most loads) and 6 $\mu$ A typical shutdown current, the LM2685 is ideal for use in battery powered systems. The device is in a small 14-pin TSSOP package.

- TSSOP-14 package
- 80% typical conversion efficiency at 25mA
- Input voltage range of 2.85V to 6.5V
- Independent shutdown control pins

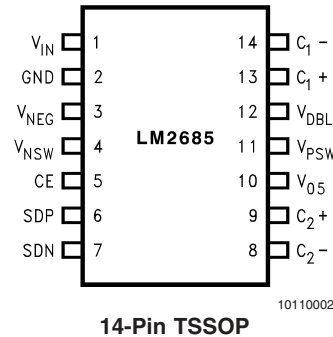
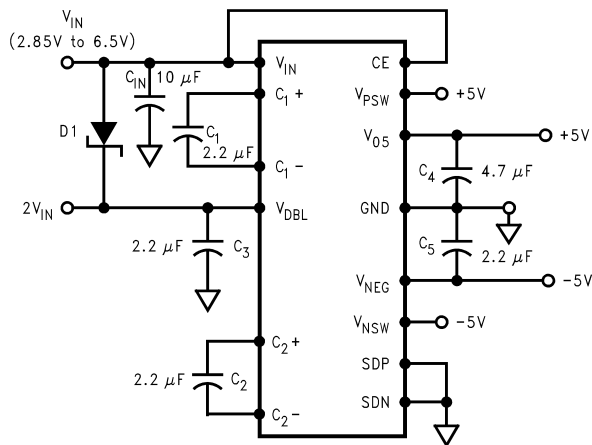
### Applications

- Cellular phones
- Pagers
- PDAs
- Handheld instrumentation
- 3.3V to 5V voltage conversion applications

### Features

- +5V regulated output
- Inverts  $V_{OS}(+5V)$  to  $V_{NEG}(-5V)$
- Doubles input supply voltage

### Typical Application and Connection Diagram



10110001

### Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2685MTC	TSSOP-14	MTC14	94 Units, Rail
LM2685MTCX	TSSOP-14	MTC14	2.5k Units, Tape and Reel

## Pin Description

Pin No.	Name	Function
1	$V_{IN}$	Power supply input voltage.
2	GND	Power supply ground.
3	$V_{NEG}$	Negative output voltage created by inverting $V_{05}$ .
4	$V_{NSW}$	$V_{NEG}$ output connected through a series switch, NSW.
5	CE	Chip enable input. This pin is high for normal operation and low for shutdown. (See Shutdown and Load Disconnect section in the Detailed Device Description division).
6	SDP	Positive side shutdown input. This pin is low for normal operation and high for positive side shutdown and $V_{PSW}$ load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division).
7	SDN	Negative side shutdown input. This pin is low for normal operation and high for negative side shutdown and $V_{NSW}$ load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division).
8	$C_2^-$	The negative terminal of inverting charge-pump capacitor, C2.
9	$C_2^+$	The positive terminal of inverting charge-pump capacitor, C2.
10	$V_{05}$	Regulated +5V output.
11	$V_{PSW}$	$V_{05}$ output connected through a series switch, PSW.
12	$V_{DBL}$	Voltage Doubler Output. ( $2.85V \leq V_{IN} \leq 5.4V$ . See Voltage Doubler section).
13	$C_1^+$	The positive terminal of doubling charge-pump capacitor, C1.
14	$C_1^-$	The negative terminal of doubling charge-pump capacitor, C1.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{IN}$ to GND or GND to $V_{NEG}$ )	6.8V
SDN, SDP, CE	(GND – 0.3V) to ( $V_{IN} + 0.3V$ )
$V_{O5}$ Continuous Output Current	80mA
$V_{O5}$ Short-Circuit Duration to GND (Note 2)	Indefinite

Continuous Power Dissipation ( $T_A = 25^\circ\text{C}$ ) (Note 3)	600mW
$T_{JMAX}$ (Note 3)	150°C
$\theta_{JA}$ (Note 3)	140°C/W
Operating Ambient Temp. Range	-40°C to 85°C
Operating Junction Temp. Range	-40°C to 125°C
Storage Temp. Range	-65°C to 150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD Rating (Note 4)	2kV

**Electrical Characteristics**

Limits with standard typeface apply for  $T_J = 25^\circ\text{C}$ , and limits in **boldface type** apply over the full temperature range. Unless otherwise specified  $V_{IN} = 3.6V$ ,  $C_1 = C_2 = C_3 = C_5 = 2.2\mu\text{F}$ ,  $C_4 = 4.7\mu\text{F}$  (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V^+$	Supply Voltage		<b>2.85</b>		<b>6.5</b>	V
$I_Q$	Supply Current	No Load		800	<b>1600</b>	$\mu\text{A}$
		No Load, $V_{IN} = 6.5V$		300	<b>600</b>	
$I_{SD}$	Shutdown Supply Current	$V_{IN} = 6.5V$		6	30	$\mu\text{A}$
$V_{SD}$	Shutdown Pin Input Voltage for CE, SDP, SDN	Logic Input High @ 6.5V	<b>2.4</b>			V
		Logic Input Low @ 6.5V			<b>0.8</b>	
$I_L (+5V)$	Output Current at $V_{O5}$	$2.85V < V_{IN} < 6.5V$			<b>50</b>	mA
$R_O (-5V)$	Output Resistance at $V_{NEG}$	$I_L = 15\text{mA}$ (Note 6)		20	<b>40</b>	$\Omega$
$F_{SW}$	Switch Frequency		<b>85</b>	130	<b>180</b>	kHz
$P_{EFF}$	Average Power Efficiency at $V_{O5}$	$2.85V \leq V_{IN} \leq 6.5V$ $I_L = 25\text{mA}$ to GND		82		%
$V_{O5}$	Output Regulation	$1\text{mA} < I_L < 50\text{mA}$ , $V_{IN} = 6.5V$ (Note 7)	4.848	5.05	5.252	V
		$1\text{mA} < I_L < 50\text{mA}$ , $V_{IN} = 6.5V$ (Note 7)	<b>4.797</b>	5.05	<b>5.303</b>	
$G_{LINE}$	Line Regulation	$2.85V < V_{IN} < 3.6V$		0.25		%V
		$3.6V < V_{IN} < 6.5V$		0.05		
$G_{LOAD}$	Load Regulation	$1\text{mA} < I_L < 50\text{mA}$ , $V_{IN} = 6.5V$		0.3	1.0	%
$R_{SW}$	Series Switch Resistance $V_{NEG}$ to $V_{NSW}$	$V_{IN} > 2.85V$		1.5		$\Omega$
	$V_{O5}$ to $V_{PSW}$			5.0		

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

**Note 2:**  $V_{O5}$  may be shorted to GND without damage. However, shorting  $V_{NEG}$  to  $V_{O5}$  may damage the device and must be avoided. Also, for temperature above 85°C,  $V_{O5}$  must not be shorted to GND or device may be damaged.

**Note 3:** The maximum allowable power dissipation is calculated by using  $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ , where  $T_{JMAX}$  is the maximum junction temperature,  $T_A$  is the ambient temperature and  $\theta_{JA}$  is the junction-to-ambient thermal resistance of the specified package.

**Note 4:** The human body model is a 100 pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin.

**Note 5:** In the typical operating circuit, capacitors  $C_1$  and  $C_2$  are 2.2 $\mu\text{F}$ , 0.3 $\Omega$  maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.

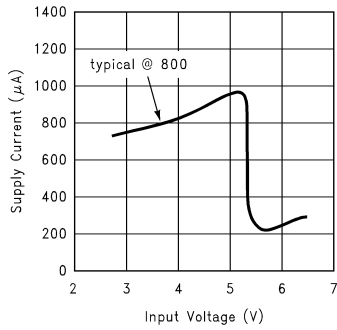
**Note 6:** Specified output resistance includes internal switch resistance and ESR of capacitors. See the Detailed Device Description section.

**Note 7:** The 50 mA maximum current assumes no current is drawn from  $V_{DBL}$  pin. See Voltage Doubler section in the Detailed Device Description.

# Typical Performance Characteristics

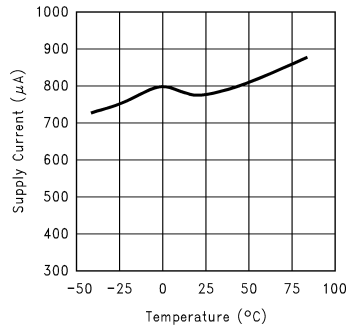
Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 3.6\text{V}$ .

**Supply Current vs Input Voltage**



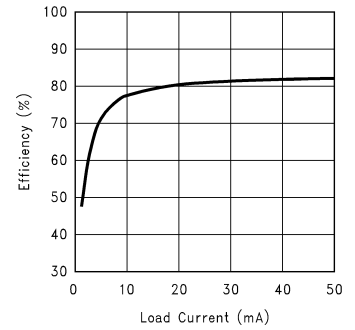
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**Supply Current vs Temperature**



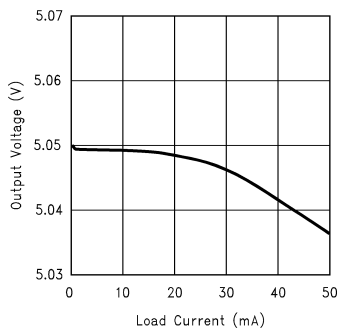
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**Efficiency vs Load Current**



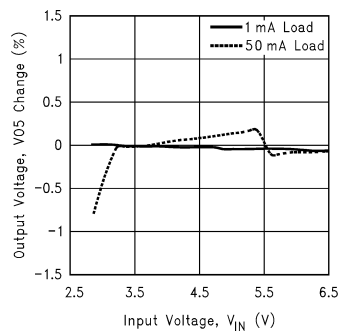
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**Output Voltage ( $V_{O5}$ ) vs. Load Current**



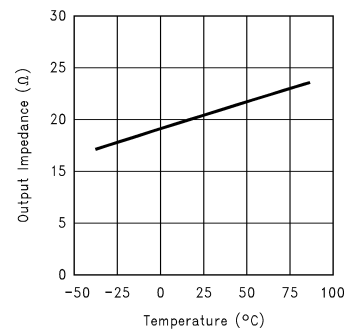
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**$V_{O5}$  Voltage vs. Input Voltage**



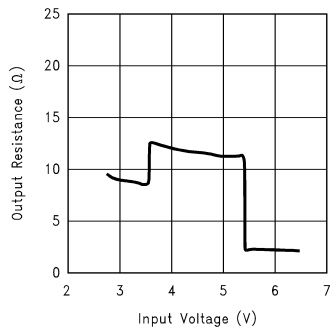
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**Output Resistance ( $V_{NEG}$ ) vs. Temperature**



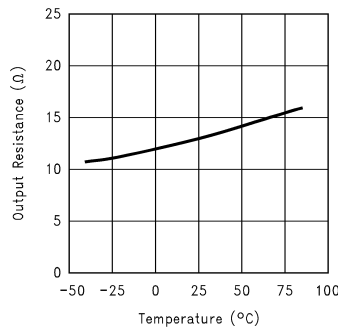
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**Output Resistance ( $V_{DBL}$ ) vs. Input Voltage**



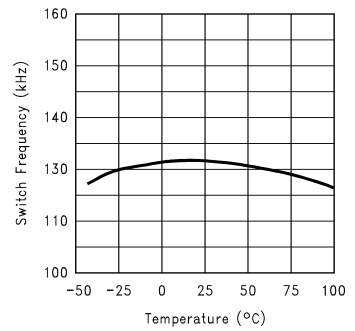
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**Output Resistance ( $V_{DBL}$ ) vs. Temperature**



10110012

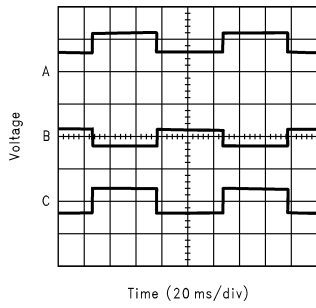
**Switch Frequency vs. Temperature**



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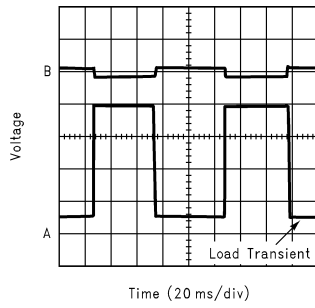
# Typical Performance Characteristics Unless otherwise specified, $T_A = 25^\circ\text{C}$ , $V_{IN} = 3.6\text{V}$ . (Continued)

## Line Transient Response (with 5mA Load)



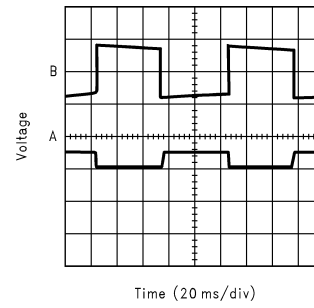
A: INPUT VOLTAGE:  $V_{IN} = 3.2\text{V}$  to  $6.0\text{V}$ , 5V/div  
 B: OUTPUT VOLTAGE:  $V_{PSW} = 100\text{mV/div}$   
 C: OUTPUT VOLTAGE:  $V_{NSW} = 100\text{mV/div}$

## $V_{O5}$ Load Transient Response



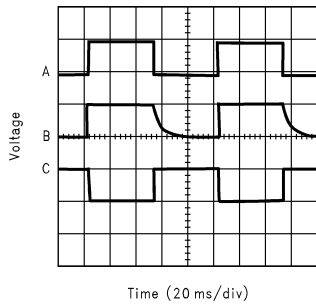
A: LOAD CURRENT:  $I_{LOAD} = 5\text{mA}$  to  $39.6\text{mA}$ , 10mA/div  
 B: OUTPUT VOLTAGE:  $V_{O5} = 10\text{mV/div}$

## $V_{NSW}$ Load Transient Response



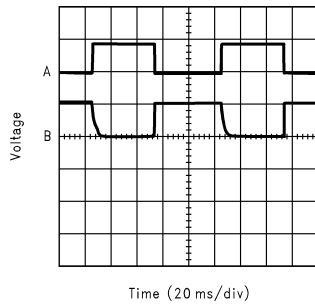
A: LOAD CURRENT:  $I_{LOAD} = 4.4\text{mA}$  to  $-9.4\text{mA}$ , 10mA/div  
 B: OUTPUT VOLTAGE:  $V_{NSW} = 50\text{mV/div}$

## $V_{PSW}$ and $V_{NSW}$ Response to CE (with 5mA Load)



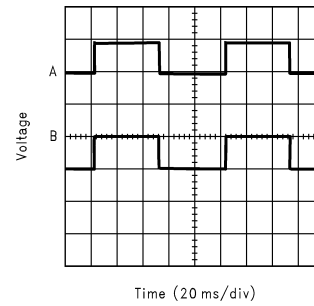
A: CE INPUT: 5V/div  
 B: OUTPUT VOLTAGE:  $V_{PSW} = 5\text{V/div}$   
 C: OUTPUT VOLTAGE:  $V_{NSW} = 5\text{V/div}$

## $V_{O5}$ Response to SDP (with 5mA Load)



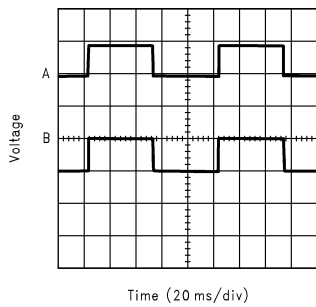
A: SDP INPUT: 5V/div  
 B: OUTPUT VOLTAGE: 5V/div

## $V_{NSW}$ Response to SDP (with 5mA Load)



A: SDP INPUT: 5V/div  
 B: OUTPUT VOLTAGE ( $V_{NSW}$ ): 5V/div

## $V_{NSW}$ Response to SDN (with 5mA Load)



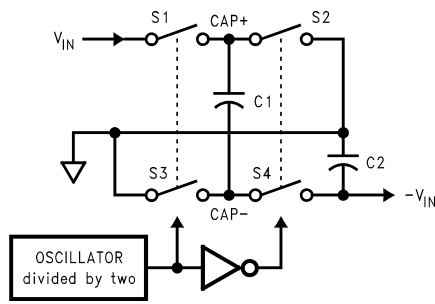
A: SDN INPUT: 5V/div  
 B: OUTPUT VOLTAGE ( $V_{NSW}$ ): 5V/div



## Detailed Device Description

(Continued)

CMOS switches which are in a sequence to invert the input supply voltage. *Figure 3* illustrates the voltage conversion scheme. When S1 and S3 are closed, C1 charges to the supply voltage  $V_{O5}$ . During this time interval, switches S2 and S4 are open. In the second time interval, S1 and S3 are open; at the same time, S2 and S4 are closed, C1 is charging C2. After a number of cycles, the voltage across C2 will be pumped to  $V_{O5}$ . Since the anode of C2 is connected to ground, the output at the cathode of C2 equals  $-(V_{O5})$  when there is no load current. The output voltage drop when a load is added is determined by the parasitic resistance ( $R_{ds(on)}$ ) of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors.



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FIGURE 3. Voltage Inverter Principle

### SHUTDOWN AND LOAD DISCONNECT

In addition to the nominal charge pump and regulator functions, the LM2685 features shutdown and load disconnect circuitry. CE (chip enable) and SDP (shutdown positive) perform the same task with opposite input polarities. When CE is low or SDP is high, all circuit blocks are disabled and  $V_{O5}$  falls to ground potential. This is the same result as when the die temperature exceeds 150°C (typical), and the device's internal thermal shutdown is triggered.

Forcing SDN (shutdown negative) high disables only the inverting charge pump. The doubling charge pump and the LDO regulator continue to operate, so the  $V_{O5}$  and the  $V_{PSW}$  remain at 5V.

The LM2685 incorporates two low impedance switches tied to the  $V_{O5}$  and  $V_{NEG}$  outputs, because some special applications require load disconnect and this is achievable via the switches. Switch PSW connects  $V_{O5}$  to  $V_{PSW}$ , and switch NSW connects  $V_{NEG}$  to  $V_{NSW}$ . In normal operation, these switches are closed, allowing 5V loads to be tied to either  $V_{O5}$  or  $V_{PSW}$  and -5V loads to be tied to either  $V_{NEG}$  or  $V_{NSW}$ . Driving SDN high opens switch NSW only, while forcing CE low or SDP high, opens both the PSW and NSW.

## Application Information

### CAPACITOR SELECTION

The output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors.

### VOLTAGE DOUBLER EXTERNAL CAPACITORS

The selection of capacitors are based on the specifications of the dropout voltage (which equals  $I_{OUT} R_{OUT}$ ), the output voltage ripple, and the converter efficiency.

$$R_{OUT} = 2 R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4 ESR_{C_1} + ESR_{C_3}$$

where  $R_{SW}$  is the sum of the ON resistance of the internal MOSFET switches as shown in *Figure 2*.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the capacitor C3.

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C_3}$$

High capacitance (2.2μF to higher), low ESR capacitors can reduce the output resistance and the voltage ripple.

$$\text{Power efficiency of} = \frac{P_{OUT}}{P_{IN}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{OUT} + I_Q (V+)}$$

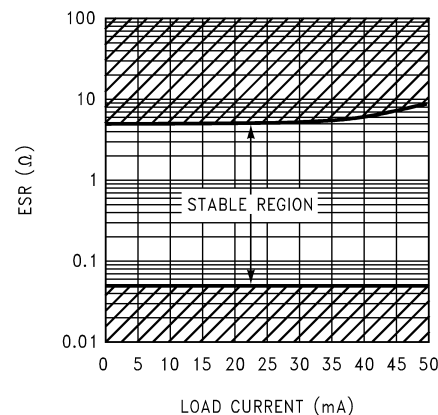
where  $I_Q(V+)$  is the quiescent power loss of the IC device, and  $I_L^2 R_L$  is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

Low ESR capacitors (table to be referenced) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

### +5 LDO REGULATOR EXTERNAL CAPACITORS

The voltage doubler output capacitor, C3, serves as the input capacitor of the +5 LDO regulator. The output capacitor C4, must meet the requirement for minimum amount of capacitance and appropriate ESR (Equivalent Serving Resistance) for proper operation. The ESR value must remain within the regions of stability as shown in *Figure 4*, *Figure 5* and *Figure 6* to ensure output's stability. A minimum capacitance of 1μF is required at the output. This can be increased without limit, but a 4.7μF tantalum capacitor is recommended for loads ranging up to the maximum specification. With lighter loads of less or equal to 10mA, ceramic capacitor of at least 1μF and ESR in the milliohms can be used. This has to be connected to  $V_{PSW}$  pin instead of the  $V_{O5}$  pin.

Any output capacitor used should have a good tolerance over temperature for capacitance and ESR values. The larger the capacitor, with ESR within the stable region, the better the stability and noise performance.



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FIGURE 4. ESR Curve for  $C_{OUT} = 2.2\mu F$

## Application Information (Continued)

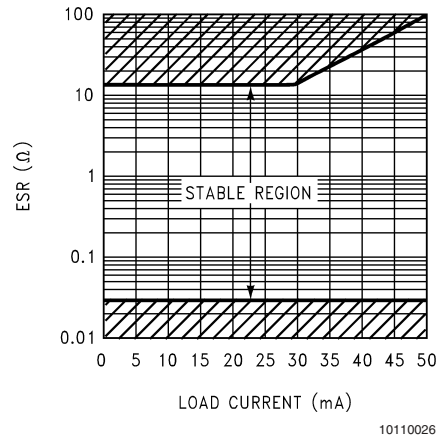


FIGURE 5. ESR Curve for  $C_{OUT} = 4.7\mu\text{F}$

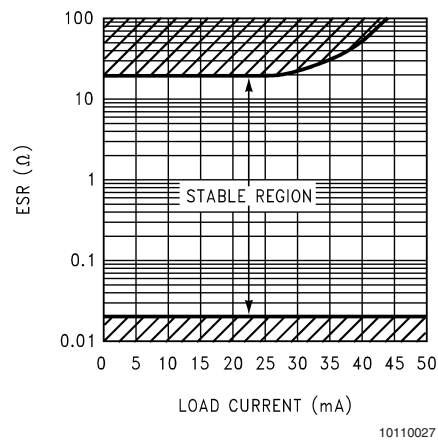


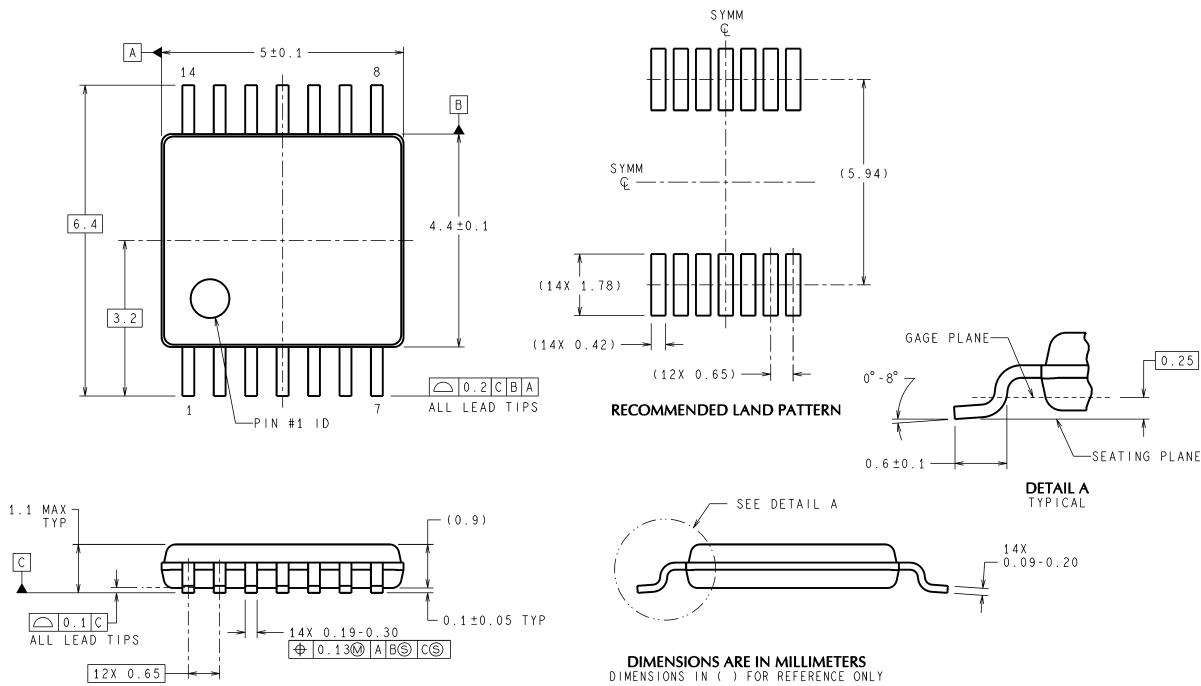
FIGURE 6. ESR Curve for  $C_{OUT} = 10\mu\text{F}$

### INVERTER EXTERNAL CAPACITORS

As discussed in the +5 LDO Regulator External Capacitors section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. A minimum of  $1\mu\text{F}$  capacitor with good tolerance over temperature for capacitance and ESR values. The capacitance value can be increased without limit while still maintain high low ESR value.  $2.2\mu\text{F}$  capacitors are recommended for the two external capacitors,  $C_2$  and  $C_5$  of the inverter.



**Physical Dimensions** inches (millimeters) unless otherwise noted



MTC14 (Rev D)

**TSSOP-14 Package**  
**14-Lead Thin Shrink Small-Outline Package**  
**For Ordering, Refer to Ordering Information Table**  
**NS Package Number MTC14**

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