National Semiconductor

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LM26484
Power Management Unit

General Description

The LM26484 is a multi-function, configurable Power Management Unit. This device integrates two highly efficient 2.0A Step-Down DC/DC converters, one LDO Controller, a POR (Power On Reset) circuit, and thermal overload protection circuitry. All regulator output voltages are externally adjustable. The LDO controller is a low-voltage NMOS voltage regulator. The LM26484 is offered in a 5 x 4 x 0.8 mm LLP-24 pin package.

Key Specifications

STEP-DOWN DC/DC CONVERTER (BUCK)

- 3.0–5.5V Input Range
- Externally adjustable V_{OUT}:
  - Buck1 : 0.8V–3.5V @ 2A
  - Buck2 : 0.8V–3.5V @ 2A
- 180° Phase Shift between Bucks Clocks
- 2 MHz PWM switching frequency
- ±1% feedback voltage accuracy
- Automatic soft start
- Current overload protection
- PWM/PFM efficiency modes available

LINEAR REGULATOR (LDO) CONTROLLER

- 3.0V–5.5V Input range
- Externally adjustable V_{OUT}
- ±1.5% feedback voltage accuracy
- Regulated to Low V_{IN} - Low V_{OUT} LI-LO (Low Input Low Output) NFET operation
- Input to the LI-LO configuration, can be post regulated when supply is regulated by Buck2
- Up to 1000 mA output current by selection of external FET

Applications

- Digital Cores and I/Os (FPGAs, ASICs, DSPs)
- Automotive infotainment
- Set-top-box
- Cordless phone base station
- Networking router
- Printers

Application Circuit

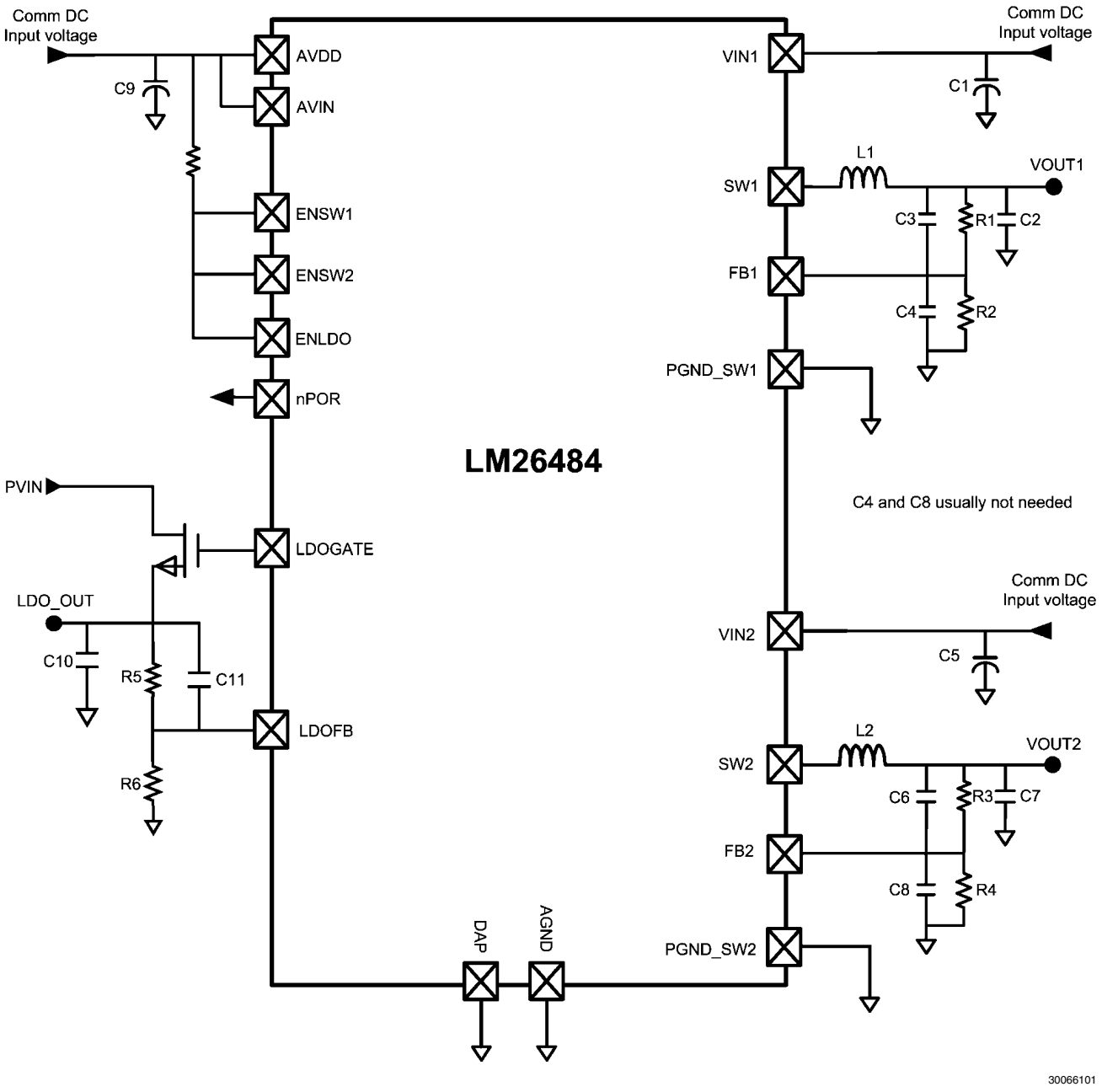
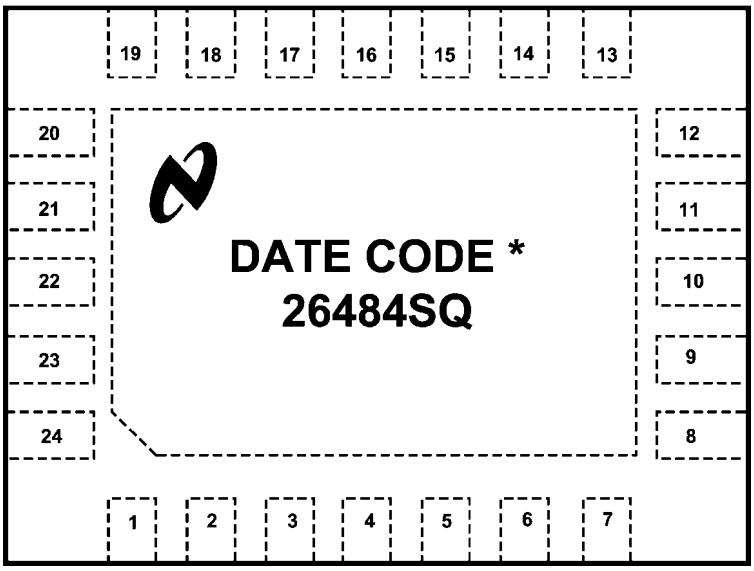


FIGURE 1. Application Circuit

Connection Diagram and Package Mark Information



24-Lead LLP Package (top view)

Note: The physical placement of the package marking will vary from part to part.
(*) UZXYTT format: 'U' – wafer fab code; 'Z' – assembly code; 'XY' 2 digit date code; 'TT" – die run code.
See http://www.national.com/quality/marking_conventions.html for more information on marking information.

Ordering Information

Part Number	Package Marking	Ordering Spec	Buck1	Buck2	Supplied As
LM26484SQE	26484SQ	NOPB	PWM	PWM	250 units, tape-and-reel
LM26484SQ	26484SQ	NOPB	PWM	PWM	1000 units, tape-and-reel
LM26484SQX	26484SQ	NOPB	PWM	PWM	4500 units, tape-and-reel

Pin Descriptions

Pins	Name	I/O	Type	Description
1	VIN1	I	PWR	Power in DC source Buck1 PMOS
2	ENSW1	I	D	Enable for Buck1 switcher, a logic HIGH enables Buck1
3	FB1	I	A	Buck1 input feedback terminal
4	AVIN	I	PWR	Analog power for internal circuits
5	FB2	I	A	Buck2 input feedback terminal
6	ENSW2	I	D	Enable for Buck2 switcher, a logic HIGH enables Buck2
7	VIN2	I	PWR	Power in DC source Buck2 PMOS
8	VIN2	I	PWR	Power in DC source Buck2 PMOS
9	SW2	O	A	Buck2 switcher output
10	SW2	O	A	Buck2 switcher output
11	PGND_SW2	G	G	Buck2 NMOS Power Ground
12	PGND_SW2	G	G	Buck2 NMOS Power Ground
13	ENLDO	I	D	Enable for LDO, a logic HIGH enables LDO
14	LDOGATE	O	A	LDO Controller output to NMOS power transistor Gate
15	LDOFB	I	A	LDO Controller input to feedback terminal
16	AGND	G	G	Analog GND
17	GND	G	G	Ground
18	nPOR	O	D	nPOR Active low Reset output. nPOR remains LOW while the input supply is below threshold, and goes HIGH after the threshold is reached and timed delay
19	AVDD	I	PWR	Analog Power Pin
20	PGND_SW1	G	G	Buck1 NMOS Power Ground
21	PGND_SW1	G	G	Buck1 NMOS Power Ground
22	SW1	O	A	Buck1 switcher output
23	SW1	O	A	Buck1 switcher output
24	VIN1	I	PWR	Power in DC source Buck1 PMOS
DAP	DAP	GND	GND	Connection isn't necessary for electrical performance, but it is recommended for better thermal dissipation.

A: Analog Pin **D:** Digital Pin **G:** Ground Pin **PWR:** Power Pin

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN1, VIN2, AVDD, AVIN	−0.3V to +6V
nPOR, ENSW1, FB1, ENSW2, FB2, ENLDO, LDO_FB	−0.3 to VIN + 0.3V
GND to GND SLUG	±0.3V
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering)	260°C

ESD Ratings

Human Body Model (Note 4)	2 kV
Machine Model:	
VIN1,2; SW1,2 PGND1,2	150V
All other pins	200V

Operating Ratings:

VIN1, VIN2, AVDD, AVIN	3.0V to 5.5V
nPOR, ENSW1, ENSW2, ENLDO, LDO_GATE, SW1, SW2	0V to V_{IN} + 0.3V
FB1, FB2	0v to VBuck1 and VBuck2 respectively
LDOFB	0v to V_{LDO}
Power Dissipation (P_{D-MAX}) T_A = 85°C, T_{MAX} = 125°C	1.2W
Junction Temperature (T_J) Range (Note 3)	−40°C to +125°C

Thermal Properties (Notes 5, 6)

Junction-to-Ambient Thermal Resistance (θ_{JA})	33.1°C/W based on a 4-layer 1 oz. PCB
Junction-to-Case Thermal Resistance (θ_{JC})	4.3°C/W

General Electrical Characteristics

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (Notes 2, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Operational Voltage Range	AVDD, AVIN	**3.0**	3.3	**5.5**	V
T_{SD}	Thermal Shutdown	(Note 3)		160		°C
C_{IN}	Input Capacitor	C9, *Figure 1*		10		µF
I_q	Quiescent Current “Off”	VIN = 3.3V, ENSW1, ENSW2, ENLDO = 0		0.03	1	µA

LDO Controller

Unless otherwise noted, AVDD = AVIN 3.3V, PVIN = 1.8V. Typical values and limits appearing in normal type apply for T_A = 25° C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (Notes 2, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Operational Voltage Range	AVIN LDO internal circuits	**3.0**	3.3	**5.5**	V
V_{OUT}	NMOS configuration	Externally configured	**0.8**		**1.5**	V
V_{FB}	Feedback Voltage Accuracy			0.5		V
			−1.5		1.5	%
			−2		**2**	
PSRR	Power Supply Ripple Rejection	F = 10 kHz, Load Current = I_{MAX}		−30		dB
T_{ON}	Turn On Time	Start up from shut-down		500		µsec
C_{FB}	Feedback Capacitor	C11, *Figure 1*		12		pF
C_{OUT}	Output Capacitor C10, (Note 1)	Capacitance for stability: −40°C ≤ T_J ≤ 125°C	**10**	**22**		µF
		ESR (Equivalent Series Resistance)		0.5		Ω

Buck Converters SW1, SW2

Unless otherwise noted, AVDD=AVIN=VIN1=VIN2 = 3.3V, C_{IN} = 10 µF, C_{OUT} = 22 µF, L_{OUT} = 0.5 µH. Buck1 is configured to 1.8V. Buck2 is configured to 1.0V. Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (Notes 2, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	VIN Range	AVDD=VIN1=VIN2	**3.0**	3.3	**5.5**	V
V_{FB}	Feedback Voltage Accuracy			0.5		
			−1.0		+1.0	%
			−1.5		**+1.5**	
ΔV_{OUT}	DC Line Regulation	3.0 < V_{IN} < 3.6 I_O =1000 mA		0.174		%/V
	DC Load Regulation	100 mA < I_O < I_{MAX}		0.75		%/A
f_{OSC}	Oscillator Frequency		1.8	2.0		MHz
I_{PEAK}	Peak Switching Current Limit			3.2		A
R_{DSON} (P)	Pin-Pin Resistance PFET			70	100	mΩ
R_{DSON} (N)	Pin-Pin Resistance NFET			80	100	mΩ
T_{ON}	Turn On Time	Start up from shut-down		500		µsec
C_{IN}	Input Capacitor	Capacitance for stability	10			µF
C_O	Output Capacitor	Capacitance for stability	10	22		µF

I/O Electrical Characteristics

Unless otherwise noted: AVDD=AVIN=VIN1=VIN2 = 3.3V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in boldface type apply over the entire junction temperature range for operation, T_J = -40 to +125°C (Notes 2, 7)

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input Low Level, ENSW1, ENSW2, ENLDO			**0.4**	V
V_{IH}	Input High Level, ENSW1, ENSW2, ENLDO	**0.8*V_{IN}**			V
I_{OH}	nPOR		0.01	**2**	µA
V_{OL}	nPOR		0.125	**0.25**	V
T_{nPOR}	nPOR Delay	60	200	475	msec

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 130°C (typ.)

Note 4: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. (MILSTD - 883 3015.7)

Note 5: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature, the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX} - (\theta_{JA} \times P_{D-MAX})$.

Refer to dissipation rating table for P_{D-MAX} values at different ambient temperatures.

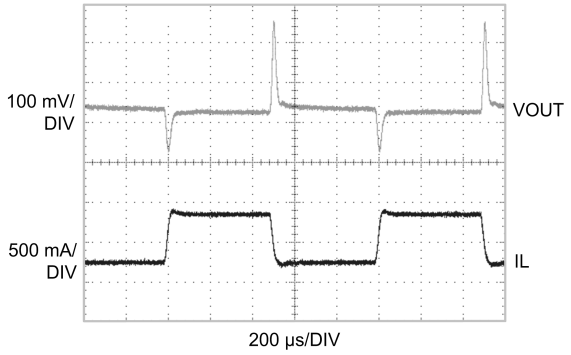
Note 6: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. More information is available in National Semiconductor Application Note AN1187.

Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 8: This specification is guaranteed by design.

Typical Performance Characteristics — LDO T_A = 25°C unless otherwise noted.

Load Transient V_{OUT} — 1.0V, I_{OUT} = 200 mA-1A



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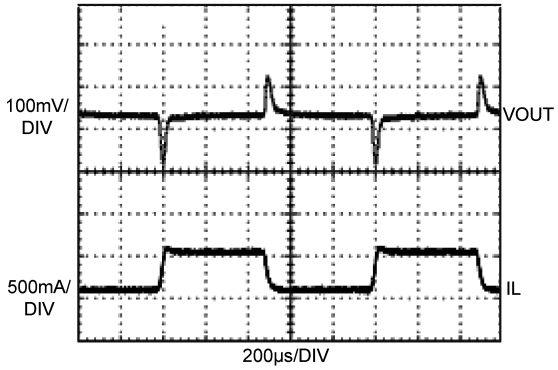
Load Transient V_{OUT} — 1.0V, I_{OUT} = 50 mA- 500 mA



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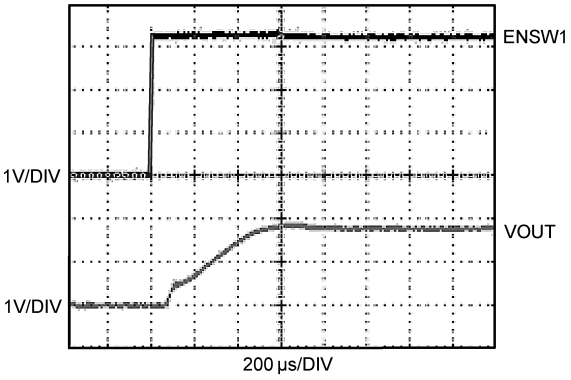
Typical Performance Characteristics — Buck T_A = 25°C unless otherwise noted.

Startup of Buck1: V_{OUT} = 1.8V; I_{OUT} = 100 mA



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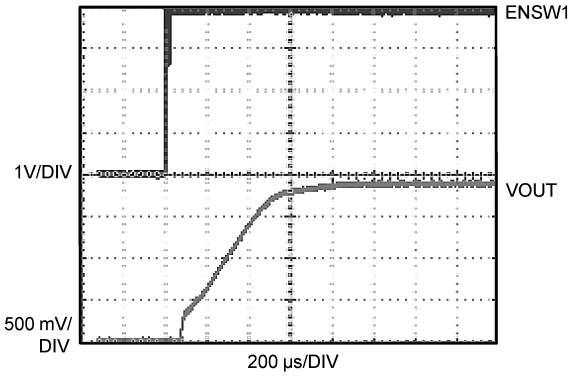
Startup of Buck1: V_{OUT} = 1.8V; I_{OUT} = 2A



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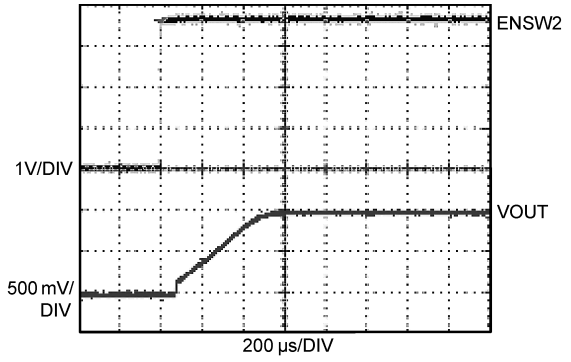
Startup of Buck2: V_{OUT} = 1.0V; I_{OUT} = 100 mA



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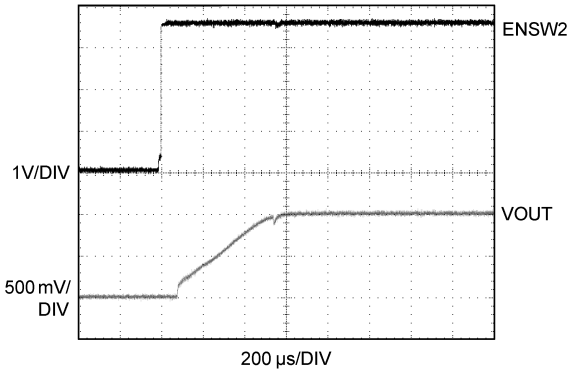
Startup of Buck2: V_{OUT} = 1.0V; I_{OUT} = 2A



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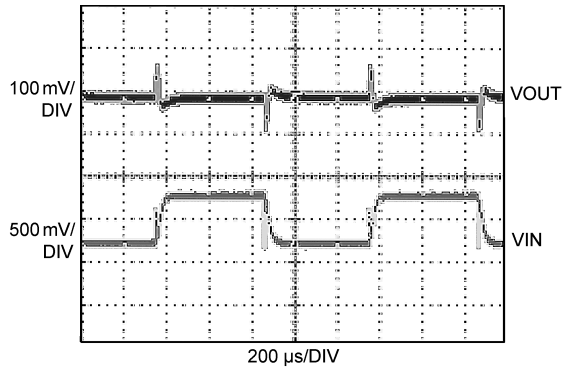
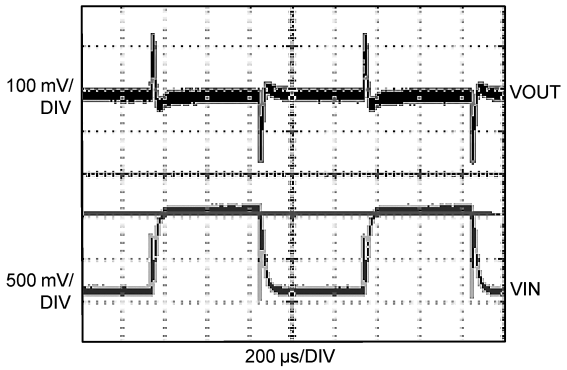
Line Transient: V_{IN} = 3.0V - 3.6V; I_{OUT} = 250 mA; V_{OUT} = 1.8V



30066157

Line Transient: V_{IN} = 3.3V - 4.2V; I_{OUT} = 250 mA; V_{OUT} = 1.0V



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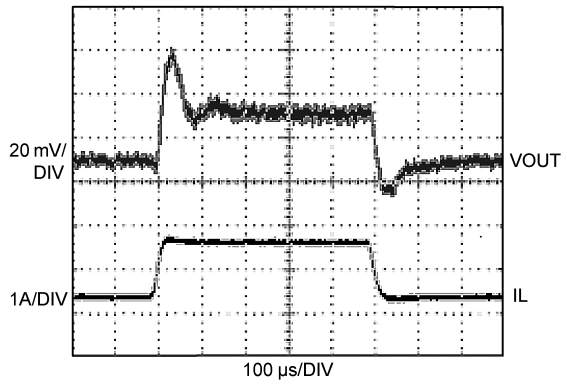
Buck1 Load Transient: V_{IN} = 3.3V; V_{OUT} = 1.8V; I_{OUT} = 250 mA - 1.5A



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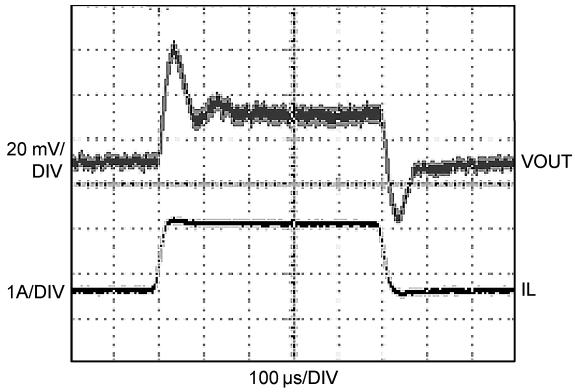
Buck1 Load Transient: V_{IN} = 3.3V; V_{OUT} = 1.8V; I_{OUT} = 500 mA - 2A



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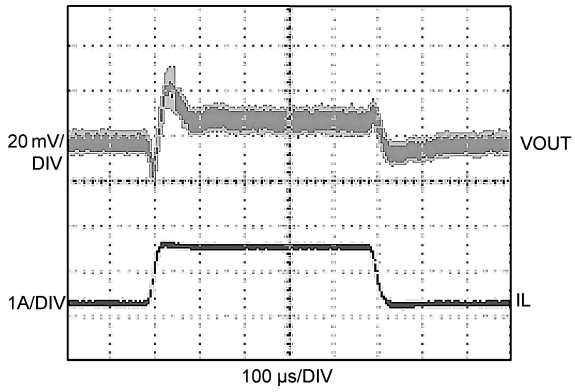
Buck2 Load Transient: V_{IN} = 3.3V; V_{OUT} = 1.0V; I_{OUT} = 250 mA - 1.5A



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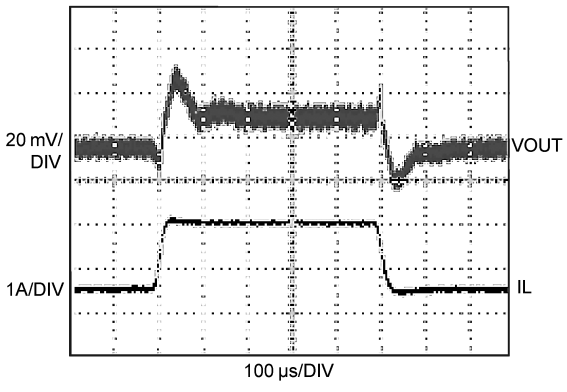
Buck2 Load Transient: V_{IN} = 3.3V; V_{OUT} = 1.0V; I_{OUT} = 500 mA - 2A



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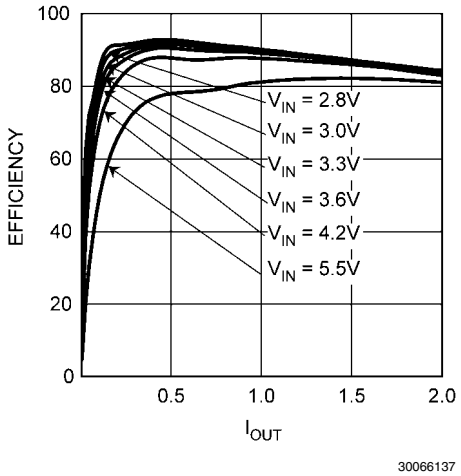
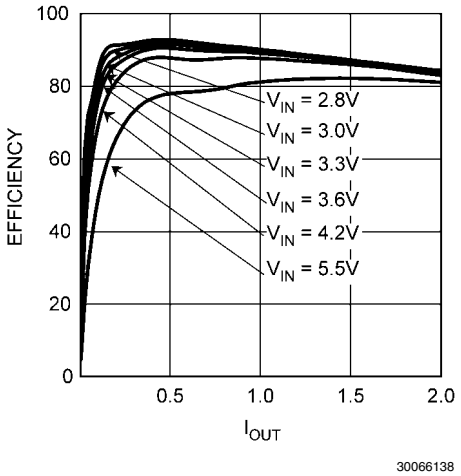
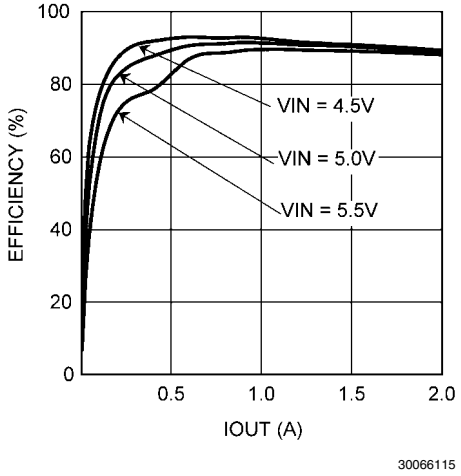
Efficiency of Buck1, V_{OUT} = 1.8V, at Room Temp



Efficiency of Buck2, V_{OUT} = 1.0V, at Room Temp



Efficiency of Buck1, V_{OUT} = 3.5V at Room Temp



Flexible Power Sequencing of Multiple Power Supplies

The two bucks and the LDO in the LM26484 can be individually controlled with ENSW1, ENSW2, and ENLDO, respectively. All the enable inputs need to be either grounded or tied to V_{IH}.

Power-On Reset

The LM26484 provides an active low reset output nPOR. Typical waveform is as shown in *Figure 2* below:

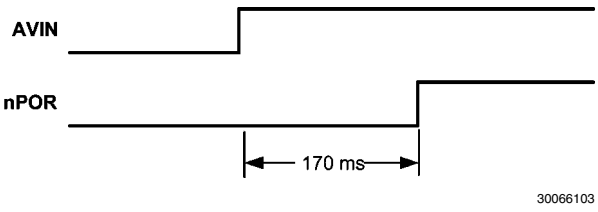


FIGURE 2. Power-On Reset Waveform

LDO Functional Description

The LDO is a linear regulator which targets analog loads characterized by low noise requirements. The LDO is enabled through the ENLDO pin. The output voltage is determined by the configuration of the external feedback resistors, as seen in the typical application circuit (*Figure 1*), R5 and R6.

NO-LOAD STABILITY

The LDO will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

TABLE 1. LDO Configuration and Component Selection Guide

Target	Ideal Resistor Values		Common R Values		Actual V_{OUT} with Com R (V)	Feedback Capacitor
V_{OUT}(V)	R5 (KΩ)	R6 (KΩ)	R5 (KΩ)	R6 (KΩ)		C11 (pF)
0.8	120	200	120	200	0.8	15
0.9	160	200	162	200	0.905	15
1	200	200	200	200	1	15
1.1	240	200	240	200	1.1	15
1.2	280	200	280	200	1.2	12
1.3	320	200	324	200	1.31	12
1.4	360	200	357	200	1.393	10
1.5	400	200	402	200	1.505	10

RESISTOR SELECTION FOR LDO

The output voltage of the LDO on the LM26484 is established by the feed back resistor divider R5 and R6 shown on the typical application circuit (*Figure 1*). The equation for determining V_{OUT} is: $V_{OUT} = V_{FB}*(R5+R6)/R6$, where V_{FB} is the voltage on the LDO_FB pin.

The LDO control loop will force the voltage on V_{FB} to be 0.50V.

Table 1 shows ideal resistor values to establish LDO voltages from 0.8V to 1.5V along with common resistor values to establish these voltages. Common resistors do not always produce the target value. The resulting output voltage using common resistors is also found in *Table 1*. To keep the power consumed by the feedback network low it is recommended that R6 be established as about 200 kΩ. Lesser values of R6 are OK and can be used at the user's discretion.

NFET SELECTION

There are a few major concerns when selecting an NFET for the LM26484 controller. The most important factor to consider is the maximum power rating. It is important for the NFET to have a maximum power rating larger than the application will need. The LM26484 has the ability to drive the gate voltage very close to VIN and down to approximately 1.5V. Selecting an NFET where the guaranteed operation of the V_{GS} is ≥1.5V is important.

Recommended NFET

Part Number	Vendor	V_{GS}	$P_{DISSIPATION}$
Si1450DH	Vishay	1.5V	2.78W

EXTERNAL CAPACITORS

The LDO on the LM26484 requires external capacitors for regulator stability. These are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance. The tolerance and temperature coefficient must be considered when selecting the capacitor to ensure that the capacitance will remain close to ideal over the entire operating temperature range.

FEEDBACK CAPACITOR

A Feedback capacitor is required for stability; recommended values can be seen in *Table 1*. This capacitor must be located a distance of not more than 1 cm from the LDO_FB pin and LDO_OUT. Any good quality ceramic or film capacitor should be used.

OUTPUT CAPACITOR

The LDO on the LM26484 is designed specifically to work with very small ceramic output capacitors. A 10.0 µF ceramic capacitor, marked as C10 in *Figure 1*, temperature types Z5U, Y5V or X7R with ESR between 5 mΩ to 500 mΩ, is suitable for proper operation.

It is also possible to use tantalum or film capacitors, but these are not as attractive for reasons of size and cost. The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 50 mΩ to 500 mΩ for stability.

CAPACITOR CHARACTERISTICS

The LDO is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 44 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 10 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LDO.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependent on the particular case size, with smaller sizes giving poorer performance figures in general.

Buck Regulator Functional Description

The LM26484 incorporates two high efficiency synchronous switching buck regulators which are 180° out of phase, SW1 and SW2 that deliver voltages from a single DC input voltage. Using a voltage mode architecture with synchronous rectification, both bucks have the ability to deliver up to 2A depending on the input voltage and output voltage (voltage head room), and the inductor chosen (maximum current capability).

There are three modes of operation depending on the current required - PWM, PFM, and shutdown. PWM mode handles current loads of approximately 70 mA or higher, delivering voltage precision with high efficiency. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption (I_q = 15 µA typ.) and a longer battery life. The Standby operating mode turns off the device, offering the lowest current consumption. Forced PWM is factory programmed. For Auto PFM-PWM please contact National Semiconductor Sales.

Both SW1 and SW2 can operate up to a 100% duty cycle (PMOS switch always on) for low drop out control of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage.

Additional features include soft-start, under-voltage lockout, current overload protection, and thermal overload protection.

PWM OPERATION

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward voltage inversely proportional to the input voltage is introduced.

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the buck uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

CURRENT LIMITING

A current limit feature allows the converter to protect the LM26484 and any external components during overload conditions. An internal comparator senses the voltage across an internal sense resistor and will turn on the NFET when the output current is sensed at 2.5A (min.) with 0.5 µH inductors. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

PFM OPERATION

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency. For the PFM mode to be enabled, please contact National Semiconductor Sales.

The part will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A. The inductor current becomes discontinuous

or

B. The peak PMOS switch current drops below the I_{MODE} level

$$\left(\text{Typically } I_{MODE} < 66\ \text{mA} + \frac{V_{IN}}{100\Omega}\right)$$

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typ.) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is:

$$I_{PFM} = 66\ \text{mA} + \frac{V_{IN}}{80\Omega}$$

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see *Figure 3*), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is less than 30 µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage to ~1.6% above the nominal PWM output voltage.

If the load current should increase during PFM mode (see *Figure 3*) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

During shutdown the PFET switch, reference, control and bias circuitry of the converters are turned off. The NFET switch will be on in shutdown to discharge the output. When the converter is enabled, soft start is activated. It is recommended to disable the converter during the system power up and under voltage conditions when the supply is less than 3.0V.

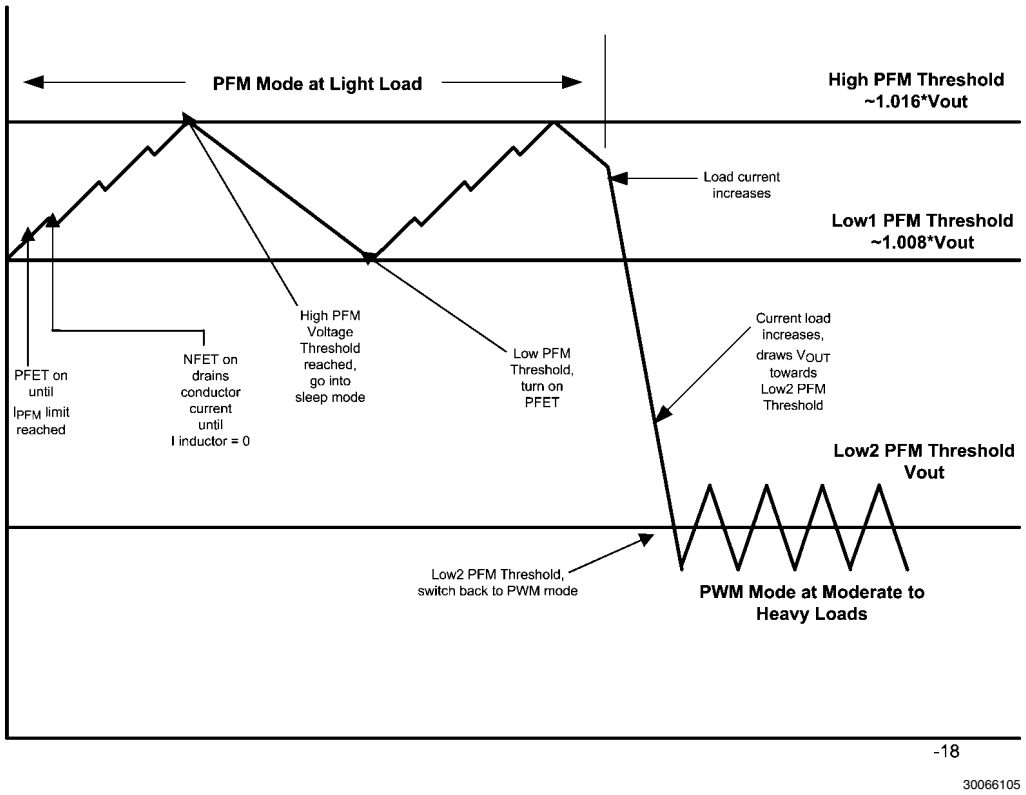


FIGURE 3. PFM vs PWM

SOFT START

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The two LM26484 buck converters have a soft-start circuit that limits in-rush current during start-up or the one which ramps up output voltage linearly over about 500 µs. During start-up the switch current limit is ramped up (100 µs, typ.), depending on the kind of soft-start. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.8V.

LOW DROPOUT OPERATION

The LM26484 can operate at 100% duty cycle (no switching; PMOS switch completely on) for low dropout support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV. The minimum input voltage needed to support the output voltage is

$$V_{IN,}\,MIN = I_{LOAD} * (R_{DSON,\,PFET} + R_{INDUCTOR}) + V_{OUT}$$

— I_{LOAD} Load current

— $R_{DSON,\,PFET}$ Drain to source resistance of PFET switch in the triode region

— $R_{INDUCTOR}$ Inductor resistance

Component Selection

SW1, SW2 OPERATION

TABLE 2. Buck1/2 Configuration and Component Selection Guide

Target	Ideal Resistor Values		Common R Values		Actual V_{OUT} with Com/R (V)	Actual V_{OUT} Delta from Target (V)	Feedback Capacitors	
V_{OUT} (V)	R1/3 (KΩ)	R2/4 (KΩ)	R1/3 (KΩ)	R2/4 (KΩ)	(V)	(V)	C3/6 (pF)	C4/8 (pF)
0.8	120	200	121	200	0.803	0.002	15	none
0.9	160	200	162	200	0.905	0.005	15	none
1	200	200	200	200	1	0	15	none
1.1	240	200	240	200	1.1	0	15	none
1.2	280	200	280	200	1.2	0	12	none
1.3	320	200	324	200	1.31	0.01	12	none
1.4	360	200	357	200	1.393	-0.008	10	none
1.5	400	200	402	200	1.505	0.005	10	none
1.6	440	200	442	200	1.605	0.005	8.2	none
1.7	427	178	432	178	1.713	0.013	8.2	none
1.8	463	178	464	178	1.803	0.003	8.2	none
1.9	498	178	499	178	1.902	0.002	8.2	none
2	450	150	453	150	2.01	0.01	8.2	none
2.1	480	150	475	150	2.083	-0.017	8.2	none
2.2	422	124	422	124	2.202	0.002	8.2	none
2.3	446	124	442	124	2.282	-0.018	8.2	none
2.4	471	124	475	124	2.415	0.015	8.2	none
2.5	400	100	402	100	2.51	0.01	8.2	none
2.6	420	100	422	100	2.61	0.01	8.2	none
2.7	440	100	442	100	2.71	0.01	8.2	33
2.8	460	100	464	100	2.82	0.02	8.2	33
2.9	480	100	475	100	2.875	-0.025	8.2	33
3	500	100	499	100	2.995	-0.005	6.8	33
3.1	520	100	523	100	3.115	0.015	6.8	33
3.2	540	100	536	100	3.18	-0.02	6.8	33
3.3	560	100	562	100	3.31	0.01	6.8	33
3.4	580	100	576	100	3.38	-0.02	6.8	33
3.5	600	100	604	100	3.52	0.02	6.8	33

The Buck control loop will force the voltage on V_{FB} to be 0.50V.

shows ideal resistor values to establish buck voltages from 0.8V to 3.5V along with common resistor values to establish these voltages. Common resistors do not always produce the target value, error is given in the delta column.

In addition to the resistor feedback, feedback capacitors are also required. (— C3/4/6/8) When choosing the output voltage for the two bucks, please take into account the fact that, the factory has optimized the accuracy of Buck1 at the top end of the V_{OUT} range and Buck2 for the bottom end of the V_{OUT} range.

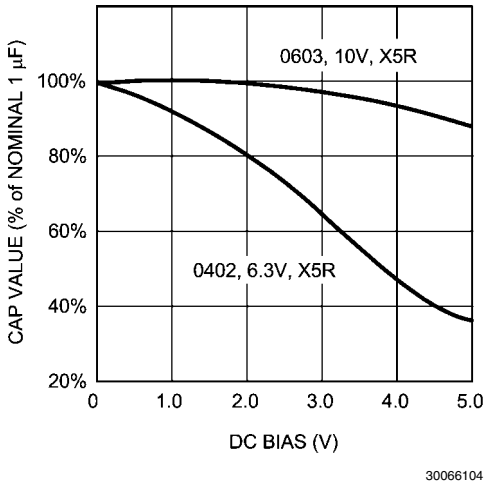


FIGURE 4. Typical Variation in Capacitance vs. DC Bias

As shown in , increasing the DC Bias condition can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 44 µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

OUTPUT INDUCTORS & CAPACITORS FOR SW1 AND SW2

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response;
- Stability;
- Efficiency;
- Output ripple voltage; and
- Over-current ruggedness.

The LM26484 has been optimized for use with nominal values 0.5 µH and 22 µF. If other values are needed for the design, please contact National Semiconductor sales with any concerns.

INDUCTOR SELECTION FOR SW1 AND SW2

A nominal inductor value of 0.5 µH is recommended. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation.

Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25ºC, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

There are two methods to choose the inductor saturation current rating:

Recommended method:

The best way to guarantee the inductor does not saturate is to choose an inductor that has saturation current rating greater than the maximum LM26484 current limit of 3.0A. In this case the device will prevent inductor saturation.

Alternate method:

If the recommended approach cannot be used, care must be taken to guarantee that the saturation current is greater than the peak inductor current:

$$I_{SAT} > IL_{PEAK}$$

$$IL_{PEAK} = I_{OUTMAX} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{L \times F}$$

$$D = \frac{V_{OUT}}{V_{IN} \times EFF}$$

30066106

I_{SAT}: Inductor saturation current at operating temperature

I_{LPEAK}: Peak inductor current during worst case conditions

I_{OUTMAX}: Maximum average inductor current

I_{RIPPLE}: Peak-to-Peak inductor current

V_{OUT}: Output voltage

V_{IN}: Input voltage

L: Inductor value in Henries at I_{OUTMAX}

F: Switching frequency, Hertz

D: Estimated duty factor

EFF: Estimated power supply efficiency

I_{SAT} may not be exceeded during any operation, including transients, startup, high temperature, worst case conditions, etc.

Inductor	Value	Unit	Description	Notes
L1 and L2	0.5	µH	SW1 and SW2 inductor	D.C.R. 50 mΩ

SUGGESTED INDUCTORS AND THEIR SUPPLIERS

Model	Vendor	Dimensions (mm)	DCR (max)
LPS4414–501ML	Coilcraft	4.3 x 4.3 x 1.4	50 mΩ

OUTPUT CAPACITOR SELECTION FOR SW1 AND SW2

A ceramic output capacitor of 10 µF, 6.3V is recommended with an ESR of about 2 mΩ or less.

Output ripple can be estimated from the vector sum of the reactive (Capacitor) voltage component and the real (ESR) voltage component of the output capacitor.

$$V_{COUT} = \frac{I_{RIPPLE}}{8 \times F \times C_{OUT}}$$

$$V_{ROUT} = I_{RIPPLE} \times ESR_{COUT}$$

$$V_{PPOUT} = \sqrt{V_{COUT}^2 + V_{ROUT}^2}$$

V_{COUT}: Estimated reactive output ripple

V_{ROUT}: Estimated real output ripple

V_{PPOUT}: Estimated peak-to-peak output ripple

The output capacitor needs to be mounted as close as possible to the output pin of the device.

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (ESR_{COUT}). ESR_{COUT} is frequency dependent as well as temperature dependent. The R_{ESR} should be calculated with the applicable switching frequency and ambient temperature.

INPUT CAPACITOR SELECTION FOR SW1 AND SW2

It is required to use a ceramic input capacitor of at least 10 µF and 6.3V with an ESR of under 10 mΩ.

The input power source supplies average current continuously. During the PFET switch on-time, however, the demanded di/dt is higher than can be typically supplied by the input power source. This delta is supplied by the input capacitor.

A simplified “worst case” assumption is that all of the PFET current is supplied by the input capacitor. This will result in conservative estimates of input ripple voltage and capacitor RMS current. Input ripple voltage is estimated as follows:

$$V_{PPIN} = \frac{I_{OUT} \times D}{C_{IN} \times F} + I_{OUT} \times ESR_{CIN}$$

V_{PPIN}: Estimated peak-to-peak input ripple voltage
I_{OUT}: Output current, Amps
C_{IN}: Input capacitor value, Farads
ESR_{IN}: Input capacitor ESR, Ohms

This capacitor is exposed to significant RMS current, so it is important to select a capacitor with an adequate RMS current rating. Capacitor RMS current estimated as follows:

$$I_{RMSCIN} = \sqrt{D \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}}{12} \right)^2}$$

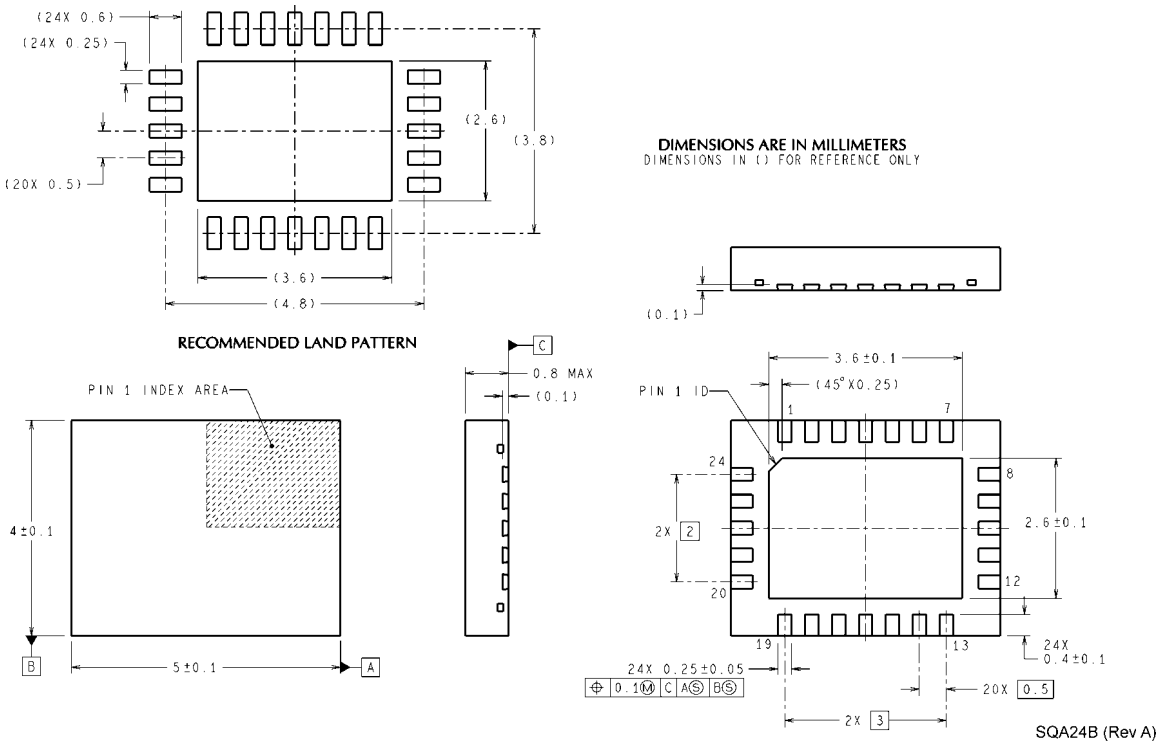
I_{RSCIN} Estimated input capacitor RMS current

Model	Type	Vendor	Voltage Rating	Case Size Inch (mm)
10 µF for CIN or COUT; C9, C2, C1, C5, C7, C10				
GRM21BR60J106K	Ceramic, X7R	Murata	6.3V	0805, (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805, (2012)
LMK212C106KG-T	Ceramic, X7R	Taiyo-Yuden	10V	0805, (2012)
C1608X5R0J106K	Ceramic, X5R	TDK	6.3V	0603, (1608)

Model	Type	Vendor	Voltage Rating	Case Size Inch (mm)
22 µF for COUT; C10, C2, C7				
GRM31CR70J226KE23L	Ceramic, X7R	Murata	6.3V	1206, (3216)
JMK316B7226ML-T	Ceramic, X7R	Taiyo-Yuden	6.3V	1206, (3216)

Capacitor	Min Value	Unit	Description	Recommended Type
C10,	10.0	µF	LDO1 output capacitor	Ceramic, 6.3V, X5R
C2,	10.0	µF	SW1 output capacitor	Ceramic, 6.3V, X5R
C7,	10.0	µF	SW2 output capacitor	Ceramic, 6.3V, X5R

Physical Dimensions inches (millimeters) unless otherwise noted



5 X 4 X 0.8 mm 24-Pin LLP Package
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Notes

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