

Structure Silicon Monolithic Integrated Circuit

Product Name Compound LED Driver for cellular phone

Type BD6083GUL

Features Charge pump system DC/DC

LED Driver for LCD Backlight (3~6ch)

Ambient light sensor interface

Series Regulator (4ch)

### ● Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Limits	Unit
Maximum Applied voltage	VMAX	7	V
Power Dissipation	Pd	1280 note1)	mW
Operating Temperature Range Topr		-30 ∼ +85	°C
Storage Temperature Range	Tstg	-55 ∼ +150	°C

note1) Power dissipation deleting is 10.24mW/  $^{\circ}$ C, when it's used in over 25  $^{\circ}$ C.

(It's deleting is on the board that is ROHM's standard)

Dissipation by LSI should not exceed tolerance level of Pd.

## Operating conditions (VBAT≥VIO, Ta=-30~85 °C)

Parameter	Symbol	Limits	Unit
VBAT input voltage	VBAT	2.7~5.5	V
VIO pin voltage	VIO	1.65~3.3	V

<sup>\*</sup> Radiation-proof is not designed.



## ● Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VIO=1.8V)

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Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
[Circuit Current]				1		<u> </u>
VBAT Circuit current 1	IBAT1	-	0.1	3.0	μA	RESETB=0V, VIO= 0V
VBAT Circuit current 2	IBAT2	-	0.5	3.0	μA	RESETB=0V, VIO=1.8V
VBAT Circuit current 3	IBAT3	-	61	65	mA	DC/DC x1 mode, Io=60mA VBAT=4.0V
VBAT Circuit current 4	IBAT4	-	92	102	mA	DC/DC x1.5 mode, lo=60mA VBAT=3.6V
VBAT Circuit current 5	IBAT5	-	123	140	mA	DC/DC x2 mode, lo=60mA VBAT=2.7V
VBAT Circuit current 6	IBAT6	-	0.25	1.0	mA	ALC Operating ALCEN=1, AD cycle=0.5s setting Except sensor current
VBAT Circuit current 7	IBAT7	-	90	150	μΑ	LDO1,2=ON, I <sub>LDO</sub> =0mA
VBAT Circuit current 8	IBAT8		90	150	μΑ	LDO3,4=ON, I <sub>LDO</sub> =0mA
[LED Driver]						T.
LED current Step (DC Setup)	ILEDSTP1		128		Step	LED1~6
LED current Step (At slope)	ILEDSTP2		256		Step	LED1~6
LED Maximum setup current	IMAXWLED	-	25.6	_	mA	LED1~6
LED current accuracy	IWLED	-7%	15	+7%	mA	I <sub>LED</sub> =15mA setting VLED=1.0V
LED current Matching	ILEDMT	-7 70	13	4	%	Between LED1~6 at VLED=1.0V, ILED=15mA
LED OFF Leak current	ILKLED	-	-	1.0	μA	VLED=4.5V
[DC/DC (Charge Pump)]	ILINEED			1.0	μΛ	VLLD-4.3V
Output Voltage	VoCP	-	Vf+0.2	Vf+0.25	V	Vf is forward voltage of LED
Drive ability	IOUT	-	-	150	mA	VBAT≥3.2V, VOUT=3.9V
,						VBA123.2V, VOOT=3.9V
Switching frequency	fosc	0.8	1.0	1.2	MHz	
Over Voltage Protection detect voltage	OVP	-	5.6	-	V	
Over Current Protection detect Current	OCP	-	250	375	mA	VOUT=0V
[Sensor Interface]						
SBIAS Output Voltage	VoS	2.85	3.0	3.15	V	Io=200μA
SBIAS Maximum Output Current	IomaxS	30	-	-	mA	
SBIAS Discharge resister at OFF	ROFFS	-	1.0	1.5	kΩ	
SSENS Input range	VISS	0	-	VoS× 255/256	V	
ADC resolution	ADRES		8	'	bit	
ADC integral calculus non-linearity	ADINL	-3	-	+3	LSB	
ADC differential calculus	ADDI				1.00	
non-linearity	ADDNL	-1		+1	LSB	
[Regulator]						
		1.164	1.20	1.236	V	Io=50mA
		1.261	1.30	1.339	V	Io=50mA
		1.455	1.50	1.545	V	lo=50mA
		1.552	1.60	1.648	V	Io=50mA
		1.746	1.80	1.854	V	Io=50mA
		2.134	2.20	2.266	V	Io=50mA
		2.328	2.40	2.472	V	Io=50mA
		2.425	2.50	2.575	V	Io=50mA
Output voltage	Vo1	2.522	2.60	2.678	V	Io=50mA
		2.619	2.70	2.781	V	Io=50mA
		2.716	2.80	2.884	V	Io=50mA
		2.813	2.90	2.004	V	Io=50mA
					V	
		2.910	3.00	3.090	V	lo=50mA
		3.007	3.10	3.193		Io=50mA
		3.104	3.20	3.296	V	Io=50mA
		3.201	3.30	3.399	V	Io=50mA



## ● Electrical Characteristics ((Unless otherwise specified, Ta=25°C, VBAT=3.6V, VIO=1.8V)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition	
[Regulator]	[Regulator]						
Output Current	lo1	-	-	150	mA	Vo=* Refer to following	
Dropout Voltage	Vsat1	-	0.2	0.3	V	VBAT=2.5V, Io=150mA, Vo=2.8V setting	
Load stability	∆ Vo11	-	10	60	mV	Io=1~150mA, Vo=* Refer to following	
Input voltage stability	Δ Vo12	-	10	60	mV	VBAT=3.4~4.5V, Io=50mA Vo=* Refer to following	
Ripple Rejection Ratio	RR1	-	65	-	dB	f=100Hz, Vin=200mVp-p, Vo=1.2V setting Io=50mA, BW=20Hz~20kHz	
Short circuit current limit	llim1	-	200	400	mA	Vo=0V	
Discharge resister at OFF	ROFF1	-	1.0	1.5	kΩ		
【SDA, SCL】(I <sup>2</sup> C Interface)							
L level input voltage	VILI	-0.3	-	0.25 × VIO	V		
H level input voltage	VIHI	0.75 x VIO	-	VBAT +0.3	٧		
Hysteresis of Schmitt trigger input	Vhysl	0.05 × VIO	-	-	V		
L level output voltage	VOLI	0	-	0.3	V	SDA Pin, IOL=3 mA	
Input current	linl	-	-	1	μA	Input Voltage = 0.1xVIO~0.9xVIO	
【RESETB】(CMOS Input Pin)					•		
L level input voltage	VILR	-0.3	-	0.25 x VIO	V		
H level input voltage	VIHR	0.75 × VIO	-	VBAT +0.3	<b>V</b>		
Input current	linR	-	-	1	μΑ	Input Voltage = 0.1×VIO~0.9×VIO	
【WPWMIN】 (NMOS Input Pin)	[WPWMIN] (NMOS Input Pin)						
L level input voltage	VILA	-0.3	-	0.3	V		
H level input voltage	VIHA	1.4	-	VBAT +0.3	V		
Input Current	linA	-	3.6	10	μA	Input Voltage = 1.8V	
PWM input minimum High pulse width	PWmin	120	-	-	μs	WPWMIN Pin	
【GC1, GC2】(Sensor Gain Control CMOS Output Pin)							
L level output voltage	VOLS	-	-	0.2	V	IOL=1mA	
H level output voltage	VOHS	VoS -0.2	-	-	V	IOH=1mA	

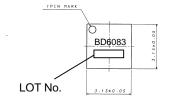
\*Regulator (LDO1): Vo=1.8V Setting

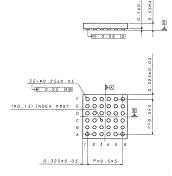
\*Regulator (LDO3) : Vo=1.8V Setting

\*Regulator (LDO2) : Vo=2.5V Setting

\*Regulator (LDO4): Vo=2.8V Setting

## Package

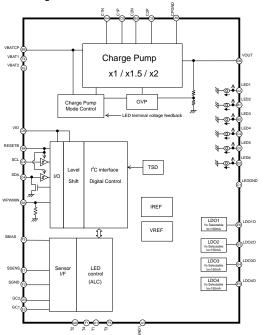




VCSP50L3 (36 Pin) (Unit:mm)



### Block Diagram



#### Pin Functions

PIN	Pin Name	PIN	Pin Name
B6	VBATCP	D6	VOUT
F4	VBAT1	A2	LED1
F5	VBAT2	B1	LED2
A1	T1	B2	LED3
A6	T2	C2	LED4
F6	T3	D1	LED5
F1	T4	D2	LED6
D5	VIO	F3	SBIAS
B4	RESETB	E1	SSENS
D4	SDA	E2	GC1
C4	SCL	D3	GC2
A5	CPGND	F2	SGND
A3	GND1	В3	WPWMIN
C1	LEDGND	E6	LDO10
A4	C1N	E5	LDO2O
C5	C1P	E4	LDO3O
B5	C2N	E3	LDO40
C6	C2P		

### Cautions on use

#### (1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

#### (2) Power supply and ground line

Design PCB pattern to provide low impedance for the wiring between the power supply and the ground lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and ground lines. Especially, when there are ground pattern for small signal and ground pattern for large current included the external circuits, please separate each ground pattern. Furthermore, for all power supply pins to ICs, mount a capacitor between the power supply and the ground pin. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

### (3) Ground voltage

Make setting of the potential of the ground pin so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins are at a potential lower than the ground voltage including an actual electric transient.

## (4) Short circuit between pins and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the ground pin, the ICs can break down.

### (5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

### (6) Input pins

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input pin. Therefore, pay thorough attention not to handle the input pins, such as to apply to the input pins a voltage lower than the ground respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input pins a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

### (7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

#### (8) Thermal shutdown circuit (TSD)

This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

#### (9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

### (10) LDO

Use each output of LDO by the independence. Don't use under the condition that each output is short-circuited because it has the possibility that an operation becomes unstable.

### (11) About the pin for the test, the un-use pin

Prevent a problem from being in the pin for the test and the un-use pin under the state of actual use. Please refer to a function manual and an application notebook. And, as for the pin that doesn't specially have an explanation, ask our company person in charge.

#### (12) About the rush current

For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of wiring.

### (13) About the function description or application note or more.

The function description and the application notebook are the design materials to design a set. So, the contents of the materials aren't always guaranteed. Please design application by having fully examination and evaluation include the external elements.

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