S-8205A/B Series

BATTERY PROTECTION IC FOR 4-SERIES OR 5-SERIES CELL PACK

www.sii-ic.com

Rev.1.1_00

The S-8205A/B Series includes a voltage detection circuit with high accuracy and a delay circuit, in single use, makes it possible for users to monitor the status of 4-series or 5-series cell lithium-ion rechargeable battery.
These ICs are suitable for protecting rechargeable lithium-ion battery packs from overcharge, overdischarge, and overcurrent.

■ Features

(1) High-accuracy voltage detection for each cell
- Overcharge detection voltage n (n = 1 to 5) — 3.55 V to 4.40 V[*1] (50 mV step) — Accuracy ±25 mV
- Overcharge release voltage n (n = 1 to 5) — 3.30 V to 4.40 V[*2] — Accuracy ±50 mV
- Overdischarge detection voltage n (n = 1 to 5) — 2.0 V to 3.2 V[*1] (100 mV step) — Accuracy ±80 mV
- Overdischarge release voltage n (n = 1 to 5) — 2.0 V to 3.4 V[*3] — Accuracy ±100 mV

(2) Discharge overcurrent detection in 2-step
- Discharge overcurrent detection voltage — 0.05 V to 0.30 V[*4] (50 mV step) — Accuracy ±15 mV
- Short circuit detection voltage — 0.50 V to 1.0 V[*4] (100 mV step) — Accuracy ±100 mV

(3) Charge overcurrent detection
- Charge overcurrent detection voltage — –0.30 V to –0.05 V (50 mV step) — Accuracy ±30 mV

(4) Settable by external capacitor; Overcharge detection delay time, Overdischarge detection delay time, Discharge overcurrent detection delay time, Charge overcurrent detection delay time
(Load short circuit detection delay time is internally fixed.)

(5) S-8205A Series: used for 4-series cell, S-8205B Series: used for 5-series cell

(6) Independent charging and discharge control by the control pins

(7) Withstand voltage element — Absolute maximum rating : 28 V

(8) Wide range of operation voltage — 2 V to 24 V

(9) Wide range of operation temperature — –40°C to +85°C

(10) Low current consumption
- Operation mode — 40 µA max. (+25°C)
- Power-down mode — 0.1 µA max. (+25°C)

(11) Lead-free (Sn 100%), halogen-free[*5]

***1.** The overcharge detection voltage n (n = 1 to 5) and overdischarge detection voltage (n = 1 to 5) are not selectable if the voltage difference between them is 0.6 V or less.
***2.** Overcharge hysteresis voltage n (n = 1 to 5) is selectable in 0 V, or in 0.1 V to 0.4 V in 50 mV step.
(Overcharge hysteresis voltage = Overcharge detection voltage – Overcharge release voltage)
***3.** Overdischarge hysteresis voltage n (n = 1 to 5) is selectable in 0 V, or in 0.2 V to 0.7 V in 100 mV step.
(Overdischarge hysteresis voltage = Overdischarge release voltage – Overdischarge detection voltage)
*4. The discharge overcurrent detection voltage and load short circuit detection voltage are not selectable if the voltage difference between them is 0.3 V or less.
***5.** Refer to "■ **Product Name Structure**" for details.

■ Applications

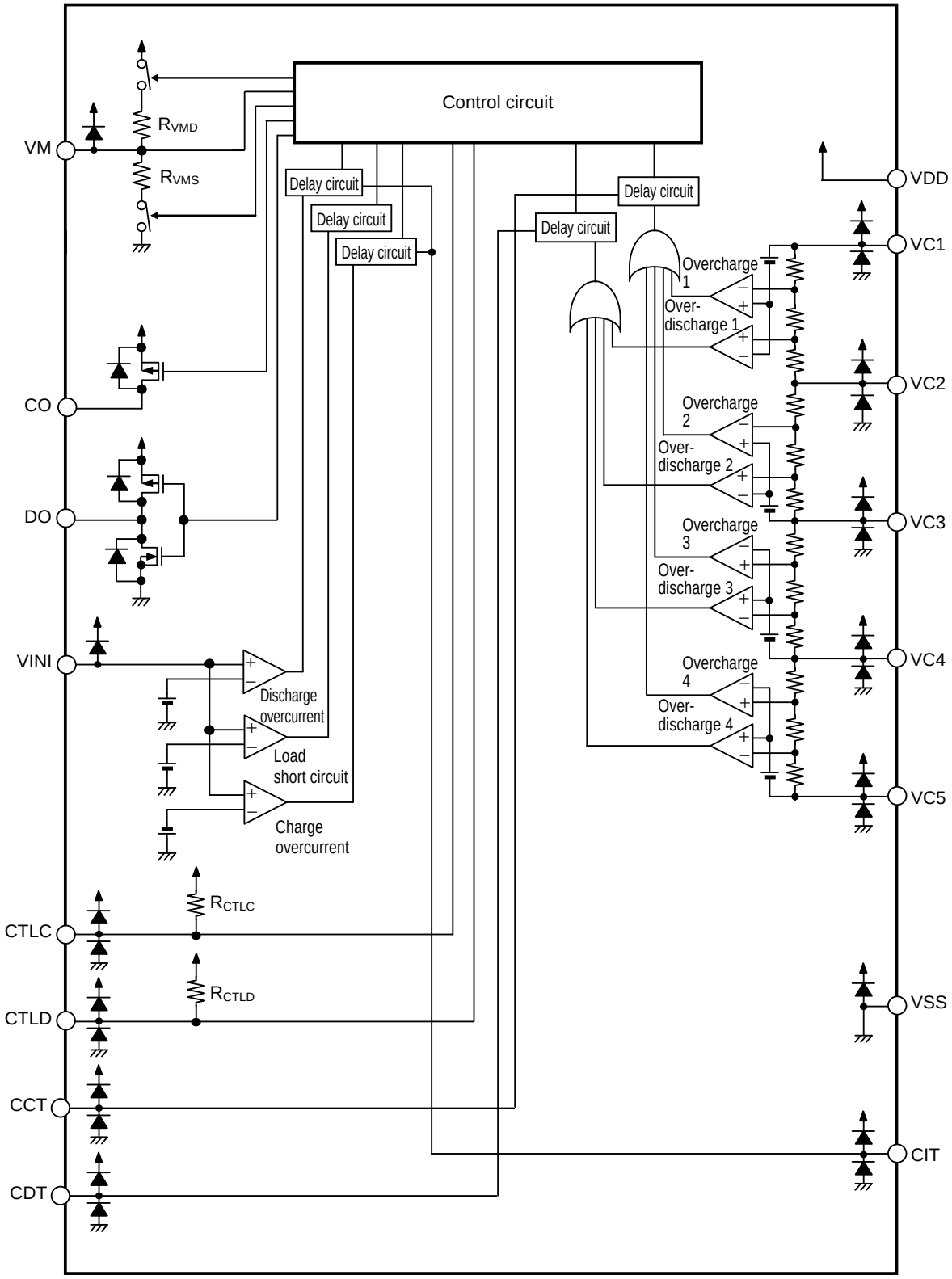
- Rechargeable lithium-ion battery packs

■ Package

- 16-Pin TSSOP

■ Block Diagram

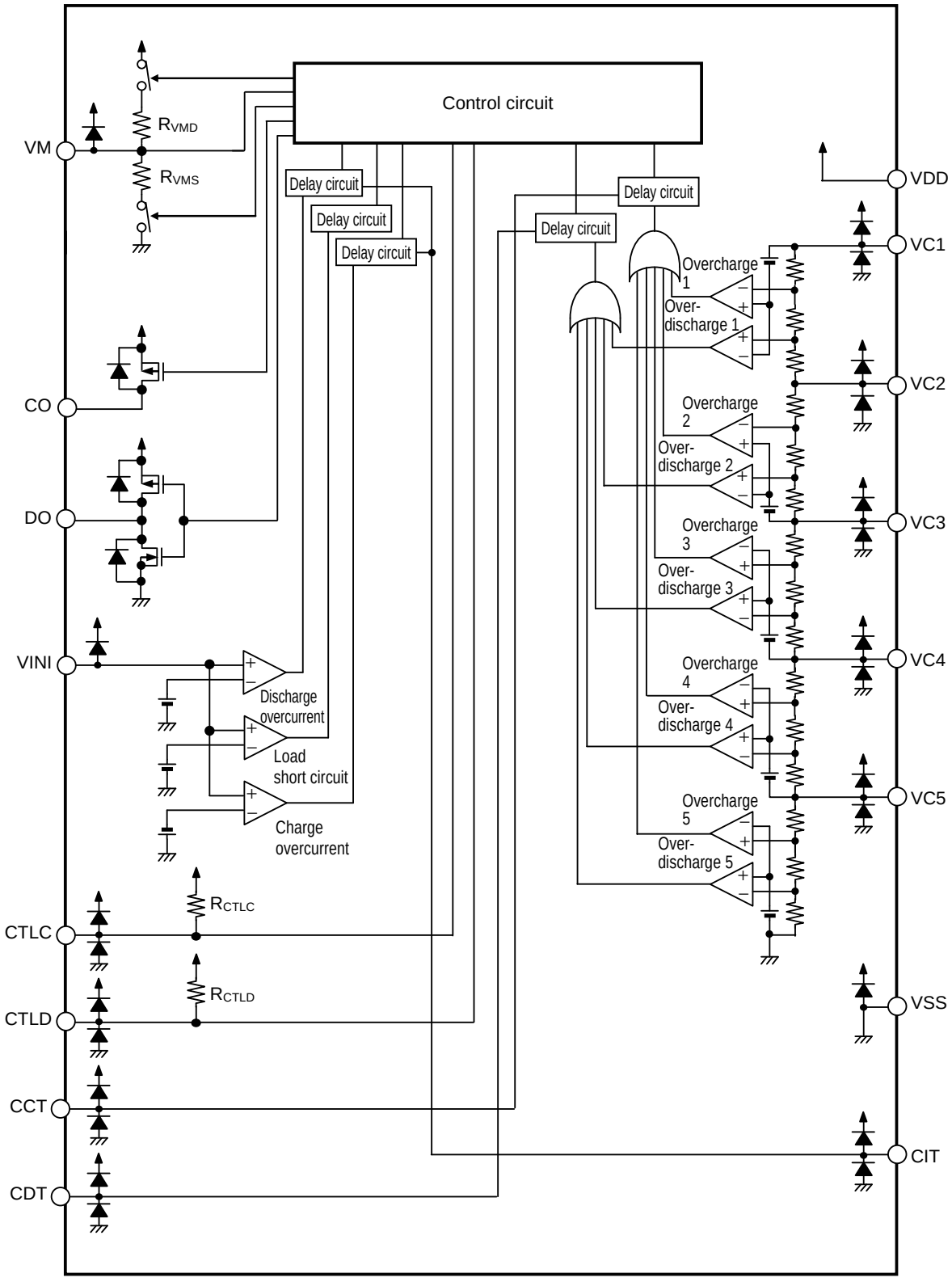
1. S-8205A Series



Remark Diodes in the figure are parasitic diodes.

Figure 1

2. S-8205B Series

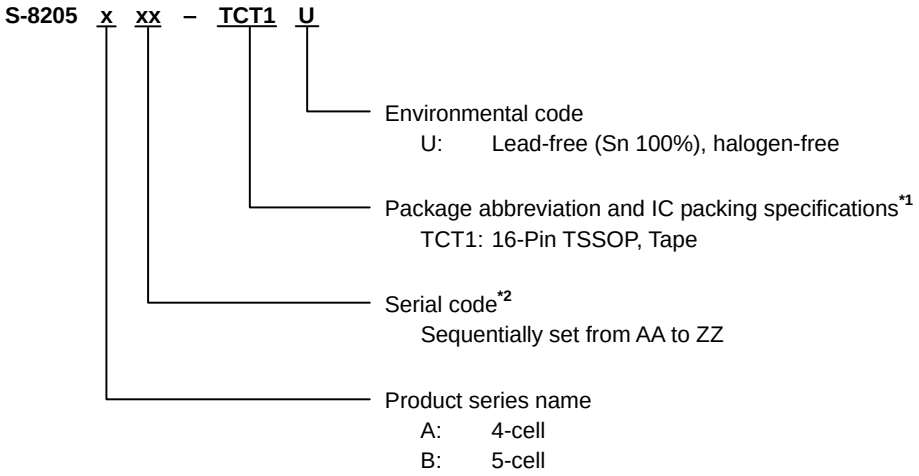


Remark Diodes in the figure are parasitic diodes.

Figure 2

■ Product Name Structure

1. Product Name



***1.** Refer to the tape specifications.
***2.** Refer to "**2. Product Name List**".

2. Package

Package Name	Drawing Code		
	Package	Tape	Reel
16-Pin TSSOP	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-S1

3. Product Name List

Table 1 S-8205A Series (For 4-Series Cell)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent Detection Voltage [V_{DIOV}]	Load Short Circuit Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]	0 V Battery Charge Function
S-8205AAA-TCT1U	4.225 V	4.125 V	2.30 V	3.00 V	0.15 V	0.50 V	–0.10 V	Available
S-8205AAB-TCT1U	4.225 V	4.075 V	2.30 V	3.00 V	0.20 V	0.50 V	–0.10 V	Available

Remark Please contact our sales office for products with detection voltage values other than those specified above.

Table 2 S-8205B Series (For 5-Series Cell)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent Detection Voltage [V_{DIOV}]	Load Short Circuit Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]	0 V Battery Charge Function
S-8205BAA-TCT1U	4.225 V	4.125 V	2.30 V	3.00 V	0.15 V	0.50 V	–0.10 V	Available
S-8205BAB-TCT1U	4.225 V	4.075 V	2.30 V	3.00 V	0.20 V	0.50 V	–0.10 V	Available
S-8205BAC-TCT1U	4.200 V	4.100 V	2.50 V	3.20 V	0.10 V	0.80 V	–0.10 V	Available

Remark Please contact our sales office for products with detection voltage values other than those specified above.

■ Pin Configuration

16-Pin TSSOP
Top view

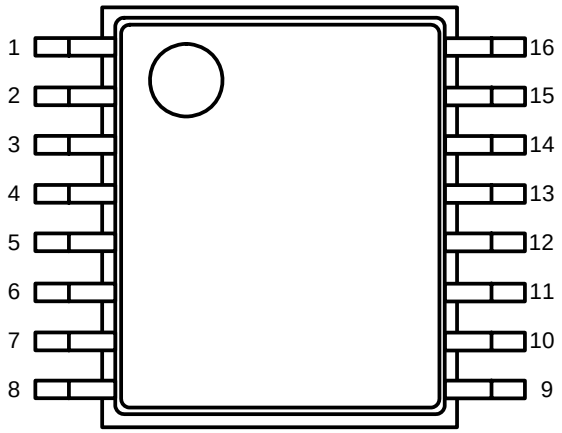


Figure 3

Table 3

Pin No.	Symbol	Description
1	VM	Pin for voltage detection between VSS and VM
2	CO	FET gate connection pin for charge control (Pch open drain output) Pin for voltage detection between VSS and CO
3	DO	FET gate connection pin for discharge control FET (CMOS output)
4	VINI	Pin for voltage detection between VSS and VINI
5	CTLC	Control pin for charge FET
6	CTLD	Control pin for discharge FET
7	CCT	Capacitor connection pin for delay for overcharge detection voltage
8	CDT	Capacitor connection pin for delay for overdischarge detection voltage
9	CIT	Capacitor connection pin for delay for discharge overcurrent detection, charge overcurrent detection
10	VSS	Input pin for negative power supply, Connection pin for battery 5's negative voltage
11	VC5	Connection pin for battery 4's negative voltage, Connection pin for battery 5's positive voltage
12	VC4	Connection pin for battery 3's negative voltage, Connection pin for battery 4's positive voltage
13	VC3	Connection pin for battery 2's negative voltage, Connection pin for battery 3's positive voltage
14	VC2	Connection pin for battery 1's negative voltage, Connection pin for battery 2's positive voltage
15	VC1	Connection pin for battery 1's positive voltage
16	VDD	Input pin for positive power supply, Connection pin for battery 1's positive voltage

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Ratings	Unit
Input voltage between VDD and VSS	V_{DS}	VDD	V_{SS}–0.3 to V_{SS}+28	V
Input pin voltage 1	V_{IN1}	VC1, VC2, VC3, VC4, VC5, CTLC, CTLD, CCT, CDT, CIT	V_{SS}–0.3 to V_{DD}+0.3	V
Input pin voltage 2	V_{IN2}	VM, VINI	V_{DD}–28 to V_{DD}+0.3	V
DO pin output voltage	V_{DO}	DO	V_{SS}–0.3 to V_{DD}+0.3	V
CO pin input and output voltage	V_{CO}	CO	V_{DD}–28 to V_{DD}+0.3	V
Power dissipation	P_D	–	1100*1	mW
Operating ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

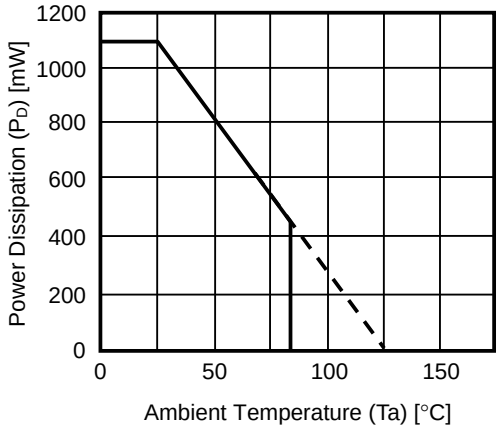


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 5 (1 / 2)

(Ta = +25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
[DETECTION VOLTAGE]							
Overcharge detection voltage n (n = 1, 2, 3, 4, 5)	V_{CUn}	V1 = V2 = V3 = V4 = V5[*1] = V_{CU} – 0.05 V	V_{CU} –0.025	V_{CU}	V_{CU} +0.025	V	2
Overcharge release voltage n (n = 1, 2, 3, 4, 5)	V_{CLn}	–	V_{CL} –0.05	V_{CL}	V_{CL} +0.05	V	2
Overdischarge detection voltage n (n = 1, 2, 3, 4, 5)	V_{DLn}	–	V_{DL} –0.08	V_{DL}	V_{DL} +0.08	V	2
Overdischarge release voltage n (n = 1, 2, 3, 4, 5)	V_{DUn}	–	V_{DU} –0.10	V_{DU}	V_{DU} +0.10	V	2
Discharge overcurrent detection voltage	V_{DIOV}	–	V_{DIO} –0.015	V_{DIOV}	V_{DIOV} +0.015	V	2
Load short circuit detection voltage	V_{SHORT}	–	V_{SHORT} –0.10	V_{SHORT}	V_{SHORT} +0.10	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} –0.03	V_{CIOV}	V_{CIOV} +0.03	V	2
Temperature coefficient 1 [*2]	T_{COE1}	Ta = 0°C to 50°C[*4]	–1.0	0	1.0	mV/°C	–
Temperature coefficient 2 [*3]	T_{COE2}	Ta = 0°C to 50°C[*4]	–0.5	0	0.5	mV/°C	–
[DELAY TIME FUNCTION] [*5]							
CCT pin internal resistance	R_{CCT}	V1 = 4.5 V, V2 = V3 = V4 = V5[*1] = 3.5 V	6.15	8.31	10.2	MΩ	3
CDT pin internal resistance	R_{CDT}	V1 = 1.5 V, V2 = V3 = V4 = V5[*1] = 3.5 V	615	831	1020	kΩ	3
CIT pin internal resistance	R_{CIT}	–	123	166	204	kΩ	3
CCT pin detection voltage	V_{CCT}	V1 = 4.5 V, V2 = V3 = V4 = V5[*1] = 3.5 V	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	3
CDT pin detection voltage	V_{CDT}	V1 = 1.5 V, V2 = V3 = V4 = V5[*1] = 3.5 V	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	3
CIT pin detection voltage	V_{CIT}	V6 = V_{DIOV} + 0.015 V	V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	3
Load short circuit detection delay time	t_{SHORT}	–	100	300	600	µs	2
CTLC pin response time	t_{CTLC}	–	–	–	2.5	ms	2
CTLD pin response time	t_{CTLD}	–	–	–	2.5	ms	2
[0 V BATTERY CHARGE FUNCTION]							
Charger voltage for start charging 0 V battery	V_{0CHA}	available 0 V charging V1 = V2 = V3 = V4 = V5[*1] = 0 V	–	0.8	1.5	V	4
Battery voltage for inhibit charging 0 V battery	V_{0INH}	inhibit 0 V charging	0.4	0.7	1.1	V	2
[INTERNAL RESISTANCE]							
CTLC pin internal resistance	R_{CTLC}	–	7	10	13	MΩ	5
CTLD pin internal resistance	R_{CTLD}	–	7	10	13	MΩ	5
Resistance between VM and VDD	R_{VMD}	V1 = V2 = V3 = V4 = V5[*1] = 1.8 V	450	900	1800	kΩ	5
Resistance between VM and VSS	R_{VMS}	–	250	500	750	kΩ	5

Table 5 (2 / 2)

(Ta = +25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
[INPUT VOLTAGE]							
Operating voltage between VDD and VSS *6	V_{DSOP}	Fixed output voltage of DO and CO	2	–	24	V	–
CTLC change voltage *6	V_{CTLC}	–	2.1	3.0	4.0	V	2
CTLD change voltage *6	V_{CTLD}	–	2.1	3.0	4.0	V	2
[INPUT CURRENT]							
Current consumption during operation	I_{OPE}	–	–	20	40	µA	1
Current consumption during power down	I_{PDN}	V1 = V2 = V3 = V4 = V5*1 = 1.5 V	–	–	0.1	µA	1
VC1 pin current	I_{VC1}	–	0	1.5	3.0	µA	5
VC2 pin current	I_{VC2}	–	–1.0	0	1.0	µA	5
VC3 pin current	I_{VC3}	–	–1.0	0	1.0	µA	5
VC4 pin current	I_{VC4}	–	–1.0	0	1.0	µA	5
VC5 pin current	I_{VC5}	S-8205A Series	–3.0	–1.5	0	µA	5
		S-8205B Series	–1.0	0	1.0	µA	5
[OUTPUT CURRENT]							
CO pin source current	I_{COH}	V13 = 0.5 V	10	–	–	µA	5
CO pin leakage current	I_{COL}	S-8205A Series V1 = V2 = V3 = V4 = 6 V S-8205B Series V1 = V2 = V3 = V4 = V5 = 4.8 V	–	–	0.1	µA	5
DO pin source current	I_{DOH}	V14 = 0.5 V	10	–	–	µA	5
DO pin sink current	I_{DOL}	V15 = 0.5 V	–	–	–10	µA	5

***1.** Because S-8205A Series are the protection ICs for 4-series cell, there is no V5 for them.

***2.** Voltage temperature coefficient 1 : Overcharge detection voltage

***3.** Voltage temperature coefficient 2 : Discharge overcurrent detection voltage

***4.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***5.** Refer to "■ **Operation**" for details of delay time function.

***6.** The S-8205A/B Series does not operate detection if the operating voltage between VDD and VSS (V_{DSOP}) is CTLC change voltage (V_{CTLC}) or CTLD change voltage (V_{CTLD}) or less.

■ Test Circuit

1. Current Consumption during Operation and Power down (Test Circuit 1)

Set S1 and S2 to OFF.

1. 1 Current Consumption during Operation (I_{OPE})

Set V1 = V2 = V3 = V4 = 3.5 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = 3.5 V (S-8205B Series), S2 to ON. I_{SS} is the current consumption during operation (I_{OPE}) at that time.

1. 2 Current Consumption during Power down (I_{PDN})

Set V1 = V2 = V3 = V4 = 1.5 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = 1.5 V (S-8205B Series), S1 to ON. I_{SS} is the current consumption during power down (I_{PDN}) at that time.

2. Overcharge Detection Voltage, Overcharge Release Voltage, Overdischarge Detection Voltage, Overdischarge Release Voltage, Discharge Overcurrent Detection Voltage, Load Short Circuit Detection Voltage, Charge Overcurrent Detection Voltage, CTLC Change Voltage, CTLD Change Voltage, Load Short Circuit Detection Delay Time, CTLC Pin Response Time, CTLD Pin Response Time (Test Circuit 2)

Set S3 to OFF.
Confirm both V_{CO} and V_{DO} are in "H" (its voltage level is $V_{DS} \times 0.9$ V or more) after setting V1 = V2 = V3 = V4 = 3.5 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = 3.5 V (S-8205B Series), V6 = V7 = V8 = 0 V (this status is referred to as initial status 1).

2. 1 Overcharge Detection Voltage (V_{CU1}), Overcharge Release Voltage (V_{CL1})

The overcharge detection voltage (V_{CU1}) is V1 when the V_{CO} is set to "L" (its voltage level is $V_{DS} \times 0.1$ V or less) after increasing V1 gradually after setting V1 = V2 = V3 = V4 = V_{CU} – 0.05 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.05 V (S-8205B Series) from the initial status 1. After that, decreasing V1 gradually, V1 is the overcharge release voltage (V_{CL1}) when the V_{CO} is set to "H" after setting V2 = V3 = V4 = 3.5 V (S-8205A Series), V2 = V3 = V4 = V5 = 3.5 V (S-8205B Series).

2. 2 Overdischarge Detection Voltage (V_{DL1}), Overdischarge Release Voltage (V_{DU1})

The overdischarge detection voltage (V_{DL1}) is V1 when the V_{DO} is set to "L" after decreasing V1 gradually from the initial status 1. After that, increasing V1 gradually, V1 is the overdischarge release voltage (V_{DU1}) when V_{DO} is set to "H".

By changing Vn (n = 2 to 4: S-8205A Series, n = 2 to 5: S-8205B Series), users can define the overcharge detection voltage (V_{CUn}), the overcharge release voltage (V_{CLn}), the overdischarge detection voltage (V_{DLn}), the overdischarge release voltage (V_{DUn}) as well when n = 1.

2. 3 Discharge Overcurrent Detection Voltage (V_{DIOV})

The discharge overcurrent detection voltage (V_{DIOV}) is V6 when V_{DO} is set to "L" after increasing V6 gradually from the initial status 1.

2. 4 Load Short Circuit Detection Voltage (V_{SHORT})

The load short circuit detection voltage (V_{SHORT}) is V6 when V_{DO} is set to "L" after increasing V6 gradually after setting S3 to ON from the initial status 1.

2. 5 Charge Overcurrent Detection Voltage (V_{CIOV})

The charge overcurrent detection voltage (V_{CIOV}) is V6 when V_{CO} is set to "L" after decreasing V6 gradually from the initial status 1.

2. 6 CTLC Change Voltage (V_{CTLC})

The CTLC change voltage (V_{CTLC}) is V7 when V_{CO} is set to "L" after increasing V7 gradually from the initial status 1.

2. 7 CTLD Change Voltage (V_{CTLD})

The CTLD change voltage (V_{CTLD}) is V8 when V_{DO} is set to "L" after increasing V8 gradually from the initial status 1.

2. 8 Load Short Circuit Detection Delay Time (t_{SHORT})

Load short circuit detection delay time (t_{SHORT}) is a period in which V_{DO} changes to "L" after changing V6 to 1.5 V instantaneously, after setting S3 to ON from the initial status 1.

2. 9 CTLC Pin Response Time (t_{CTLC})

CTLC pin response time (t_{CTLC}) is a period in which V_{CO} changes to "L" after changing V7 = V_{DS} instantaneously from the initial status 1.

2. 10 CTLD Pin Response Time (t_{CTLD})

CTLD pin response time (t_{CTLD}) is a period in which V_{DO} changes to "L" after changing V8 = V_{DS} instantaneously from the initial status 1.

3. CCT Pin Internal Resistance, CDT Pin Internal Resistance, CIT Pin Internal Resistance, CCT Pin Detection Voltage, CDT Pin Detection Voltage, CIT Pin Detection Voltage (Test Circuit 3)

Confirm both V_{CO} and V_{DO} are in "H" after setting V1 = V2 = V3 = V4 = 3.5 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = 3.5 V (S-8205B Series), V6 = V9 = V10 = V11 = 0 V (this status is referred to as initial status 2).

3. 1 CCT Pin Internal Resistance (R_{CCT})

The CCT pin internal resistance (R_{CCT}) can be defined by $R_{CCT} = V_{DS} / I_{CCT}$ by using I_{CCT} when setting V1 = 4.5 V from the initial status 2.

3. 2 CDT Pin Internal Resistance (R_{CDT})

The CDT pin internal resistance (R_{CDT}) can be defined by $R_{CDT} = V_{DS} / I_{CDT}$ by using I_{CDT} when setting V1 = 1.5 V from the initial status 2.

3. 3 CIT Pin Internal Resistance (R_{CIT})

The CIT pin internal resistance (R_{CIT}) can be defined by $R_{CIT} = V_{DS} / I_{CIT}$ by using I_{CIT} when setting V6 = V_{DIOV} + 0.015 V from the initial status 2.

3. 4 CCT Pin Detection Voltage (V_{CCT})

The CCT pin detection voltage (V_{CCT}) is V9 when V_{CO} is set to "L" after increasing V9 gradually, after setting V1 = 4.5 V from the initial status 2.

3. 5 CDT Pin Detection Voltage (V_{CDT})

The CDT pin detection voltage (V_{CDT}) is V10 when V_{DO} is set to "L" after increasing V10 gradually, after setting V1 = 1.5 V from the initial status 2.

3. 6 CIT Pin Detection Voltage (V_{CIT})

The CIT pin detection voltage (V_{CIT}) is V11 when V_{DO} is set to "L" after increasing V11 gradually, after setting V6 = V_{DIOV} + 0.015 V from the initial status 2.

4. Charger Voltage for Start Charging 0 V Battery (Product with Function to Charge 0 V Battery) (Test Circuit 4), Battery Voltage for Inhibit Charging 0 V Battery (Product with Function to Inhibit Charging 0 V Battery) (Test Circuit 2)

4. 1 Charger Voltage for Start Charging 0 V Battery (V_{0CHA}) (Product with Function to Charge 0 V Battery)

Charger voltage for start charging 0 V battery (V_{0CHA}) is V12 when V_{CO} is 0.1 V or more after increasing V12 gradually after setting V1 = V2 = V3 = V4 = 0 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = 0 V (S-8205B Series).

4. 2 Battery Voltage for Inhibit Charging 0 V Battery (V_{0INH}) (Product with Function to Inhibit Charging 0 V Battery)

Battery voltage for inhibit charging 0 V battery (V_{0INH}) is V1 when V_{CO} is set to "L" after decreasing V1 gradually from the initial status 1.

5. CTLC Pin Internal Resistance, CTLD Pin Internal Resistance, Resistance between VM and VDD, Resistance between VM and VSS, VC1 Pin Current, VC2 Pin Current, VC3 Pin Current, VC4 Pin Current, VC5 Pin Current, CO Pin Source Current, CO Pin Leakage Current, DO Pin Source Current, DO Pin Sink Current (Test Circuit 5)

Set S1, S5, S6 and S7 to OFF, set S2 and S4 to ON.
Set V1 = V2 = V3 = V4 = 3.5 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = 3.5 V (S-8205B Series), V6 = V13 = V14 = V15 = V16 = 0 V (this status is referred to as initial status 3).

5. 1 CTLC Pin Internal Resistance (R_{CTLC})

In the initial status 3, the value of CTLC pin internal resistance (R_{CTLC}) can be defined by $R_{CTLC} = V_{DS} / I_{CTLC}$ by using I_{CTLC}.

5. 2 CTLD Pin Internal Resistance (R_{CTLD})

In the initial status 3, the value of CTLD pin internal resistance (R_{CTLD}) can be defined by $R_{CTLD} = V_{DS} / I_{CTLD}$ by using I_{CTLD}.

5. 3 Resistance between VM and VDD (R_{VMD})

The value of resistance between VM and VDD (R_{VMD}) can be defined by $R_{VMD} = V_{DS} / I_{VM}$ by using I_{VM} when setting V1 = V2 = V3 = V4 = 1.8 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = 1.8 V (S-8205B Series) from the initial status 3.

5. 4 Resistance between VM and VSS (R_{VMS})

The value of resistance between VM and VSS (R_{VMS}) can be defined by $R_{VMS} = V_{DS} / I_{VM}$ by using I_{VM} when setting V6 = 1.5 V, S2 to OFF, S1 to ON from the initial status 3.

5. 5 VC1 Pin Current (I_{VC1}), VC2 Pin Current (I_{VC2}), VC3 Pin Current (I_{VC3}), VC4 Pin Current (I_{VC4}), VC5 Pin Current (I_{VC5})

In the initial status 3, I_1 is the VC1 pin current (I_{VC1}), I_2 is the VC2 pin current (I_{VC2}), I_3 is the VC3 pin current (I_{VC3}), I_4 is the VC4 pin current (I_{VC4}), I_5 is the VC5 pin current (I_{VC5}).

5. 6 CO Pin Source Current (I_{COH}), CO Pin Leakage Current (I_{COL})

The CO pin source current (I_{COH}) is I_{CO} when setting V13 = 0.5 V from the initial status 3. After that, the CO pin leakage current (I_{COL}) is I_{CO} when setting V1 = V2 = V3 = V4 = 6 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = 4.8 V (S-8205B Series), S4 to OFF, S5 to ON.

5. 7 DO Pin Source Current (I_{DOH}), DO Pin Sink Current (I_{DOL})

The DO pin source current (I_{DOH}) is I_{DO} when setting V14 = 0.5 V, S6 to ON from the initial status 3. After that, the DO pin leakage current (I_{DOL}) is I_{DO} when setting V1 = V2 = V3 = V4 = 1.8 V (S-8205A Series), V1 = V2 = V3 = V4 = V5 = 1.8 V (S-8205B Series), S6 to OFF, S7 to ON, V15 = 0.5 V.

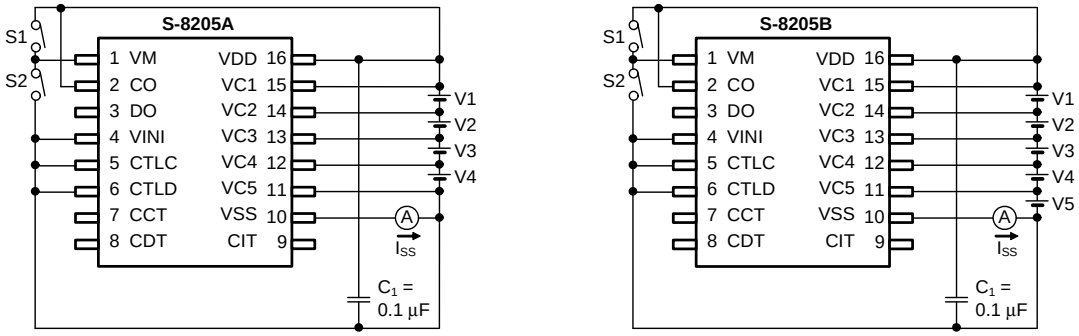


Figure 5 Test Circuit 1

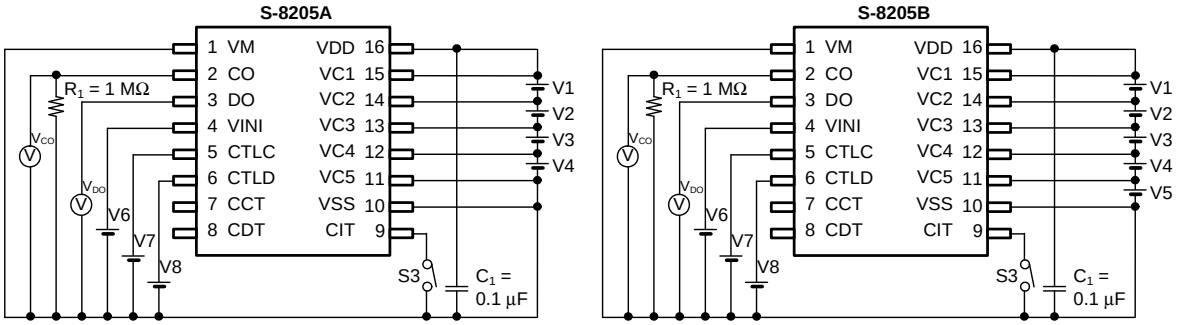


Figure 6 Test Circuit 2

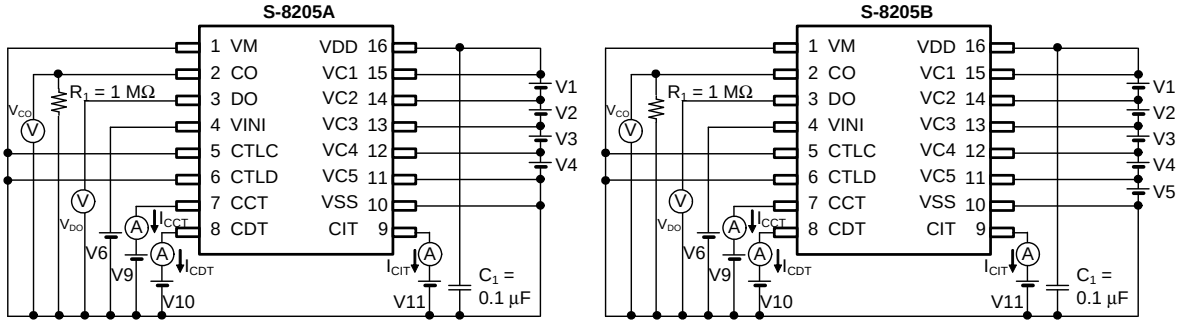


Figure 7 Test Circuit 3

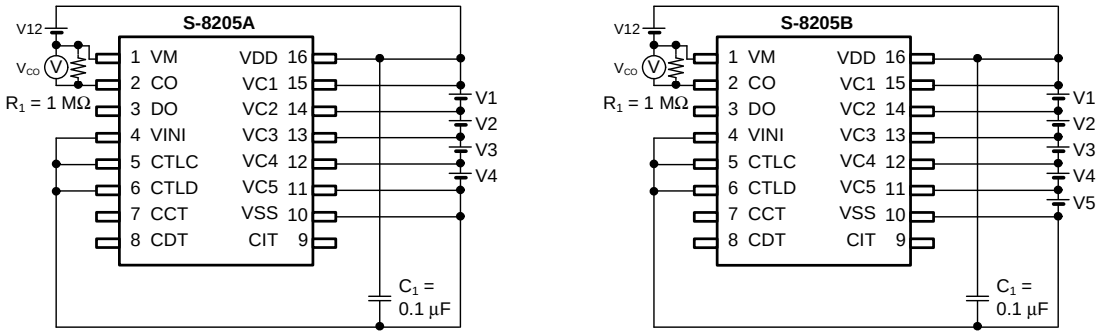


Figure 8 Test Circuit 4

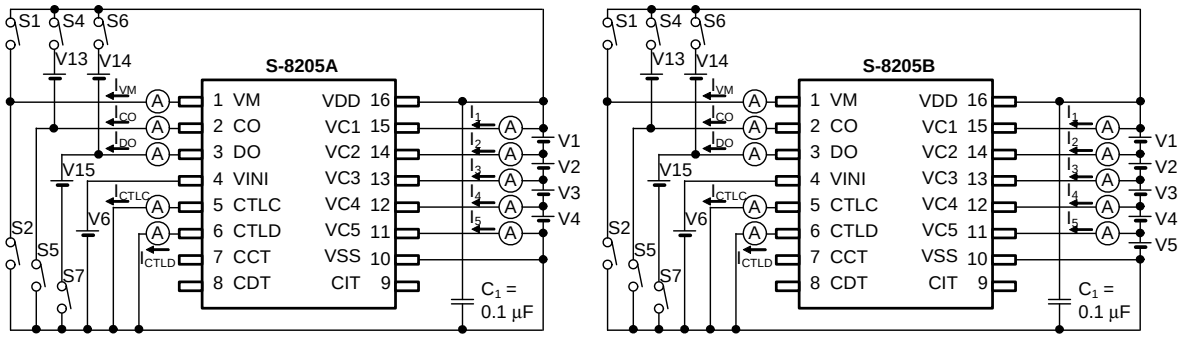


Figure 9 Test Circuit 5

■ Operation

Remark Refer to "■ **Connection Examples of Battery Protection IC**".

1. Normal Status

In the S-8205A/B Series, both of CO and DO pins get the V_{DD} level when all values of battery voltage are in the range of overdischarge detection voltage (V_{DLn}) to overcharge detection voltage (V_{CUn}), and due to the discharge current, the VINI pin's voltage is in the range of charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent detection voltage (V_{DIOV}). This is the normal status. At this time, the charge/discharge FETs are on.

2. Overcharge Status

In the S-8205A/B Series, any voltage of the batteries increases to the level of V_{CUn} or more, the CO pin is set in high impedance. This is the overcharge status. The CO pin is pulled down to EB− by an external resistor so that the charge FET is turned off and it stops charging.

This overcharge status is released if either condition 1 or 2 is satisfied;

(1) In case that the CO pin voltage is 1/50 × V_{DS} or less, and all voltages of the batteries which are V_{CUn} or more are in the level of overcharge release voltage (V_{CLn}) or less.
(2) In case that the VMP pin voltage is 1/50 × V_{DS} or more, and all voltages of the batteries are in the level of V_{CUn} or less.

3. Overdischarge Status

In the S-8205A/B Series, when any voltage of the batteries decreases to the level of V_{DLn} or less, the DO pin voltage gets the V_{SS} level. This is the overdischarge status. The discharge FET is turned off and it stops discharging.

This overcharge status is released if either condition 1 or 2 is satisfied;

(1) In case that the VM pin voltage is in the V_{SS} level or less, and all voltages of the batteries are in the V_{DLn} level or more.
(2) In case that the VM pin voltage is V_{DS}/5 (Typ.) or less and the VM pin voltage is in the V_{SS} level or more, and all voltages of the batteries which are V_{DLn} or less are in the level of overdischarge release voltage (V_{DUn}) or more.

4. Power-down Status

In the S-8205A/B Series, when it reaches the overdischarge status, the VM pin is pulled up to the V_{DD} level by a resistor between VM and VDD pin (R_{VMD}). If the VM pin voltage and the CO pin voltage increase to the level of V_{DS}/5 (Typ.) or more, almost every circuit in the S-8205A/B stops working so that the current consumption decreases to the level of current consumption during power down (I_{PDN}) or less. This is the power-down status.

The power-down status is released if the following condition is satisfied.

(1) The VM pin voltage gets V_{DS}/5 (Typ.) or less.
(2) The CO pin voltage gets V_{DS}/5 (Typ.) or less.

5. Discharge Overcurrent Status

The discharging current increases more than a certain value. As a result, if the status in which the VINI pin voltage increases to the level of V_{DIOV} or more, the DO pin gets the V_{SS} level. This is the discharge overcurrent status. The discharge control FET is turned off and it stops discharging. In the status of discharge overcurrent, the CO pin is set in high impedance. The VM pin is pulled down to the V_{SS} level by a resistor between VM and VSS pin (R_{VMS}).

S-8205A/B Series has two levels for discharge overcurrent detection (V_{DIOV}, V_{SHORT}).
The S-8205A/B Series' actions against load short circuit detection voltage (V_{SHORT}) are as well in V_{DIOV}.

The discharge overcurrent status is released if the following condition is satisfied.

(1) The VM pin voltage gets V_{DS}/10 (Typ.) or less.

6. Charge Overcurrent Status

In the S-8205A/B Series, the charge current increases more than a certain value. As a result, if the status in which the VINI pin voltage decreases to the level of V_{CIOV} or less, the CO pin is set in high impedance. This is the charge overcurrent status. The charge control FET is turned off and it stops charging. In this charge overcurrent status, DO pin gets the V_{SS} level. The VM pin is pulled-up to the V_{DD} level by resistance between VM and VDD (R_{VMD}).

The status of charge overcurrent is released if the following condition is satisfied.

(1) The CO pin voltage gets $1/50 \times V_{DS}$ (Typ.) or more.

7. 0 V Battery Charge Function

In the S-8205A/B Series, regarding how to charge a discharged battery (0 V battery), users are able to select either function of the two mentioned below.

(1) Enable to charge a 0 V battery
A 0 V battery is charged when charger voltage is more than voltage for start charging 0 V battery (V_{0CHA}).

(2) Inhibit charging a 0 V battery
A 0 V battery is not charged when any battery voltage is battery voltage for inhibit charging 0 V battery (V_{0INH}) or less.

Caution When the VDD pin voltage is less than the minimum value of operation voltage between VDD and VSS pin (V_{DSOP}), the S-8205A/B Series' action is not assured.

8. Delay Time Setting

In the S-8205A/B Series, users are able to set delay time for the period; from detecting any voltage of the batteries or detecting changes in the voltage at the VINI pin, to the output to the CO, DO pin. Each delay time is determined by a resistor in the IC and an external capacitor.

In the overchage detection, when any voltage of the batteries gets V_{CUn} or more, the S-8205A/B starts charging to the CCT pin's capacitor (C_{CCT}) via the CCT pin's internal resistor (R_{CCT}). After a certain period, the CO pin is set in high impedance if the voltage at the CCT pin reaches the CCT pin detection voltage (V_{CCT}). This period is overcharge detection delay time (t_{CU}).

t_{CU} is calculated using the following equation ($V_{DS} = V1 + V2 + V3 + V4 + V5$).

$$t_{CU}\ [s] = -\ln (1 - V_{CCT} / V_{DS}) \times C_{CCT}\ [\mu F] \times R_{CCT}\ [M\Omega]$$
$$= -\ln (1 - 0.7\ (Typ.)) \times C_{CCT}\ [\mu F] \times 8.31\ [M\Omega]\ (Typ.)$$
$$= 10.0\ [M\Omega]\ (Typ.) \times C_{CCT}\ [\mu F]$$

Overdischarge detection delay time (t_{DL}), discharge overcurrent detection delay time (t_{DIOV}), charge overcurrent detection delay time (t_{CIOV}) are calculated using the following equations as well.

$$t_{DL}\ [ms] = -\ln (1 - V_{CDT} / V_{DS}) \times C_{CDT}\ [\mu F] \times R_{CDT}\ [k\Omega]$$
$$t_{DIOV}\ [ms] = -\ln (1 - V_{CIT} / V_{DS}) \times C_{CIT}\ [\mu F] \times R_{CIT}\ [k\Omega]$$
$$t_{CIOV}\ [ms] = -\ln (1 - V_{CIT} / V_{DS}) \times C_{CIT}\ [\mu F] \times R_{CIT}\ [k\Omega]$$

In case $C_{CCT} = C_{CDT} = C_{CIT} = 0.1\ [\mu F]$, each delay time t_{CU}, t_{DL}, t_{DIOV}, t_{CIOV} is calculated as follows.

$t_{CU}\ [s] = 10.0\ [M\Omega]\ (Typ.) \times 0.1\ [\mu F] = 1.0\ [s]\ (Typ.)$
$t_{DL}\ [ms] = 1000\ [k\Omega]\ (Typ.) \times 0.1\ [\mu F] = 100\ [ms]\ (Typ.)$
$t_{DIOV}\ [ms] = 200\ [k\Omega]\ (Typ.) \times 0.1\ [\mu F] = 20\ [ms]\ (Typ.)$
$t_{CIOV}\ [ms] = 200\ [k\Omega]\ (Typ.) \times 0.1\ [\mu F] = 20\ [ms]\ (Typ.)$

Load short circuit detection delay time (t_{SHORT}) is fixed internally.

9. CTLC and CTLD Pins

The S-8205A/B Series has two pins to control.
The CTLC pin controls the CO pin, the CTLD pin controls the DO pin. Thus it is possible for users to control the CO pin and DO pin independently. These controls precede the battery protection circuit.

Table 6 Conditions Set by CTLC Pin

CTLC Pin	CO Pin
CTLC pin voltage ≥ V_{CTLC}	High impedance
Open*1	High impedance
CTLC pin voltage < V_{CTLC}	Normal status*2

***1.** Pulled up by R_{CTLC} when CTLC pin is open
***2.** The status is controlled by the voltage detection circuit.

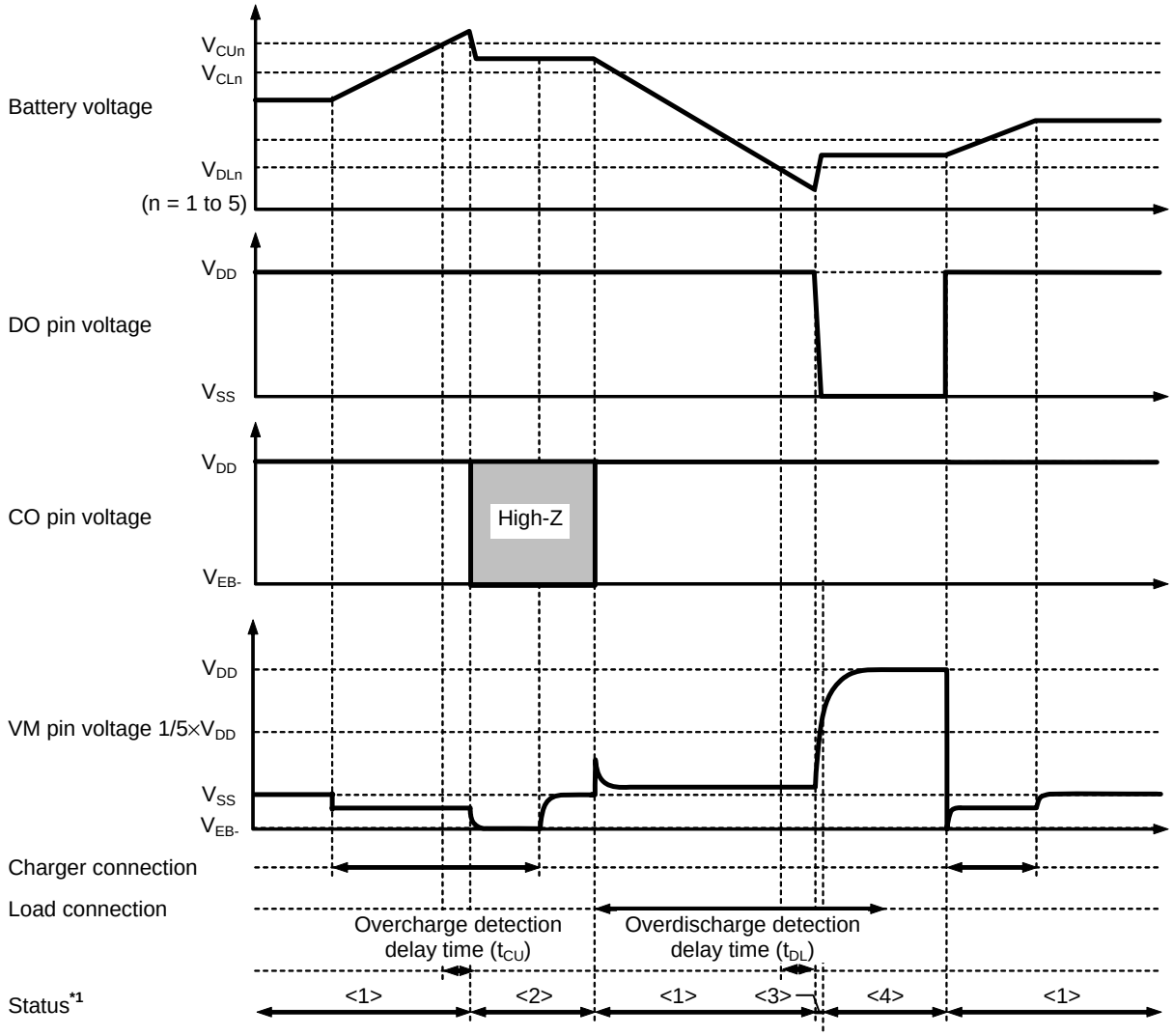
Table 7 Conditions Set by CTLD Pin

CTLD Pin	DO Pin
CTLD pin voltage ≥ V_{CTLD}	V_{SS} level
Open*1	V_{SS} level
CTLD pin voltage < V_{CTLD}	Normal status*2

***1.** Pulled up by R_{CTLD} when CTLD pin is open
***2.** The status is controlled by the voltage detection circuit.

■ Timing Chart

1. Overcharge Detection and Overdischarge Detection

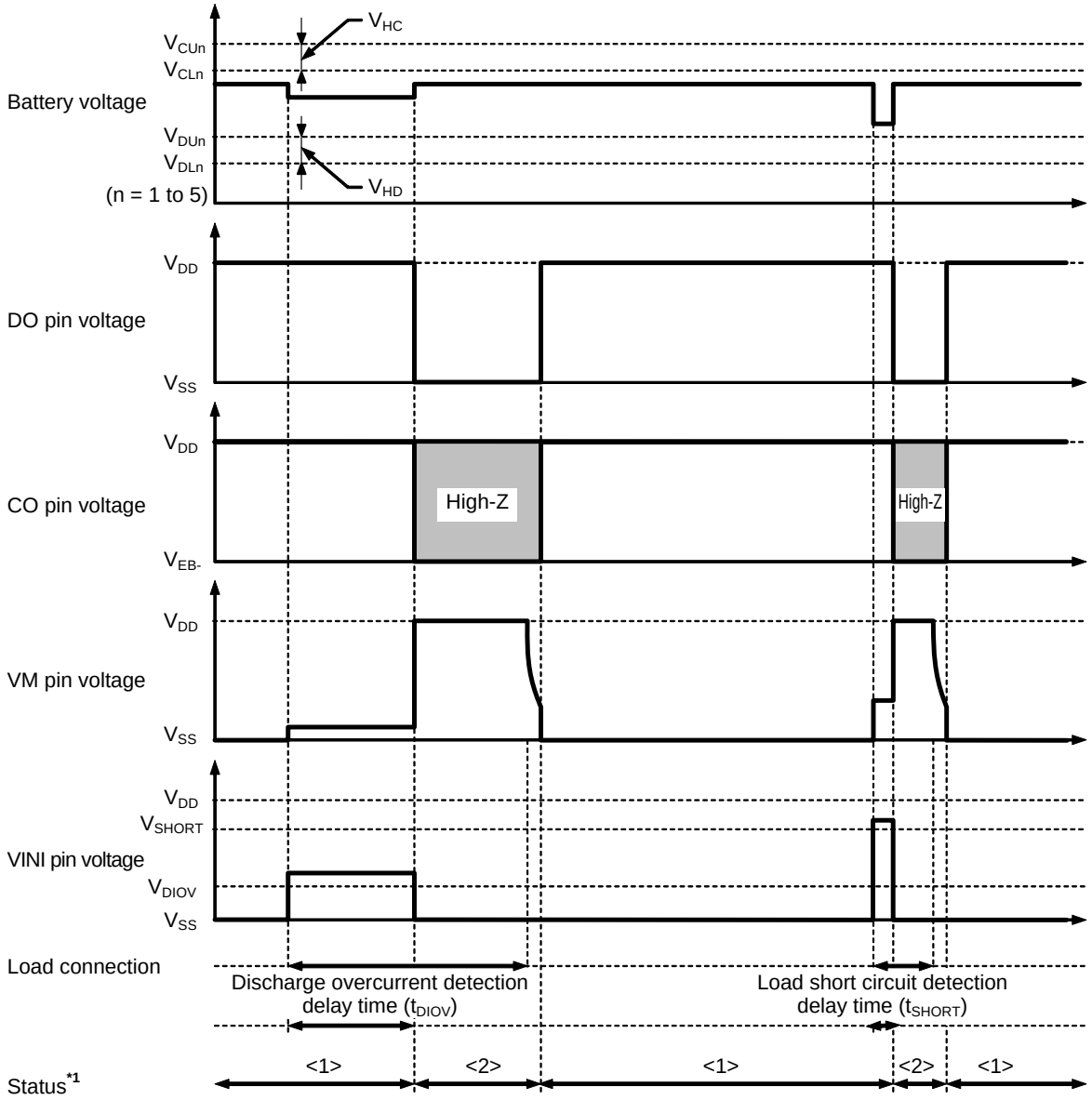


***1.** <1> : Normal status
<2> : Overcharge status
<3> : Overdischarge status
<4> : Power-down status

Remark The charger is assumed to charge with a constant current. V_{EB-} indicates the open voltage of the charger.

Figure 10

2. Discharge Overcurrent Detection

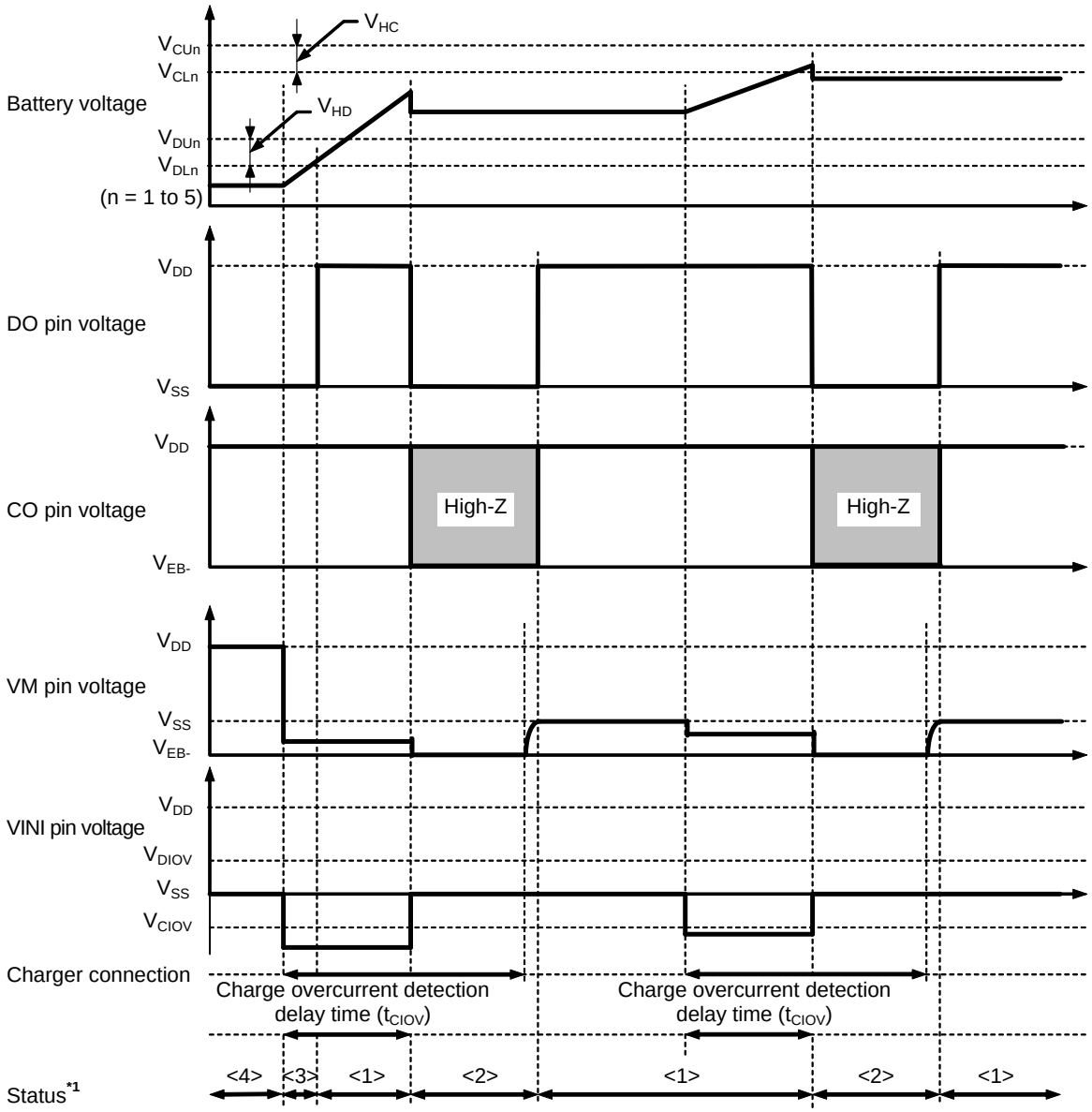


***1.** <1> : Normal status
<2> : Discharge overcurrent status

Remark The charger is assumed to charge with a constant current. V_{EB-} indicates the open voltage of the charger.

Figure 11

3. Charge Overcurrent Detection



***1.** <1> : Normal status
<2> : charge overcurrent status
<3> : Overdischarge status
<4> : Power-down status

Remark The charger is assumed to charge with a constant current. V_{EB-} indicates the open voltage of the charger.

Figure 12

■ Connection Examples of Battery Protection IC

1. S-8205A Series (4-Series Cell)

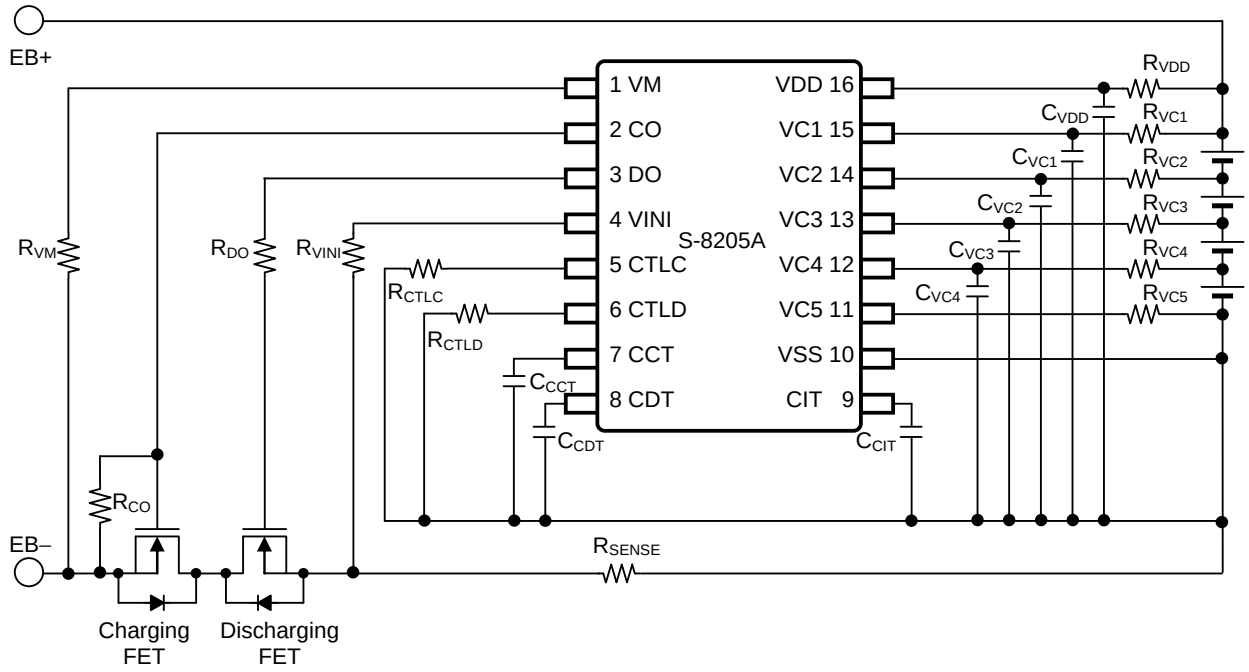


Figure 13

2. S-8205B Series (5-Series Cell)

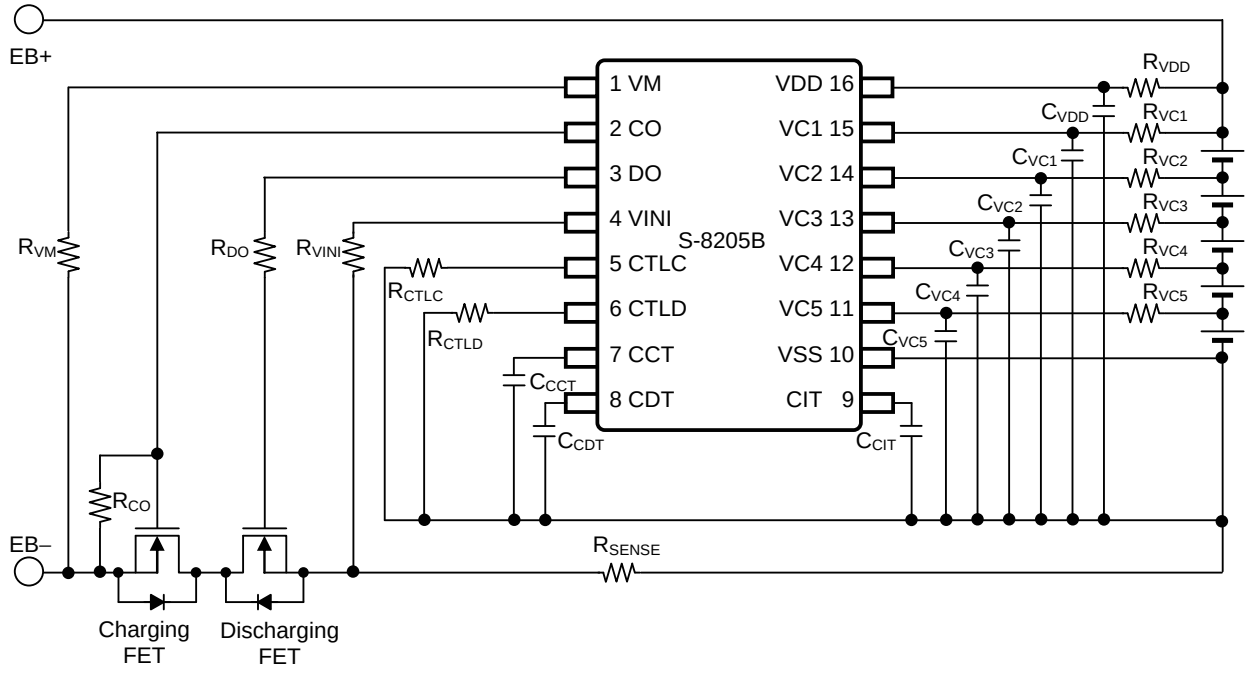


Figure 14

■ Application Circuit

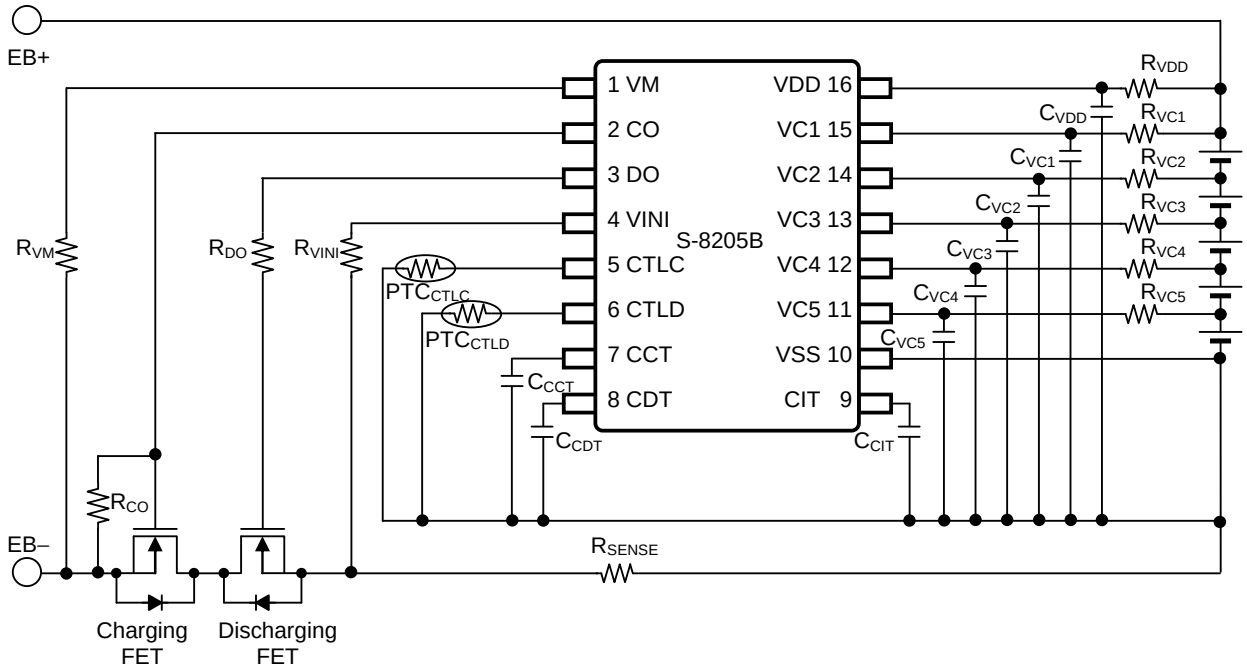


Figure 15 Overheat Protection via PTC

[For PTC, contact]

Murata Manufacturing Co., Ltd.
Thermistor Products Department
Nagaokakyo-shi, Kyoto 617-8555 Japan
TEL +81-75-955-6863
Contact Us: http://www.murata.com/contact/index.html

Table 8 Constants for External Components

Symbol	Typical	Range	Unit
R_{VC1}	1	0.47 to 1*1	kΩ
R_{VC2}	1	0.47 to 1*1	kΩ
R_{VC3}	1	0.47 to 1*1	kΩ
R_{VC4}	1	0.47 to 1*1	kΩ
R_{VC5}	1	0.47 to 1*1	kΩ
R_{DO}	5.1	1 to 10	kΩ
R_{CO}	1	0.1 to 1	MΩ
R_{VM}	5.1	3 to 10	kΩ
R_{CTLC}	1	0.1 to 1	kΩ
R_{CTLD}	1	0.1 to 1	kΩ
R_{VINI}	1	0.1 to 1	kΩ
R_{SENSE}	–	0 or higher	mΩ
R_{VDD}	100	43 to 100*1	Ω
C_{VC1}	0.1	0.068 to 1*1	µF
C_{VC2}	0.1	0.068 to 1*1	µF
C_{VC3}	0.1	0.068 to 1*1	µF
C_{VC4}	0.1	0.068 to 1*1	µF
C_{VC5}	0.1	0.068 to 1*1	µF
C_{CCT}	0.1	0.01 or higher	µF
C_{CDT}	0.1	0.01 or higher	µF
C_{CIT}	0.1	0.02 or higher	µF
C_{VDD}	1	0 to 10*1	µF

***1.** Set up a filter constant to be $R_{VDD} \times C_{VDD} = 68\ \mu F \bullet \Omega$ or more, and to be $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VC4} \times C_{VC4} = R_{VC5} \times C_{VC5} = R_{VDD} \times C_{VDD}$.

Caution 1. The above constants may be changed without notice.

2. It is recommended that filter constants between VDD and VSS should be set approximately to 100 µF • Ω.
e.g., $C_{VDD} \times R_{VDD} = 1.0\ \mu F \times 100\ \Omega = 100\ \mu F \bullet \Omega$
Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants. Contact our sales office in case the constants should be set to other than 100 µF • Ω.

3. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

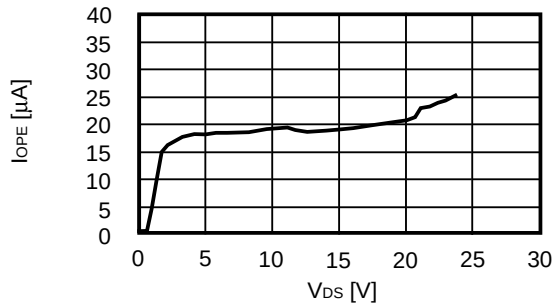
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order, however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VM pin and VSS pin or connect the battery charger to return to the normal mode.
- If both an overcharge battery and an overdischarge battery are included among the whole batteries, the condition is set in overcharge status and overdischarge status. Therefore either charging or discharging is impossible.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

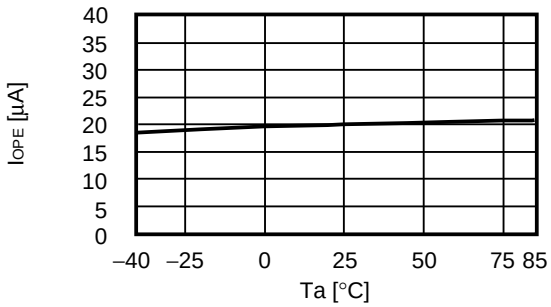
■ Characteristics (Typical Data)

1. Current Consumption

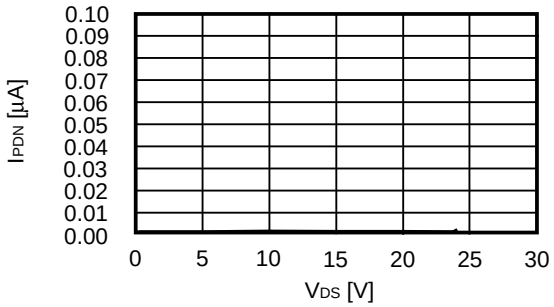
1. 1 I_{OPE} vs V_{DS}



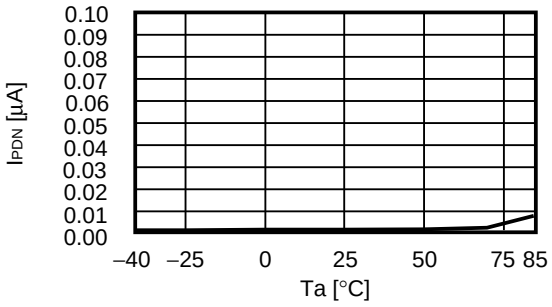
1. 2 I_{OPE} vs Ta



1. 3 I_{PDN} vs V_{DS}

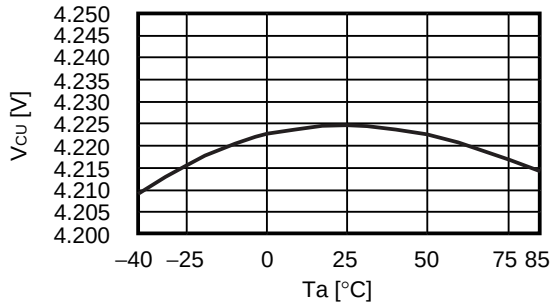


1. 4 I_{PDN} vs Ta

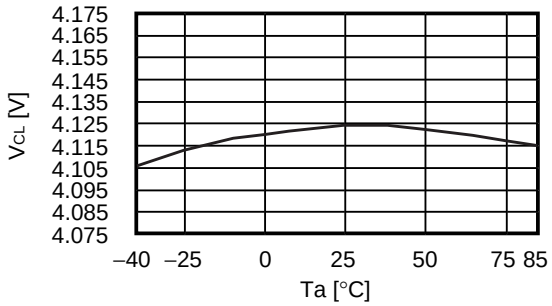


2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Discharge Overcurrent Detection Voltage, Load Short Circuit Detection Voltage, Charge Overcurrent Detection Voltage

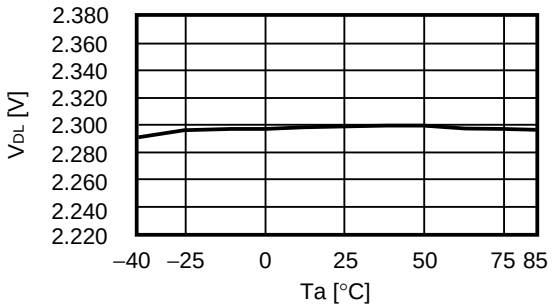
2. 1 V_{CU} vs Ta



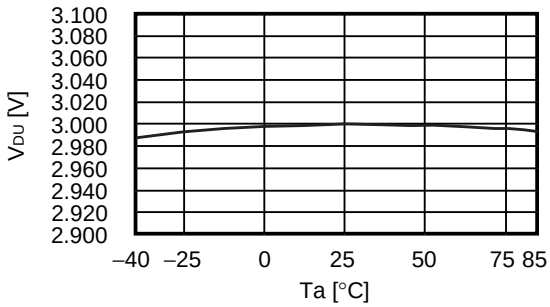
2. 2 V_{CL} vs Ta



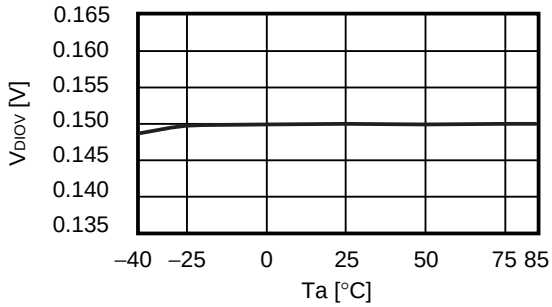
2. 3 V_{DL} vs Ta



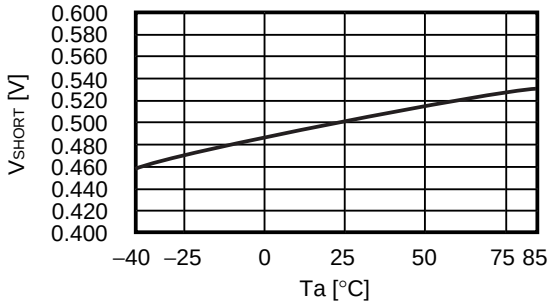
2. 4 V_{DU} vs Ta



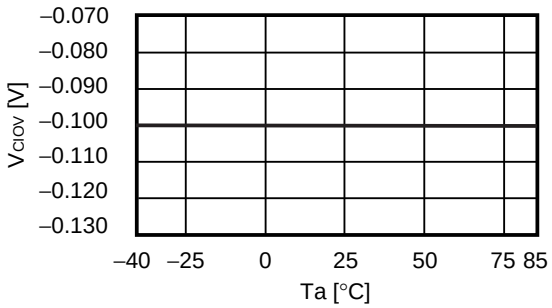
2. 5 V_{DIOV} vs Ta



2. 6 V_{SHORT} vs Ta

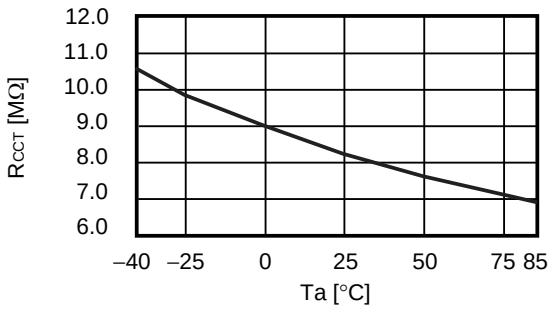


2. 7 V_{CIOV} vs Ta

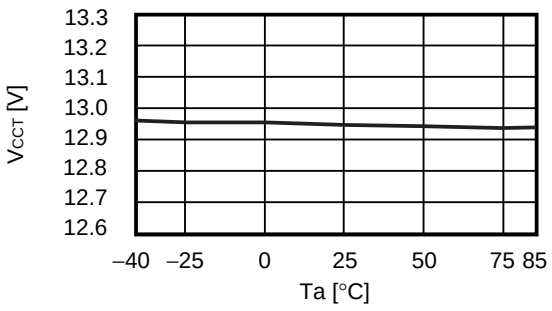


3. CCT pin Internal Resistance / Detection Voltage, CDT pin Internal Resistance / Detection Voltage, CIT pin Internal Resistance / Detection Voltage and Short circuit Detection Voltage Delay Time

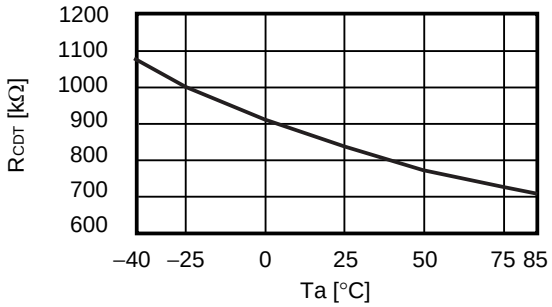
3. 1 R_{CCT} vs Ta



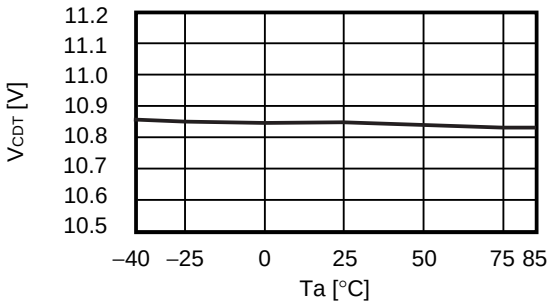
3. 2 V_{CCT} vs Ta (V_{DS} = 18.5 V)



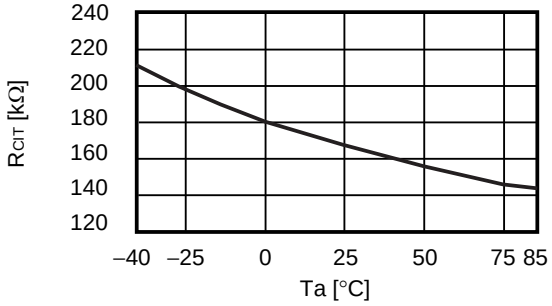
3. 3 R_{CDT} vs Ta



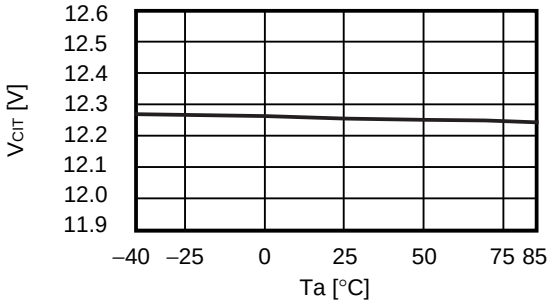
3. 4 V_{CDT} vs Ta (V_{DS} = 15.5 V)



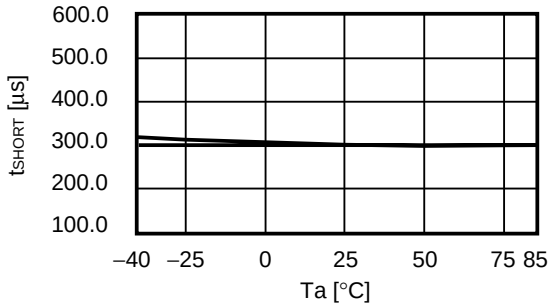
3. 5 R_{CIT} vs Ta



3. 6 V_{CIT} vs Ta (V_{DS} = 17.5 V)

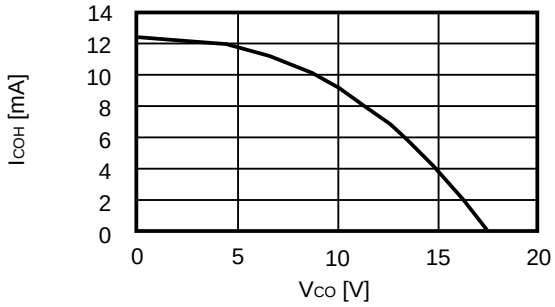


3. 7 t_{SHORT} vs Ta

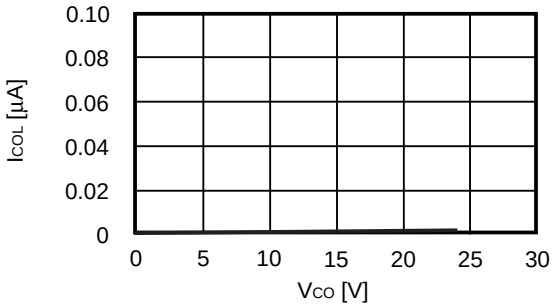


4. CO pin Source / Leakage Current, DO pin Source / Sink Current

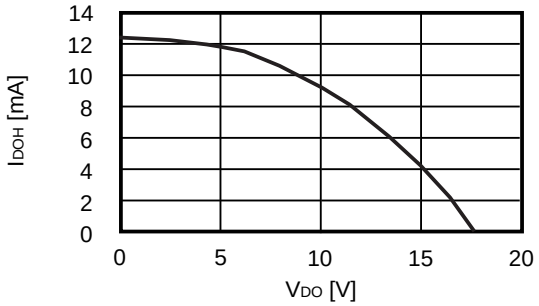
4. 1 I_{COH} vs V_{CO}



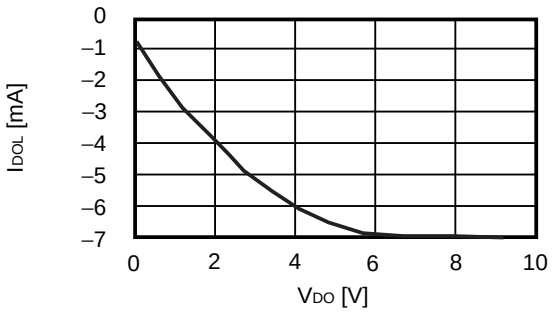
4. 2 I_{COL} vs V_{CO}

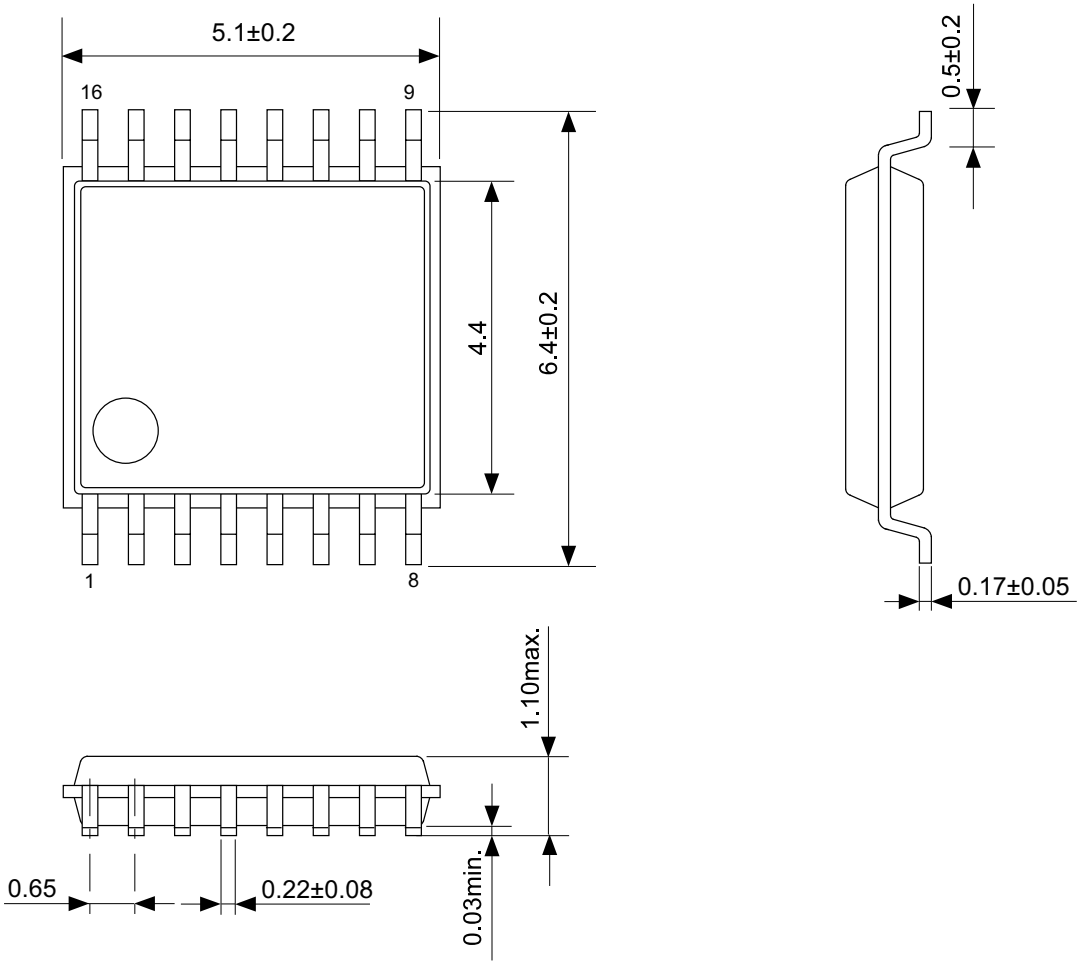


4. 3 I_{DOH} vs V_{DO}



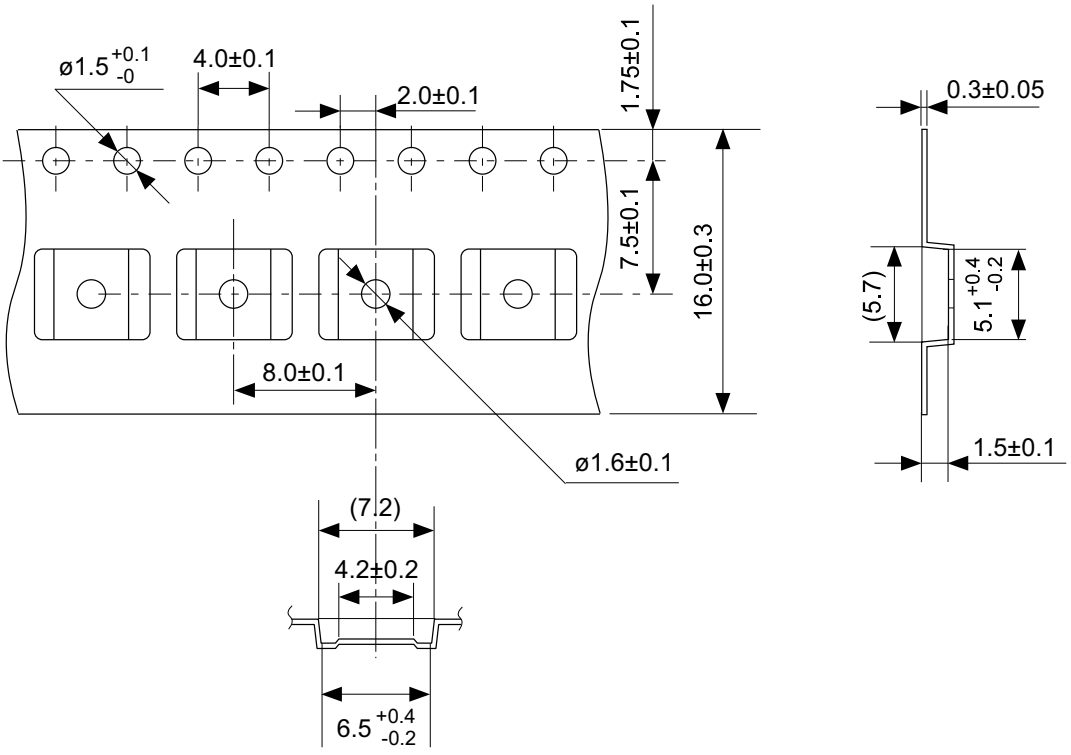
4. 4 I_{DOL} vs V_{DO}

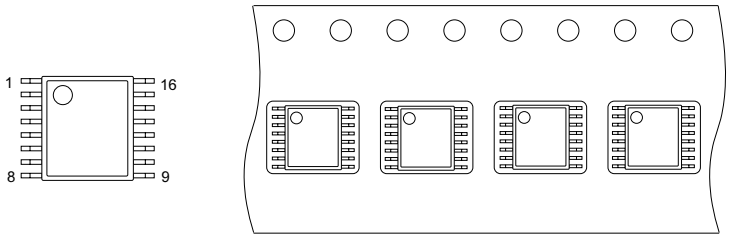




No. FT016-A-P-SD-1.1

TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

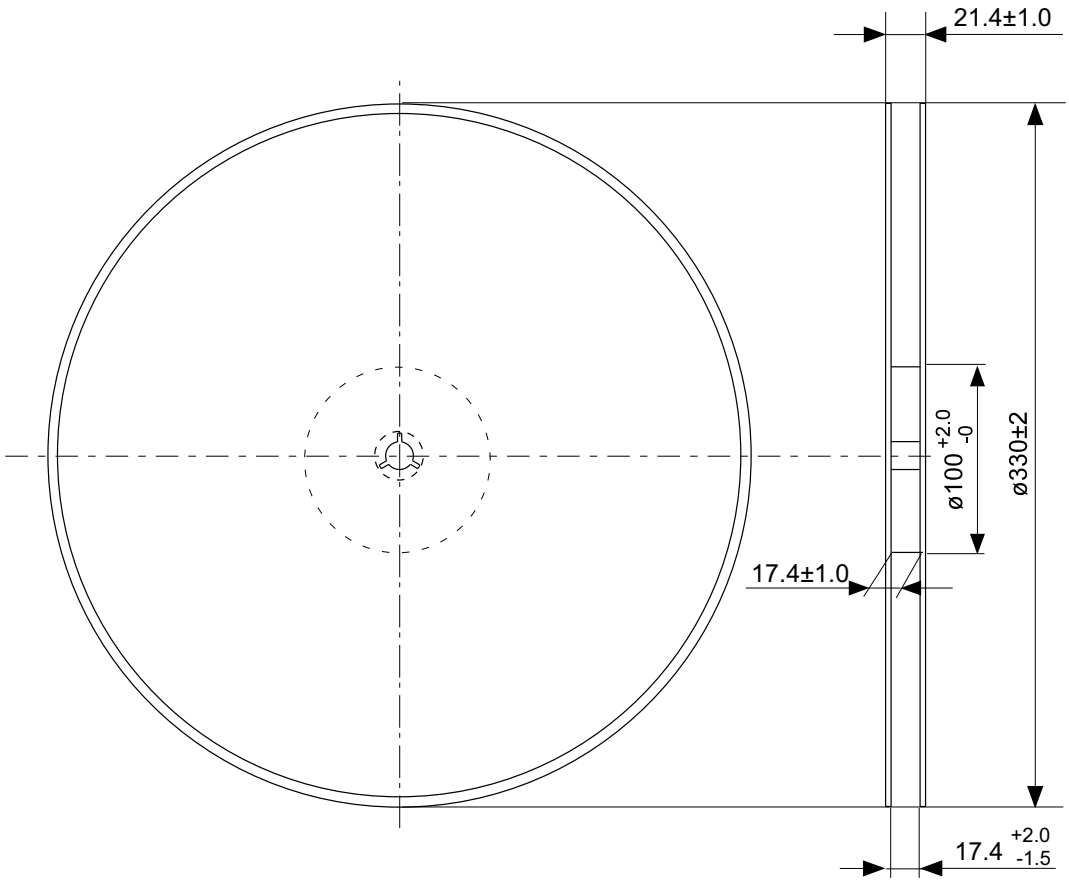




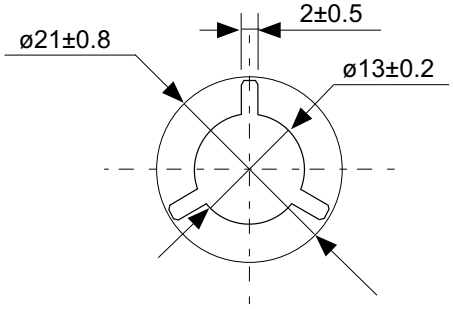
Feed direction

No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT016-A-R-S1-1.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-S1-1.0		
SCALE		QTY.	4,000
UNIT	mm		
Seiko Instruments Inc.			

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