BATTERY PROTECTION IC FOR 3-SERIES OR 4-SERIES CELL PACK

S-8204B Series

The S-8204B Series includes a voltage detection circuit with high accuracy and a delay circuit, in single use, makes it possible for users to monitor the status of 3-series or 4-series cell lithium-ion rechargeable battery. By switching the voltage level which is applied to the SEL pin, users are able to use this IC either for 3-series or 4-series cell pack.
By cascade connection using this IC, it is also possible to protect 5-series or more cells*1 rechargeable lithium-ion battery pack.

***1.** Refer to the usage guideline for connection examples of protection circuit with 5-series cell.

■ Features

(1) High-accuracy voltage detection for each cell

• Overcharge detection voltage n (n = 1 to 4)	3.65 V to 4.6 V (50 mV step)	Accuracy ±25 mV
• Overcharge release voltage n (n = 1 to 4)	3.5 V to 4.6 V*1	Accuracy ±50 mV
• Overdischarge detection voltage n (n = 1 to 4)	2.0 V to 3.0 V (100 mV step)	Accuracy ±80 mV
• Overdischarge release voltage n (n = 1 to 4)	2.0 V to 3.4 V*2	Accuracy ±100 mV

(2) Discharge overcurrent detection in 3-step

• Discharge overcurrent detection voltage 1	0.05 V to 0.30 V (50 mV step)	Accuracy ±15 mV
• Discharge overcurrent detection voltage 2	0.5 V (fixed)	Accuracy ±100 mV
• Short circuit detection voltage	1.0 V (fixed)	Accuracy ±300 mV

(3) Settable by external capacitor; Overcharge detection delay time, Overdischarge detection delay time, Discharge overcurrent detection delay time 1, Discharge overcurrent detection delay time 2

(Short circuit detection voltage delay time is internally fixed.)

(4) Switchable between 3-series and 4-series cell by using the SEL pin

(5) Independent charging and discharge control by the control pins

(6) Withstand voltage element — Absolute maximum rating : 24 V

(7) Wide range of operation voltage — 2 V to 22 V

(8) Wide range of operation temperature — −40°C to +85°C

(9) Low current consumption

• Operation mode	33 µA max. (+25°C)
• Power-down mode	0.1 µA max. (+25°C)

(10) Lead-free product

***1.** Overcharge hysteresis voltage n (n = 1 to 4) is selectable in 0 V, or in 0.1 V to 0.4 V in 50 mV step.
(Overcharge hysteresis voltage = Overcharge detection voltage − Overcharge release voltage)

***2.** Overdischarge hysteresis voltage n (n = 1 to 4) is selectable in 0 V, or in 0.2 V to 0.7 V in 100 mV step.
(Overdischarge hysteresis voltage = Overdischarge release voltage − Overdischarge detection voltage)

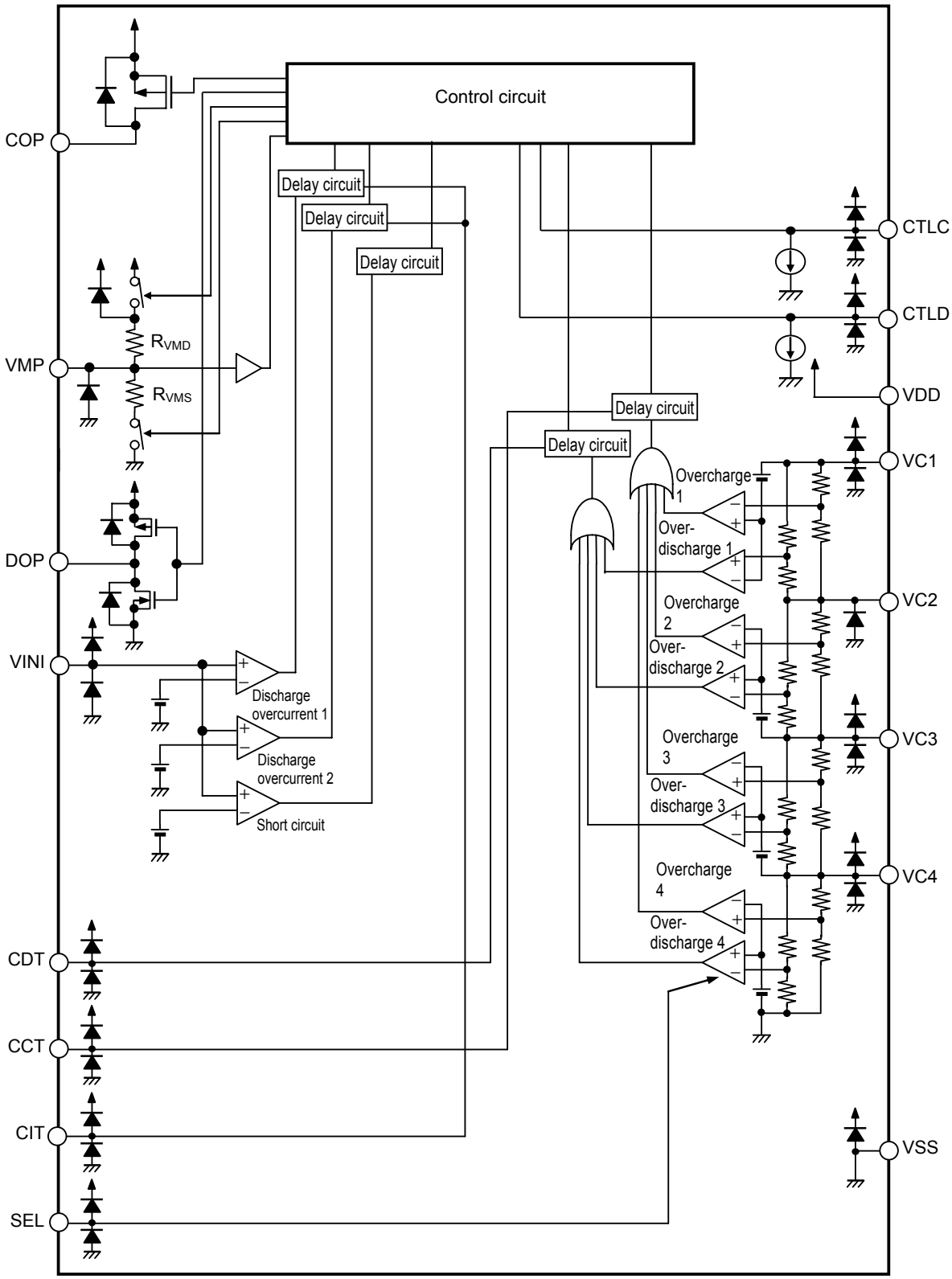
■ Applications

- Rechargeable lithium-ion battery packs

■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
16-Pin TSSOP	FT016-A	FT016-A	FT016-A

■ Block Diagram

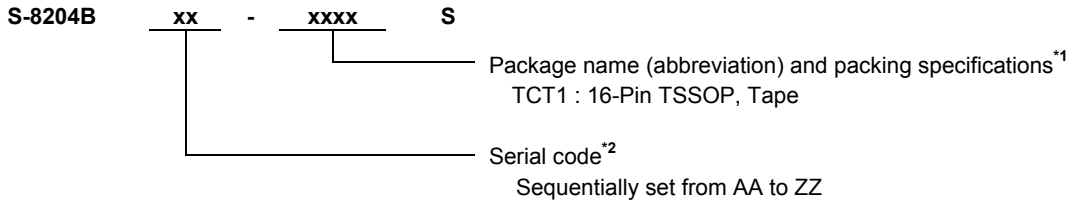


Remark Diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product Name



***1.** Refer to the tape specifications.
***2.** Refer to "**2. Product Name List**".

2. Product Name List

Table 1

Product Name / Item	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent Detection Voltage 1 [V_{DIOV1}]	0 V Battery Charge Function
S-8204BAB-TCT1S	4.350 ± 0.025 V	4.150 ± 0.050 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.25 ± 0.015 V	Available
S-8204BAC-TCT1S	4.225 ± 0.025 V	4.075 ± 0.050 V	2.30 ± 0.080 V	3.00 ± 0.100 V	0.10 ± 0.015 V	Available
S-8204BAD-TCT1S	3.800 ± 0.025 V	3.600 ± 0.050 V	2.00 ± 0.080 V	2.30 ± 0.100 V	0.30 ± 0.015 V	Available
S-8204BAE-TCT1S	4.350 ± 0.025 V	4.150 ± 0.050 V	2.50 ± 0.080 V	3.00 ± 0.100 V	0.25 ± 0.015 V	Available
S-8204BAF-TCT1S	4.350 ± 0.025 V	4.150 ± 0.050 V	2.30 ± 0.080 V	3.00 ± 0.100 V	0.10 ± 0.015 V	Available
S-8204BAG-TCT1S	4.350 ± 0.025 V	4.150 ± 0.050 V	2.80 ± 0.080 V	3.30 ± 0.100 V	0.10 ± 0.015 V	Available
S-8204BAH-TCT1S	4.200 ± 0.025 V	4.000 ± 0.050 V	2.60 ± 0.080 V	3.00 ± 0.100 V	0.10 ± 0.015 V	Available
S-8204BAI-TCT1S	3.900 ± 0.025 V	3.800 ± 0.050 V	2.00 ± 0.080 V	2.00 ± 0.100 V	0.15 ± 0.015 V	Unavailable
S-8204BAJ-TCT1S	4.300 ± 0.025 V	4.100 ± 0.050 V	2.50 ± 0.080 V	2.90 ± 0.100 V	0.25 ± 0.015 V	Available
S-8204BAK-TCT1S	3.650 ± 0.025 V	3.500 ± 0.050 V	2.40 ± 0.080 V	3.00 ± 0.100 V	0.10 ± 0.015 V	Available
S-8204BAL-TCT1S	4.200 ± 0.025 V	4.100 ± 0.050 V	2.70 ± 0.080 V	2.90 ± 0.100 V	0.25 ± 0.015 V	Available
S-8204BAM-TCT1S	4.400 ± 0.025 V	4.200 ± 0.050 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.25 ± 0.015 V	Available
S-8204BAN-TCT1S	4.100 ± 0.025 V	4.100 ± 0.025 V	2.00 ± 0.080 V	2.50 ± 0.100 V	0.15 ± 0.015 V	Unavailable
S-8204BAO-TCT1S	3.900 ± 0.025 V	3.600 ± 0.050 V	2.50 ± 0.080 V	2.70 ± 0.100 V	0.10 ± 0.015 V	Unavailable
S-8204BAP-TCT1S	4.320 ± 0.025 V	4.120 ± 0.050 V	2.40 ± 0.080 V	3.00 ± 0.100 V	0.10 ± 0.015 V	Unavailable
S-8204BAQ-TCT1S	3.800 ± 0.025 V	3.600 ± 0.050 V	2.00 ± 0.080 V	2.30 ± 0.100 V	0.15 ± 0.015 V	Available

Remark Please contact our sales office for products with detection voltage values other than those specified above.

■ Pin Configuration

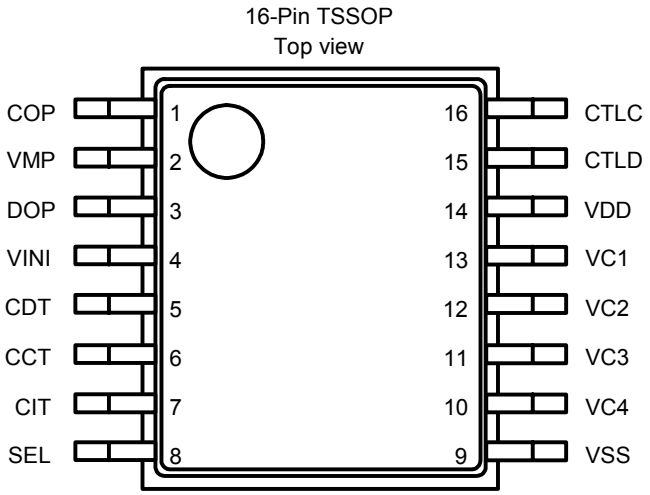


Figure 2

Table 2

Pin No.	Symbol	Description
1	COP	FET gate connection pin for charge control (Pch open drain output)
2	VMP	Pin for voltage detection between VDD and VMP
3	DOP	FET gate connection pin for discharge control FET (CMOS output)
4	VINI	Pin for voltage detection between VSS and VINI Pin for discharge overcurrent detection 1, 2/Pin for short circuit detection voltage
5	CDT	Capacitor connection pin for delay for overdischarge detection voltage
6	CCT	Capacitor connection pin for delay for overcharge detection voltage
7	CIT	Capacitor connection pin for delay for discharge overcurrent detection 1, 2
8	SEL	Pin for switching 3-series or 4-series cell • V_{SS} level : 3-series cell • V_{DD} level : 4-series cell
9	VSS	Input pin for negative power supply, Connection pin for battery 4's negative voltage
10	VC4	Connection pin for battery 3's negative voltage, Connection pin for battery 4's positive voltage
11	VC3	Connection pin for battery 2's negative voltage, Connection pin for battery 3's positive voltage
12	VC2	Connection pin for battery 1's negative voltage, Connection pin for battery 2's positive voltage
13	VC1	Connection pin for battery 1's positive voltage
14	VDD	Input pin for positive power supply, Connection pin for battery 1's positive voltage
15	CTLD	Control pin for discharge FET
16	CTLC	Control pin for charge FET

■ Absolute Maximum Ratings

Table 3

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Ratings	Unit
Input voltage between VDD and VSS	V_{DS}	–	V_{SS}–0.3 to V_{SS}+24	V
Input pin voltage	V_{IN}	VC1, VC2, VC3, VC4, CTLC, CTLD, SEL, CCT, CDT, CIT, VINI	V_{SS}–0.3 to V_{DD}+0.3	V
VMP pin input voltage	V_{VMP}	VMP	V_{SS}–0.3 to V_{SS}+24	V
DOP pin output voltage	V_{DOP}	DOP	V_{SS}–0.3 to V_{DD}+0.3	V
COP pin output voltage	V_{COP}	COP	V_{DD}–24 to V_{DD}+0.3	V
Power dissipation	P_D	–	1100*1	mW
Operating ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

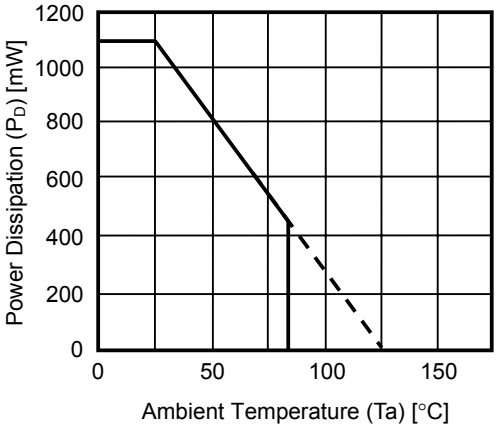


Figure 3 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 4 (1 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
[DETECTION VOLTAGE]								
Overcharge detection voltage n (n = 1, 2, 3, 4)	V_{CUn}	3.65 V to 4.6 V, Adjustable 50 mV step		V_{CUn} −0.025	V_{CUn}	V_{CUn} +0.025	V	2
Overcharge release voltage n (n = 1, 2, 3, 4)	V_{CLn}	3.5 V to 4.6 V, Adjustable 50 mV step	$V_{CL} \neq V_{CU}$	V_{CLn} −0.05	V_{CLn}	V_{CLn} +0.05	V	2
			$V_{CL} = V_{CU}$	V_{CLn} −0.025	V_{CLn}	V_{CLn} +0.025	V	2
Overdischarge detection voltage n (n = 1, 2, 3, 4)	V_{DLn}	2.0 V to 3.0 V, Adjustable 100 mV step		V_{DLn} −0.08	V_{DLn}	V_{DLn} +0.08	V	2
Overdischarge release voltage n (n = 1, 2, 3, 4)	V_{DUn}	2.0 V to 3.4 V, Adjustable 100 mV step	$V_{DL} \neq V_{DU}$	V_{DUn} −0.10	V_{DUn}	V_{DUn} +0.10	V	2
			$V_{DL} = V_{DU}$	V_{DUn} −0.08	V_{DUn}	V_{DUn} +0.08	V	2
Discharge overcurrent detection voltage 1	V_{DIOV1}	0.05 V to 0.30 V, Adjustable		V_{DIOV1} −0.015	V_{DIOV1}	V_{DIOV1} +0.015	V	2
Discharge overcurrent detection voltage 2	V_{DIOV2}	−		0.4	0.5	0.6	V	2
Short circuit detection voltage	V_{SHORT}	−		0.7	1.0	1.3	V	2
Temperature coefficient 1 *1	T_{COE1}	Ta = 0°C to 50°C*3		−1.0	0	1.0	mV/°C	2
Temperature coefficient 2 *2	T_{COE2}	Ta = 0°C to 50°C*3		−0.5	0	0.5	mV/°C	2
[DELAY TIME FUNCTION] *4								
CCT pin internal resistance	R_{INC}	V1 = 4.7 V, V2 = V3 = V4 = 3.5 V		6.15	8.31	10.2	MΩ	3
CDT pin internal resistance	R_{IND}	V1 = 1.5 V, V2 = V3 = V4 = 3.5 V		615	831	1020	kΩ	3
CIT pin internal resistance 1	R_{INI1}	V1 = V2 = V3 = V4 = 3.5 V		123	166	204	kΩ	3
CIT pin internal resistance 2	R_{INI2}	V1 = V2 = V3 = V4 = 3.5 V		12.3	16.6	20.4	kΩ	3
CCT pin detection voltage	V_{CCT}	V_{DS} = 15.2 V V1 = 4.7 V, V2 = V3 = V4 = 3.5 V		V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	3
CDT pin detection voltage	V_{CDT}	V_{DS} = 12.0 V V1 = 1.5 V, V2 = V3 = V4 = 3.5 V		V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	3
CIT pin detection voltage	V_{CIT}	V_{DS} = 14.0 V V1 = V2 = V3 = V4 = 3.5 V		V_{DS} × 0.68	V_{DS} × 0.70	V_{DS} × 0.72	V	3
Short circuit detection voltage delay time	t_{SHORT}	FET gate capacitance = 2000 pF		100	300	600	µs	3
[0 V BATTERY CHARGE FUNCTION]								
Voltage for start charging 0 V battery	V_{0CHA}	available 0 V charging		−	1.2	2.0	V	2
Battery voltage for inhibit charging 0 V battery	V_{0INH}	inhibit 0 V charging		0	0.7	1.1	V	2
[INTERNAL RESISTANCE]								
Resistance between VMP and VDD	R_{VMD}	−		0.5	1	1.5	MΩ	4
Resistance between VMP and VSS	R_{VMS}	−		450	900	1800	kΩ	4

Table 4 (2 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
[INPUT VOLTAGE]							
Operating voltage between VDD and VSS	V_{DSOP}	Fixed output voltage of DOP and COP	2	–	22	V	2
CTLC input voltage "H"	V_{CTLCH}	V1 = V2 = V3 = V4 = 3.5 V	–	–	13.2	V	2
CTLC input voltage "L"	V_{CTLCL}	V1 = V2 = V3 = V4 = 3.5 V	10.1	–	–	V	2
CTLD input voltage "H"	V_{CTLDH}	V1 = V2 = V3 = V4 = 3.5 V	–	–	13.2	V	2
CTLD input voltage "L"	V_{CTLDL}	V1 = V2 = V3 = V4 = 3.5 V	10.1	–	–	V	2
SEL input voltage "H"	V_{SELH}	V_{DS} = 14.0 V V1 = V2 = V3 = V4 = 3.5 V	V_{DS} × 0.8	–	–	V	2
SEL input voltage "L"	V_{SELL}	V_{DS} = 14.0 V V1 = V2 = V3 = V4 = 3.5 V	–	–	V_{DS} × 0.2	V	2
[INPUT CURRENT]							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = 3.5 V	–	15	33	µA	1
Current consumption at power down	I_{PDN}	V1 = V2 = V3 = V4 = 1.5 V	–	–	0.1	µA	1
VC1 pin current	I_{VC1}	V1 = V2 = V3 = V4 = 3.5 V	0.5	1.5	3.0	µA	4
VC2 pin current	I_{VC2}	V1 = V2 = V3 = V4 = 3.5 V	–0.3	0	0.3	µA	4
VC3 pin current	I_{VC3}	V1 = V2 = V3 = V4 = 3.5 V	–0.3	0	0.3	µA	4
VC4 pin current	I_{VC4}	V1 = V2 = V3 = V4 = 3.5 V	–0.3	0	0.3	µA	4
CTLC pin current "H"	I_{CTLCH}	V1 = V2 = V3 = V4 = 3.5 V, $V_{CTLC} = V_{DD}$	0.4	0.6	0.8	µA	4
CTLC pin current "L"	I_{CTLCL}	V1 = V2 = V3 = V4 = 3.5 V, Maximum flow current at CTLC pin	–20.0	–10.0	–3.0	µA	4
CTLD pin current "H"	I_{CTLDH}	V1 = V2 = V3 = V4 = 3.5 V, $V_{CTLD} = V_{DD}$	0.4	0.6	0.8	µA	4
CTLD pin current "L"	I_{CTLDL}	V1 = V2 = V3 = V4 = 3.5 V, Maximum flow current at CTLD pin	–20.0	–10.0	–3.0	µA	4
SEL pin current "H"	I_{SELH}	V1 = V2 = V3 = V4 = 3.5 V, $V_{SEL} = V_{DD}$	–	–	0.1	µA	4
SEL pin current "L"	I_{SELL}	V1 = V2 = V3 = V4 = 3.5 V, $V_{SEL} = V_{SS}$	–0.1	–	–	µA	4
[OUTPUT CURRENT]							
COP pin source current	I_{COH}	$V_{COP} = V_{DD}$ –0.5 V	10	–	–	µA	4
COP pin leakage current	I_{COL}	V_{COP} = 0 V	–	–	0.1	µA	4
DOP pin source current	I_{DOH}	$V_{DOP} = V_{DD}$ –0.5 V	10	–	–	µA	4
DOP pin sink current	I_{DOL}	$V_{DOP} = V_{SS}$ +0.5 V	10	–	–	µA	4

***1.** Voltage temperature coefficient 1 : Overcharge detection voltage

***2.** Voltage temperature coefficient 2 : Discharge overcurrent detection voltage 1

***3.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***4.** Delay time function is described in "■ **Operation**" in detail.

■ Test Circuit

In this chapter, describing how to test the S-8204B Series. In case of selecting to use it for 4-series cell battery, set SEL pin = V_{DD} level. For 3-series cell battery, set SEL pin = V_{SS} level and short between VC4 and VSS pin.

1. Current consumption during operation and power-down (Test circuit 1)

1. 1 Current Consumption during Operation (I_{OPE})

The current at the VSS pin when V1 = V2 = V3 = V4 = 3.5 V and V_{VMP} = V_{DD} is the current consumption during operation (I_{OPE}).

1. 2 Current Consumption at Power-down (I_{PDN})

The current at the VSS pin when V1 = V2 = V3 = V4 = 1.5 V and V_{VMP} = V_{SS} is the current consumption at power-down (I_{PDN}).

2. Overcharge Detection Voltage, Overcharge Release Voltage, Overdischarge Detection Voltage, Overdischarge Release Voltage, Discharge Overcurrent Detection Voltage 1, Discharge Overcurrent Detection Voltage 2, Short Circuit Detection Voltage, CTLC Input Voltage "H", CTLC Input Voltage "L", CTLD Input Voltage "H", CTLD Input Voltage "L", SEL Input Voltage "H", SEL Input Voltage "L" (Test circuit 2)

Confirm both COP and DOP pins are in "H" (its voltage level is $V_{DS} \times 0.9$ V or more) after setting V_{VMP} = V_{SEL} = V_{CTLC} = V_{CTLD} = V_{DD}, V_{VINI} = V_{SS}, CCT pin = Open, CDT pin = Open, CIT pin = Open, V1 = V2 = V3 = V4 = 3.5 V. (This status is referred to as initial status.)

2. 1 Overcharge Detection Voltage (V_{CU1}), Overcharge Release Voltage (V_{CL1})

The overcharge detection voltage (V_{CU1}) is a voltage at V1; when the COP pin's voltage is set to "L" (its voltage level is $V_{DD} \times 0.1$ V or less) after increasing a voltage at V1 gradually from the initial status. After that, decreasing a voltage at V1 gradually, a voltage at V1 when the COP pin's voltage is set to "H"; is the overcharge release voltage (V_{CL1}).

2. 2 Overdischarge Detection Voltage (V_{DL1}), Overdischarge Release Voltage (V_{DU1})

The overdischarge detection voltage (V_{DL1}) is a voltage at V1; when the DOP pin's voltage is set to "L" after decreasing a voltage at V1 gradually from the initial status. After that, increasing a voltage at V1 gradually, a voltage at V1 when the DOP pin's voltage is set to "H"; is the overdischarge release voltage (V_{DU1}).

By changing the voltage at Vn (n = 2 to 4), users can define the overcharge detection voltage (V_{CUn}), the overcharge release voltage (V_{CLn}), the overdischarge detection voltage (V_{DLn}), the overdischarge release voltage (V_{DUn}) as well when n = 1.

2. 3 Discharge Overcurrent Detection Voltage 1 (V_{DIOV1})

The discharge overcurrent detection voltage 1 (V_{DIOV1}) is the VINI pin's voltage; when the DOP pin's voltage is set to "L" after increasing the VINI pin's voltage gradually from the initial status.

2. 4 Discharge Overcurrent Detection Voltage 2 (V_{DIOV2})

The discharge overcurrent detection voltage 2 (V_{DIOV2}) is a voltage at the VINI pin; when a flowing current from the CIT pin reaches 500 μA or more after increasing the VINI pin's voltage gradually from the initial status.

2. 5 Short circuit detection voltage (V_{SHORT})

The short circuit detection voltage (V_{SHORT}) is the VINI pin's voltage; when the DOP pin's voltage is set to "L" after increasing the VINI pin's voltage gradually after setting the CIT pin's voltage V_{SS} level from the initial status.

2. 6 CTLC Input Voltage "H" (V_{CTLCH}), CTLC Input Voltage "L" (V_{CTLCL})

The CTLC input voltage "L" (V_{CTLCL}) is the CTLC pin's voltage; when the COP pin's voltage is set to "L" after decreasing the CTLC pin's voltage gradually from the initial status. After that, increasing the CTLC pin's voltage gradually, the CTLC pin's voltage when the COP pin's voltage is set to "H"; is the CTLC input voltage "H" (V_{CTLCH}).

2. 7 CTLD Input Voltage "H" (V_{CTLDH}), CTLD Input Voltage "L" (V_{CTLDL})

The CTLD input voltage "L" (V_{CTLDL}) is the CTLD pin's voltage; when the DOP pin's voltage is set to "L" after decreasing the CTLD pin's voltage gradually from the initial status. After that, increasing the CTLD pin's voltage gradually, the CTLD pin's voltage when the DOP pin's voltage is set to "H"; is the CTLD input voltage "H" (V_{CTLDH}).

2. 8 SEL Input Voltage "H" (V_{SELH}), SEL Input Voltage "L" (V_{SELL})

Start from the initial status, set V4 = 0 V. Confirm the DOP pin is in "L". After that, decreasing the SEL pin's voltage gradually, the SEL pin's voltage when the DOP pin's voltage is set to "H"; is the SEL input voltage "L" (V_{SELL}). After that, increasing the SEL pin's voltage gradually, the SEL pin's voltage when the DOP pin's voltage is set to "L"; is the SEL input voltage "H" (V_{SELH}).

3. CCT pin Internal Resistance, CDT pin Internal Resistance, CIT pin Internal Resistance 1, CIT pin Internal Resistance 2, CCT pin Detection Voltage, CDT pin Detection Voltage, CIT pin Detection Voltage, Short circuit Detection Voltage Delay Time (Test circuit 3)

Confirm both COP and DOP pins are in "H" (its voltage level is $V_{DS} \times 0.9$ V or more) after setting $V_{VMP} = V_{SEL} = V_{CTLC} = V_{CTLD} = V_{DD}$, $V_{VINI} = CCT = CDT = CIT = V_{SS}$, V1 = V2 = V3 = V4 = 3.5 V. (This status is referred to as initial status.)

3. 1 CCT pin Internal Resistance (R_{INC})

The CCT pin internal resistance (R_{INC}) is $R_{INC} = V_{DS} / I_{CCT}$, I_{CCT} is the current which flows from the CCT pin when setting V1 = 4.7 V from the initial status.

3. 2 CDT pin Internal Resistance (R_{IND})

The CDT pin internal resistance (R_{IND}) is $R_{IND} = V_{DS} / I_{CDT}$, I_{CDT} is the current which flows from the CDT pin when setting V1 = 1.5 V from the initial status.

3. 3 CIT pin Internal Resistance 1 (R_{INI1})

The CIT pin internal resistance 1 (R_{INI1}) is $R_{INI1} = V_{DS} / I_{CIT1}$, I_{CIT1} is the current which flows from the CIT pin when setting $V_{VINI} = V_{DIOV1}$ max. + 0.05 V from the initial status.

3. 4 CIT pin Internal Resistance 2 (R_{INI2})

The CIT pin internal resistance 2 (R_{INI2}) is $R_{INI2} = V_{DS} / I_{CIT2}$, I_{CIT2} is the current which flows from the CIT pin when setting $V_{VINI} = V_{DIOV2}$ max. + 0.05 V from the initial status.

3. 5 CCT pin Detection Voltage (V_{CCT})

The CCT pin detection voltage (V_{CCT}) is the voltage at the CCT pin when the COP pin's voltage is set to "L" (voltage $V_{DS} \times 0.1$ V or less) after increasing the CCT pin's voltage gradually, after setting V1 = 4.7 V from the initial state.

3. 6 CDT pin Detection Voltage (V_{CDT})

The CDT pin detection voltage (V_{CDT}) is the voltage at the CDT pin when the DOP pin's voltage is set to "L" (voltage $V_{DS} \times 0.1$ V or less) after increasing the CDT pin's voltage gradually, after setting V1 = 1.5 V from the initial state.

3. 7 CIT pin Detection Voltage (V_{CIT})

The CIT pin detection voltage (V_{CIT}) is the voltage at the CIT pin when the DOP pin's voltage is set to "L" (voltage $V_{DS} \times 0.1$ V or less) after increasing the CIT pin's voltage gradually, after setting $V_{VINI} = V_{DIOV1}$ max. + 0.05 V from the initial state.

3. 8 Short circuit Detection Voltage Delay Time (t_{SHORT})

Short circuit detection voltage delay time (t_{SHORT}) is a period in which the VINI pin's voltage changes from "H" to "L" by changing the VINI pin's voltage instantaneously from the initial status to V_{SHORT} max.+0.05 V.

4. Voltage for Start Charging 0 V Battery, Battery Voltage for Inhibit Charging 0 V Battery (Test circuit 2)

Confirm both COP and DOP pins are in "H" (its voltage level is $V_{DS} \times 0.9$ V or more) after setting $V_{VMP} = V_{SEL} = V_{CTLC} = V_{CTLD} = V_{DD}$, $V_{VINI} = V_{SS}$, CCT pin = Open, CDT pin = Open, CIT pin = Open, V1 = V2 = V3 = V4 = 3.5 V. (This status is referred to as initial status.)

According to user's selection of the function to charge 0 V battery, either function of Voltage for start charging 0 V battery or Battery voltage for inhibit charging 0 V battery is applied to each product.

4. 1 Voltage for Start Charging 0 V Battery (V_{0CHA}) (Product with function to charge 0 V battery)

Voltage for start charging 0 V battery (V_{0CHA}) is a voltage at V1; when a voltage at the COP pin is set to "H" after increasing a voltage at V1 gradually, after setting V1 = V2 = V3 = V4 = 0 V from the initial status.

4. 2 Battery Voltage for Inhibit Charging 0 V Battery (V_{0INH}) (Product with function to inhibit charging 0 V battery)

Battery voltage for inhibit charging 0 V battery (V_{0INH}) is a voltage at V1; when a voltage at the COP pin is set to "L" after decreasing a voltage at V1 gradually from the initial status.

5. Resistance between VMP and VDD, Resistance between VMP and VSS, VC1 Pin Current, VC2 Pin Current, VC3 Pin Current, VC4 Pin Current, CTLC Pin Current "H", CTLC Pin Current "L", CTLD Pin Current "H", CTLD Pin Current "L", SEL Pin Current "H", SEL Pin Current "L", COP Pin Source Current, COP Pin Leakage Current, DOP Pin Source Current, DOP Pin Sink Current (Test circuit 4)

Set $V_{CTLC} = V_{CTLD} = V_{VMP} = V_{SEL} = V_{DD}$, $V_{VINI} = V_{SS}$, V1 = V2 = V3 = V4 = 3.5 V, set other pins open. (This status is referred to as initial status.)

5. 1 Resistance between VMP and VDD (R_{VMD})

The value of resistance between VMP and VDD (R_{VMD}) can be defined by $R_{VMD} = V_{DS}/I_{VMD}$ by using the VMP pin's current (I_{VMD}) when V_{VINI} = 1.5 V and $V_{VMP} = V_{SS}$ after the initial status.

5. 2 Resistance between VMP and VSS (R_{VMS})

The value of resistance between VMP and VSS (R_{VMS}) can be defined by $R_{VMS} = V_{DS}/I_{VSM}$ by using the VMP pin's current (I_{VMS}) when V1 = V2 = V3 = V4 = 1.8 V after the initial status.

5. 3 VC1 Pin Current (I_{VC1}), VC2 Pin Current (I_{VC2}), VC3 Pin Current (I_{VC3}), VC4 Pin Current (I_{VC4})

In the initial status, each current flows in the VC1 pin, VC2 pin, VC3 pin, VC4 pin is the VC1 pin current (I_{VC1}), the VC2 pin current (I_{VC2}), the VC3 pin current (I_{VC3}), the VC4 pin current (I_{VC4}), respectively.

5. 4 CTLC Pin Current "H" (I_{CTLCH}), CTLC Pin Current "L" (I_{CTLCL})

In the initial status, a current which flows in the CTLC pin is the CTLC pin current "H" (I_{CTLCH}). After that, decreasing a voltage at the CTLC pin gradually, the maximum current which flows in the CTLC pin is; the CTLC pin current "L" (I_{CTLCL}).

5. 5 CTLD Pin Current "H" (I_{CTLDH}), CTLD Pin Current "L" (I_{CTLDL})

In the initial status, a current which flows in the CTLD pin is the CTLD pin current "H" (I_{CTLDH}). After that, decreasing a voltage at the CTLD pin gradually, the maximum current which flows in the CTLD pin is; the CTLD pin current "L" (I_{CTLDL}).

5. 6 SEL Pin Current "H" (I_{SELH}), SEL Pin Current "L" (I_{SELL})

In the initial status, a current which flows in the SEL pin is the SEL pin current "H" (I_{SELH}). After that, a current which flows in the SEL pin when setting $V_{SEL} = V_{SS}$ is; the SEL pin current "L" (I_{SELL}).

5. 7 COP Pin Source Current (I_{COH}), COP Pin Leakage Current (I_{COL})

Start from the initial status, set $V_{COP} = V_{DD} - 0.5$ V, a current which flows in the COP pin is the COP pin source current (I_{COH}). After that, a current which flows in the COP pin when setting V1 = V2 = V3 = V4 = 5.5 V, $V_{COP} = V_{SS}$ is; the COP pin leakage current (I_{COL}).

5. 8 DOP Pin Source Current (I_{DOH}), DOP Pin Sink Current (I_{DOL})

Start from the initial status, set $V_{DOP} = V_{DD} - 0.5$ V, a current which flows in the DOP pin is the DOP pin source current (I_{DOH}). After that, a current which flows in the DOP pin when setting V1 = V2 = V3 = V4 = 1.8 V, $V_{DOP} = V_{SS} + 0.5$ V is; the DOP pin sink current (I_{DOL}).

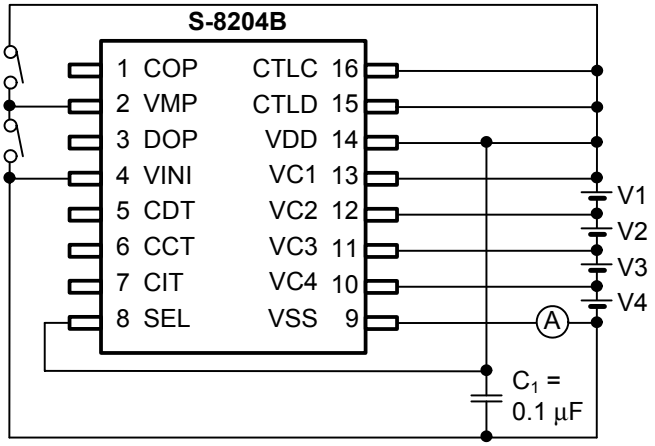


Figure 4 Test Circuit 1

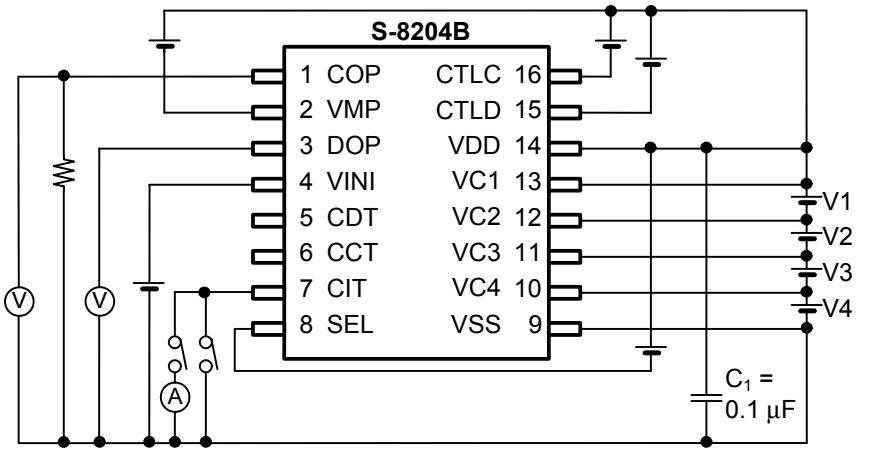


Figure 5 Test Circuit 2

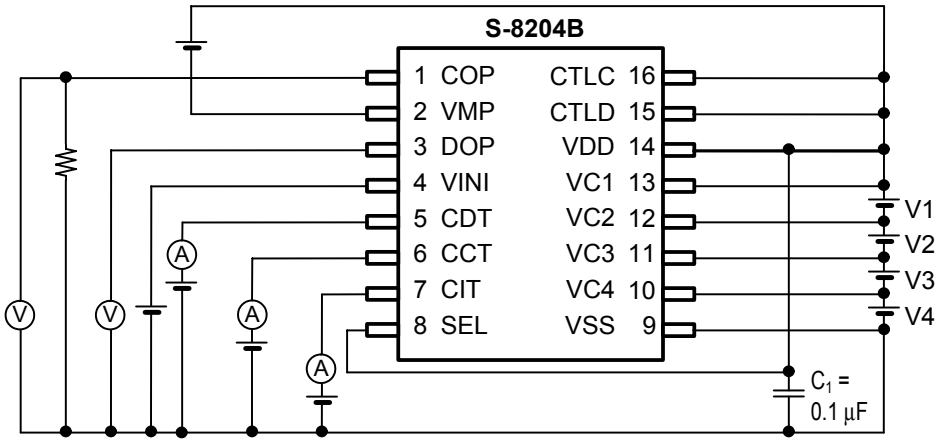


Figure 6 Test Circuit 3

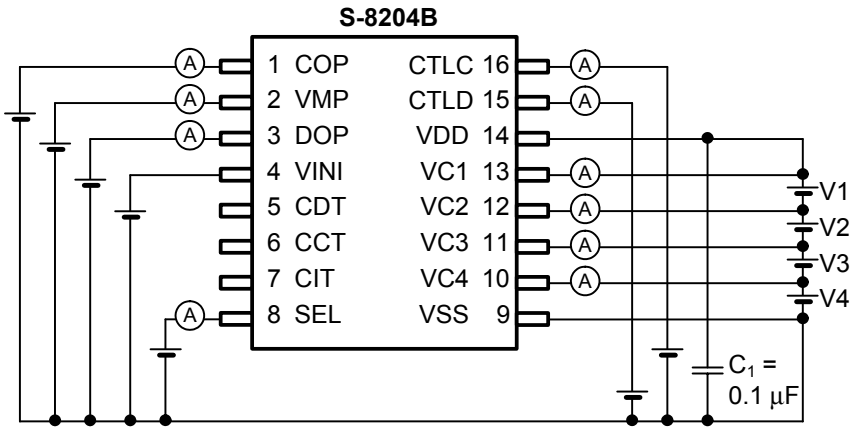


Figure 7 Test Circuit 4

■ Operation

Remark Refer to "■ **Connection Examples of Battery Protection IC (cascade connection)**".

1. Normal Status

In the S-8204B Series, both of COP and DOP pins get the V_{DD} level; when all values of battery voltage are in the range of overdischarge detection voltage (V_{DLn}) to overcharge detection voltage (V_{CUn}), and due to the discharge current, the VINI pin's voltage is discharge overcurrent detection voltage (V_{DIOV1}) or less. This is the normal status.
In addition, the charge/discharge FETs are on.

2. Overcharge Status

In the S-8204B Series, any voltage of the batteries increases to the level of V_{CUn} or more, the COP pin is set in high impedance. This is the overcharge status. The COP pin is pulled down to EB– by an external resistor so that the charge FET is turned off and it stops charging.

This overcharge status is released if either condition 1 or 2 is satisfied;

(1) In case that the VMP pin voltage is 39/40 × V_{DS} or more; all voltages of the batteries are in the level of overcharge release voltage (V_{CLn}) or less.
(2) In case that the VMP pin voltage is 39/40 × V_{DS} or less; all voltages of the batteries are in the level of V_{CUn} or less.

3. Overdischarge Status

In the S-8204B Series, when any voltage of the batteries decreases to the level of V_{DLn} or less, the DOP pin voltage gets the V_{SS} level. This is the overdischarge status. The discharge FET is turned off and it stops discharging.

This overcharge status is released/maintained if either condition 1 to 3 is satisfied;

(1) To release; the VMP pin voltage is in the V_{DD} level or more, all voltages of the batteries are in the V_{DLn} level or more.
(2) To release; the VMP pin voltage is V_{DS}/2 or more and the VMP pin voltage is in the V_{DD} level or less, all voltages of the batteries are in the level of overdischarge release voltage (V_{DUn}) or more.
(3) The VMP pin voltage is V_{DS}/2 or less, the S-8204B Series maintains the power-down status.

4. Power-down Status

In the S-8204B Series, when it reaches the overdischarge status, the VMP pin is pulled down to the V_{SS} level by a resistor between VMP and VSS pin (R_{VMS}). If the VMP pin voltage decreases to the level of V_{DS}/2 or less, almost every circuit in the S-8204B stops working so that the current consumption decreases to the level of current consumption at power down (I_{PDN}) or less. This is the power-down status.

The power-down status is released if the following condition is satisfied.

(1) The VMP pin voltage gets V_{DS}/2 or more.

5. Discharge Overcurrent Status

In batteries in the normal status, the discharging current increases more than a certain value. As a result, if the status in which the VINI pin voltage increases to the level of V_{DIOV1} or more, the DOP pin gets the V_{SS} level. This is the discharge overcurrent status. The discharge control FET is turned off and it stops discharging.

This IC has three levels for discharge overcurrent detection (V_{DIOV1}, V_{DIOV2}, V_{SHORT}). In the status of discharge overcurrent, the COP pin is set in high impedance. The VMP pin is pulled up to the V_{DD} level by a resistor between VMP and VDD pin (R_{VMD}).
The S-8204B Series' actions against discharge overcurrent detection voltage 2 (V_{DIOV2}) and short circuit detection voltage (V_{SHORT}) are as well in V_{DIOV1}.

The discharge overcurrent status is released if the following condition is satisfied.

(1) The VMP pin voltage gets V_{DS} –1.2 V (Typ.) or more.

6. 0 V Battery Charge Function

In this IC, regarding how to charge a discharged battery (0 V battery), users are able to select either function of the two mentioned below.

(1) Allow to charge a 0 V battery (enable to charge a 0 V battery)
A 0 V battery is charged when the voltage between VDD and VSS (V_{DS}) is voltage for start charging 0 V battery (V_{0CHA}) or more.

(2) Inhibit charging a 0 V battery (unable to charge a 0 V battery)
A 0 V battery is not charged when the battery voltage is battery voltage for inhibit charging 0 V battery (V_{0INH}) or less.

Caution When the VDD pin voltage is less than the minimum value of operation voltage between VDD and VSS pin (V_{DSOP}), this IC's action is not assured.

7. Delay Time Setting

In the S-8204B Series, users are able to set delay time for the period; from detecting any voltage of the batteries or detecting changes in the voltage at the VINI pin, to the output to the COP, DOP pin. Each delay time is determined by a resistor in the IC and an external capacitor.

In the overchage detection, when any voltage of the batteries gets V_{CUn} or more, the S-8204B starts charging to the CCT pin's capacitor (C_{CCT}) via the CCT pin's internal resistor (R_{INC}). After a certain period, the COP pin is set in high impedance if the voltage at the CCT pin reaches the CCT pin detection voltage (V_{CCT}). This period is overcharge detection delay time (t_{CU}).

t_{CU} is calculated using the following equation (V_{DS} = V1 + V2 + V3 + V4).

$$t_{CU}\ [s] = -\ln (1 - V_{CCT} / V_{DS}) \times C_{CCT}\ [\mu F] \times R_{INC}\ [M\Omega]$$
$$= -\ln (1 - 0.7\ (Typ.)) \times C_{CCT}\ [\mu F] \times 8.31\ [M\Omega]\ (Typ.)$$
$$= 10.0\ [M\Omega]\ (Typ.) \times C_{CCT}\ [\mu F]$$

Overdischarge detection delay time (t_{DL}), discharge overcurrent detection delay time 1 (t_{DIOV1}), discharge overcurrent detection delay time 2 (t_{DIOV2}) are calculated using the following equations as well.

$$t_{DL}\ [ms] = -\ln (1 - V_{CDT} / V_{DS}) \times C_{CDT}\ [\mu F] \times R_{IND}\ [k\Omega]$$
$$t_{DIOV1}\ [ms] = -\ln (1 - V_{CIT} / V_{DS}) \times C_{CIT}\ [\mu F] \times R_{INI1}\ [k\Omega]$$
$$t_{DIOV2}\ [ms] = -\ln (1 - V_{CIT} / V_{DS}) \times C_{CIT}\ [\mu F] \times R_{INI2}\ [k\Omega]$$

In case $C_{CCT} = C_{CDT} = C_{CIT} = 0.1\ [\mu F]$, each delay time t_{CU}, t_{DL}, t_{DIOV1}, t_{DIOV2} is calculated as follows.

$$t_{CU}\ [s] = 10.0\ [M\Omega]\ (Typ.) \times 0.1\ [\mu F] = 1.0\ [s]\ (Typ.)$$
$$t_{DL}\ [ms] = 1000\ [k\Omega]\ (Typ.) \times 0.1\ [\mu F] = 100\ [ms]\ (Typ.)$$
$$t_{DIOV1}\ [ms] = 200\ [k\Omega]\ (Typ.) \times 0.1\ [\mu F] = 20\ [ms]\ (Typ.)$$
$$t_{DIOV2}\ [ms] = 20\ [k\Omega]\ (Typ.) \times 0.1\ [\mu F] = 2.0\ [ms]\ (Typ.)$$

Short circuit detection voltage delay time (t_{SHORT}) is fixed internally.

8. CTLC and CTLD Pins

The S-8204B Series has two pins to control. The CTLC pin controls the output voltage from the COP pin, the CTLD pin controls the output voltage from the DOP pin. Thus it is possible for users to control the output voltages from the COP pin and DOP pin independently. These controls precede the battery protection circuit.

Table 5 Conditions Set by CTLC Pin

CTLC Pin	COP Pin
High*1	Normal status*4
Open*2	High impedance
Low*3	High impedance

***1.** High; CTLC ≥ V_{CTLCH}
***2.** Pulled down by I_{CTLCH}
***3.** Low; CTLC ≤ V_{CTLCL}
***4.** The status is controlled by the voltage detection circuit.

Table 6 Conditions Set by CTLD Pin

CTLD Pin	DOP Pin
High*1	Normal status*4
Open*2	V_{SS} level
Low*3	V_{SS} level

***1.** High; CTLD ≥ V_{CTLDH}
***2.** Pulled down by I_{CTLDH}
***3.** Low; CTLD ≤ V_{CTLDL}
***4.** The status is controlled by the voltage detection circuit.

Caution Note that when the power supply fluctuates, unexpected behavior might occur if an electrical potential is generated between the potentials of "H" level input to the CTLC/CTLD pins and IC's V_{DD} by external filters R_{VDD1} and C_{VDD1}.

9. SEL pin

The S-8204B Series has a pin to switch-control the protection for 3-cell or 4-cell battery.
The overdischarge detection for V4-cell is inhibited by setting the SEL pin "L", so that short-circuiting the V4 cell does not allow the overdischarge detection. This setting makes it possible to use the S-8204B Series for 3-cell protection.
The control by this SEL pin precedes the battery protection circuit. Be sure to use the SEL pin in "H" or "L".

Table 7 Conditions Set by SEL Pin

SEL Pin	Condition
High*1	4-cell protection
Open	Indefinite
Low*2	3-cell protection

***1.** High; SEL ≥ V_{SELH}
***2.** Low; SEL ≤ V_{SELL}

In cascade connection, it is possible to use the S-8204B Series for protecting 6, 7 or 8-cell battery by combining the electrical level of SEL pin.

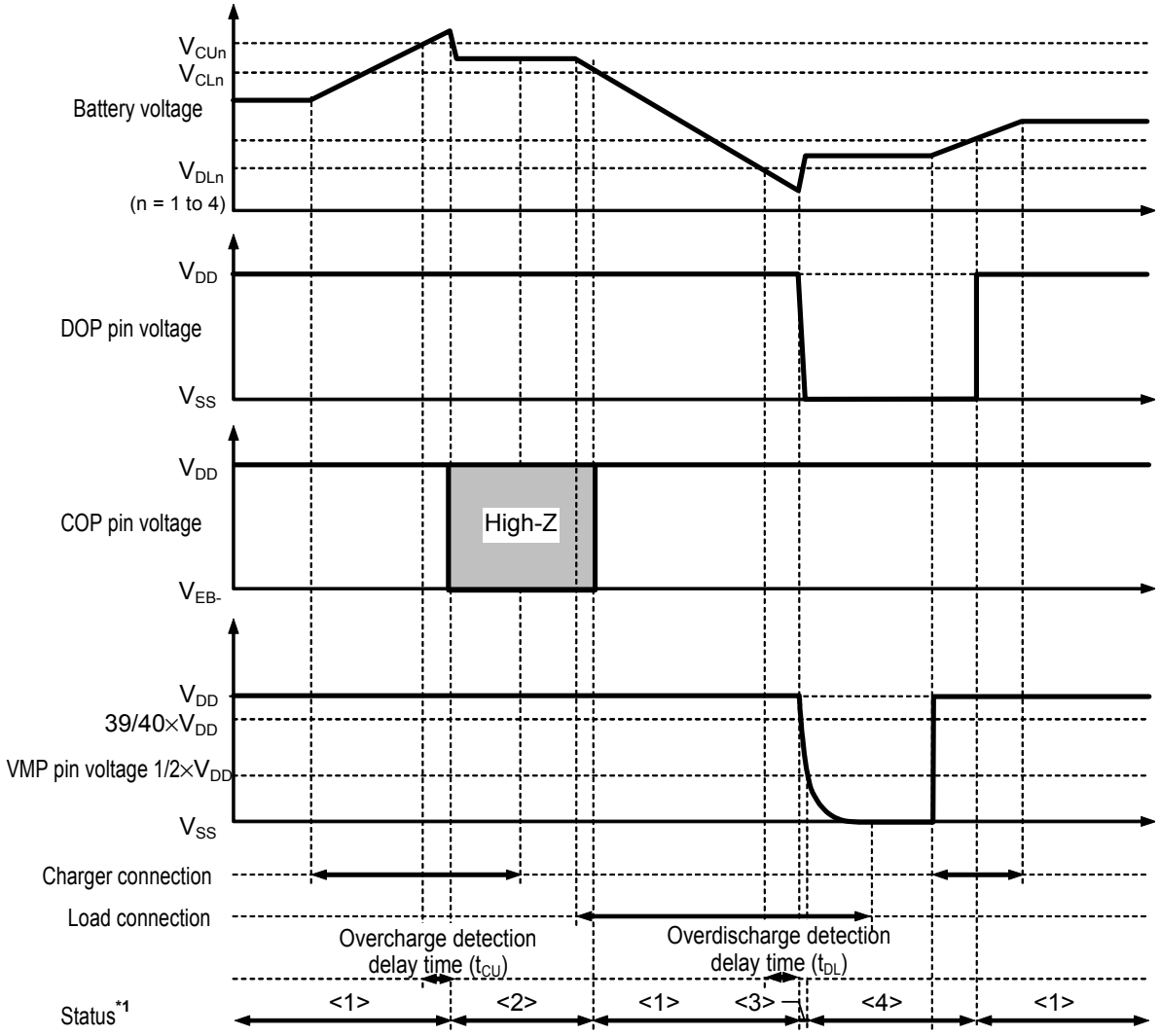
Table 8 Conditions Set by SEL Pin in Cascade Connection

SEL pin in S-8204B (1)	SEL pin in S-8204B (2)	Condition
Low*1	Low*1	6-series cell protection
Low*1	High*2	7-series cell protection
High*2	High*2	8-series cell protection

***1.** Low; SEL ≤ V_{SELL}
***2.** High; SEL ≥ V_{SELH}

■ Timing Chart (in the circuit in Figure 10)

1. Overcharge Detection and Overdischarge Detection

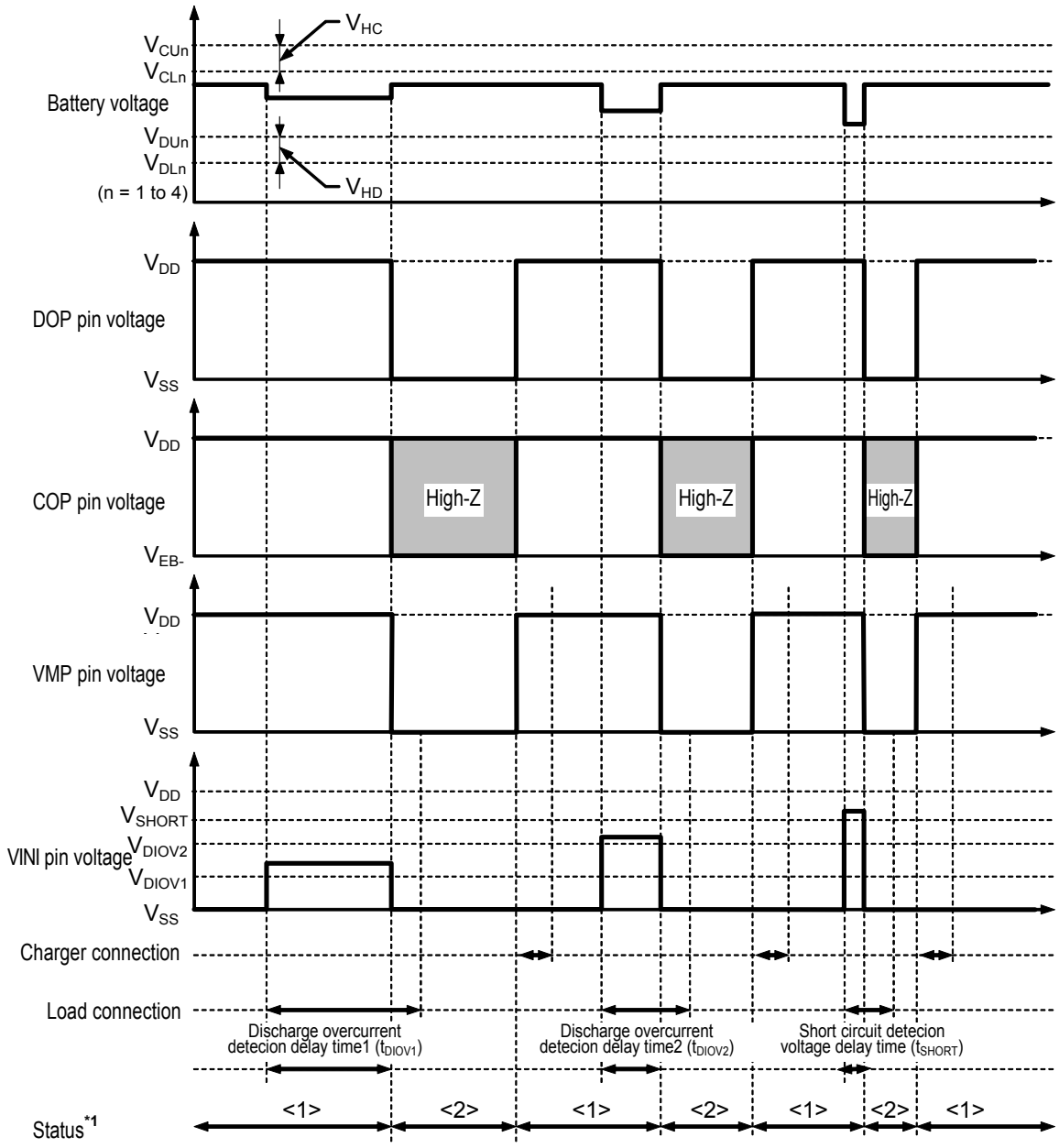


***1.** <1> : Normal status
<2> : Overcharge status
<3> : Overdischarge status
<4> : Power-down status

Remark The charger is assumed to charge with a constant current. V_{EB-} indicates the open voltage of the charger.

Figure 8

2. Discharge Overcurrent Detection



***1.** <1> : Normal status
<2> : Discharge overcurrent status

Remark The charger is assumed to charge with a constant current. V_{EB-} indicates the open voltage of the charger.

Figure 9

■ Connection Examples of Battery Protection IC

1. 4-Series Cell (with protect overcurrent function)

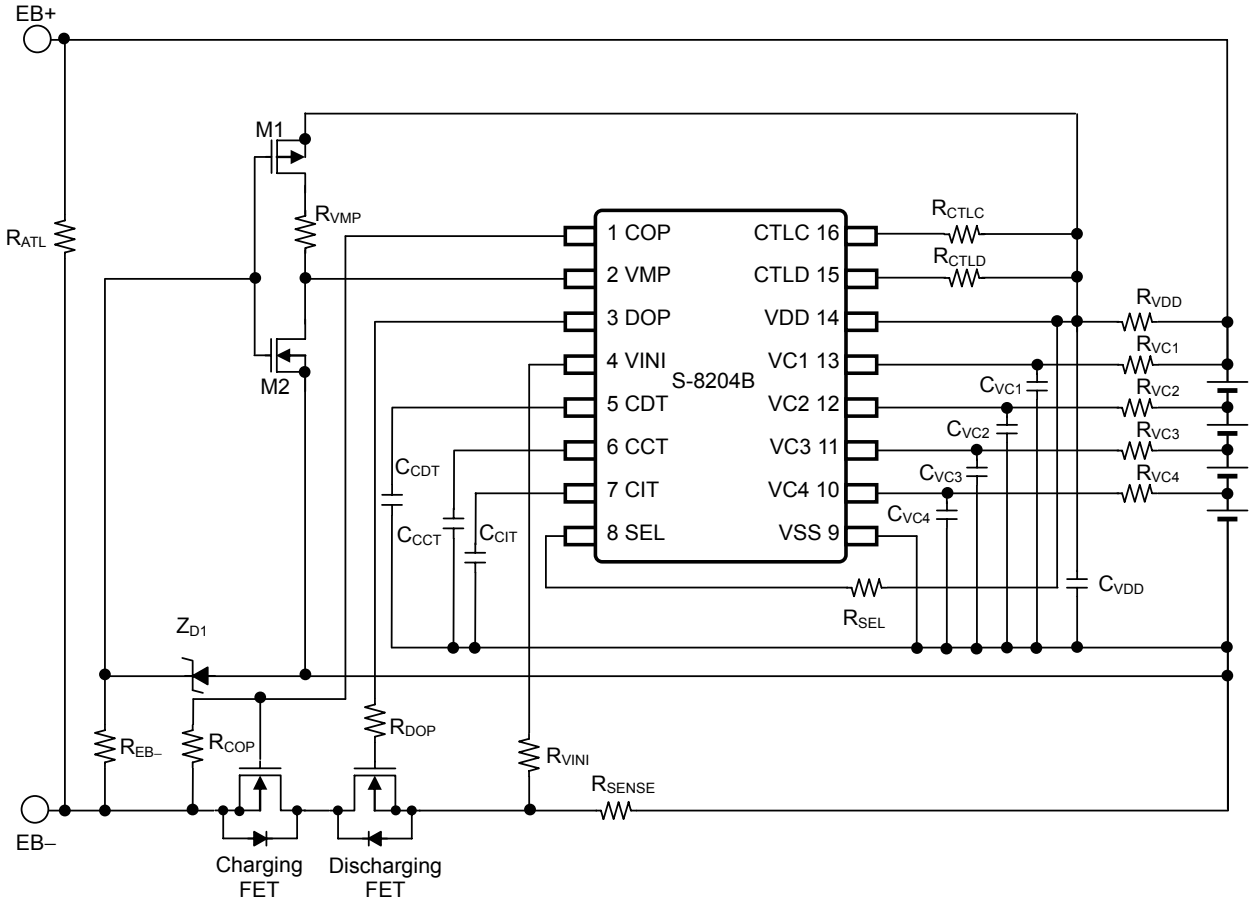


Figure 10

2. 7-Series Cell (cascade connection without protect overcurrent function)

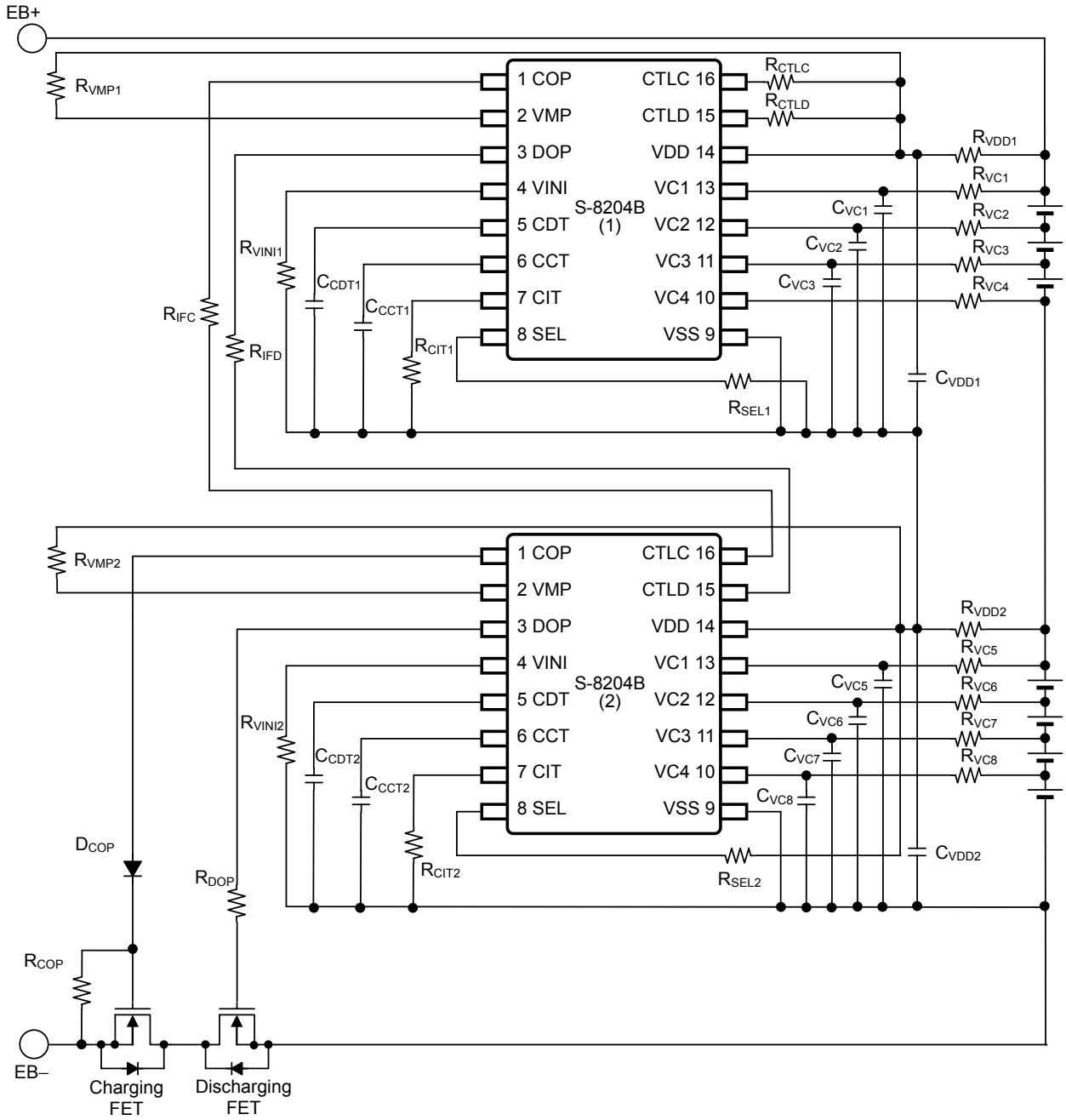


Figure 11

3. 8-Series Cell (cascade connection with protect overcurrent function)

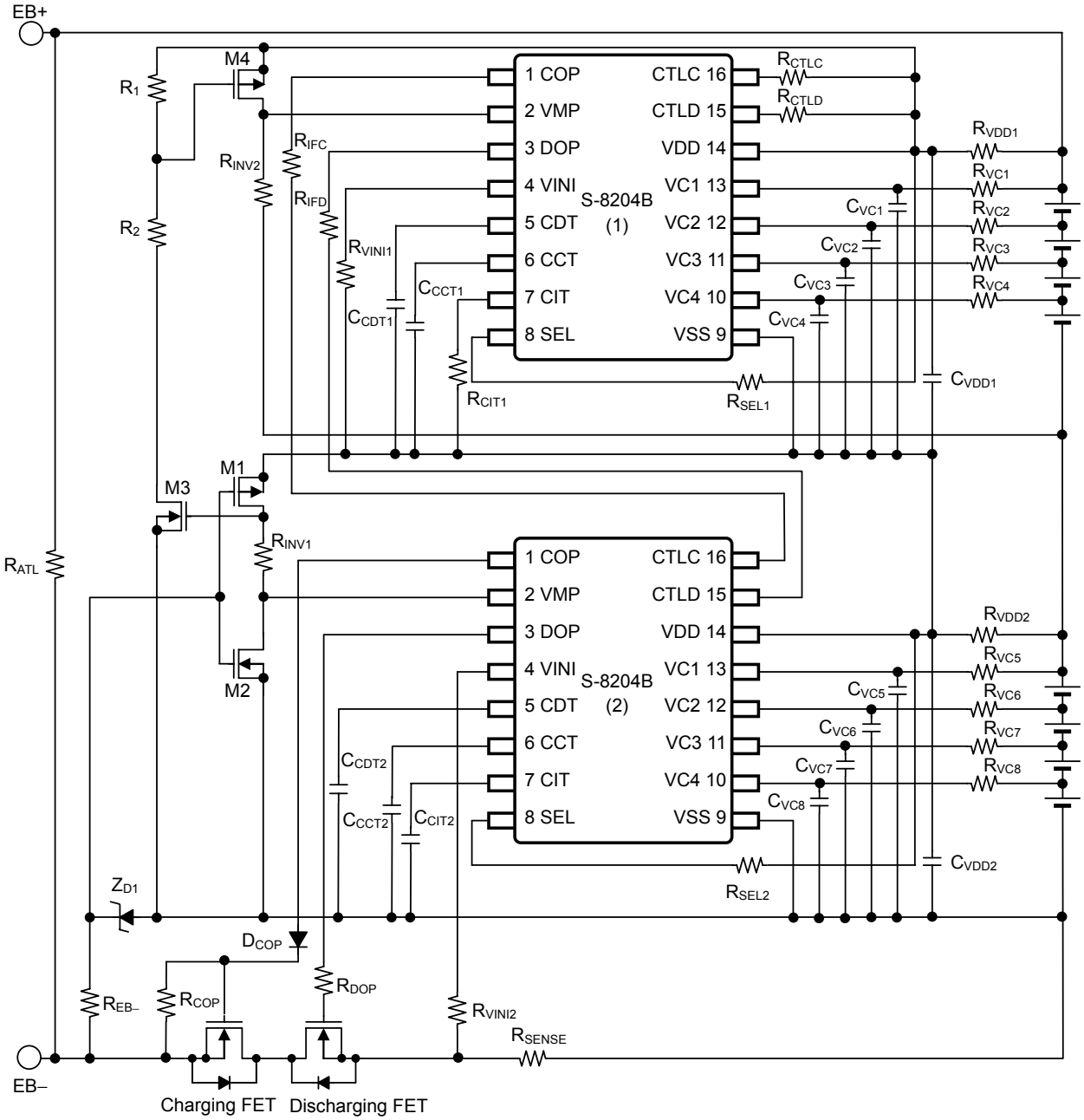


Figure 12

Table 9 Constants for External Components (in the circuit in Figure 11)

Symbol	Typical	Range	Unit
R_{VC1}, R_{VC5}	1	0.51 to 1*1	kΩ
R_{VC2}, R_{VC6}	1	0.51 to 1*1	kΩ
R_{VC3}, R_{VC7}	1	0.51 to 1*1	kΩ
R_{VC4}, R_{VC8}	1	0.51 to 1*1	kΩ
R_{DOP}	51	20 to 68	kΩ
R_{COP}	1	0.1 to 1	MΩ
R_{VMP1}, R_{VMP2}	5.1	1 to 10	kΩ
R_{CTLC}	1	1 to 10	kΩ
R_{CTLD}	1	1 to 10	kΩ
R_{VINI}	1	1 to 10	kΩ
R_{SEL1}, R_{SEL2}	1	1 to 100	kΩ
R_{IFC}	5.1	5.1 to 6.8	MΩ
R_{IFD}	5.1	5.1 to 6.8	MΩ
R_{CIT1}, R_{CIT2}	1	1 to 100	kΩ
R_{VDD1}, R_{VDD2}	47	22 to 100*1	Ω
C_{VC1}, C_{VC5}	47	0 to 100*1	nF
C_{VC2}, C_{VC6}	47	0 to 100*1	nF
C_{VC3}, C_{VC7}	47	0 to 100*1	nF
C_{VC4}, C_{VC8}	47	0 to 100*1	nF
C_{CCT1}, C_{CCT2}	0.1	0.01 or higher	μF
C_{CDT1} C_{CDT2}	0.1	0.01 or higher	μF
C_{VDD1}	1	0 to 2.2	μF
C_{VDD2}	1.5	0 to 3.3	μF

***1.** Set up a filter constant to be $R_{VDD1} \times C_{VDD1} = R_{VDD2} \times C_{VDD2} \times 2/3 = 47\ \mu F \bullet \Omega$ or more, and to be $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VC4} \times C_{VC4} = R_{VDD1} \times C_{VDD1}$, $R_{VC5} \times C_{VC5} = R_{VC6} \times C_{VC6} = R_{VC7} \times C_{VC7} = R_{VC8} \times C_{VC8} = R_{VDD2} \times C_{VDD2} \times 2/3$.

Caution
1. **The above constants may be changed without notice.**
2. **It is recommended that filter constants between VDD and VSS should be set approximately to 47 μF • Ω.**
   e.g., $C_{VDD} \times R_{VDD} = 1.0\ \mu F \times 47\ \Omega = 47\ \mu F \bullet \Omega$
   Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants. Contact our sales office in case the constants should be set to other than 47 μF • Ω.
3. **It has not been confirmed whether the operation is normal in circuits other than the above example of connection. In addition, the example of connection shown above and the constants do not guarantee proper operation. Perform thorough evaluation using an actual application to set the constant.**

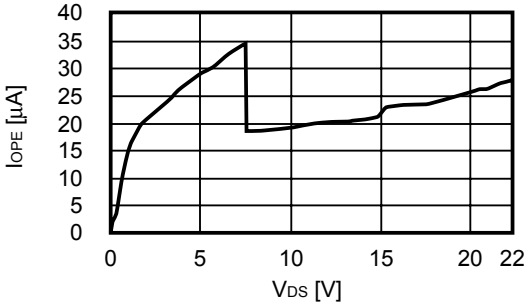
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order; however, there may be cases when discharging cannot be performed when a battery is connected. In such a case, short the VMP pin and VDD pin to return the IC to the normal mode.
- If both an overcharge battery and an overdischarge battery are included among the whole batteries, the condition is set in overcharge status and overdischarge status. Therefore either charging or discharging is impossible.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

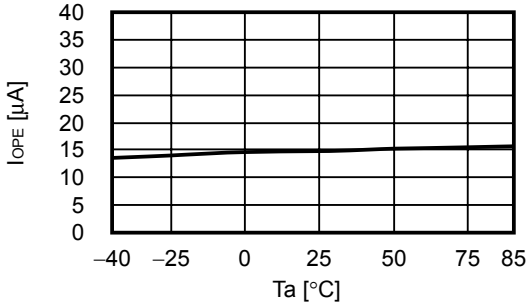
■ Characteristics (Typical Data)

1. Current Consumption

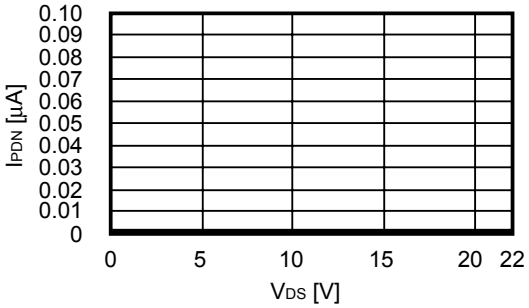
1.1 I_{OPE} vs. V_{DS}



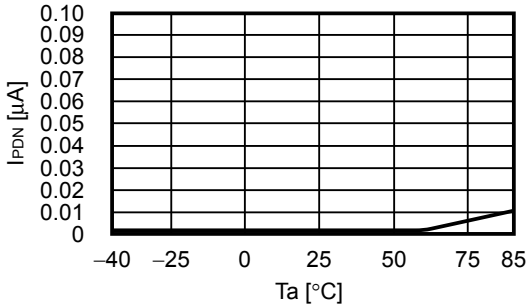
1.2 I_{OPE} vs. Ta



1.3 I_{PDN} vs. V_{DS}

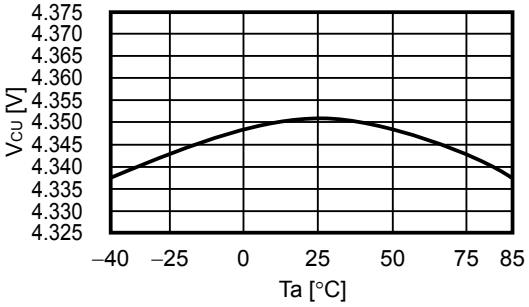


1.4 I_{PDN} vs. Ta

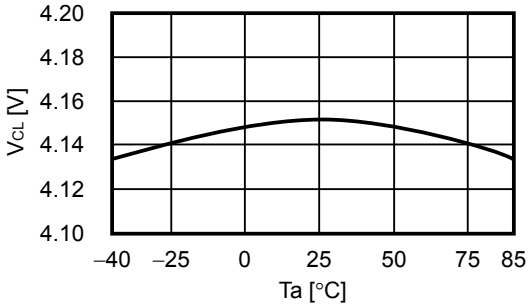


2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Overcurrent Detection Voltage

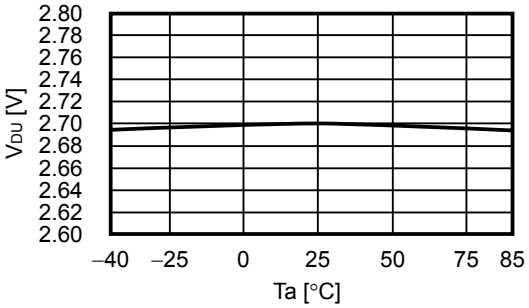
2.1 V_{CU} vs. Ta



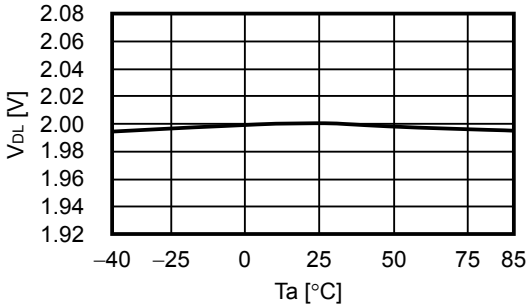
2.2 V_{CL} vs. Ta



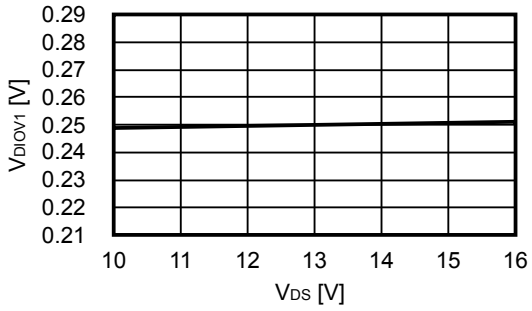
2.3 V_{DU} vs. Ta



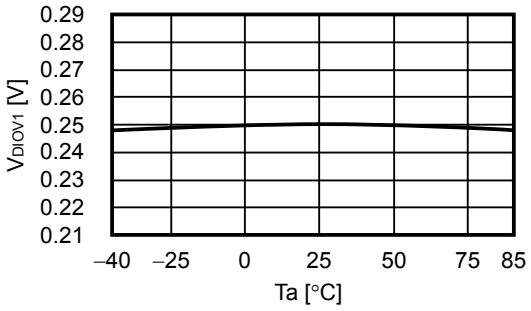
2.4 V_{DL} vs. Ta



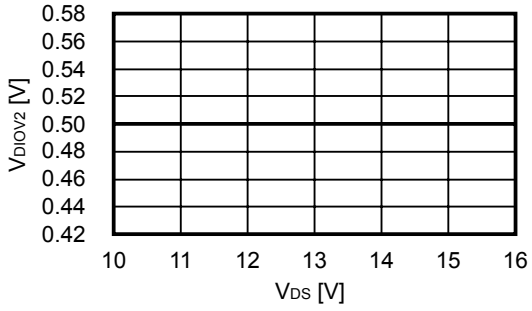
2.5 V_{DIOV1} vs. V_{DS}



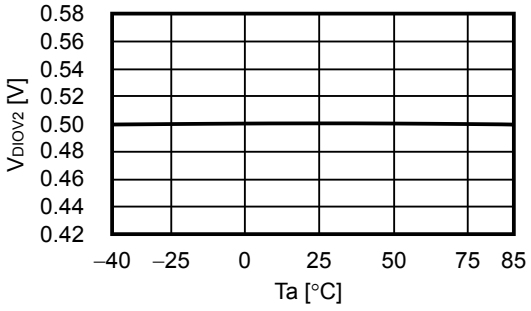
2.6 V_{DIOV1} vs. Ta



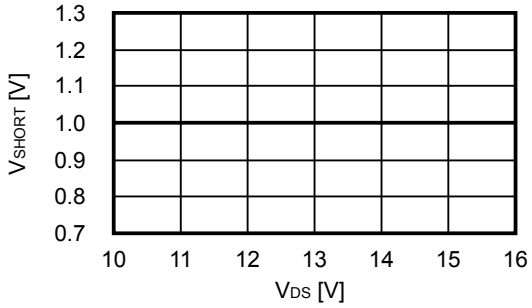
2.7 V_{DIOV2} vs. V_{DS}



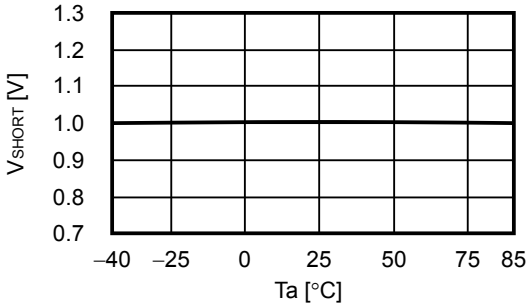
2.8 V_{DIOV2} vs. Ta



2.9 V_{SHORT} vs. V_{DS}

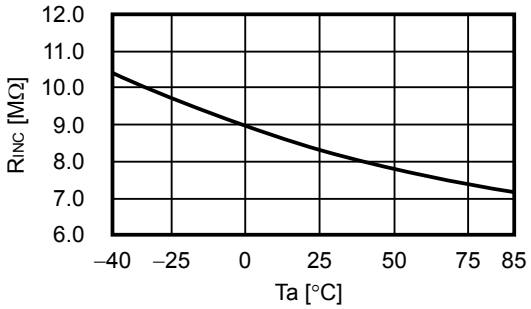


2.10 V_{SHORT} vs. Ta

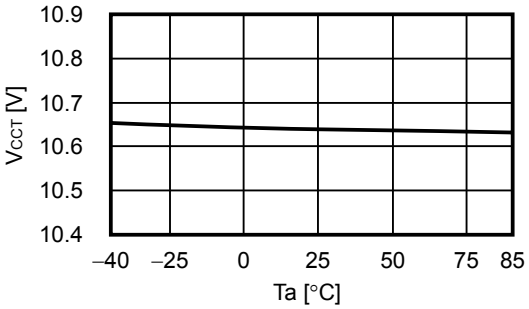


3. CCT pin Internal Resistance / Detection Voltage, CDT pin Internal Resistance / Detection Voltage, CIT pin Internal Resistance / Detection Voltage and Short circuit Detection Voltage Delay Time

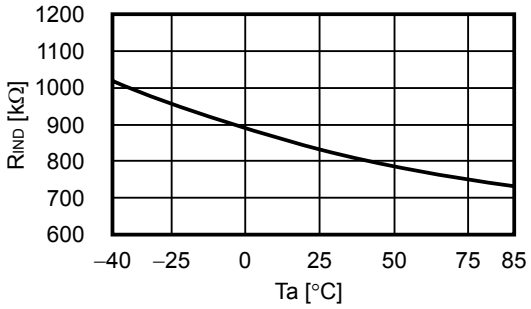
3. 1 R_{INC}–Ta



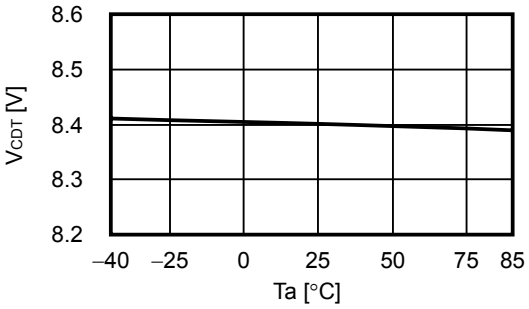
3. 2 V_{CCT}–Ta (V_{DS} = 15.2 V)



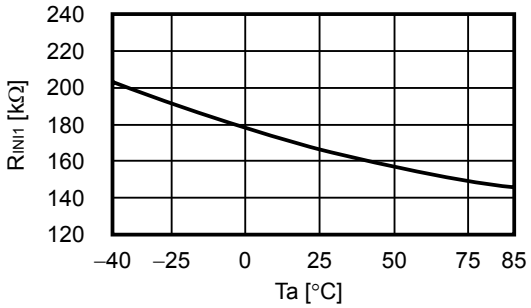
3. 3 R_{IND}–Ta



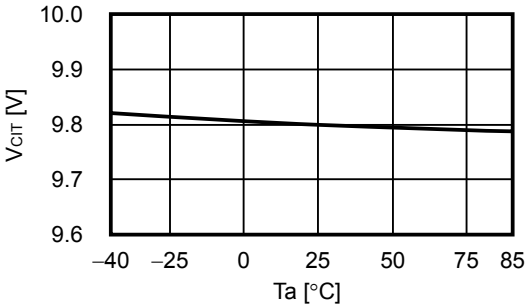
3. 4 V_{CDT}–Ta (V_{DS} = 12.0 V)



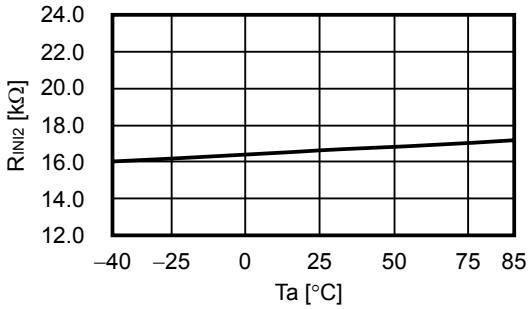
3. 5 R_{INI1}–Ta



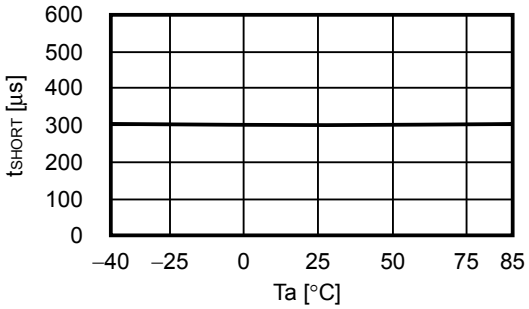
3. 6 V_{CIT}–Ta (V_{DS} = 14.0 V)



3. 7 R_{INI2}–Ta

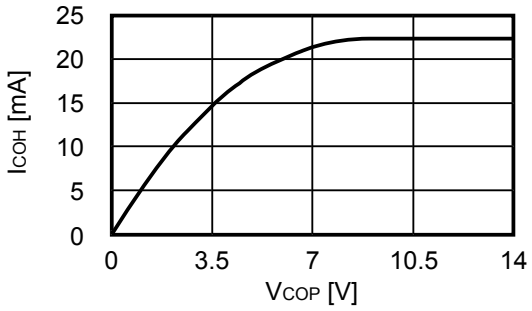


3. 8 t_{SHORT}–Ta

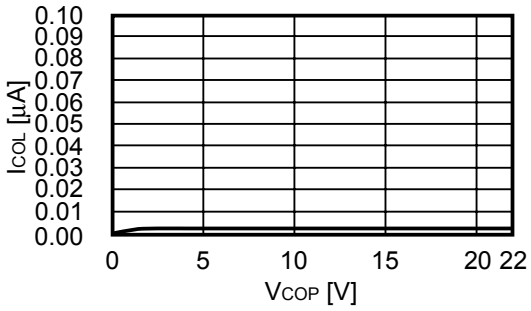


4. COP / DOP Pin

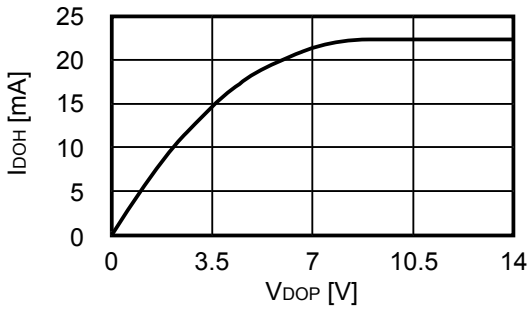
4.1 I_{COH} vs. V_{COP}



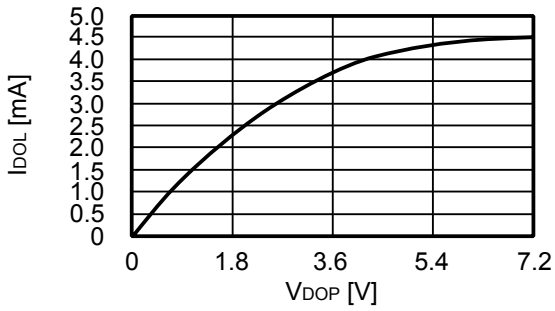
4.2 I_{COL} vs. V_{COP}

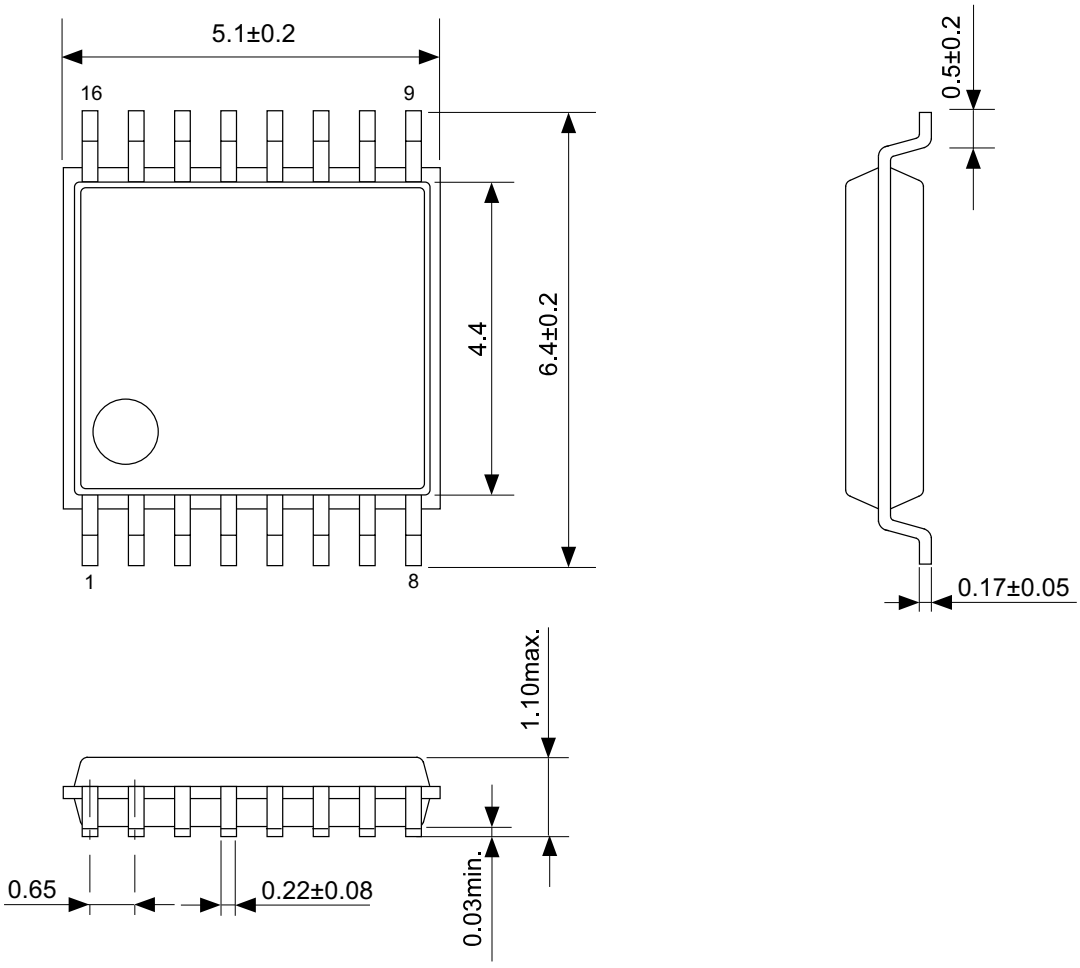


4.3 I_{DOH} vs. V_{DOP}



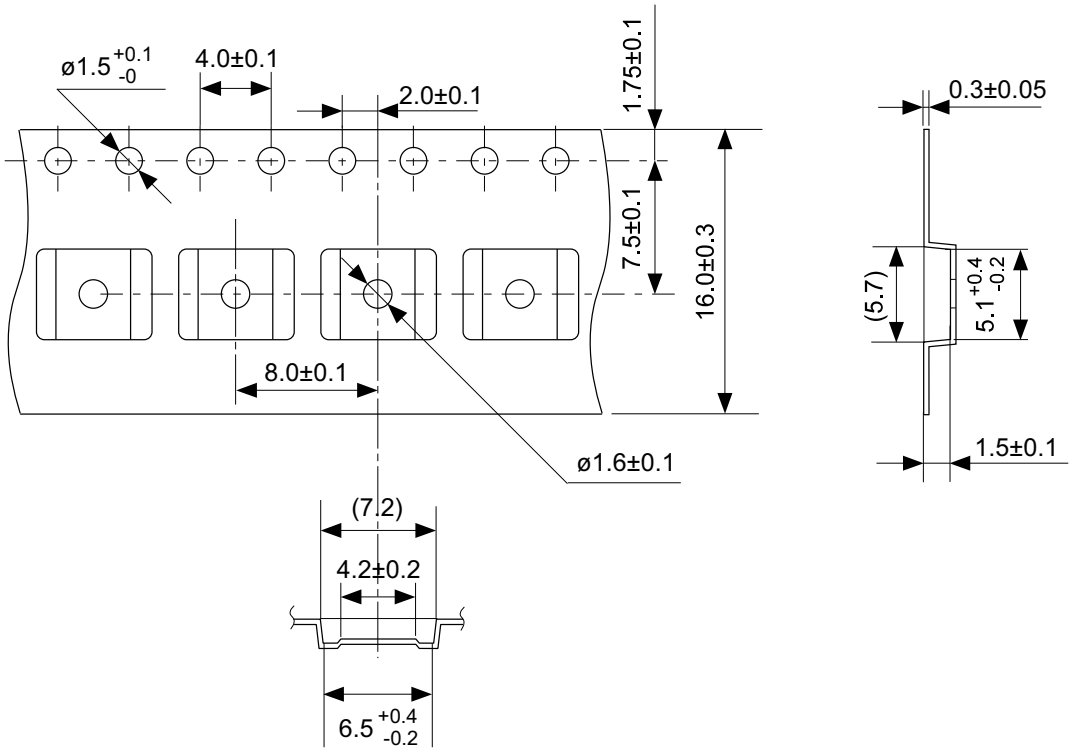
4.4 I_{DOL} vs. V_{DOP}

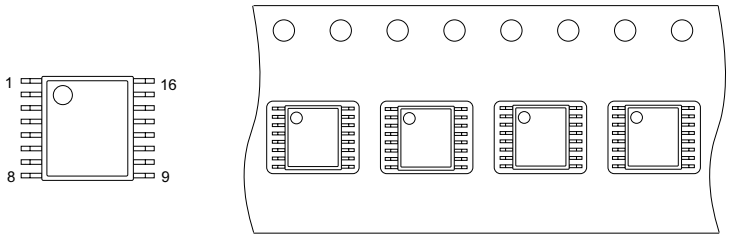




No. FT016-A-P-SD-1.1

TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

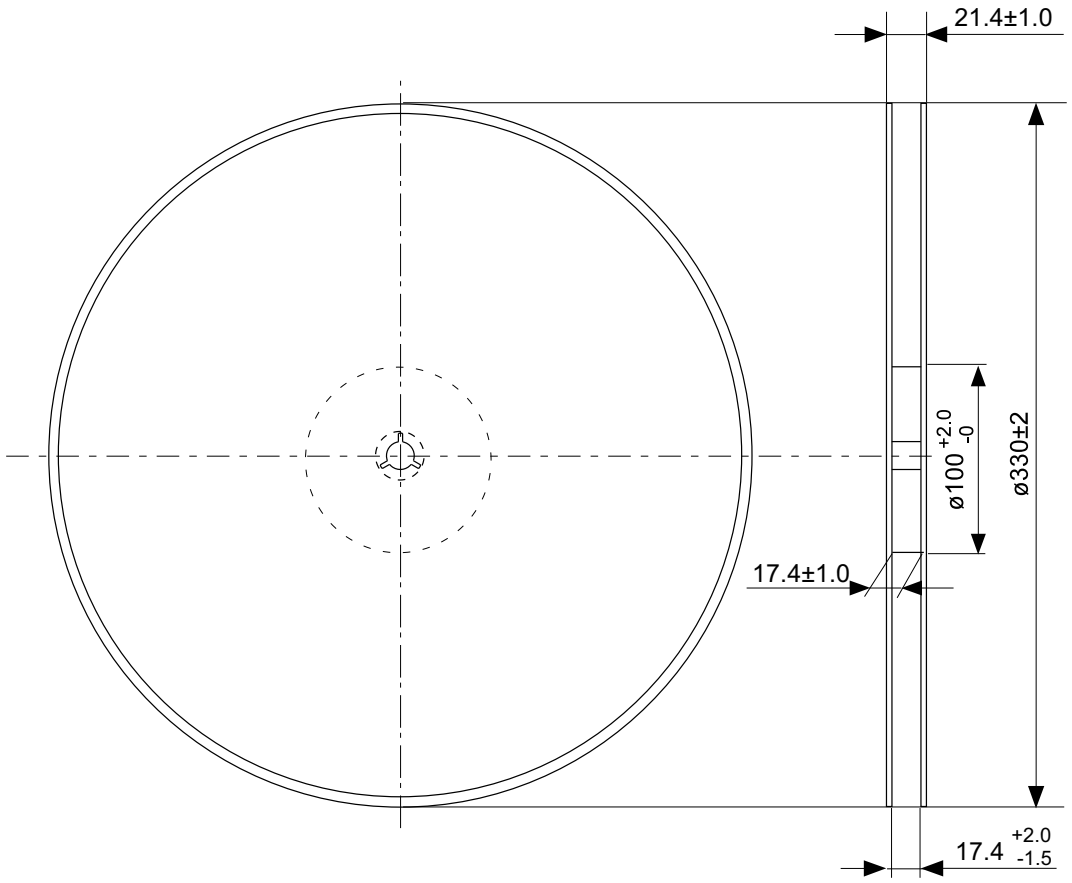




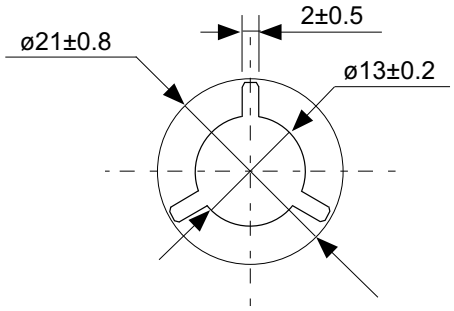
Feed direction

No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT016-A-R-SD-2.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-SD-2.0		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			

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