BATTERY PROTECTION IC FOR 3-SERIAL-CELL PACK

S-8233B Series

The S-8233B is a series of lithium-ion rechargeable battery protection ICs incorporating high-accuracy (±25 mV) voltage detection circuits and delay circuits. It is suitable for a 3-serial-cell lithium-ion rechargeable battery pack.

■ Features

(1) Internal high-accuracy voltage detection circuit
- Over charge detection voltage: 3.80 ± 0.025 V to 4.40 ± 0.025 V, 5 mV - step
- Over charge release voltage: 3.45 ± 0.100 V to 4.40 ± 0.100 V, 5 mV - step

  (The over charge release voltage can be selected within the range where a difference from over charge detection voltage is 0 to 0.35 V with 50 mV - step)
- Over discharge detection voltage: 2.00 ± 0.08 V to 2.80 ± 0.08 V, 50 mV - step
- Over discharge release voltage: 2.00 ± 0.10 V to4.00 ± 0.10 V, 50 mV - step

  (The over discharge release voltage can be selected within the range where a difference from over discharge detection voltage is 0 to 1.2 V with 50 mV - step)
- Over current detection voltage 1: 0.15 ± 0.015 V to 0.5 ± 0.05 V, 50 mV - step

(2) High input-voltage device (absolute maximum rating: 26 V)
(3) Wide operating voltage range: 2 V to 24 V
(4) The delay time for every detection can be set via an external capacitor.
(5) Three over current detection levels (protection for short-circuiting)
(6) Internal charge/discharge prohibition circuit via the control terminal
(7) The function for charging batteries from 0 V is available.
(8) Low current consumption
- Operation: 50 μA max. (+25°C)
- Power-down: 0.1 μA max. (+25°C)

(9) Lead-free products

■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
16-PIN TSSOP	FT016-A	FT016-A	FT016-A

■ Block Diagram

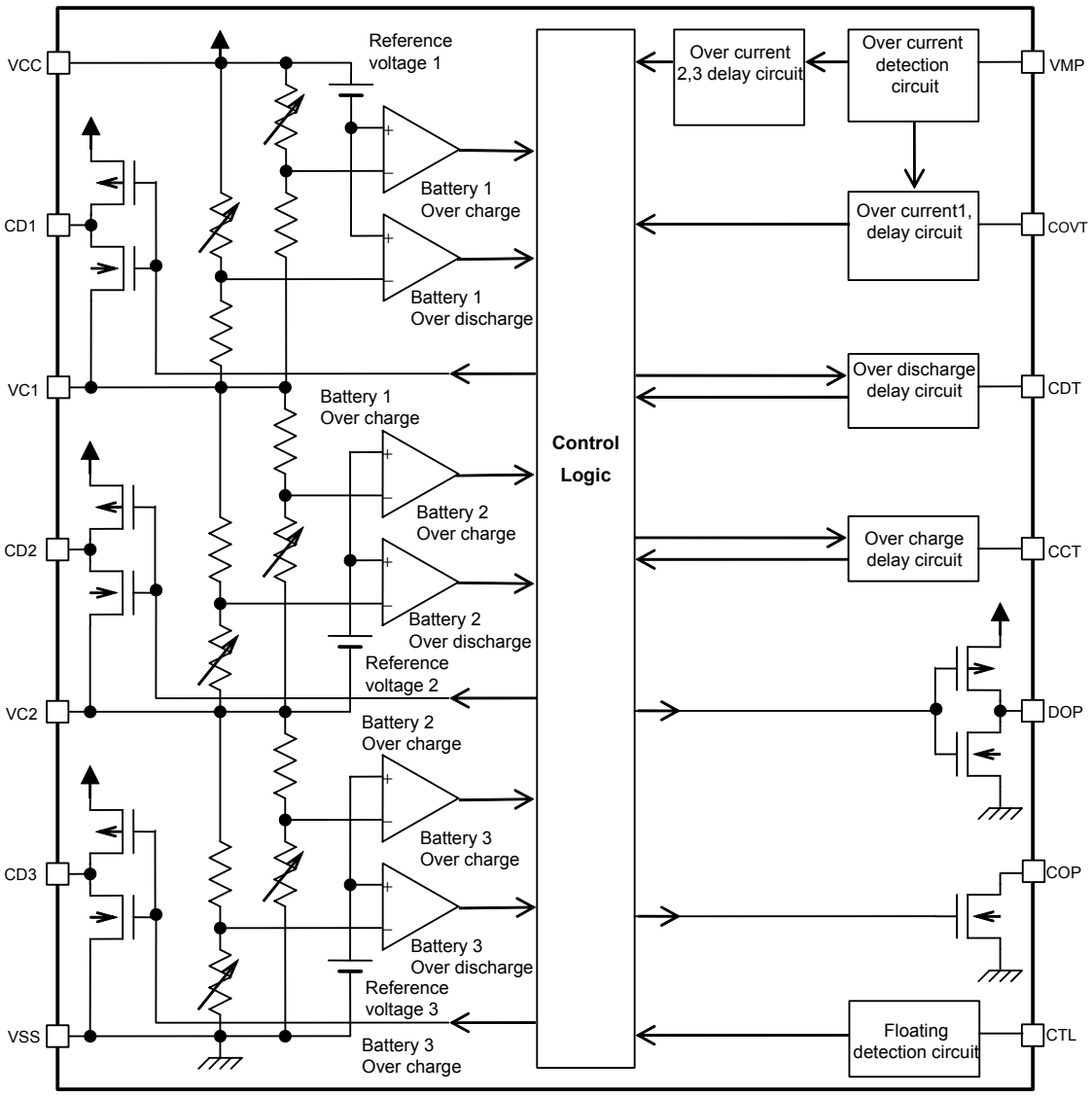


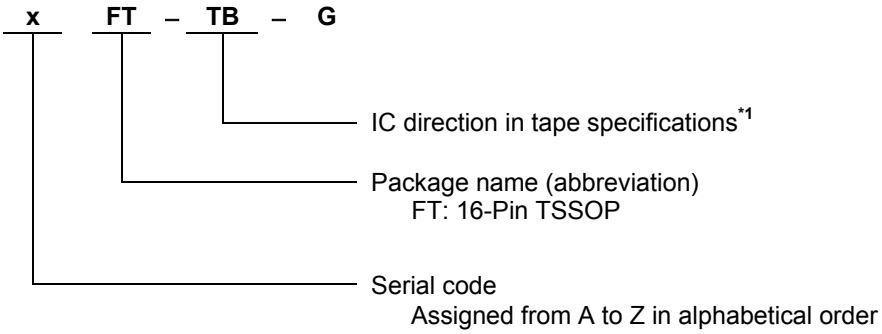
Figure 1

Remark The delay time for over current detection 2 and 3 is fixed by an internal IC circuit. The delay time cannot be changed via an external capacitor.

■ Product Name Structure

1. Product name

S-8233B x FT – TB – G



***1.** Refer to the tape specifications.

2. Product name list

Table 1

Product name / Item	Over charge detection voltage V_{CU}	Over charge release voltage V_{CD}	Overdischarge detection voltage V_{DD}	Overdischarge release voltage V_{DU}	Overcurrent detection voltage1 V_{IOV1}	0V battery charging function	Conditioning function	CTL logic*1
S-8233BAFT-TB-G	4.225±0.025 V	4.225 V*2	2.30±0.08 V	2.70±0.10 V	0.20±0.02 V	–	Available	normal
S-8233BBFT-TB-G	4.325±0.025 V	4.15±0.10 V	2.30±0.08 V	2.70±0.10 V	0.20±0.02 V	–	Unavailable	reverse
S-8233BCFT-TB-G	4.200±0.025 V	4.2 V	2.80±0.08 V	3.30±0.10 V	0.25±0.025 V	Available	Available	normal
S-8233BDFT-TB-G	4.325±0.025 V	4.15±0.10 V	2.00±0.08 V	2.70±0.10 V	0.50±0.05 V	–	Unavailable	reverse
S-8233BEFT-TB-G	4.080±0.025 V	3.90±0.10 V	2.50±0.08 V	2.75±0.10 V	0.20±0.02 V	Available	Available	normal

***1.** The input voltage of CTL for normal condition is changed by the CTL logic. (Please refer to **"Operation"**).

***2.** Without over charge detection / release hysteresis.

Remark Please contact our sales office for the products with the detection voltage value other than those specified above.

■ Pin Configuration

16-Pin TSSOP
Top view

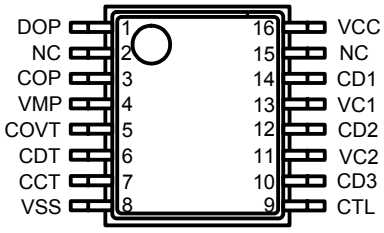


Figure 2

Table 2

Pin No.	Symbol	Description
1	DOP	Connects FET gate for discharge control (CMOS output)
2	NC	Non connect*1
3	COP	Connects FET gate for charge control (Nch open-drain output)
4	VMP	Detects voltage between VCC to VMP(Over current detection pin)
5	COVT	Connects capacitor for over current detection1delay circuit
6	CDT	Connects capacitor for over discharge detection delay circuit
7	CCT	Connects capacitor for over charge detection delay circuit
8	VSS	Negative power input, and connects negative voltage for battery 3
9	CTL	Charge/discharge control signal input
10	CD3	Battery 3 conditioning signal output
11	VC2	Connects battery 2 negative voltage and battery 3 positive voltage
12	CD2	Battery 2 conditioning signal output
13	VC1	Connects battery 1 negative voltage and battery 2 positive voltage
14	CD1	Battery 1 conditioning signal output
15	NC	Non connect*1
16	VCC	Positive power input and connects battery 1 positive voltage

***1**. The NC pin is electrically open. The NC pin can be connected to VCC or VSS.

■ Absolute Maximum Ratings

Table 3

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applied Pins	Absolute Maximum Ratings	Unit
Input voltage between VCC and VSS	V_{DS}	−	V_{SS}-0.3 to V_{SS}+26	V
Input terminal voltage	V_{IN}	VC1, VC2, CTL, CCT, CDT, COVT	V_{SS}-0.3 to V_{CC}+0.3	V
VMP Input terminal voltage	V_{VMP}	VMP	V_{SS}-0.3 to V_{SS}+26	V
CD1 output terminal voltage	V_{CD1}	CD1	VC1-0.3 to V_{CC}+0.3	V
CD2 output terminal voltage	V_{CD2}	CD2	VC2-0.3 to V_{CC}+0.3	V
CD3 output terminal voltage	V_{CD3}	CD3	V_{SS}-0.3 to V_{CC}+0.3	V
DOP output terminal voltage	V_{DOP}	DOP	V_{SS}-0.3 to V_{CC}+0.3	V
COP output terminal voltage	V_{COP}	COP	V_{SS}-0.3 to V_{VMP}+0.3	V
Power dissipation	P_D	−	300 (When not mounted on board)	mW
		−	1100*1	mW
Operating ambient temperature	T_{opr}	−	-20 to +70	°C
Storage temperature	T_{stg}	−	-40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

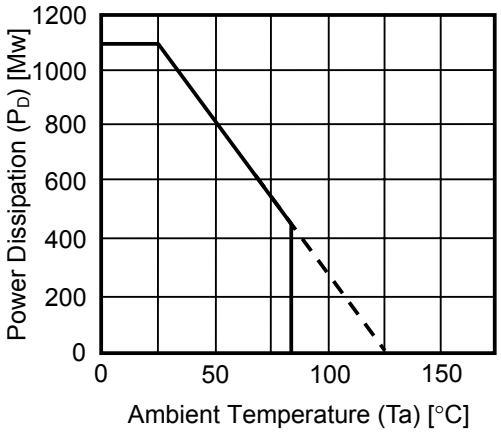


Figure 3 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 4 (1 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test condition	Test circuit
Detection voltage								
Over charge detection voltage 1	V_{CU1}	3.80 to 4.40 Adjustment	V_{CU1}-0.025	V_{CU1}	V_{CU1}+0.025	V	1	1
Over charge release voltage 1	V_{CD1}	3.45 to 4.40 Adjustment	V_{CD1}-0.10	V_{CD1}	V_{CD1}+0.10	V	1	1
Over discharge detection voltage 1	V_{DD1}	2.00 to 2.80 Adjustment	V_{DD1}-0.08	V_{DD1}	V_{DD1}+0.08	V	1	1
Over discharge release voltage 1	V_{DU1}	2.00 to 4.00 Adjustment	V_{DU1}-0.10	V_{DU1}	V_{DU1}+0.10	V	1	1
Over charge detection voltage 2	V_{CU2}	3.80 to 4.40 Adjustment	V_{CU2}-0.025	V_{CU2}	V_{CU2}+0.025	V	2	1
Over charge release voltage 2	V_{CD2}	3.45 to 4.40 Adjustment	V_{CD2}-0.10	V_{CD2}	V_{CD2}+0.10	V	2	1
Over discharge detection voltage 2	V_{DD2}	2.00 to 2.80 Adjustment	V_{DD2}-0.08	V_{DD2}	V_{DD2}+0.08	V	2	1
Over discharge release voltage 2	V_{DU2}	2.00 to 4.00 Adjustment	V_{DU2}-0.10	V_{DU2}	V_{DU2}+0.10	V	2	1
Over charge detection voltage 3	V_{CU3}	3.80 to 4.40 Adjustment	V_{CU3}-0.025	V_{CU3}	V_{CU3}+0.025	V	3	1
Over charge release voltage 3	V_{CD3}	3.45 to 4.40 Adjustment	V_{CD3}-0.10	V_{CD3}	V_{CD3}+0.10	V	3	1
Over discharge detection voltage 3	V_{DD3}	2.00 to 2.80 Adjustment	V_{DD3}-0.08	V_{DD3}	V_{DD3}+0.08	V	3	1
Over discharge release voltage 3	V_{DU3}	2.00 to 4.00 Adjustment	V_{DU3}-0.10	V_{DU3}	V_{DU3}+0.10	V	3	1
Over current detection voltage 1 *1	V_{IOV1}	0.15 to 0.50V Adjustment	V_{IOV1}×0.9	V_{IOV1}	V_{IOV1}×1.1	V	4	2
Over current detection voltage 2	V_{IOV2}	V_{CC} Reference	0.54	0.6	0.66	V	4	2
Over current detection voltage 3	V_{IOV3}	V_{SS} Reference	1.0	2.0	3.0	V	4	2
Voltage temperature factor 1 *2	T_{COE1}	Ta=-20 to 70°C *4	-1.0	0	1.0	mV/°C	–	–
Voltage temperature factor 2 *3	T_{COE2}	Ta=-20 to 70°C *4	-0.5	0	0.5	mV/°C	–	–
Delay time								
Over charge detection delay time 1	t_{CU1}	C_{CCT}=0.47 µF	0.5	1.0	1.5	s	9	6
Over charge detection delay time 2	t_{CU2}	C_{CCT}=0.47 µF	0.5	1.0	1.5	s	10	6
Over charge detection delay time 3	t_{CU3}	C_{CCT}=0.47 µF	0.5	1.0	1.5	s	11	6
Over discharge detection delay time 1	t_{DD1}	C_{CDT}=0.1 µF	20	40	60	ms	9	6
Over discharge detection delay time 2	t_{DD2}	C_{CDT}=0.1 µF	20	40	60	ms	10	6
Over discharge detection delay time 3	t_{DD3}	C_{CDT}=0.1 µF	20	40	60	ms	11	6
Over current detection delay time 1	t_{IOV1}	C_{COVT}=0.1 µF	10	20	30	ms	12	7
Over current detection delay time 2	t_{IOV2}	–	2	4	8	ms	12	7
Over current detection delay time 3	t_{IOV3}	FET gate capacitor =2000 pF	100	300	550	µs	12	7
Operating voltage								
Operating voltage between VCC and VSS *5	V_{DSOP}	–	2.0	–	24	V	–	–
Current consumption								
Current consumption (during normal operation)	I_{OPE}	V1=V2=V3=3.5 V	–	20	50	µA	5	3
Current consumption for cell 1	I_{CELL1}	V1=V2=V3=3.5 V	–300	0	300	nA	5	3
Current consumption for cell 2	I_{CELL2}	V1=V2=V3=3.5 V	–300	0	300	nA	5	3
Current consumption for cell 3	I_{CELL3}	V1=V2=V3=3.5 V	–300	0	300	nA	5	3
Current consumption at power down	I_{PDN}	V1=V2=V3=1.5 V	–	–	0.1	µA	5	3
Internal resistance with 0V battery charging function type								
Resistance between VCC and VMP	R_{VCM}	V1=V2=V3=3.5 V	0.20	0.50	0.80	MΩ	6	3
Resistance between VSS and VMP	R_{VSM}	V1=V2=V3=1.5 V	0.20	0.50	0.80	MΩ	6	3
Internal resistance without 0V battery charging function type.								
Resistance between VCC and VMP	R_{VCM}	V1=V2=V3=3.5 V	0.40	0.90	1.40	MΩ	6	3
Resistance between VSS and VMP	R_{VSM}	V1=V2=V3=1.5 V	0.40	0.90	1.40	MΩ	6	3
Input voltage								
CTL"H" Input voltage	$V_{CTL(H)}$	–	V_{CC} x 0.8	–	–	V	16	1
CTL"L" Input voltage	$V_{CTL(L)}$	–	–	–	V_{CC} x 0.2	V	16	1

Table 4 (2 / 2)

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test condition	Test circuit
Output voltage								
DOP"H" voltage	$V_{DO(H)}$	I_{OUT}=10 µA	V_{CC}-0.5	–	–	V	7	4
DOP"L" voltage	$V_{DO(L)}$	I_{OUT}=10 µA	–	–	V_{SS}+0.1	V	7	4
COP"L" voltage	$V_{CO(L)}$	I_{OUT}=10 µA	–	–	V_{SS}+0.1	V	8	5
COP OFF LEAK current	I_{COL}	V1=V2=V3=4.5 V	–	–	100	nA	14	9
CD1"H" voltage	$V_{CD1(H)}$	I_{OUT}=0.1 µA	V_{CC}-0.5	–	–	V	13	8
CD1"L" voltage	$V_{CD1(L)}$	I_{OUT}=10 µA	–	–	V_{C1}+0.1	V	13	8
CD2"H" voltage	$V_{CD2(H)}$	I_{OUT}=0.1 µA	V_{CC}-0.5	–	–	V	13	8
CD2"L" voltage	$V_{CD2(L)}$	I_{OUT}=10 µA	–	–	V_{C2}+0.1	V	13	8
CD3"H" voltage	$V_{CD3(H)}$	I_{OUT}=0.1 µA	V_{CC}-0.5	–	–	V	13	8
CD3"L" voltage	$V_{CD3(L)}$	I_{OUT}=10 µA	–	–	V_{SS}+0.1	V	13	8
0V battery charging function[*6]								
0V charging start voltage	V_{0CHAR}	V1=V2=V3=0 V	–	–	1.4	V	15	10

***1.** If over current detection voltage 1 is 0.50 V, both over current detection voltages 1 and 2 are 0.54 to 0.55 V, but $V_{IOV2} > V_{IOV1}$.

***2.** Voltage temperature factor 1 indicates over charge detection voltage, over charge release voltage, over discharge detection voltage, and over discharge release voltage.

***3.** Voltage temperature factor 2 indicates over current detection voltage.

***4.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***5.** The DOP and COP logic must be established for the operating voltage.

***6.** This spec applies for only 0 V battery charging function available type.

■ Test Circuits

Caution At the Test circuit from (1) to (15).

If the device's CTL logic is "normal" (S-8233BA, S-8233BC, S-8233BE) then set the CTL voltage at V_{SS} (V4=0V).

If the device's CTL logic is "reverse" (S-8233BB, S-8233BD) then set the CTL voltage at V_{CC} (V4=V1+V2+V3).

(1) Test condition 1 Test circuit 1

Set V1, V2, and V3 to 3.5 V under normal condition. Increase V1 from 3.5 V gradually. The V1 voltage when COP = 'H' is over charge detection voltage 1 (V_{CU1}). Decrease V1 gradually. The V1 voltage when COP = 'L' is over charge release voltage 1 (V_{CD1}). Further decrease V1. The V1 voltage when DOP = 'H' is over discharge voltage 1 (V_{DD1}). Increase V1 gradually. The V1 voltage when DOP = 'L' is over discharge release voltage 1 (V_{DU1}).

Remark: The voltage change rate is 150 V/s or less.

(2) Test condition 2 Test circuit 1

Set V1, V2, and V3 to 3.5 V under normal condition. Increase V2 from 3.5 V gradually. The V2 voltage when COP = 'H' is over charge detection voltage 2 (V_{CU2}). Decrease V2 gradually. The V2 voltage when COP = 'L' is over charge release voltage 2 (V_{CD2}). Further decrease V2. The V2 voltage when DOP = 'H' is over discharge voltage 2 (V_{DD2}). Increase V2 gradually. The V2 voltage when DOP = 'L' is over discharge release voltage 2 (V_{DU2}).

Remark: The voltage change rate is 150 V/s or less.

(3) Test condition 3 Test circuit 1

Set V1, V2, and V3 to 3.5 V under normal condition. Increase V3 from 3.5 V gradually. The V3 voltage when COP = 'H' is over charge detection voltage 3 (V_{CU3}). Decrease V3 gradually. The V3 voltage when COP = 'L' is over charge release voltage 3 (V_{CD3}). Further decrease V3. The V3 voltage when DOP = 'H' is over discharge voltage 3 (V_{DD3}). Increase V3 gradually. The V3 voltage when DOP = 'L' is over discharge release voltage 3 (V_{DU3}).

Remark: The voltage change rate is 150 V/s or less.

(4) Test condition 4 Test circuit 2

Set V1, V2, V3 to 3.5 V and V5 to 0 V under normal condition. Increase V5 from 0 V gradually. The V5 voltage when DOP = 'H' and COP = 'H', is over current detection voltage 1 (V_{IOV1}).

Set V1, V2, and V3 to 3.5 V and V5 to 0 V under normal condition. Fix the COVT terminal at V_{SS}, increase V5 from 0 V gradually. The V5 voltage when DOP = 'H' and COP = 'H' is over current detection voltage 2 (V_{IOV2}).

Set V1, V2, and V3 to 3.5 V and V5 to 0 V under normal condition. Fix the COVT terminal at V_{SS}, increase V5 gradually from 0 V at 400 μs to 2 ms. The V5 voltage when DOP = 'H' and COP = 'H' is over current detection voltage 3 (V_{IOV3}).

(5) Test condition 5 Test circuit 3

Set S1 to ON, V1, V2, and V3 to 3.5 V, and V5 to 0 V under normal condition and measure current consumption. I1 is the normal condition current consumption (I_{OPE}), I2, the cell 2 current consumption (I_{CELL2}), and I3, the cell 3 current consumption (I_{CELL3}).

Set S1 to ON, V1, V2, and V3 to 1.5 V, and V5 to 4.5 V under over discharge condition. Current consumption I1 is power-down current consumption (I_{PDN}).

(6) Test condition 6 Test circuit 3

Set S1 to ON, V1, V2, and V3 to 3.5 V, and V5 to 10.5 V under normal condition. V5/I5 is the internal resistance between VCC and VMP (R_{VCM}).

Set S1 to ON, V1, V2, and V3 to 1.5 V, and V5 to 4.1 V under over discharge condition. (4.5-V5)/I5 is the internal resistance between VSS and VMP (R_{VCM}).

(7) Test condition 7 Test circuit 4

Set S1 to ON, S2 to OFF, V1, V2, and V3 to 3.5 V, and V5 to 0 V under normal condition. Increase V6 from 0 V gradually. The V6 voltage when I6 = 10 μA is DOP'L' voltage ($V_{D0\,(L)}$).

Set S1 to OFF, S2 to ON, V1, V2, V3 to 3.5 V, and V5 to V_{IOV2}+0.1 V under over current condition. Increase V7 from 0 V gradually. The V7 voltage when I7 = 10 μA is the DOP'H' voltage ($V_{DO\,(H)}$).

(8) Test condition 8 Test circuit 5

Set V1, V2, V3 to 3.5 V and V5 to 0 V under normal condition. Increase V6 from 0 V gradually. The V6 voltage when I1 = 10 μA is the COP'L' voltage ($V_{C0\,(L)}$).

(9) Test condition 9 Test circuit 6

Set V1, V2, V3 to 3.5 V under normal condition. Increase V1 from 3.5 V to 4.5 V immediately (within 10 μs). The time after V1 becomes 4.5 V until COP goes 'H' is the over charge detection delay time 1 (t_{CU1}).

Set V1, V2, V3 to 3.5 V under normal condition. Decrease V1 from 3.5 V to 1.9 V immediately (within 10 μs). The time after V1 becomes 1.9 V until DOP goes 'H' is the over discharge detection delay time 1 (t_{DD1}).

(10) Test condition 10 Test circuit 6

Set V1, V2, V3 to 3.5 V under normal condition. Increase V2 from 3.5 V to 4.5 V immediately (within 10 μs). The time after V2 becomes 4.5 V until COP goes 'H' is the over charge detection delay time 2 (t_{CU2}).

Set V1, V2, V3 to 3.5 V under normal condition. Decrease V2 from 3.5 V to 1.9 V immediately (within 10 μs). The time after V2 becomes 1.9 V until DOP goes 'H' is the over discharge detection delay time 2 (t_{DD2}).

(11) Test condition 11 Test circuit 6

Set V1, V2, V3 to 3.5 V under normal condition. Increase V3 from 3.5 V to 4.5 V immediately (within 10 μs). The time after V3 becomes 4.5 V until COP goes 'H' is the over charge detection delay time 3 (t_{CU3}).

Set V1, V2, V3 to 3.5 V under normal condition. Decrease V3 from 3.5 V to 1.9 V immediately (within 10 μs). The time after V3 becomes 1.9 V until DOP goes 'H' is the over discharge detection delay time 3 (t_{DD3}).

(12) Test condition 12 Test circuit 7

Set V1, V2, V3 to 3.5 V and S1 to OFF under normal condition. Increase V5 from 0 V to 0.55 V immediately (within 10 μs). The time after V5 becomes 0.55 V until DOP goes 'H' is the over current detection delay time 1 (t_{IOV1}).

Set V1, V2, V3 to 3.5 V and S1 to OFF under normal condition. Increase V5 from 0 V to 0.75 V immediately (within 10 μs). The time after V4 becomes 0.75 V until DOP goes 'H' is the over current detection delay time 2 (t_{IOV2})

Set S1 to ON to inhibit over discharge detection. Set V1, V2, V3 to 4.0 V and increase V5 from 0 V to 6.0 V immediately (within 1 μs) and decrease V1, V2, and V3 to 2.0 V at a time. The time after V5 becomes 6.0 V until DOP goes 'H' is the over current detection delay time 3 (t_{IOV3}).

(13) Test condition 13 Test circuit 8

Set S4 to ON, S1, S2, S3, S5, and S6 to OFF, V1, V2, V3 to 3.5 V and V6, V7, and V8 to 0 V under normal condition. Increase V5 from 0 V gradually. The V5 voltage when I5 = 10 μA is the CD1'L' voltage ($V_{CD1(L)}$)

Set S5 to ON, S1, S2, S3, S4, and S6 to OFF, V1, V2, and V3 to 3.5 V and V5, V7, and V8 to 0 V under normal condition. Increase V6 from 0 V gradually. The V6 voltage when I6 = 10 μA is the CD2'L' voltage ($V_{CD2(L)}$).

Set S6 to ON, S1, S2, S3, S4, and S5 to OFF, V1, V2, and V3 to 3.5 V and V5, V6, and V8 to 0 V under normal condition. Increase V7 from 0 V gradually. The V7 voltage when I7 = 10 μA is the CD3'L' voltage ($V_{CD3(L)}$).

Set S1 to ON, S2, S3, S4, S5, and S6 to OFF, V1 to 4.5 V, V2 and V3 to 3.5 V and V5, V6, and V7 to 0 V under over charge condition. Increase V8 from 0 V gradually. The V8 voltage when I8 = 0.1 μA is the CD1'H' voltage ($V_{CD1(H)}$).

Set S2 to ON, S1, S3, S4, S5, and S6 to OFF, V2 to 4.5 V, V1 and V3 to 3.5 V and V5, V6, and V7 to 0 V under over charge condition. Increase V4 from 0 V gradually. The V4 voltage when I1 = 0.1 μA is the CD2'H' voltage ($V_{CD2(H)}$).

Set S3 to ON, S1, S2, S4, S5, and S6 to OFF, V3 to 4.5 V, V1 and V2 to 3.5 V and V5, V6, and V7 to 0 V under over charge condition. Increase V8 from 0 V gradually. The V8 voltage when I8 = 0.1 μA is the CD3'H' voltage ($V_{CD3(H)}$).

(14) Test condition 14 Test circuit 9

Set V1, V2, and V3 to 4.5 V under over charge condition. The current I1 flowing to COP terminal is COP OFF LEAK current (I_{COL}).

(15) Test condition 15 Test circuit 10

Set V1, V2, and V3 to 0 V, and V5 to 2 V, and decrease V5 gradually. The V5 voltage when COP = 'H' (V_{SS} + 0.3 V or higher) is the 0 V charge start voltage (V_{0CHAR}).

(16) Test condition 16 Test circuit 1

Test condition will be changed by the CTL logic

<1> **If the CTL logic is "normal"**

Set V1, V2, and V3 to 3.5 V, and V4 to 0 V, and increase V4 gradually. The V4 voltage when COP = 'H' (V_{SS} + 0.3 V or higher) and DOP = 'H' (V_{SS} + 0.3 V or higher) is the CTL 'H' input voltage ($V_{CTL(H)}$).

After that decrease V4 gradually. The V4 voltage when COP = 'L' (V_{CC} - 0.3 V or lower) and DOP = 'L' (V_{CC} - 0.3 V or lower) is the CTL'L' input voltage ($V_{CTL(L)}$).

<2> **If the CTL logic is "reverse"**

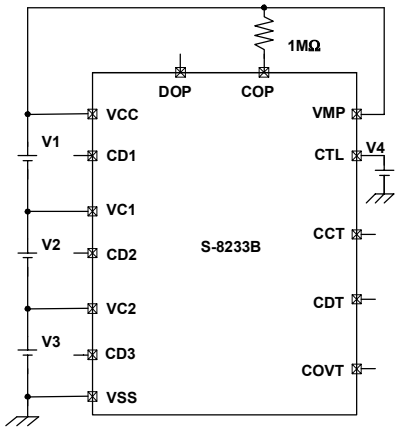
Set V1, V2, and V3 to 3.5 V, and V4 to10.5 V, and decrease V4 gradually. The V4 voltage when COP = 'H' (V_{SS} + 0.3 V or higher) and DOP = 'H' (V_{SS} + 0.3 V or higher) is the CTL'L' input voltage ($V_{CTL(L)}$).

After that increase V4 gradually. The V4 voltage when COP ='L' (V_{VMP} - 0.3 V or lower) and DOP = 'L' (V_{CC} - 0.3 V or lower) is the CTL'H' input voltage ($V_{CTL(H)}$).

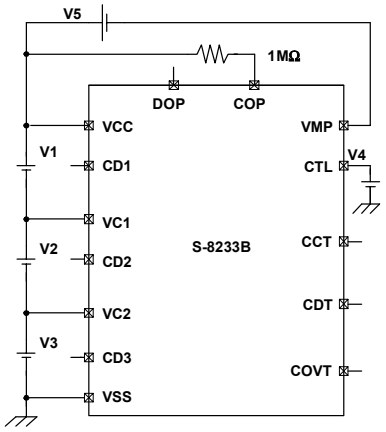
Caution At the Test circuit from 1 to 10.

If the device's CTL logic is "normal" (S-8233BA, S-8233BC, S-8233BE) then set the CTL voltage at V_{SS} (V4=0 V).

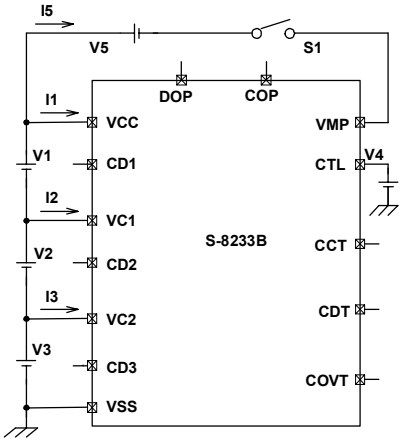
If the device's CTL logic is "reverse" (S-8233BB, S-8233BD) then set the CTL voltage at V_{CC} (V4=V1+V2+V3).



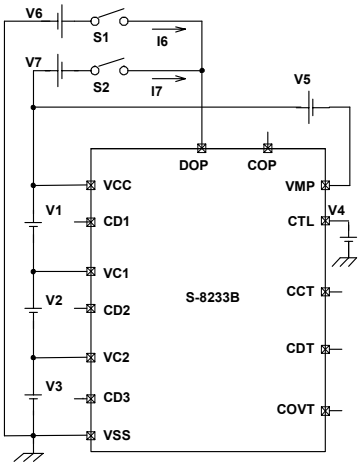
Test circuit 1



Test circuit 2

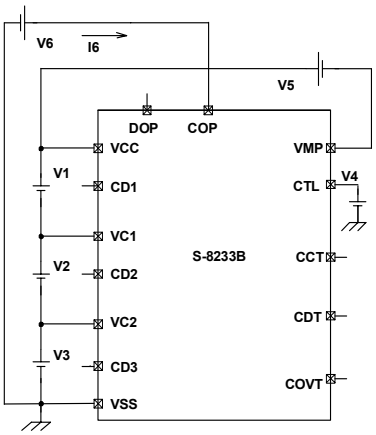


Test circuit 3

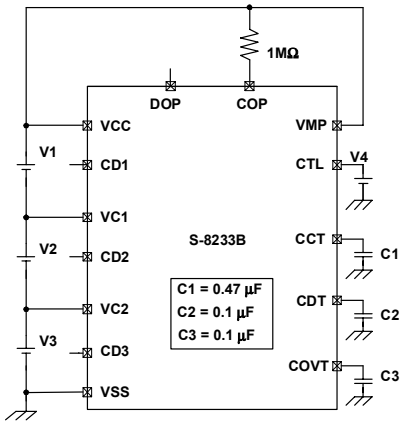


Test circuit 4

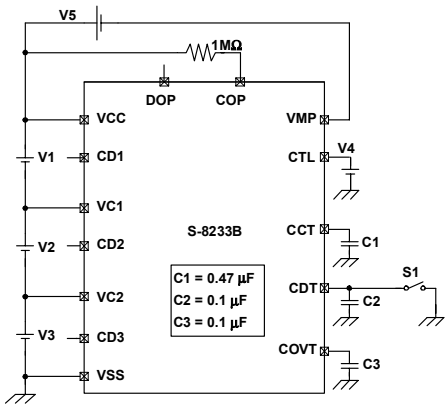
Figure 4 (1/2)



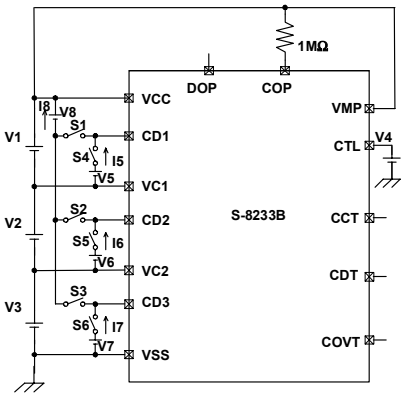
Test circuit 5



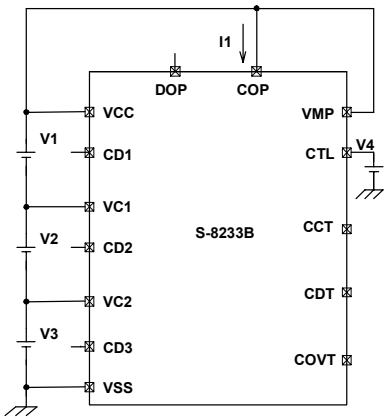
Test circuit 6



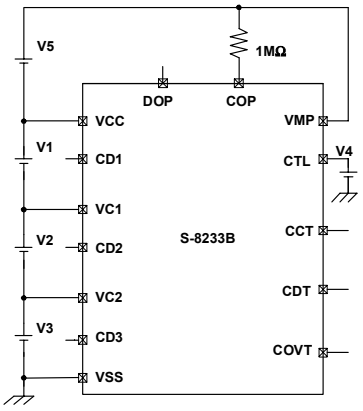
Test circuit 7



Test circuit 8



Test circuit 9



Test circuit 10

Figure 4 (2/2)

■ Operation

Remark Refer to "**Battery Protection IC Connection Example**".

Normal condition

This IC monitors the voltages of the three serially-connected batteries and the discharge current to control charging and discharging. If the voltages of all the three batteries are in the range from the over discharge detection voltage (V_{DD}) to the over charge detection voltage (V_{CU}), and the current flowing through the batteries becomes equal or lower than a specified value (the VMP terminal voltage is equal or lower than over current detection voltage 1), the charging and discharging FETs turn on. In this condition, charging and discharging can be carried out freely. This condition is called the normal condition. In this condition, the VMP and VCC terminals are shorted by the R_{VCM} resistor.

Over current condition

This IC is provided with the three over current detection levels (V_{IOV1},V_{IOV2} and V_{IOV3}) and the three over current detection delay time (t_{IOV1},t_{IOV2} and t_{IOV3}) corresponding to each over current detection level.

If the discharging current becomes equal to or higher than a specified value (the VMP terminal voltage is equal to or higher than the over current detection voltage) during discharging under normal condition and it continues for the over current detection delay time (t_{IOV}) or longer, the discharging FET turns off to stop discharging. This condition is called an over current condition. The VMP and VCC terminals are shorted by the R_{VCM} resistor at this time. The charging FET turns off.

When the discharging FET is off and a load is connected, the VMP terminal voltage equals the V_{SS} potential.

The over current condition returns to the normal condition when the load is released and the impedance between the EB- and EB+ terminals (see **Figure 9** for a connection example) is 100 MΩ or higher. When the load is released, the VMP terminal, which and the VCC terminal are shorted with the R_{VCM} resistor, goes back to the V_{CC} potential. The IC detects that the VMP terminal potential returns to over current detection voltage 1 (V_{IOV1}) or lower (or the over current detection voltage 2 (V_{IOV2}) or lower if the COVT terminal is fixed at the 'L' level and over current detection 1 is inhibited) and returns to the normal condition.

Over charge condition

If one of the battery voltages becomes higher than the over charge detection voltage (V_{CU}) during charging under normal condition and it continues for the over charge detection delay time (t_{CU}) or longer, the charging FET turns off to stop charging. This condition is called the over charge condition. The 'H' level signal is output to the conditioning terminal corresponding to the battery which exceeds the over charge detection voltage until the battery becomes equal to lower than the over charge release voltage (V_{CD}). The battery can be discharged by connecting an Nch FET externally. The discharging current can be limited by inserting R11, R12 and R13 resistors (see **Figure 9** for a connection example). The VMP and VCC terminals are shorted by the R_{VCM} resistor under the over charge condition.

The over charge condition is released in two cases:

<1> The battery voltage which exceeded the over charge detection voltage (V_{CU}) falls below the over charge release voltage (V_{CD}), the charging FET turns on and the normal condition returns.

<2> If the battery voltage which exceeded the over charge detection voltage (V_{CU}) is equal or higher than the over charge release voltage (V_{CD}), but the charger is removed, a load is placed, and discharging starts, the charging FET turns on and the normal condition returns.

The release mechanism is as follows: the discharge current flows through an internal parasitic diode of the charging FET immediately after a load is installed and discharging starts, and the VMP terminal voltage decreases by about 0.6 V from the VCC terminal voltage momentarily. The IC detects this voltage (over current detection voltage 1 or higher), releases the over charge condition and returns to the normal condition.

Over discharge condition

If any one of the battery voltages falls below the over discharge detection voltage (V_{DD}) during discharging under normal condition and it continues for the over discharge detection delay time (t_{DD}) or longer, the discharging FET turns off and discharging stops. This condition is called the over discharge condition. When the discharging FET turns off, the VMP terminal voltage becomes equal to the V_{SS} voltage and the IC's current consumption falls below the power-down current consumption (I_{PDN}). This condition is called the power-down condition. The VMP and VSS terminals are shorted by the R_{VSM} resistor under the over discharge and power-down conditions.

The power-down condition is canceled when the charger is connected and the voltage between VMP and V_{SS} is 3.0 V or higher (over current detection voltage 3). When all the battery voltages becomes equal to or higher than the over discharge release voltage (V_{DU}) in this condition, the over discharge condition changes to the normal condition.

Delay circuits

The over charge detection delay time (t_{CU1} to t_{CU3}), over discharge detection delay time (t_{DD1} to t_{DD3}), and over current detection delay time 1 (t_{IOV1}) are changed with external capacitors (C4 to C6).
The delay times are calculated by the following equations:

	Min.	Typ.	Max.	
t_{CU}[S] =Delay factor	(1.07,	2.13,	3.19)×C4	[uF]
t_{DD}[S] =Delay factor	(0.20,	0.40,	0.60)×C5	[uF]
t_{IOV1}[S]=Delay factor	(0.10,	0.20,	0.30)×C6	[uF]

Caution The delay time for over current detection 2 and 3 is fixed by an internal IC circuit. The delay time cannot be changed via an external capacitor.

CTL terminal

[If the CTL logic is “normal”]<S-8233BA, S-8233BC, S-8233BE>

If the CTL terminal is floated under normal condition, it is pulled up to the V_{CC} potential in the IC, and both the charging and discharging FETs turn off to inhibit charging and discharging. Both charging and discharging are also inhibited by applying the VCC terminal to the CTL terminal externally. At this time, the VMP and VCC terminals are shorted by the R_{VCM} resistor.

When the CTL terminal becomes equal to V_{SS} potential, charging and discharging are enabled and go back to their appropriate conditions for the battery voltages.

[If the CTL logic is“reverse”]<S-8233BB, S-8233BD>

When the CTL terminal becomes equal to V_{SS} potential, both the charging and discharging FETs turn off to inhibit charging and discharging. If the CTL terminal is floated under normal condition, charging and discharging are enabled and go back to their appropriate conditions for the battery voltages.

Caution Please note unexpected behavior might occur when electrical potential difference between the CTL pin ('L' level) and VSS is generated through the external filter (R_{VSS} and C_{VSS}) as a result of input voltage fluctuations.

Table.5 Output voltage & current consumption by CTL terminal voltage.

Statements		Normal &Over voltage state		Power down mode (Without charger)		
CTL terminal voltage		High & Floated	Low	High	Low	Floated
CTL logic "normal" S-8233BA S-8233BC S-8233BE	COP (Charge control)	High	Comply with battery voltage	High	Low	Unknown
	DOP (Discharge control)	High	Comply with battery voltage	High	High	High
	Current consumption	Typ.20 μA	Typ.20 μA	Typ. 1 nA	Typ. 1 nA	Unknown
CTL logic "reverse" S-8233BB S-8233BD	COP	Comply with battery voltage	High	Low	High	Unknown
	DOP	Comply with battery voltage	High	High	High	High
	Current consumption	Typ.20 μA	Typ.20 μA	Typ. 1 nA	Typ. 1 nA	Unknown

0 V battery charging function

This function is used to recharge the three serially-connected batteries after they self-discharge to 0 V. When the 0 V charging start voltage (V_{0CHAR}) or higher is applied to between VMP and VSS by connecting the charger, the charging FET gate is fixed to V_{SS} potential.

When the voltage between the gate sources of the charging FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging FET turns on to start charging. At this time, the discharging FET turns off and the charging current flows through the internal parasitic diode in the discharging FET. If all the battery voltages become equal to or higher than the over discharge release voltage (V_{DU}), the normal condition returns.

Caution In the products without 0 V battery charging function, the resistance between VCC and VMP and between VSS and VMP are lower than the products with 0 V battery charging function. It causes to that over charge detection voltage increases by the drop voltage of R5 (see Figure 9 for a connection example) with sink current at VMP.
The COP output is undefined below 2.0 V on VCC-VSS voltage in the products without 0 V battery charging function.

Voltage temperature factor

Voltage temperature factor 1 indicates over charge detection voltage, over charge release voltage, over discharge detection voltage, and over discharge release voltage.

Voltage temperature factor 2 indicates over current detection voltage.

The Voltage temperature factors 1 and 2 are expressed by the oblique line parts in **Figure 5**.

Ex. Voltage temperature factor of over charge detection voltage Typ.

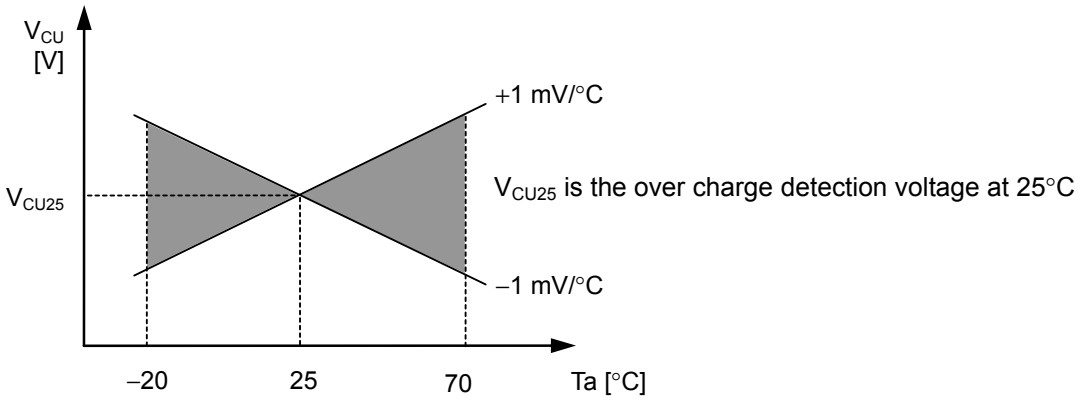
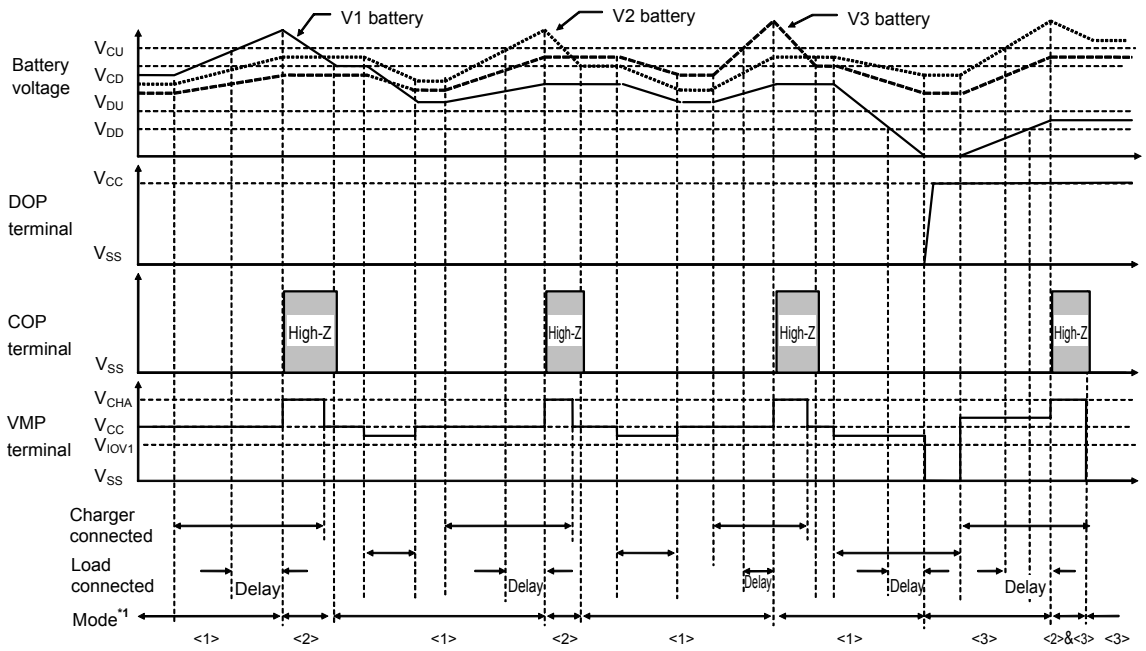


Figure 5

■ Timing Charts

1. Over charge detection

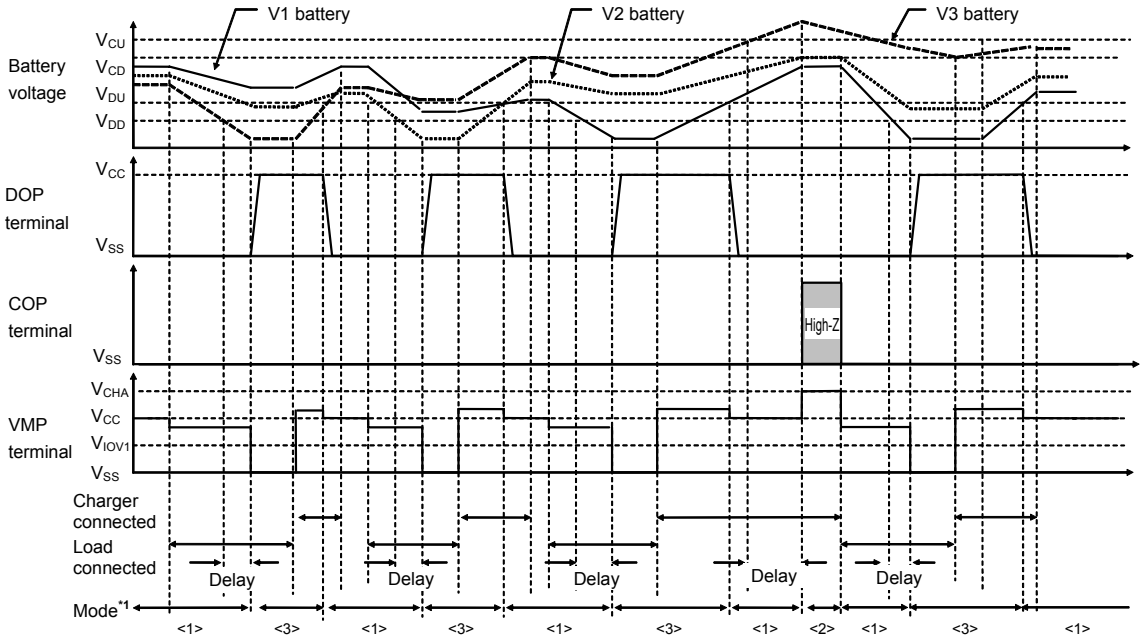


***1.** <1> Normal mode, <2> Over charge mode, <3> Over discharge mode, <4> Over current mode

Remark The charger is assumed to charge with a constant current. V_{CHA} indicates the open voltage of the charger.

Figure 6

2. Over discharge detection

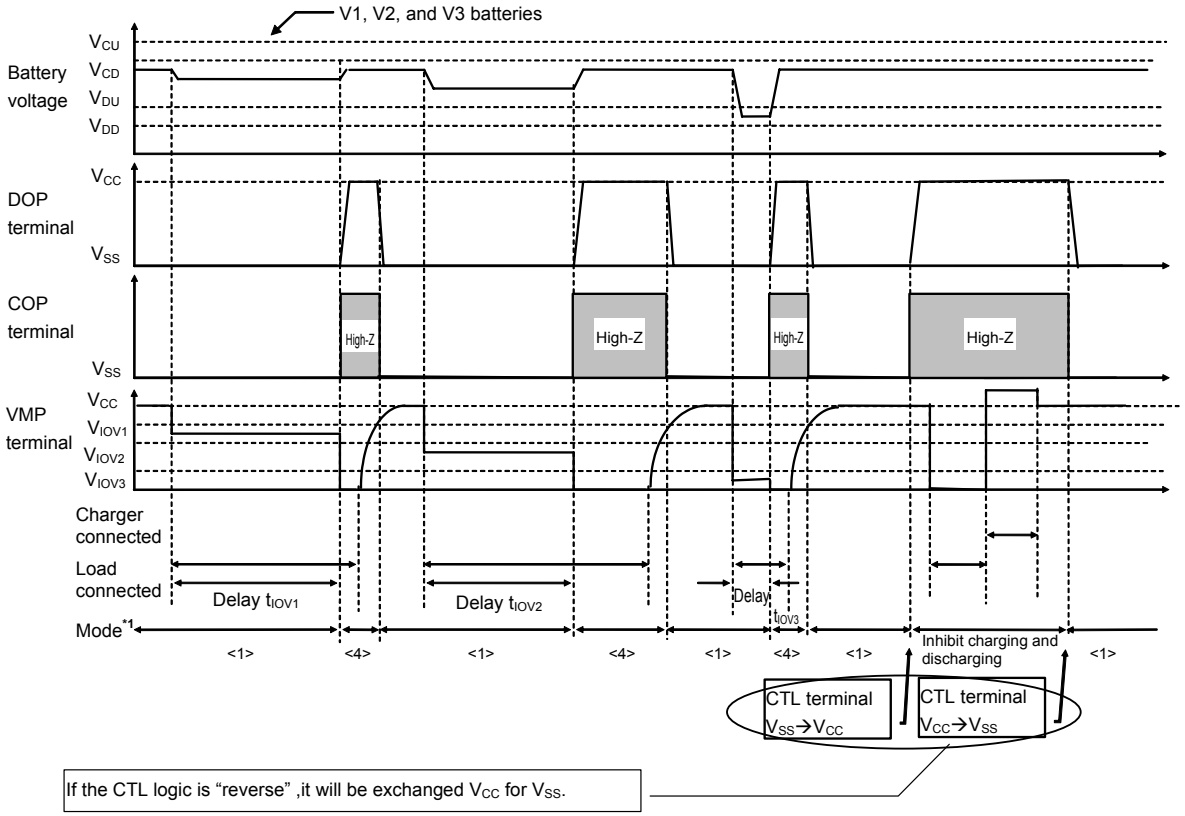


***1.** <1>Normal mode, <2>Over charge mode, <3>Over discharge mode, <4>Over current mode

Remark The charger is assumed to charge with a constant current. V_{CHA} indicates the open voltage of the charger.

Figure 7

3. Over current detection



***1.** <1>Normal mode, <2>Over charge mode, <3>Over discharge mode, <4>Over current mode

Figure 8

■ Battery Protection IC Connection Example

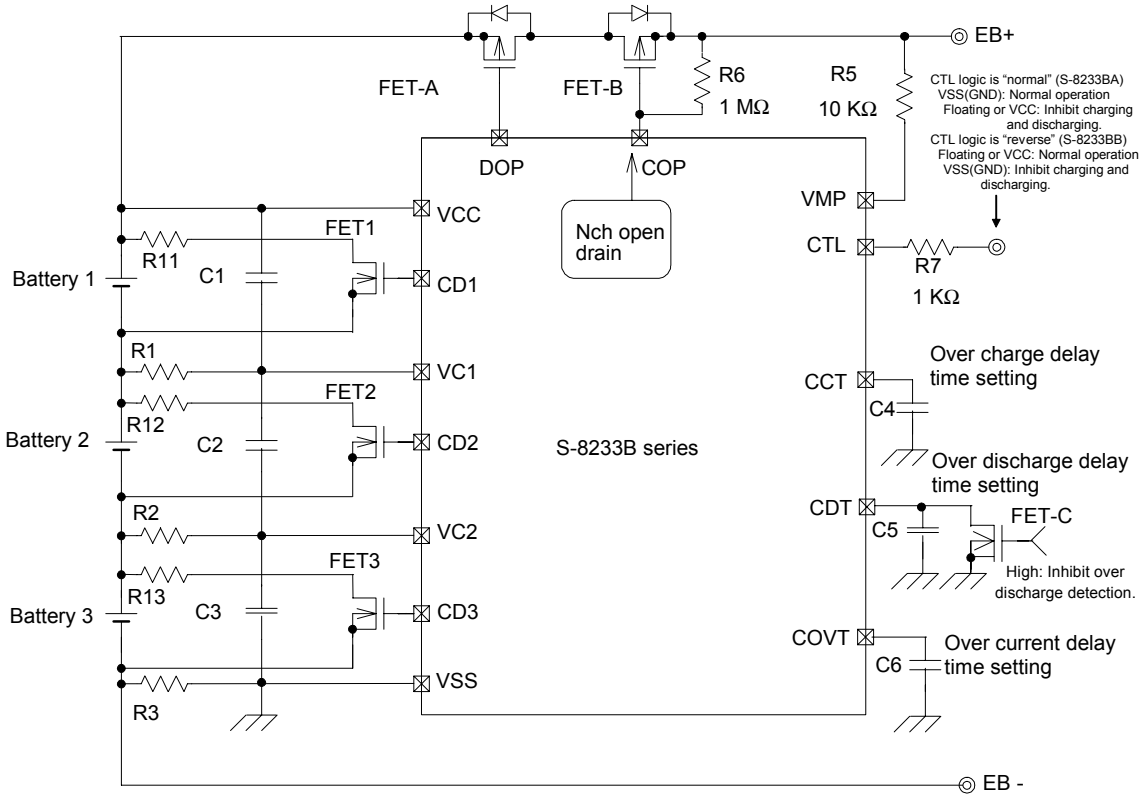


Figure 9

[Description of **Figure 9**]

- R11, R12, and R13 are used to adjust the battery conditioning current. The conditioning current during over charge detection is given by Vcu (over charge detection voltage)/R (R: resistance). To disable the conditioning function, open CD1, CD2, and CD3.
- The over charge detection delay time (t_{CU1} to t_{CU3}), over discharge detection delay time (t_{DD1} to t_{DD3}), and over current detection delay time (t_{I0V1}) are changed with external capacitors (C4 to C6). See the electrical characteristics.
- R6 is a pull-up resistor that turns FET-B off when the COP terminal is opened. Connect a 100 kΩ to 1 MΩ resistor.
- R5 is used to protect the IC if the charger is connected in reverse. Connect a 10 kΩ to 50 kΩ resistor.
- If capacitor C6 is absent, rush current occurs when a capacitive load is connected and the IC enters the over current mode. C6 must be connected to prevent it.
- If capacitor C5 is not connected, the IC may enter the over discharge condition due to variations of battery voltage when the over current occurs. In this case, a charger must be connected to return to the normal condition. To prevent this, connect an at least 0.01 μF capacitor to C5.
- If a leak current flows between the delay capacitor connection terminal (CCT, CDT, or COVT) and VSS, the delay time increases and an error occurs. The leak current must be 100 nA or less.
- Over discharge detection can be disabled by using FET-C. The FET-C off leak must be 0.1 μA or less. If over discharge is inhibited by using this FET, the current consumption does not fall below 0.1 μA even when the battery voltage drops and the IC enters the over discharge detection mode.
- R1, R2, and R3 must be 1 kΩ or less.
- R7 is the protection of the CTL when the CTL terminal voltage higher than V_{CC} voltage. Connect a 300 Ω to 5 kΩ resistor. If the CTL terminal voltage never greater than the V_{CC} voltage (ex. R7 connect to V_{SS}), without R7 resistance is allowed .

Caution 1. The above constants may be changed without notice.

2. If any electrostatic discharge of 2000 V or higher is not applied to the S-8233B series with a human body model, R1, R2, R3, C1, C2, and C3 are unnecessary.

3. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform through evaluation using the actual application to set the constant.

■ Precautions

- If a charger is connected in the over discharge condition and one of the battery voltages becomes equal to or higher than the over charge release voltage (V_{CU}) before the battery voltage which is below the over discharge detection voltage (V_{DD}) becomes equal to or higher than the over discharge release voltage (V_{DU}), the over discharge and over charge conditions are entered and the charging and discharging FETs turn off. Both charging and discharging are disabled. If the battery voltage which was higher than the over charge detection voltage (V_{CU}) falls to the over charge release voltage (V_{CD}) due to internal discharging, the charging FET turns on.
  If the charger is detached in the over charge and over discharge condition, the over charge condition is released, but the over discharge condition remains. If the charger is connected again, the battery condition is monitored after that. The charging FET turns off after the over charge detection delay time, the over charge and over discharge conditions are entered.

- If any one of the battery voltages is equal to or lower than the over discharge release voltage (V_{DU}) when they are connected for the first time, the normal condition may not be entered. If the VMP terminal voltage is made equal to or higher than the $\mathbf{v_{cc}}$ voltage (if a charger is connected), the normal condition is entered.

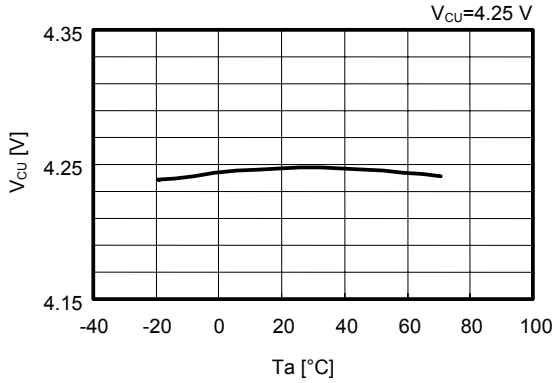
- If the CTL terminal floats in power-down mode, it is not pulled up in the IC, charging may not be inhibited. However, the over discharge condition becomes effective. At that time, current consumption would be increase because CTL terminal is affected by noise. If the charger is connected, the CTL terminal is pulled up, and charging and discharging are inhibited immediately.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

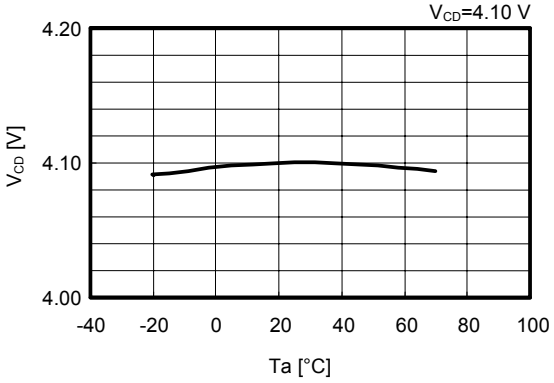
■ Characteristics (Typical Data)

1. Detection voltage temperature characteristics

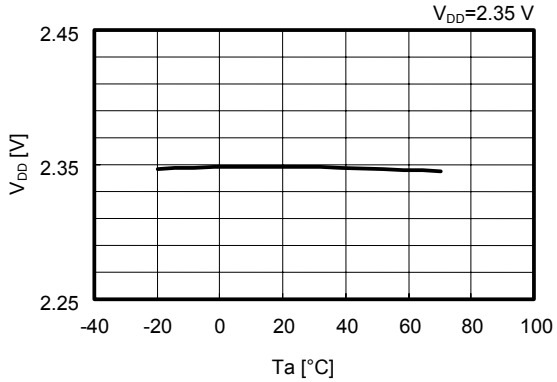
Overcharge detection voltage vs. temperature



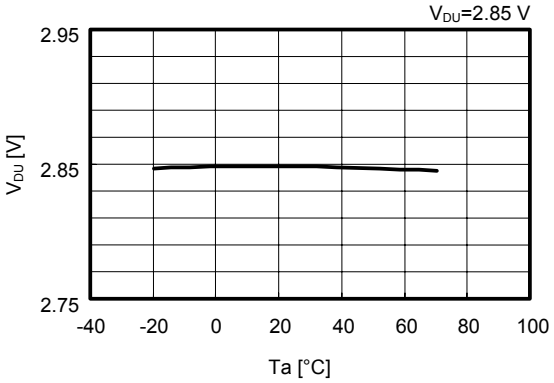
Overcharge release voltage vs. temperature



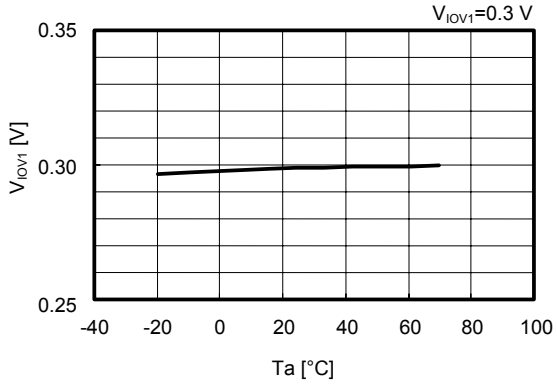
Overdischarge detection voltage vs. temperature



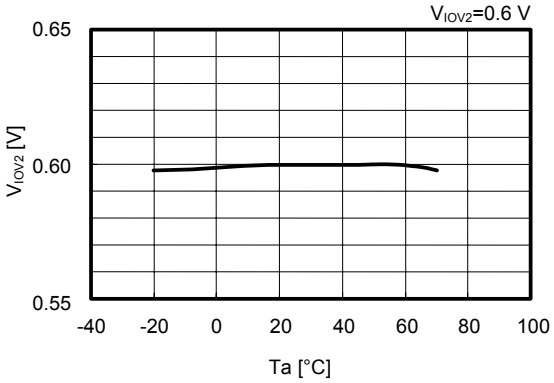
Overdischarge release voltage vs. temperature



Overcurrent1 detection voltage vs. temperature

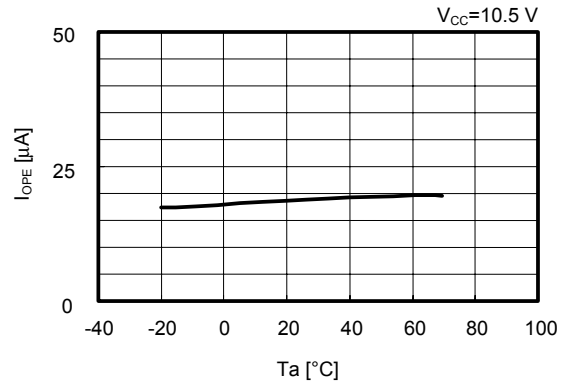


Overcurrent2 detection voltage vs. temperature

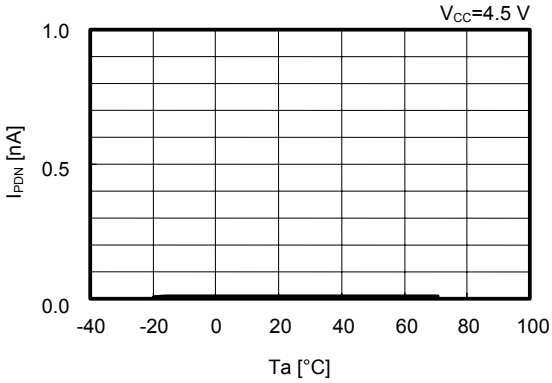


2. Current consumption temperature characteristics

Current consumption vs. temperature in normal mode

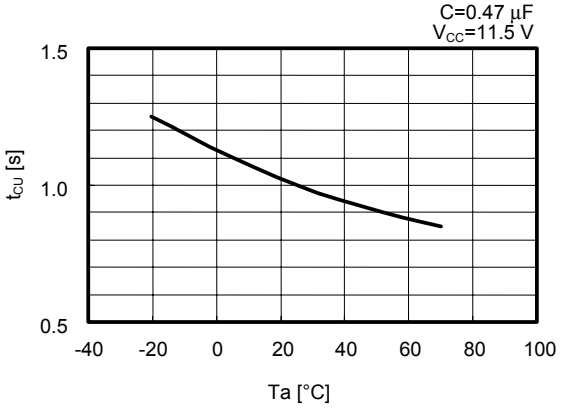


Current consumption vs. temperature in power-down mode

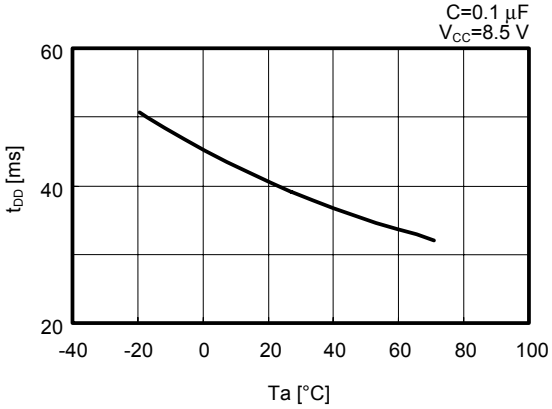


3. Delay time temperature characteristics

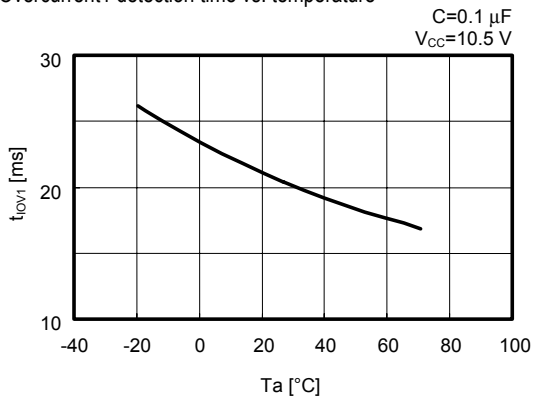
Overcharge detection time vs. temperature



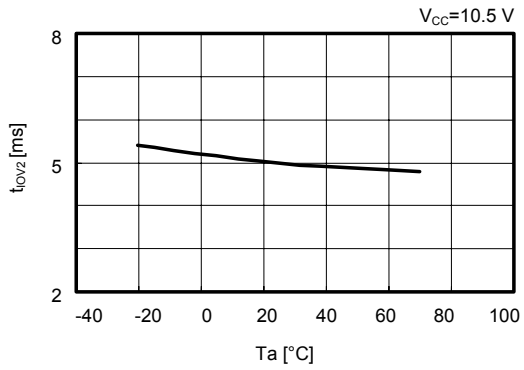
Overdischarge detection time vs. temperature

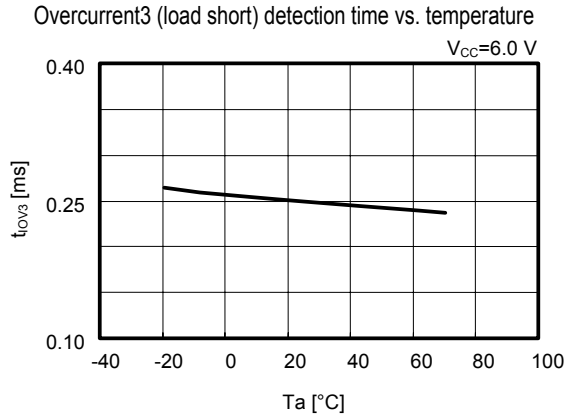


Overcurrent1 detection time vs. temperature

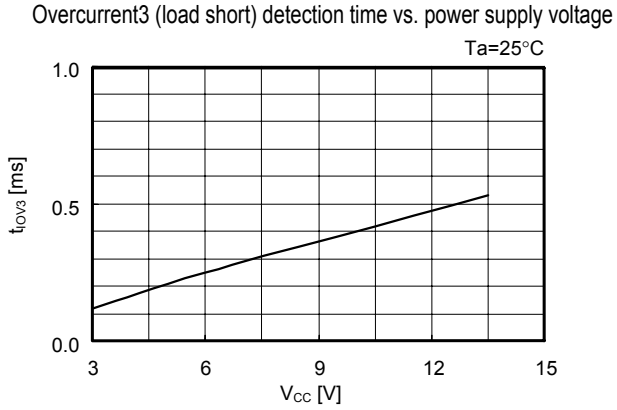


Overcurrent2 detection time vs. temperature

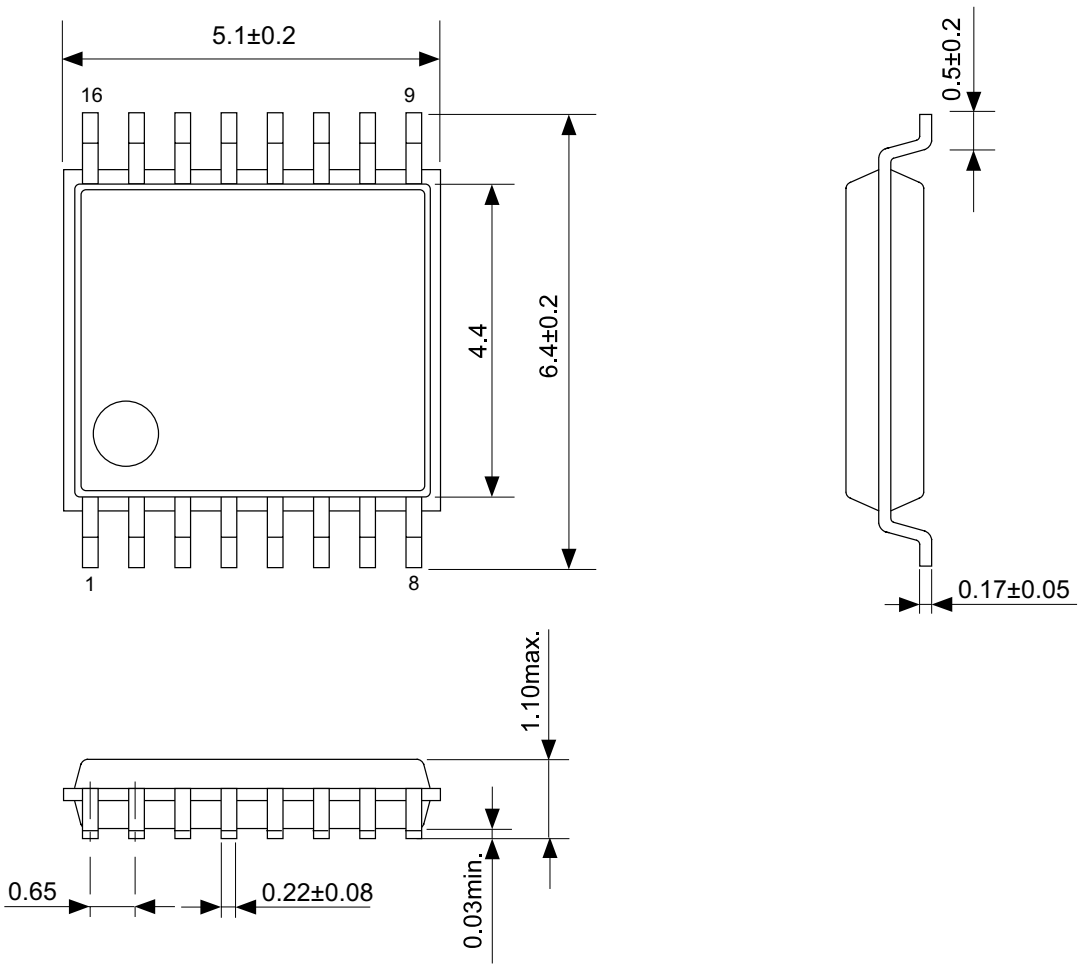




4. Delay time vs. power supply voltage

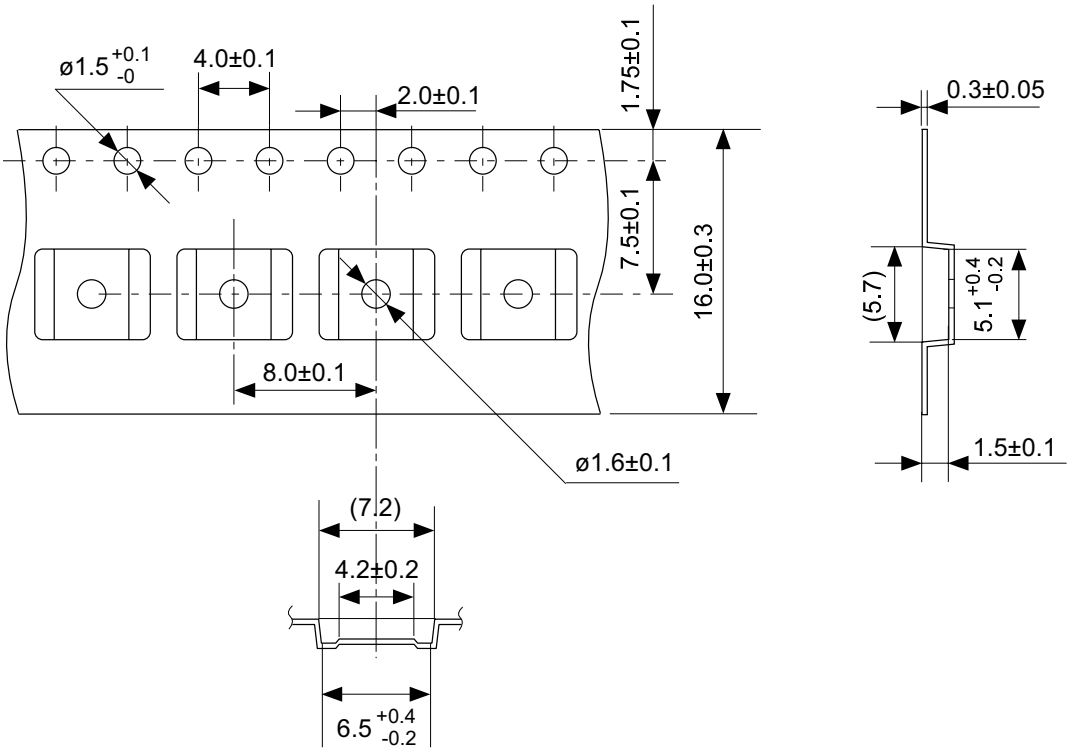


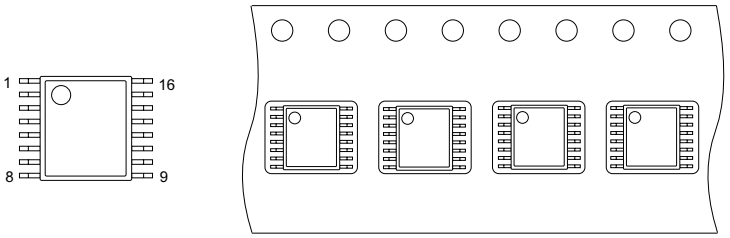
Caution Please design all applications of the S-8233B Series with safety in mind.



No. FT016-A-P-SD-1.1

TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

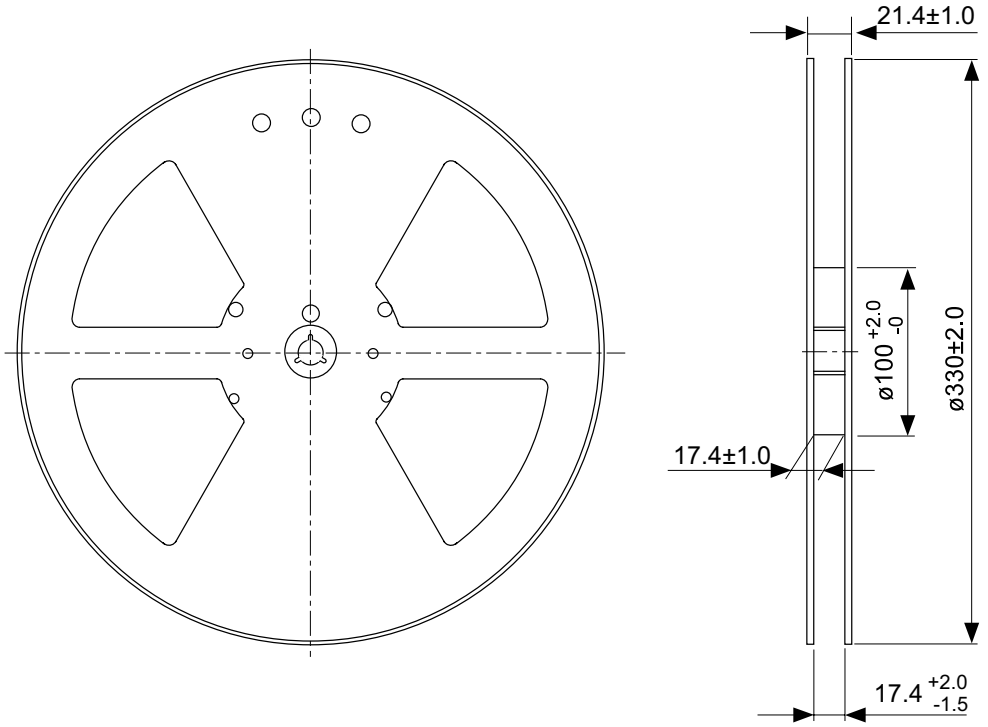




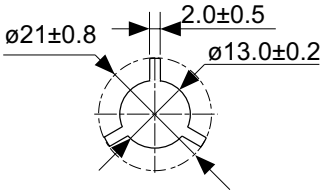
Feed direction

No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT016-A-R-SD-1.1

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			

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