S-8215A Series

BATTERY PROTECTION IC FOR 4-SERIAL / 5-SERIAL CELL PACK (SECONDARY PROTECTION)

www.sii-ic.com

Rev.1.1_00

The S-8215A Series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit. Short-circuits between VC5 to VSS accommodate series connection of four cells or five cells.

■ Features

- High-accuracy voltage detection circuit for each cell
  Overcharge detection voltage n (n = 1 to 5)
  3.60 V to 4.70 V (in 50 mV steps)
  Accuracy : ±25 mV (+25°C)
  Accuracy : ±30 mV (–5°C to +55°C)
  Overcharge hysteresis voltage n (n = 1 to 5)
  0.0 mV to –550 mV (in 50 mV steps)
  –300 mV to –500 mV Accuracy : ±20%
  –100 mV to –250 mV Accuracy : ±50 mV
  0.0 mV to –50 mV Accuracy : ±25 mV
- Delay times for overcharge detection can be set by an internal circuit only (external capacitors are unnecessary)
- Output form is selectable: CMOS output, Nch open-drain output, Pch open-drain output
- Output logic is selectable: Active “H”, Active “L”
- High withstand voltage devices Absolute maximum rating : 28 V
- Wide operating voltage range 3.6 V to 26 V
- Wide operating temperature range –40°C to +85°C
- Low current consumption
  At V_{CUn} – 1.0 V for each cell 3.0 μA max. (+25°C)
  At 2.3 V for each cell 1.7 μA max. (+25°C)
- Lead-free (Sn 100%), halogen-free*1

***1.** Refer to “■ **Product Name Structure**” for details.

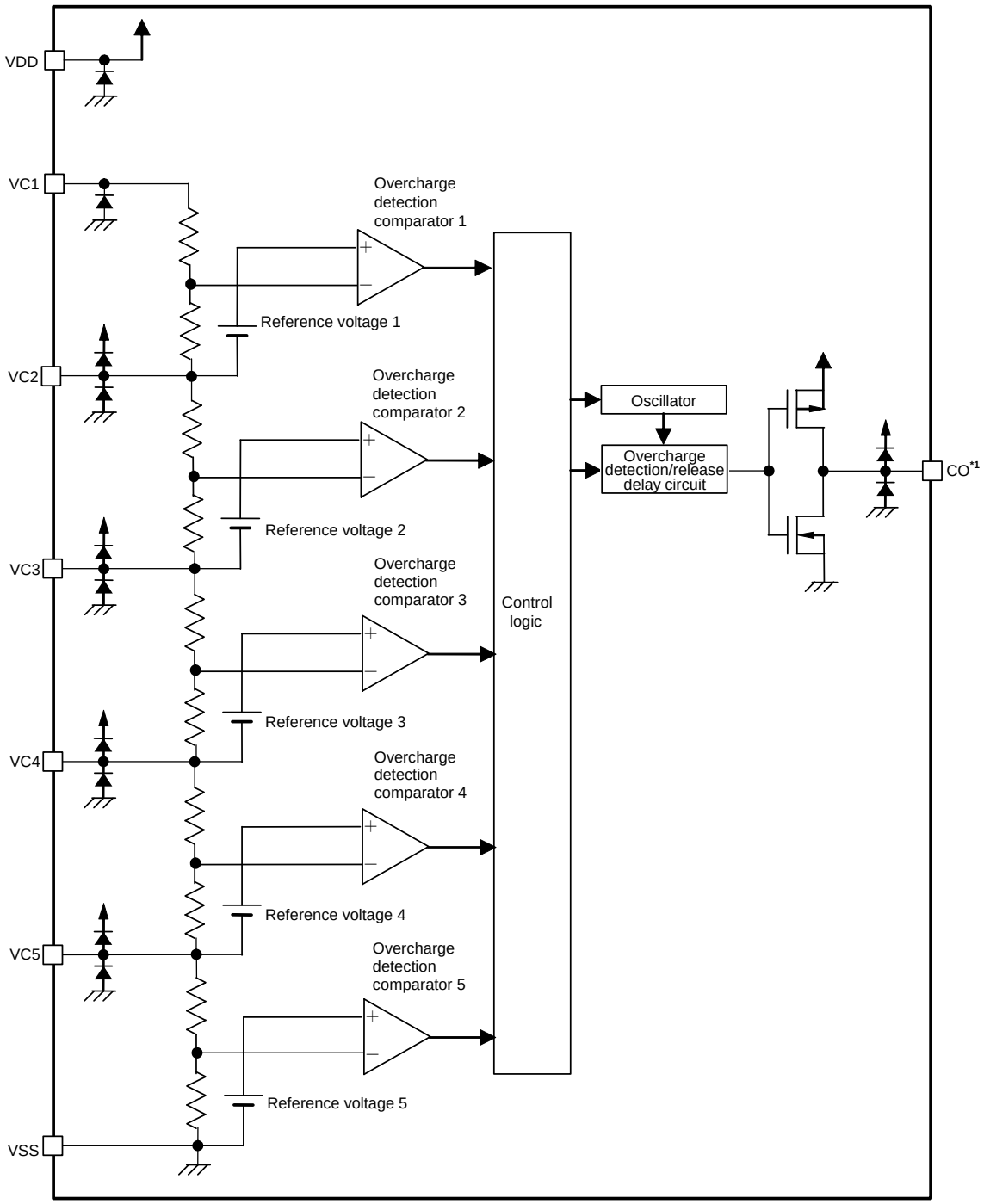
■ Application

- Lithium-ion rechargeable battery packs (for secondary protection)

■ Packages

- SNT-8A
- TMSOP-8

■ Block Diagram



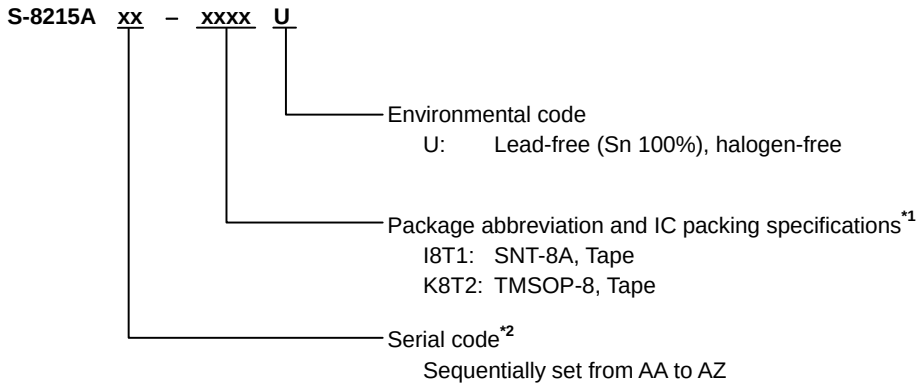
***1.** Only Nch transistor is connected to the CO pin in the case of Nch open- drain output.
Only Pch transistor is connected to the CO pin in the case of Pch open-drain output.

Remark The diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product Name



***1.** Refer to the tape specifications at the end of this book.
***2.** Refer to "**3. Product Name List**".

2. Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	—

3. Product Name List

Table 1 SNT-8A

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time [t_{CU}]	Output Form
S-8215AAA-I8T1U	4.300 V	−0.3 V	4.0 s	CMOS output active "H"

Remark Please contact our sales department for the products with detection voltage value other than those specified above.

Table 2 TMSOP-8

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time [t_{CU}]	Output Form
S-8215AAA-K8T2U	4.300 V	−0.3 V	4.0 s	CMOS output active "H"
S-8215AAB-K8T2U	4.275 V	−0.05 V	2.0 s	Nch open-drain output active "L"
S-8215AAC-K8T2U	4.150 V	−0.25 V	1.0 s	CMOS output active "H"
S-8215AAD-K8T2U	4.350 V	−0.25 V	2.0 s	CMOS output active "H"
S-8215AAE-K8T2U	4.325 V	−0.05 V	1.0 s	Nch open-drain output active "L"

Remark Please contact our sales department for the products with detection voltage value other than those specified above.

■ Pin Configurations

SNT-8A
Top view

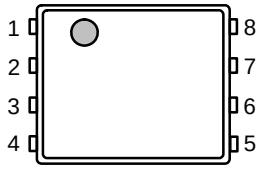


Figure 2

Table 3

Pin No.	Symbol	Description
1	VDD	Positive power input pin
2	VC1	Positive voltage connection pin of battery 1
3	VC2	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC3	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC4	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	VC5	Negative voltage connection pin of battery 4 Positive voltage connection pin of battery 5
7	VSS	Negative power input pin Negative voltage connection pin of battery 5
8	CO	FET gate connection pin for charge

TMSOP-8
Top view

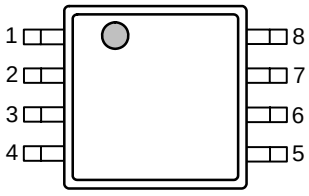


Figure 3

Table 4

Pin No.	Symbol	Description
1	VDD	Positive power input pin
2	VC1	Positive voltage connection pin of battery 1
3	VC2	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC3	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC4	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	VC5	Negative voltage connection pin of battery 4 Positive voltage connection pin of battery 5
7	VSS	Negative power input pin Negative voltage connection pin of battery 5
8	CO	FET gate connection pin for charge

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item		Symbol	Applied Pins	Rating	Unit
Input voltage between VDD and VSS		V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 28	V
Input pin voltage		V_{IN}	VC1, VC2, VC3, VC4, VC5	V_{SS} − 0.3 to V_{DD} + 0.3	V
CO output pin voltage	CMOS output	V_{CO}	CO	V_{SS} − 0.3 to V_{DD} + 0.3	V
	Nch open-drain output			V_{SS} − 0.3 to V_{SS} + 28	V
	Pch open-drain output			V_{DD} − 28 to V_{DD} + 0.3	V
Power dissipation	SNT-8A	P_D	—	450[*1]	mW
	TMSOP-8			650[*1]	mW
Operation ambient temperature		T_{opr}	—	−40 to +85	°C
Storage temperature		T_{stg}	—	−40 to +125	°C

***1.** When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

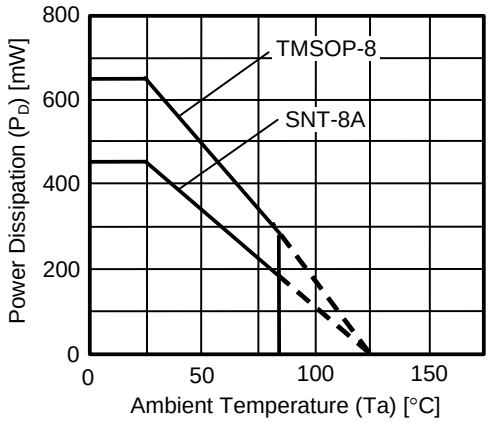


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
DETECTION VOLTAGE							
Overcharge detection voltage n (n = 1, 2, 3, 4, 5)	V_{CUn}	—	V_{CU} − 0.025	V_{CU}	V_{CU} + 0.025	V	1
		Ta = −5°C to +55°C*1	V_{CU} − 0.030	V_{CU}	V_{CU} + 0.030	V	1
Overcharge hysteresis voltage n (n = 1, 2, 3, 4, 5)	V_{HCn}	−550 mV ≤ V_{HC} ≤ −300 mV	V_{HC} × 0.8	V_{HC}	V_{HC} × 1.2	V	1
		−250 mV ≤ V_{HC} ≤ −100 mV	V_{HC} − 0.050	V_{HC}	V_{HC} + 0.050	V	1
		V_{HC} = −50 mV, 0 mV	V_{HC} − 0.025	V_{HC}	V_{HC} + 0.025	V	1
INPUT VOLTAGE							
Operating voltage between VDD and VSS	V_{DSOP}	—	3.6	—	26	V	—
INPUT CURRENT							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = V5 = V_{CU} − 1.0 V	—	1.6	3.0	μA	3
Current consumption during overdischarge	I_{OPED}	V1 = V2 = V3 = V4 = V5 = 2.3 V	—	0.8	1.7	μA	3
VC1 pin current	I_{VC1}	V1 = V2 = V3 = V4 = V5 = V_{CU} − 1.0 V	—	0.2	0.4	μA	4
VCn pin current (n = 2, 3, 4, 5)	I_{VCn}	V1 = V2 = V3 = V4 = V5 = V_{CU} − 1.0 V	−0.3	0	0.3	μA	4
OUTPUT CURRENT (CMOS output)							
CO pin sink current	I_{COL}	—	0.4	—	—	mA	5
CO pin source current	I_{COH}	—	20	—	—	μA	5
OUTPUT CURRENT (Nch open-drain output)							
CO pin sink current	I_{COL}	—	0.4	—	—	mA	5
CO pin leakage current “L”	I_{COLL}	—	—	—	0.1	μA	5
OUTPUT CURRENT (Pch open-drain output)							
CO pin source current	I_{COH}	—	20	—	—	μA	5
CO pin leakage current “H”	I_{COLH}	—	—	—	0.1	μA	5
DELAY TIME							
Overcharge detection delay time	t_{CU}	—	t_{CU} × 0.8	t_{CU}	t_{CU} × 1.2	s	1
Overcharge timer reset delay time	t_{TR}	—	6	12	20	ms	1
Transition time to test mode	t_{TST}	—	—	—	80	ms	2

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

1. Overcharge Detection Voltage, Overcharge Hysteresis Voltage (Test Circuit 1)

1. 1 Overcharge Detection Voltage n (V_{CUn})

Set V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.05 V. The Overcharge detection voltage 1 (V_{CU1}) is the V1 voltage when the CO pin's output changes after the voltage of V1 has been gradually increased.
Overcharge detection voltage V_{CUn} (n = 2 to 5) can be determined in the same way as when n = 1.

1. 2 Overcharge Hysteresis Voltage n (V_{HCn})

Set V1 = V_{CU} + 0.05 V, V2 = V3 = V4 = V5 = 2.5 V. The overcharge hysteresis voltage 1 (V_{HC1}) is the difference between V1 voltage and V_{CU1} when the CO pin's output changes after the V1 voltage has been gradually decreased.
Overcharge hysteresis voltage V_{HCn} (n = 2 to 5) can be determined in the same way as when n = 1.

2. Output Current (Test Circuit 5)

2. 1 CMOS Output Current

Set SW1 and SW2 to OFF.

2. 1. 1 Active "H"

(1) CO pin source current (I_{COH})

Set SW1 to ON after setting V1 = 5.5 V, V2 to V5 = 3.0 V, V6 = 0.5 V. I1 is the CO pin source current (I_{COH}) at that time.

(2) CO pin sink current (I_{COL})

Set SW2 to ON after setting V1 to V5 = 3.5 V, V7 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

2. 1. 2 Active "L"

(1) CO pin source current (I_{COH})

Set SW1 to ON after setting V1 to V5 = 3.5 V, V6 = 0.5 V. I1 is the CO pin source current (I_{COH}) at that time.

(2) CO pin sink current (I_{COL})

Set SW2 to ON after setting V1 = 5.5 V, V2 to V5 = 3.0 V, V7 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

2. 2 Nch Open Drain Output Current

Set SW1 and SW2 to OFF.

2. 2. 1 Active "H"

(1) CO pin leakage current "L" (I_{COLL})

Set SW2 to ON after setting V1 = 5.5 V, V2 to V5 = 3.0 V, V7 = 17.5 V. I2 is the CO pin leakage current "L" (I_{COLL}) at that time.

(2) CO pin sink current (I_{COL})

Set V1 to V5 = 3.5 V, V7 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

2. 2. 2 Active "L"

(1) CO pin leakage current "L" (I_{COLL})

Set SW2 to ON after setting V1 to V5 = 3.5 V, V7 = 17.5 V. I2 is the CO pin leakage current "L" (I_{COLL}) at that time.

(2) CO pin sink current (I_{COL})

Set V1 = 5.5 V, V2 to V5 = 3.0 V, V7 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

2. 3 Pch Open Drain Output Current

Set SW1 and SW2 to OFF.

2. 3. 1 Active "H"

(1) CO pin source current (I_{COH})

Set SW1 to ON after setting V1 = 5.5 V, V2 to V5 = 3.0 V, V6 = 0.5 V. I1 is the CO pin source current (I_{COH}) at that time.

(2) CO pin leakage current "H" (I_{COLH})

Set V1 to V5 = 3.5 V, V6 = 17.5 V. I1 is the CO pin leakage current "H" (I_{COLH}) at that time.

2. 3. 2 Active "L"

(1) CO pin source current (I_{COH})

Set SW1 to ON after setting V1 to V5 = 3.5 V, V6 = 0.5 V. I1 is the CO pin source current (I_{COH}) at that time.

(2) CO pin leakage current "H" (I_{COLH})

Set V1 = 5.5 V, V2 to V5 = 3.0 V, V6 = 17.5 V. I1 is the CO pin leakage current "H" (I_{COLH}) at that time.

3. Overcharge Detection Delay Time (t_{CU}) (Test Circuit 1)

Increase V1 up to 5.0 V after setting V1 = V2 = V3 = V4 = V5 = 3.5 V. The overcharge detection delay time (t_{CU}) is the time period until the CO pin output changes.

4. Overcharge Timer Reset Delay Time (t_{TR}) (Test Circuit 1)

Increase V1 up to 5.0 V (first rise), and decrease V1 down to 3.5 V within the overcharge detection delay time (t_{CU}) after setting V1 = V2 = V3 = V4 = V5 = 3.5 V. After that, increase V1 up to 5.0 V again (second rise), and detect the time period till the CO pin output changes.

When the period from when V1 has fallen to the second rise is short, CO pin output changes after t_{CU} has elapsed since the first rise. If the period is gradually made longer, CO pin output changes after t_{CU} has elapsed since the second rise. The overcharge timer reset delay time (t_{TR}) is the period from V1 fall till the second rise at that time.

5. Transition Time to Test Mode (t_{TST}) (Test circuit 2)

Increase V6 up to 4.0 V, and decrease V6 again to 0 V after setting V1 = V2 = V3 = V4 = V5 = 3.5 V, and V6 = 0 V.

When the period from when V6 was raised to when it has fallen is short, if an overcharge detection operation is performed subsequently, the delay time is t_{CU}. However, when the period from when V6 is raised to when it has fallen is gradually made longer, the delay time during the subsequent overcharge detection operation is shorter than t_{CU}. The transition time to test mode (t_{TST}) is the period from when V6 was raised to when it has fallen at that time.

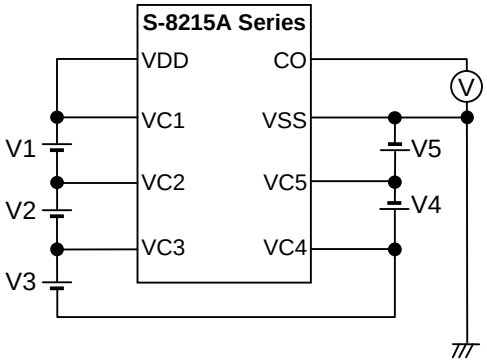


Figure 5 Test Circuit 1

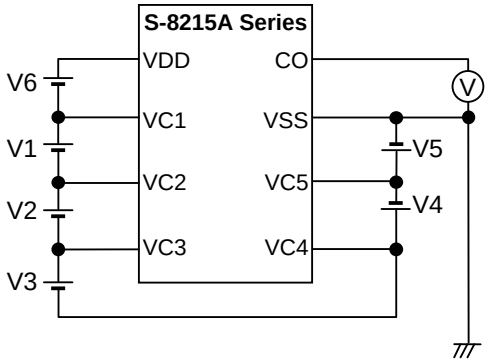


Figure 6 Test Circuit 2

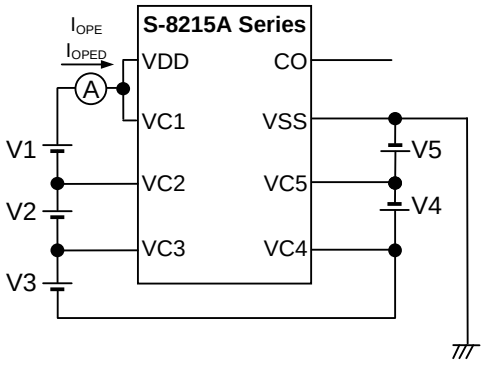


Figure 7 Test Circuit 3

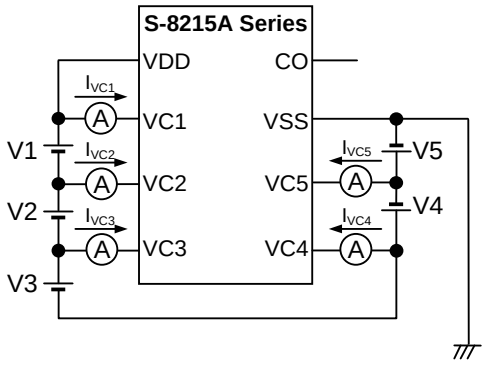


Figure 8 Test Circuit 4

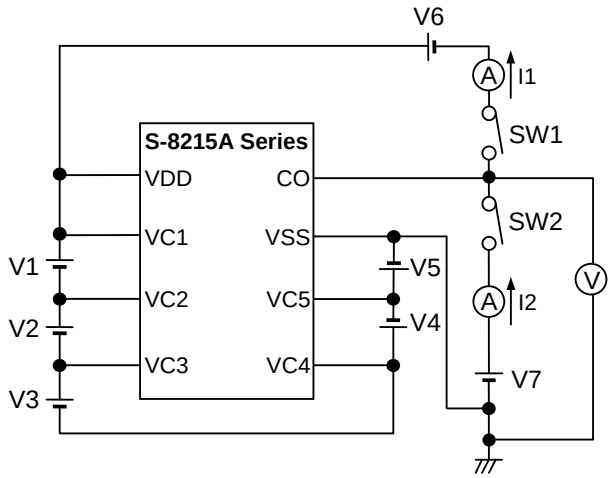


Figure 9 Test Circuit 5

■ Operation

Remark Refer to **"■ Battery Protection IC Connection Example".**

1. Normal status

If the voltage of all the batteries is lower than "the overcharge detection voltage (V_{CUn}) + the overcharge hysteresis voltage (V_{HCn})",CO pin output changes to "L" (Active "H") or "H"(Active L"). This is called normal status.

2. Overcharge status

When the voltage of one of the batteries exceeds V_{CUn} during charging under normal conditions and the status is retained for the overcharge detection delay time (t_{CU}) or longer, CO pin output changes. This status is called overcharge. Connecting FET to the CO pin provides charge control and a second protection.

If the voltage of all the batteries is lower than $V_{CUn} + V_{HCn}$ and the status is retained for typ. 2.0 ms or longer, S-8215A Series changes to normal status.

3. Overcharge Timer Reset

When an overcharge release noise that forces the voltage of the battery temporarily below V_{CUn} is input during t_{CU} from when V_{CUn} is exceeded to when charging is stopped, t_{CU} is continuously counted if the time the overcharge release noise persists is shorter than the overcharge timer reset delay time (t_{TR}). Under the same conditions, if the time the overcharge release noise persists is t_{TR} or longer, counting of t_{CU} is reset once. After that, when V_{CUn} has been exceeded, counting t_{CU} resumes.

4. Test Mode

The overcharge detection delay time (t_{CU}) can be shortened by entering the test mode.

The test mode can be set by retaining the VDD pin voltage 4.0 V or more higher than the VC1 pin voltage for the transition time to test mode (t_{TST}) or longer. The status is retained by the internal latch and the test mode is retained even if the VDD pin voltage is decreased to the same voltage as that of the VC1 pin voltage.

After that, the latch for retaining the test mode is reset and the S-8215A Series exits from test mode under the overcharge state.

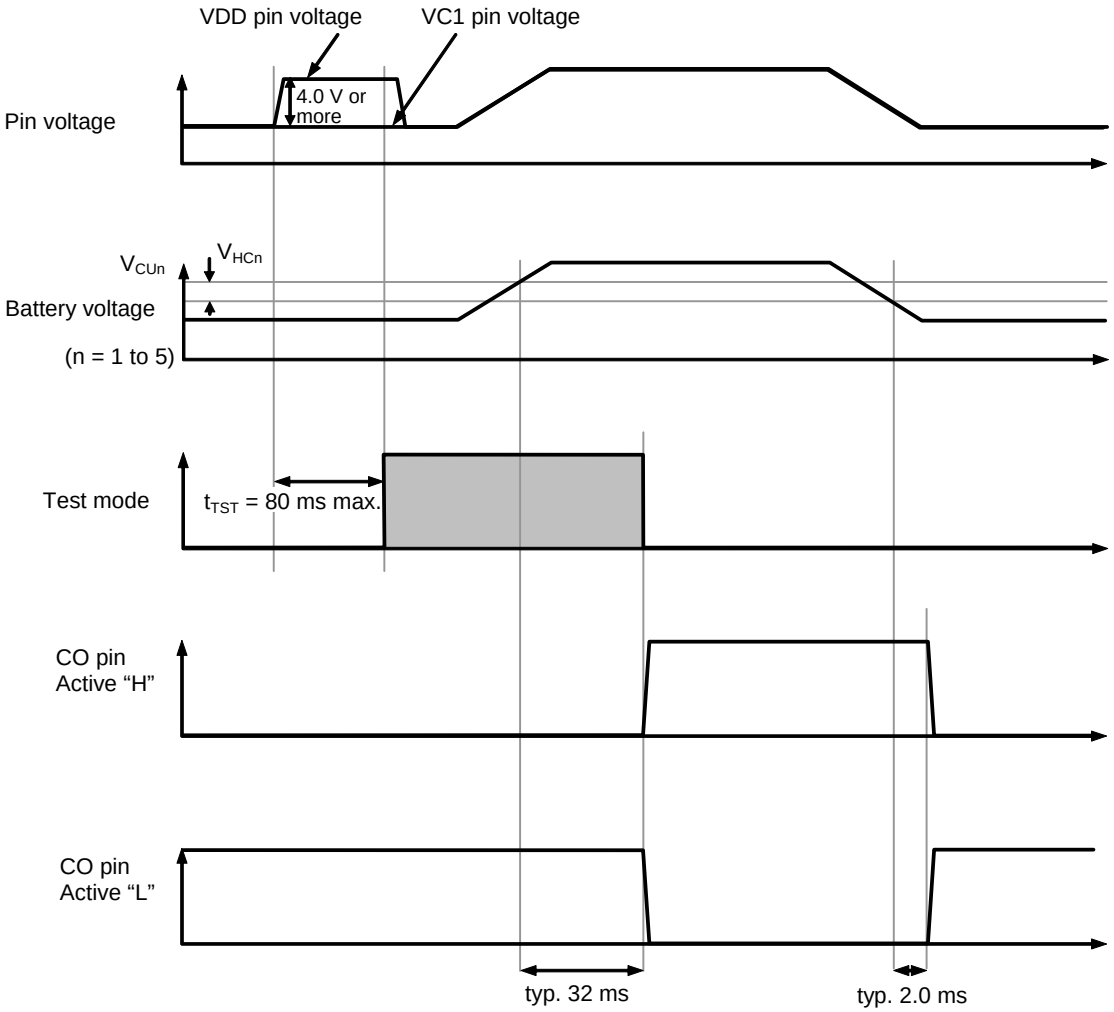


Figure 10

Caution
1. **When the VDD pin voltage is decreased to lower than the UVLO voltage of 2 V (Typ.), the S-8215A Series exits from test mode.**
2. **Set the test mode when no batteries are overcharged.**
3. **The overcharge timer reset delay time (t_{TR}) is not shortened in the test mode.**

■ Timing Charts

1. Overcharge Detection Operation

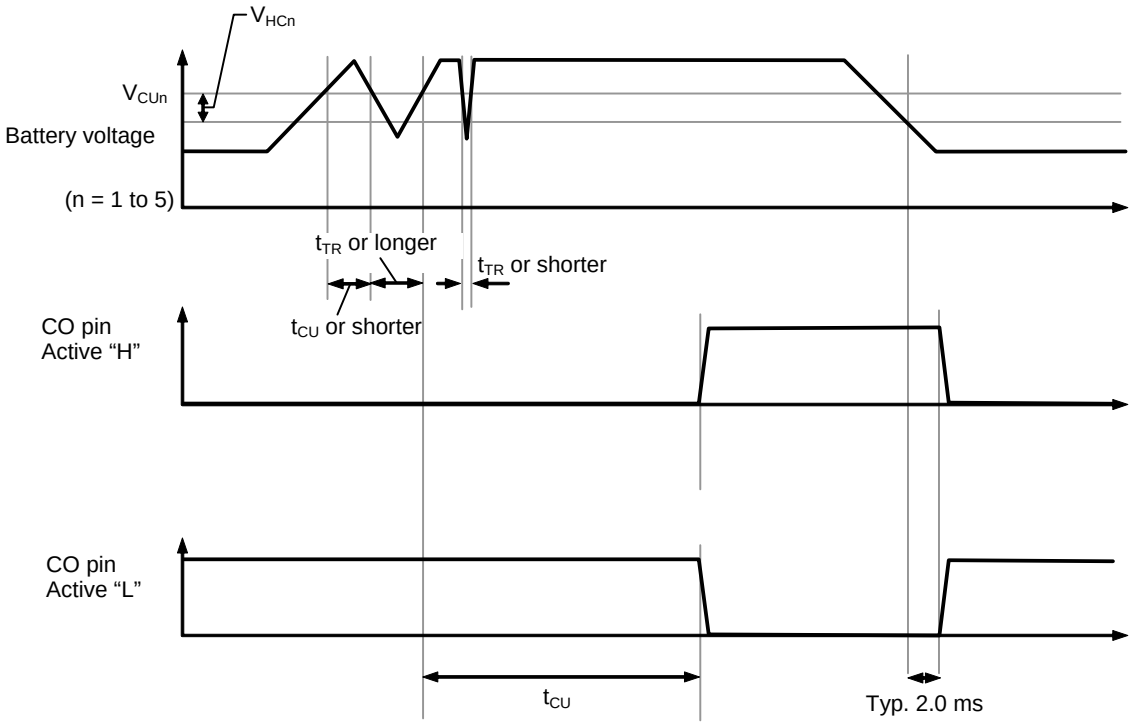


Figure 11

2. Overcharge Timer Reset Operation

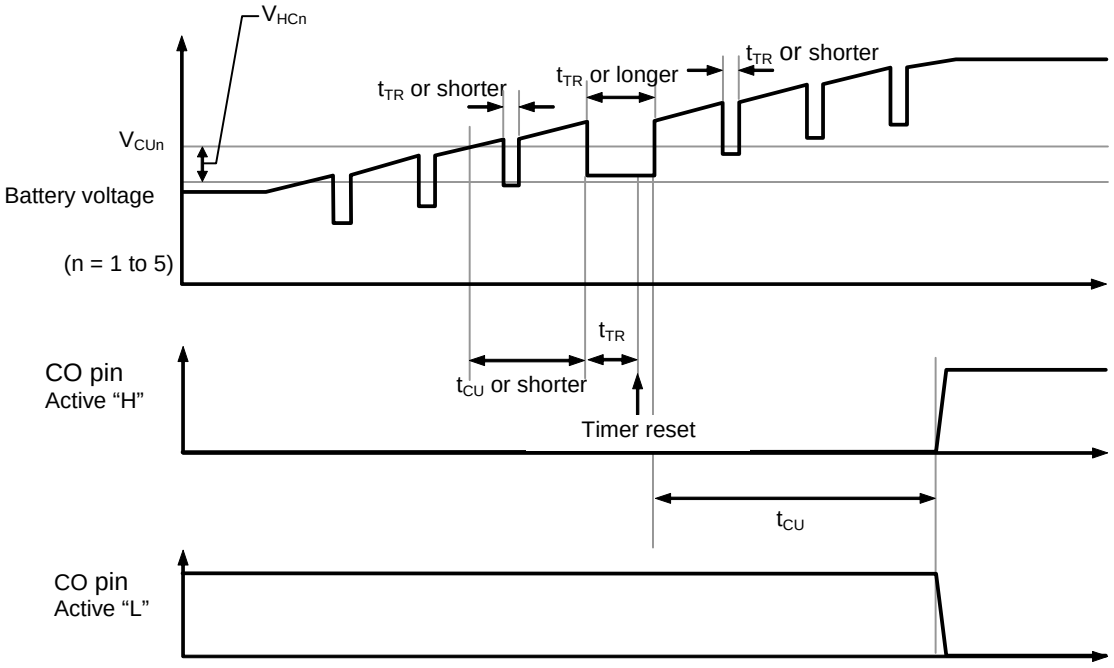


Figure 12

■ Battery Protection IC Connection Examples

1. 5-serial cell

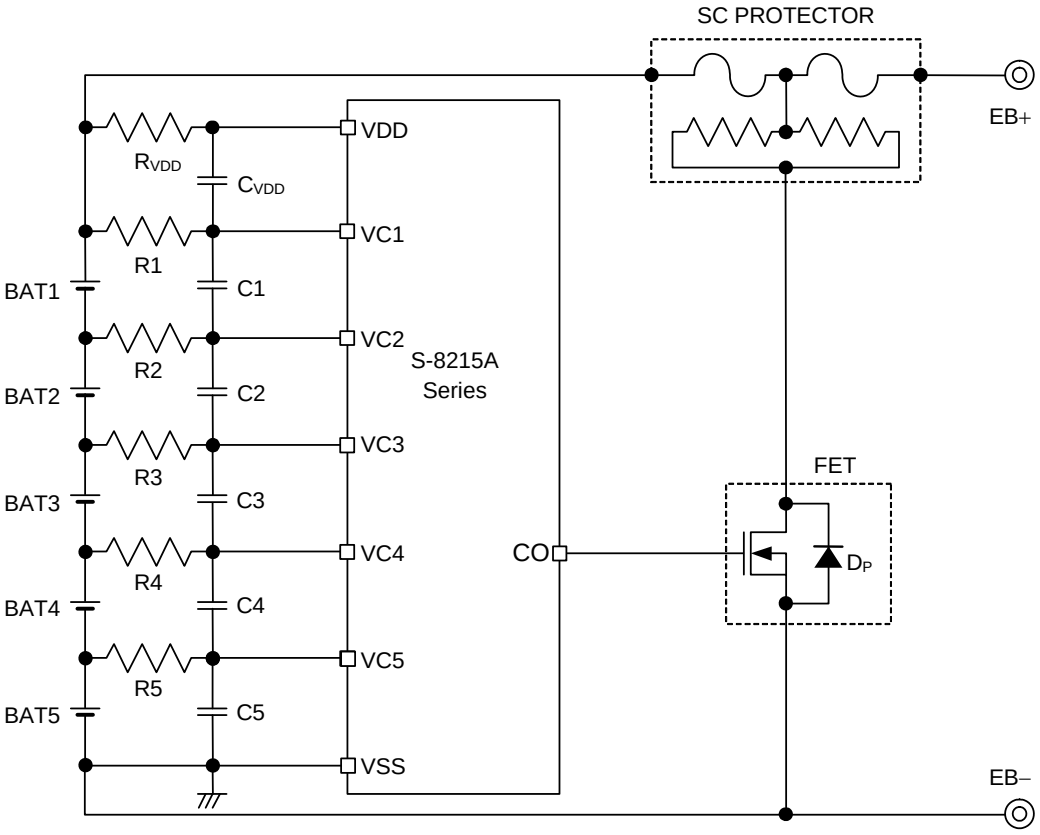


Figure 13

Table 7 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R5	0.5	1	10	kΩ
2	C1 to C5, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	50	100	500	Ω

Caution
1. **The above constants are subject to change without prior notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
3. **Set the same constants to R1 to R5 and to C1 to C5 and C_{VDD}.**
4. **Set R_{VDD}, C1 to C5, and C_{VDD} so that the condition (R_{VDD}) × (C1 to C5, C_{VDD}) ≥ 5×10^{-6} is satisfied.**
5. **Set R1 to R5, C1 to C5, and C_{VDD} so that the condition (R1 to R5) × (C1 to C5, C_{VDD}) ≥ 1×10^{-4} is satisfied.**
6. **Since CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.**

2. 4-serial cell

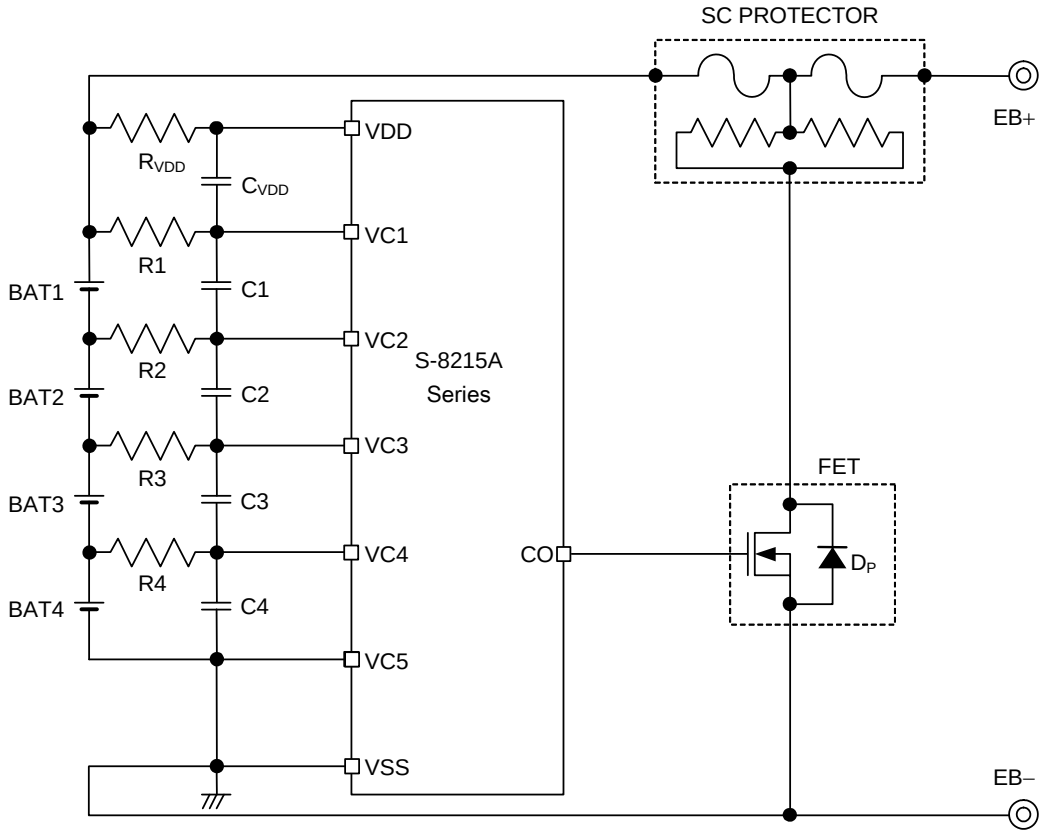


Figure 14

Table 8 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R4	0.5	1	10	kΩ
2	C1 to C4, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	50	100	500	Ω

Caution
1. **The above constants are subject to change without prior notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
3. **Set the same constants to R1 to R4 and to C1 to C4 and C_{VDD}.**
4. **Set R_{VDD}, C1 to C4, and C_{VDD} so that the condition (R_{VDD}) × (C1 to C4, C_{VDD}) ≥ 5×10^{-6} is satisfied.**
5. **Set R1 to R4, C1 to C4, and C_{VDD} so that the condition (R1 to R4) × (C1 to C4, C_{VDD}) ≥ 1×10^{-4} is satisfied.**
6. **Since CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.**

[For SC PROTECTOR, contact]

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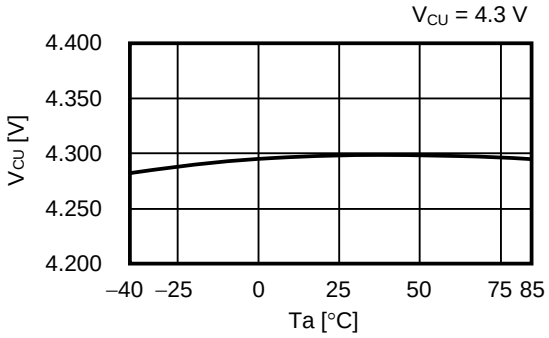
■ Precaution

- Do not connect batteries charged with $V_{CUn} + V_{HCn}$ or higher. If the connected batteries include a battery charged with $V_{CUn} + V_{HCn}$ or more, the S-8215A series may become overcharge status after all pins are connected.
- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
- Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figure in "■ **Battery Protection IC Connection Examples**".
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

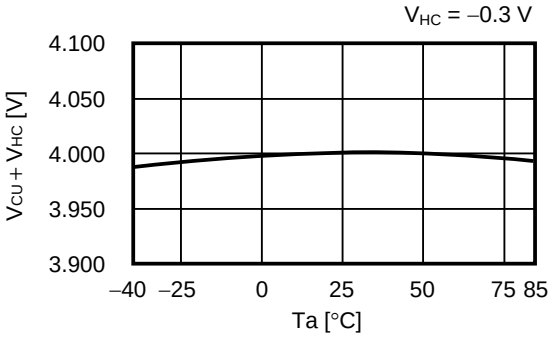
■ Characteristics (Typical Data)

1. Detection Voltage

1. 1 V_{CU} vs. Ta

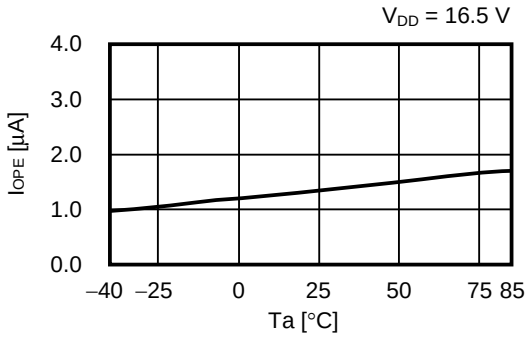


1. 2 $V_{CU} + V_{HC}$ vs. Ta

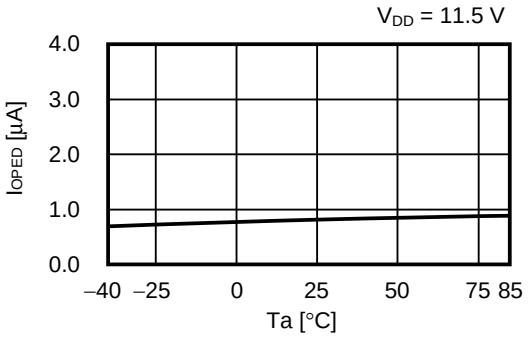


2. Current Consumption

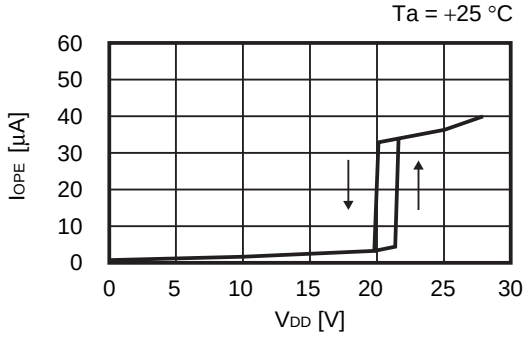
2. 1 I_{OPE} vs. Ta



2. 2 I_{OPED} vs. Ta

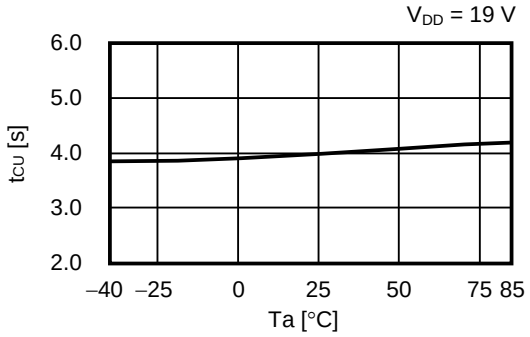


2. 3 I_{OPE} vs. V_{DD}



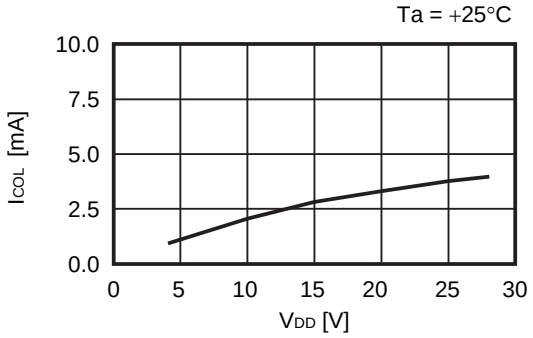
3. Delay Time

3. 1 t_{CU} vs. Ta

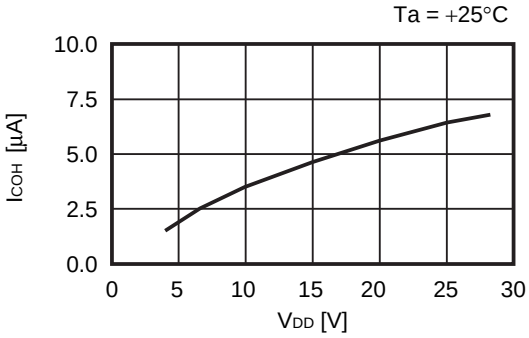


4. Output Current

4. 1 I_{COL} vs. V_{DD}



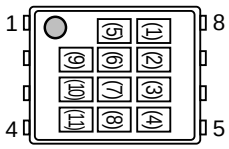
4. 2 I_{COH} vs. V_{DD}



■ Marking Specifications

1. SNT-8A

SNT-8A
Top view



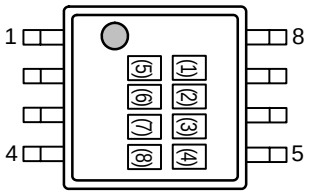
(1)	Blank
(2) to (4)	Product code (Refer to **Product name vs. Product code**)
(5), (6)	Blank
(7) to (11)	Lot number

Product name vs. Product code

Product name	Product code		
	(2)	(3)	(4)
S-8215AAA-I8T1U	V	6	A

2. TMSOP-8

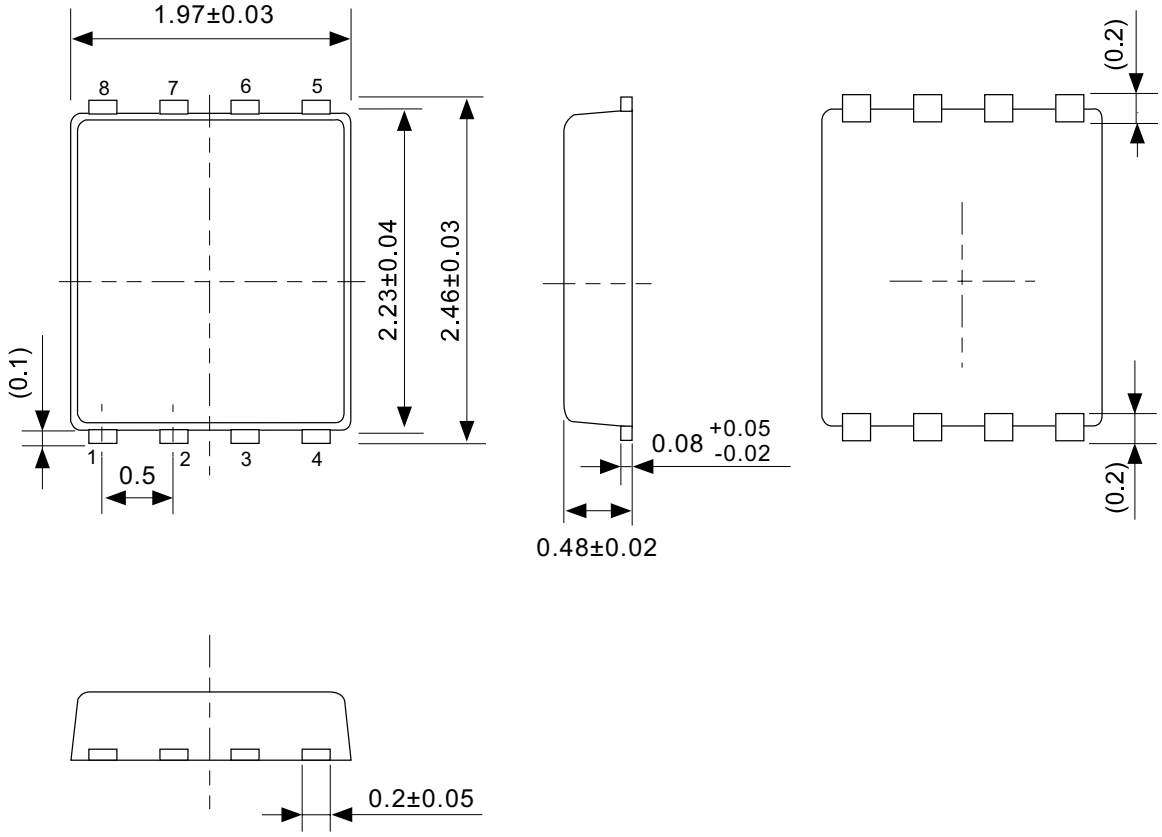
TMSOP-8
Top view



(1)	Blank
(2) to (4)	Product code (Refer to **Product name vs. Product code**)
(5)	Blank
(6) to (8)	Lot number

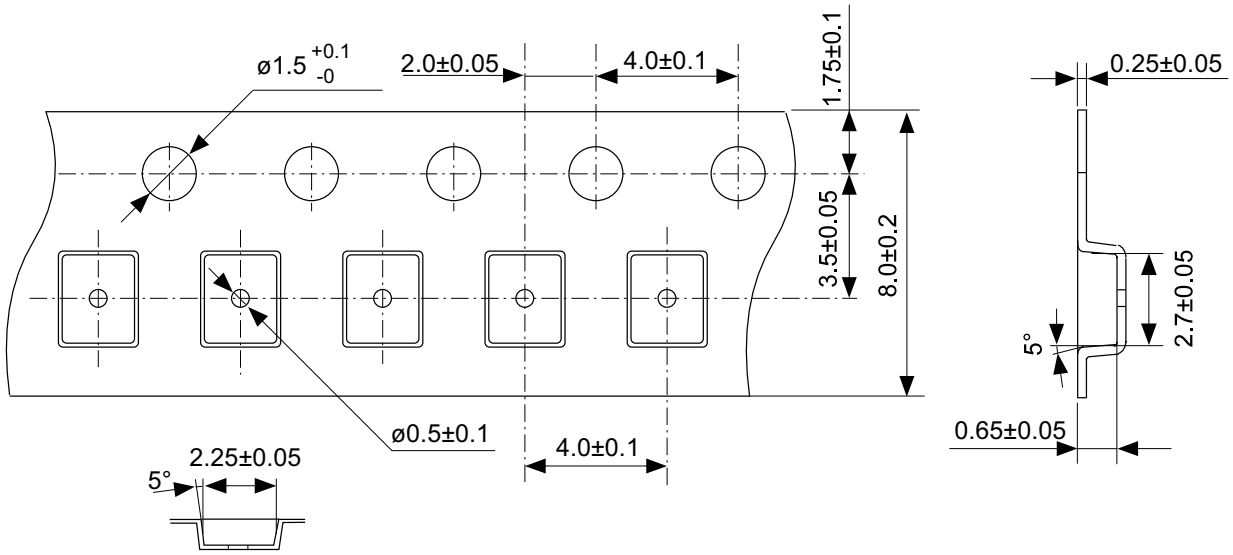
Product name vs. Product code

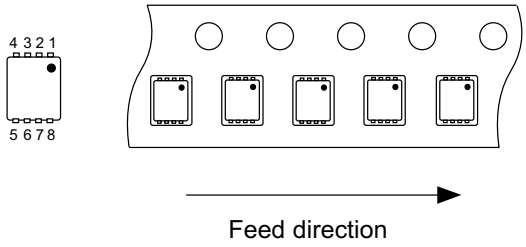
Product name	Product code		
	(2)	(3)	(4)
S-8215AAA-K8T2U	V	6	A
S-8215AAB-K8T2U	V	6	B
S-8215AAC-K8T2U	V	6	C
S-8215AAD-K8T2U	V	6	D
S-8215AAE-K8T2U	V	6	E



No. PH008-A-P-SD-2.0

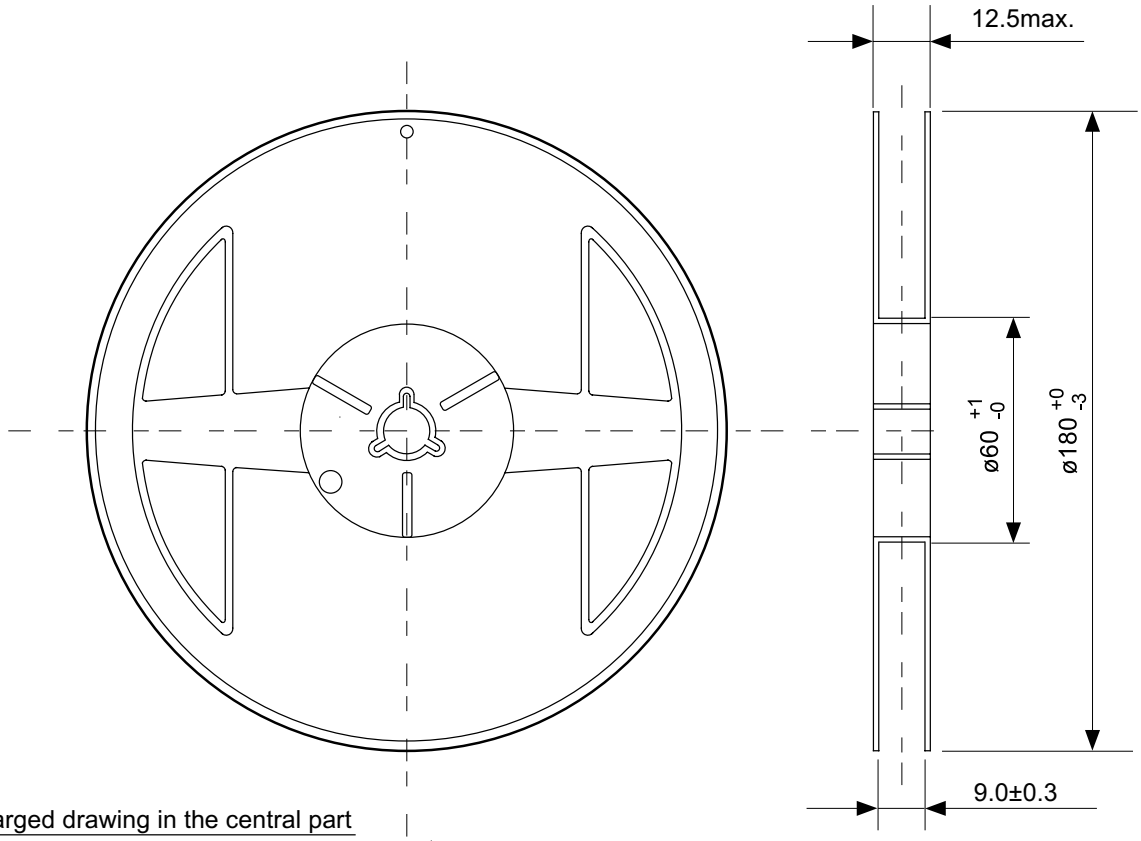
TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



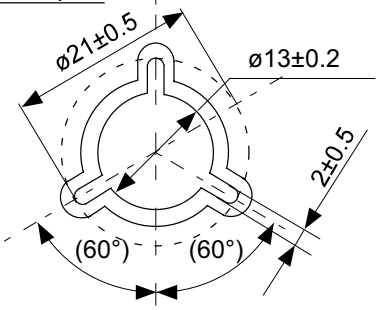


No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

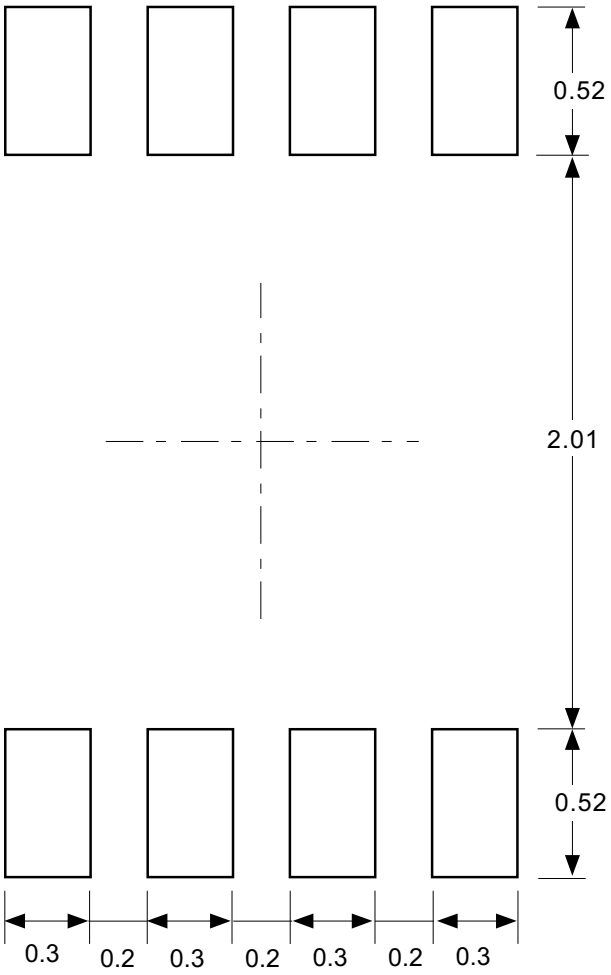


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
Seiko Instruments Inc.			

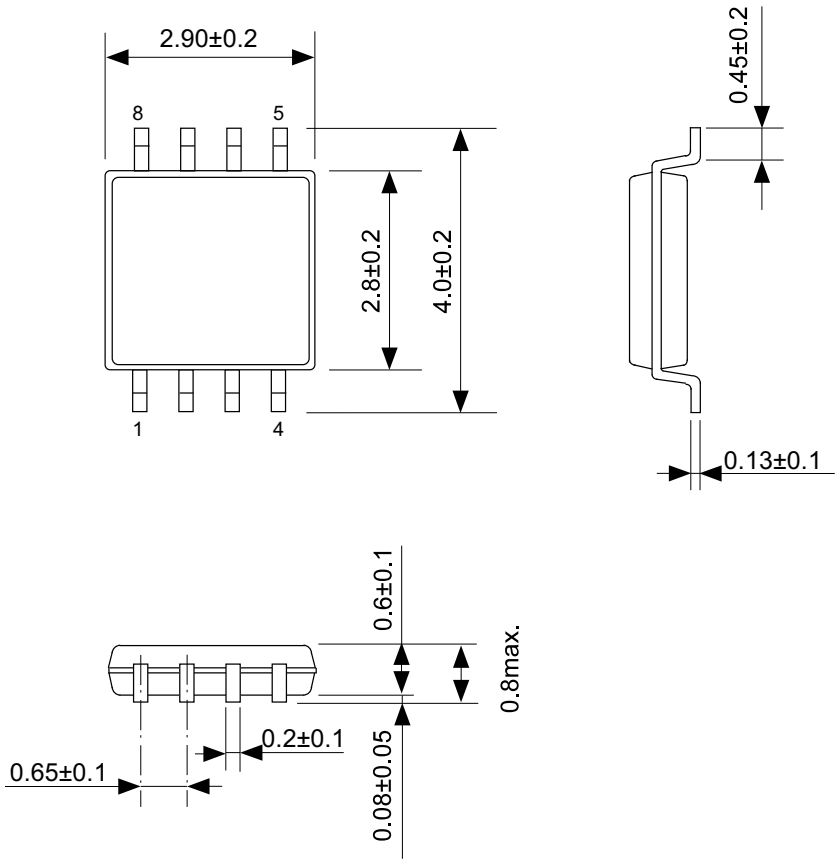


Caution Making the wire pattern under the package is possible. However, note that the package may be upraised due to the thickness made by the silk screen printing and of a solder resist on the pattern because this package does not have the standoff.

注意 パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフが無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージが持ち上がることがありますのでご配慮ください。

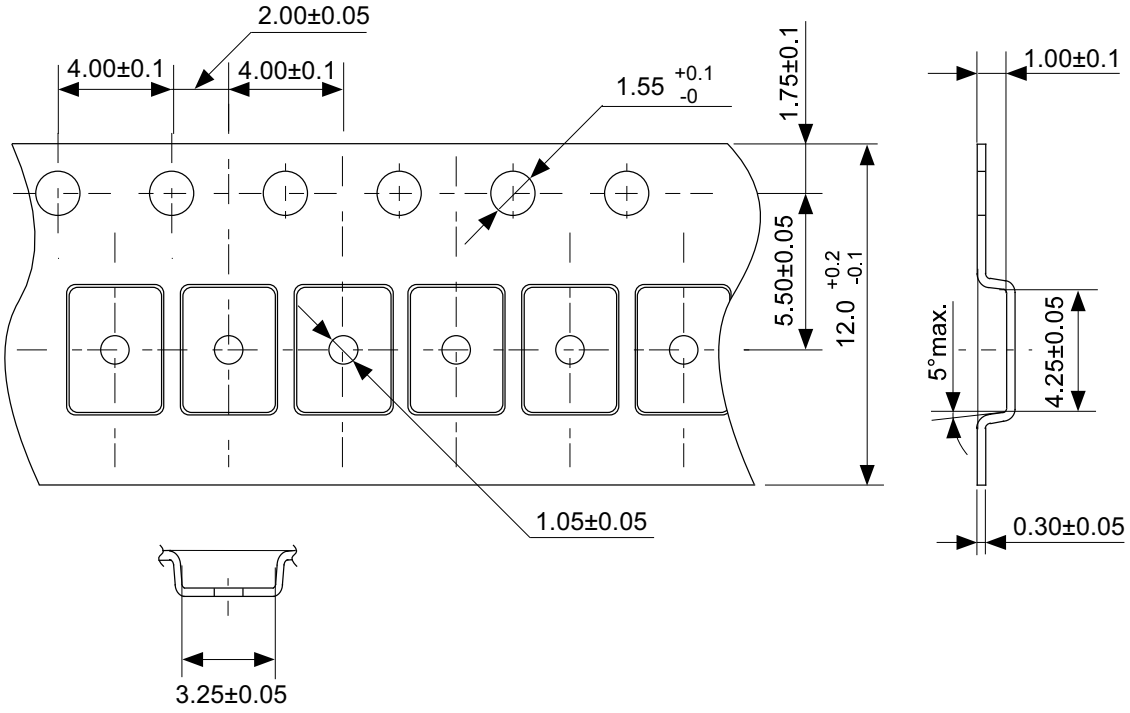
No. PH008-A-L-SD-3.0

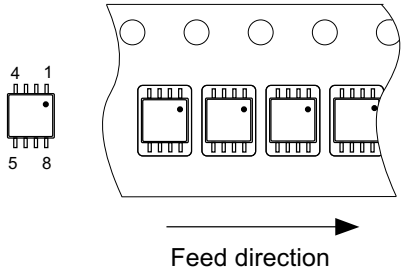
TITLE	SNT-8A-A-Land Recommendation
No.	PH008-A-L-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



No. FM008-A-P-SD-1.0

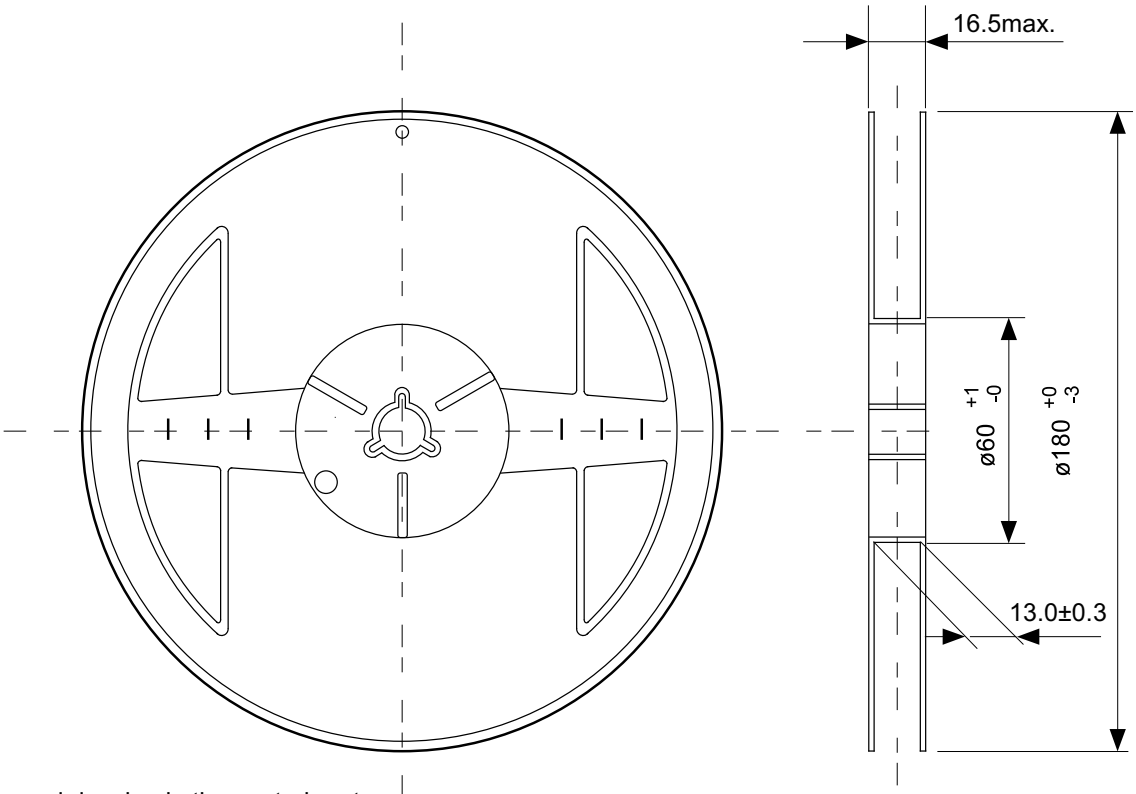
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



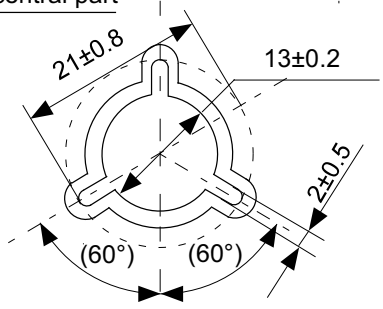


No. FM008-A-C-SD-1.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
SCALE		QTY.	4,000
UNIT	mm		
Seiko Instruments Inc.			

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