BATTERY PROTECTION IC FOR 2-SERIAL-CELL PACK

S-8242B Series

The S-8242B Series are protection ICs for 2-serial-cell lithium-ion/lithium polymer rechargeable batteries and include high-accuracy voltage detectors and delay circuits. These ICs are suitable for protecting 2-cell rechargeable lithium-ion / lithium polymer battery packs from overcharge, overdischarge, and overcurrent.

■ Features

(1) High-accuracy voltage detection for each cell

• Overcharge detection voltage n (n = 1, 2)	3.9 V to 4.5 V (50 mV steps)	Accuracy ±25 mV
• Overcharge release voltage n (n = 1, 2)	3.8 V to 4.5 V*1	Accuracy ±50 mV
• Overdischarge detection voltage n (n = 1, 2)	2.0 V to 3.0 V (100 mV steps)	Accuracy ±50 mV
• Overdischarge release voltage n (n = 1, 2)	2.0 V to 3.4 V*2	Accuracy ±100 mV

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage n (n = 1, 2) can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV steps.)

***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage n (n = 1, 2) can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV steps.)

(2) Two-level overcurrent detection (overcurrent 1, overcurrent 2)

• Overcurrent detection voltage 1	0.05 V, 0.08 V to 0.30 V (10 mV steps)	Accuracy ±15 mV
• Overcurrent detection voltage 2	1.2 V (fixed)	Accuracy ±300 mV

(3) Delay times (overcharge, overdischarge, overcurrent) are generated by an internal circuit (external capacitors are unnecessary).

(4) 0 V battery charge function available/unavailable are selectable.

(5) Charger detection function
- The overdischarge hysteresis is released by detecting negative voltage at the VM pin (–0.7 V typ.) (Charger detection function).

(6) High-withstand voltage devices — Absolute maximum rating: 28 V

(7) Wide operating temperature range — –40°C to +85°C

(8) Low current consumption

Operation mode	10 μA max. (+25°C)
Power-down mode	0.1 μA max. (+25°C)

(9) Small package — SNT-8A, 8-Pin TSSOP

(10) Lead-free product

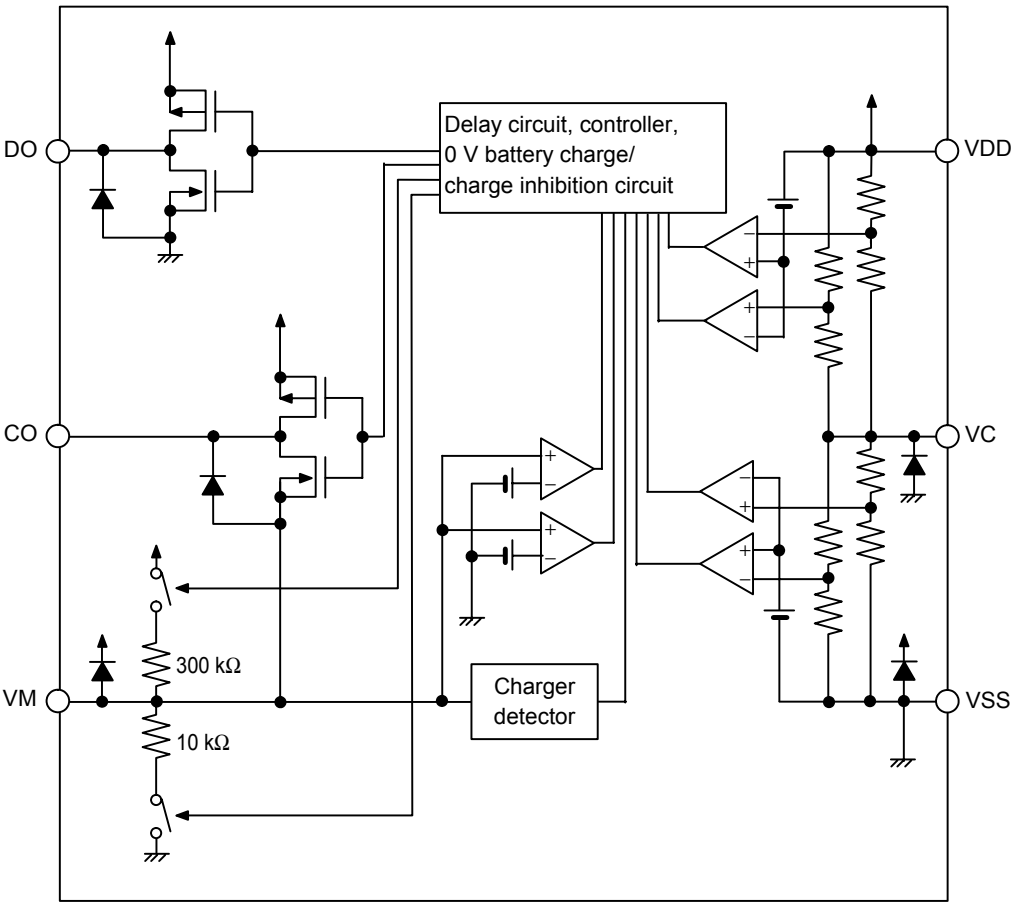
■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

■ Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SNT-8A	PH008-A	PH008-A	PH008-A	PH008-A
8-Pin TSSOP	FT008-A	FT008-E	FT008-E	—

■ Block Diagram

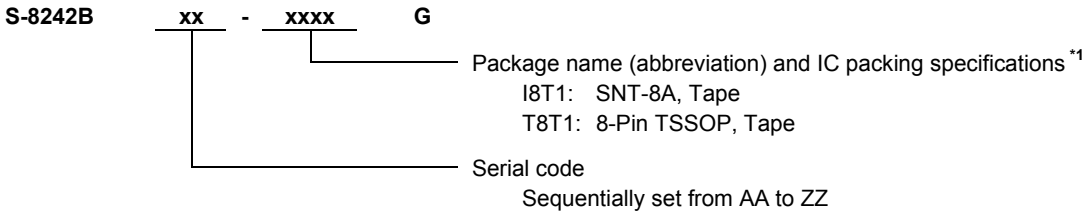


Remark All the diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product Name



***1.** Refer to the tape specifications.

2. Product Name List

(1) SNT-8A Package

Table 1

Product Name / Item	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Overcurrent Detection Voltage 1 [V_{IOV1}]	0 V Battery Charge
S-8242BAB-I8T1G	4.325 V	4.075 V	2.2 V	2.9 V	0.21 V	Unavailable
S-8242BAC-I8T1G	4.350 V	4.150 V	2.3 V	3.0 V	0.30 V	Available
S-8242BAD-I8T1G	4.350 V	4.350 V	2.3 V	2.9 V	0.08 V	Available
S-8242BAE-I8T1G	4.430 V	4.200 V	2.3 V	2.9 V	0.08 V	Available
S-8242BAF-I8T1G	4.300 V	4.100 V	2.0 V	2.0 V	0.20 V	Available
S-8242BAH-I8T1G	4.300 V	4.100 V	2.4 V	3.0 V	0.20 V	Unavailable
S-8242BAI-I8T1G	4.250 V	4.050 V	2.4 V	3.0 V	0.15 V	Available
S-8242BAM-I8T1G	4.300 V	4.100 V	2.6 V	3.0 V	0.28 V	Unavailable
S-8242BAN-I8T1G	4.350 V	4.150 V	2.3 V	2.9 V	0.25 V	Unavailable
S-8242BAO-I8T1G	4.350 V	4.150 V	2.3 V	2.9 V	0.10 V	Available
S-8242BAQ-I8T1G	4.350 V	4.150 V	2.3 V	2.9 V	0.20 V	Unavailable
S-8242BAR-I8T1G	4.300 V	4.100 V	2.6 V	3.0 V	0.21 V	Unavailable
S-8242BAU-I8T1G	4.300 V	4.100 V	2.4 V	3.0 V	0.28 V	Unavailable
S-8242BAV-I8T1G	4.350 V	4.150 V	2.2 V	2.9 V	0.20 V	Unavailable
S-8242BAW-I8T1G	4.350 V	4.150 V	2.2 V	2.9 V	0.25 V	Unavailable
S-8242BAX-I8T1G	4.300 V	4.100 V	2.4 V	3.0 V	0.21 V	Unavailable
S-8242BAY-I8T1G	4.210 V	4.210 V	2.0 V	2.0 V	0.20 V	Unavailable
S-8242BAZ-I8T1G	4.190 V	4.190 V	2.3 V	2.9 V	0.10 V	Available
S-8242BBA-I8T1G	4.350 V	4.150 V	3.0 V	3.4 V	0.25 V	Unavailable
S-8242BBB-I8T1G	4.270 V	4.070 V	2.3 V	2.3 V	0.20 V	Available
S-8242BBC-I8T1G	4.250 V	4.050 V	2.4 V	3.0 V	0.10 V	Available
S-8242BBD-I8T1G	4.310 V	4.110 V	2.0 V	2.0 V	0.20 V	Available
S-8242BBF-I8T1G	4.350 V	4.150 V	2.0 V	2.4 V	0.25 V	Unavailable
S-8242BBI-I8T1G	4.300 V	4.150 V	3.175 V	3.275 V	0.15 V	Unavailable

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

(2) 8-Pin TSSOP Package

Table 2

Product Name / Item	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Overcurrent Detection Voltage 1 [V_{IOV1}]	0 V Battery Charge
S-8242BAC-T8T1G	4.350 V	4.150 V	2.3 V	3.0 V	0.30 V	Available
S-8242BAH-T8T1G	4.300 V	4.100 V	2.4 V	3.0 V	0.20 V	Unavailable
S-8242BAI-T8T1G	4.250 V	4.050 V	2.4 V	3.0 V	0.15 V	Available
S-8242BAP-T8T1G	4.100 V	3.800 V	2.2 V	2.4 V	0.30 V	Unavailable
S-8242BAR-T8T1G	4.300 V	4.100 V	2.6 V	3.0 V	0.21 V	Unavailable
S-8242BAU-T8T1G	4.300 V	4.100 V	2.4 V	3.0 V	0.28 V	Unavailable
S-8242BAV-T8T1G	4.350 V	4.150 V	2.2 V	2.9 V	0.20 V	Unavailable
S-8242BAW-T8T1G	4.350 V	4.150 V	2.2 V	2.9 V	0.25 V	Unavailable
S-8242BAX-T8T1G	4.300 V	4.100 V	2.4 V	3.0 V	0.21 V	Unavailable
S-8242BBE-T8T1G	4.350 V	4.150 V	2.0 V	2.4 V	0.20 V	Unavailable
S-8242BBF-T8T1G	4.350 V	4.150 V	2.0 V	2.4 V	0.25 V	Unavailable
S-8242BBG-T8T1G	4.200 V	4.000 V	2.6 V	3.0 V	0.10 V	Available

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

■ Pin Configurations

SNT-8A
Top view

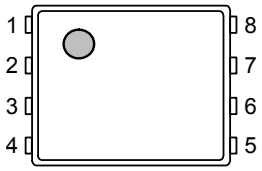


Figure 2

Table 3

Pin No.	Symbol	Description
1	CO	Connection of charge control FET gate (CMOS output)
2	DO	Connection of discharge control FET gate (CMOS output)
3	NC*1	No connection
4	VSS	Connection for negative power supply input and negative voltage of battery 2
5	VC	Connection for negative voltage of battery 1 and positive voltage of battery 2
6	VDD	Connection for positive power supply input and positive voltage of battery 1
7	NC*1	No connection
8	VM	Voltage detection between VM and VSS (overcurrent/charger detection pin)

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

Remark For the external views, refer to the package drawings.

8-Pin TSSOP
Top view

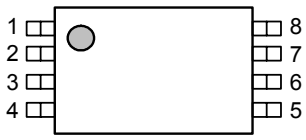


Figure 3

Table 4

Pin No.	Symbol	Description
1	CO	Connection of charge control FET gate (CMOS output)
2	DO	Connection of discharge control FET gate (CMOS output)
3	NC*1	No connection
4	VSS	Connection for negative power supply input and negative voltage of battery 2
5	VC	Connection for negative voltage of battery 1 and positive voltage of battery 2
6	VDD	Connection for positive power supply input and positive voltage of battery 1
7	NC*1	No connection
8	VM	Voltage detection between VM and VSS (overcurrent/charger detection pin)

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

Remark For the external views, refer to the package drawings.

■ Absolute Maximum Ratings

Table 5

(Ta = 25°C unless otherwise specified)

Item		Symbol	Applied pin	Absolute Maximum Ratings	Unit
Input voltage between VDD and VSS		V_{DS}	VDD	V_{SS}–0.3 to V_{SS}+12	V
VC input pin voltage		V_{VC}	VC	V_{SS}–0.3 to V_{DD}+0.3	V
VM pin input voltage		V_{VM}	VM	V_{DD}–28 to V_{DD}+0.3	V
DO pin output voltage		V_{DO}	DO	V_{SS}–0.3 to V_{DD}+0.3	V
CO pin output voltage		V_{CO}	CO	V_{VM}–0.3 to V_{DD}+0.3	V
Power dissipation	SNT-8A	P_D	—	450[*1]	mW
	8-Pin TSSOP			700[*1]	mW
Operating ambient temperature		T_{opr}	—	–40 to +85	°C
Storage temperature		T_{stg}	—	–55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

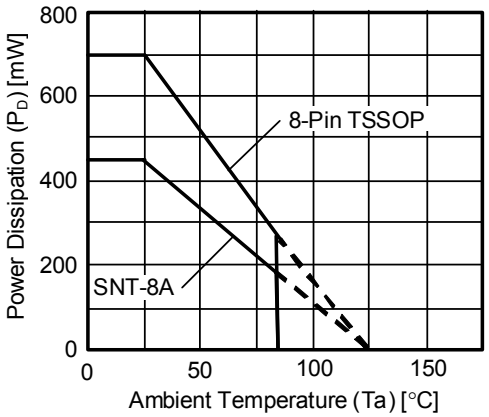


Figure 4 Power Dissipation of Package (When mounted on board)

■ Electrical Characteristics

Table 6

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test condition	Test circuit
[DETECTION VOLTAGE]								
Overcharge detection voltage n	V_{CUn}	3.90 V to 4.50 V, Adjustable	V_{CUn} –0.025	V_{CUn}	V_{CUn} +0.025	V	1	1
Overcharge release voltage n	V_{CLn}	3.80 V to 4.50 V, Adjustable	V_{CLn} –0.05	V_{CLn}	V_{CLn} +0.05	V	1	1
Overdischarge detection voltage n	V_{DLn}	2.0 V to 3.0 V, Adjustable	V_{DLn} –0.05	V_{DLn}	V_{DLn} +0.05	V	2	2
Overdischarge release voltage n	V_{DUn}	2.0 V to 3.40 V, Adjustable	V_{DUn} –0.10	V_{DUn}	V_{DUn} +0.10	V	2	2
Overcurrent detection voltage 1	V_{IOV1}	0.05 V to 0.30 V, Adjustable	V_{IOV1} –0.015	V_{IOV1}	V_{IOV1} +0.015	V	3	2
Overcurrent detection voltage 2	V_{IOV2}	—	0.9	1.2	1.5	V	3	2
Charger detection voltage	V_{CHA}	—	–1.0	–0.7	–0.4	V	4	2
Temperature coefficient 1*1	T_{COE1}	Ta = 0°C to 50°C*3	–1.0	0	1.0	mV/°C	—	—
Temperature coefficient 2*2	T_{COE2}	Ta = 0°C to 50°C*3	–0.5	0	0.5	mV/°C	—	—
[DELAY TIME]								
Overcharge detection delay time	t_{CU}	—	0.92	1.15	1.38	s	9	2
Overdischarge detection delay time	t_{DL}	—	115	144	173	ms	9	2
Overcurrent detection delay time 1	t_{IOV1}	—	7.2	9	11	ms	10	2
Overcurrent detection delay time 2	t_{IOV2}	FET gate capacitance = 2000 pF	220	300	380	µs	10	2
[0 V BATTERY CHARGE FUNCTION]								
0 V charge starting charger voltage	V_{0CHA}	0 V charge available	1.2	—	—	V	11	2
0 V battery charge inhibition battery voltage	V_{0INH}	0 V charge unavailable	—	—	0.5	V	12	2
[INTERNAL RESISTANCE]								
Resistance between VM and VDD	R_{VMD}	V1 = V2 = 1.5 V, V_{VM} = 0 V	100	300	900	kΩ	6	3
Resistance between VM and VSS	R_{VMS}	V1 = V2 = 3.5 V, V_{VM} = 1.0 V	5	10	20	kΩ	6	3
[INPUT VOLTAGE]								
Operating voltage between VDD and VSS	V_{DSOP1}	Internal circuit operating voltage	1.5	—	10	V	—	—
Operating voltage between VDD and VM	V_{DSOP2}	Internal circuit operating voltage	1.5	—	28	V	—	—
[INPUT CURRENT]								
Current consumption during operation	I_{OPE}	V1 = V2 = 3.5 V, V_{VM} = 0 V	—	5	10	µA	5	3
Current consumption at power down	I_{PDN}	V1 = V2 = 1.5 V, V_{VM} = 3.0 V	—	—	0.1	µA	5	3
VC pin current	I_{VC}	V1 = V2 = 3.5 V, V_{VM} = 0 V	–0.3	0	0.3	µA	5	3
[OUTPUT RESISTANCE]								
CO pin H resistance	R_{COH}	V_{CO} = V_{DD}–0.5 V	2	4	8	kΩ	7	4
CO pin L resistance	R_{COL}	V_{CO} = V_{VM}+0.5 V	2	4	8	kΩ	7	4
DO pin H resistance	R_{DOH}	V_{DO} = V_{DD}–0.5 V	2	4	8	kΩ	8	4
DO pin L resistance	R_{DOL}	V_{DO} = V_{SS} +0.5 V	2	4	8	kΩ	8	4

***1.** Voltage temperature coefficient 1: Overcharge detection voltage

***2.** Voltage temperature coefficient 2: Overcurrent detection voltage 1

***3.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.

1. Overcharge Detection Voltage, Overcharge Release Voltage
(Test Condition 1, Test Circuit 1)

Overcharge detection voltage 1 (V_{CU1}) is defined as the voltage between the VDD pin and VC pin at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = V2 = V_{CU}–0.05 V, V3 = 0 V. Overcharge release voltage 1 (V_{CL1}) is defined as the voltage between the VDD and VC pins at which V_{CO} goes from "L" to "H" when setting V2 = 3.5 V and the voltage V1 is then gradually decreased. Overcharge hysteresis voltage 1 (V_{HC1}) is defined as the difference between overcharge detection voltage 1 (V_{CU1}) and overcharge release voltage 1 (V_{CL1}).

Overcharge detection voltage 2 (V_{CU2}) is defined as the voltage between the VC pin and VSS pin at which V_{CO} goes from "H" to "L" when the voltage V2 is gradually increased from the starting condition of V1 = V2 = V_{CU}–0.05 V, V3 = 0 V. Overcharge release voltage 2 (V_{CL2}) is defined as the voltage between the VC and VSS pins at which V_{CO} goes from "L" to "H" when setting V1 = 3.5 V and the voltage V2 is then gradually decreased. Overcharge hysteresis voltage 2 (V_{HC2}) is defined as the difference between overcharge detection voltage 2 (V_{CU2}) and overcharge release voltage 2 (V_{CL2}).

2. Overdischarge Detection Voltage, Overdischarge Release Voltage
(Test Condition 2, Test Circuit 2)

Overdischarge detection voltage 1 (V_{DL1}) is defined as the voltage between the VDD pin and VC pin at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased from the starting condition of V1 = V2 = 3.5 V, V3 = 0 V. Overdischarge release voltage 1 (V_{DU1}) is defined as the voltage between the VDD pin and VC pin at which V_{DO} goes from "L" to "H" when setting V2 = 3.5 V and the voltage V1 is then gradually increased. Overdischarge hysteresis voltage 1 (V_{HD1}) is defined as the difference between overdischarge release voltage 1 (V_{DU1}) and overdischarge detection voltage 1 (V_{DL1}).

Overdischarge detection voltage 2 (V_{DL2}) is defined as the voltage between the VC pin and VSS pin at which V_{DO} goes from "H" to "L" when the voltage V2 is gradually decreased from the starting condition of V1 = V2 = 3.5 V, V3 = 0 V. Overdischarge release voltage 2 (V_{DU2}) is defined as the voltage between the VC pin and VSS pin at which V_{DO} goes from "L" to "H" when setting V1 = 3.5 V and the voltage V2 is then gradually increased. Overdischarge hysteresis voltage 2 (V_{HD2}) is defined as the difference between overdischarge release voltage 2 (V_{DU2}) and overdischarge detection voltage 2 (V_{DL2}).

3. Overcurrent Detection Voltage 1, Overcurrent Detection Voltage 2
(Test Condition 3, Test Circuit 2)

Overcurrent detection voltage 1 (V_{IOV1}) is defined as the voltage between the VM pin and VSS pin whose delay time for changing V_{DO} from "H" to "L" lies between the minimum and the maximum value of overcurrent delay time 1 when the voltage V3 is increased rapidly within 10 µs from the starting condition of V1 = V2 = 3.5 V, V3 = 0 V.

Overcurrent detection voltage 2 (V_{IOV2}) is defined as the voltage between the VM pin and VSS pin whose delay time for changing V_{DO} from "H" to "L" lies between the minimum and the maximum value of overcurrent delay time 2 when the voltage V3 is increased rapidly within 10 µs from the starting condition of V1 = V2 = 3.5 V, V3 = 0 V.

4. Charger Detection Voltage
(Test Condition 4, Test Circuit 2)

The charger detection voltage (V_{CHA}) is defined as the voltage between the VM pin and VSS pin at which V_{DO} goes from "L" to "H" when the voltage V3 is gradually decreased from 0 V after the voltage V1 is gradually increased from the starting condition of V1 = 1.8 V, V2 = 3.5 V, V3 = 0 V until the voltage V1 becomes V_{DL1} + (V_{HD1}/2).

The charger detection voltage can be measured only in a product whose overdischarge hysteresis $V_{HD} \neq 0$ V.

5. Operating Current Consumption, VC Pin Current, Power-down Current Consumption
(Test Condition 5, Test Circuit 3)

The operating current consumption (I_{OPE}) is the current I_{SS} that flows through the VSS pin and the VC pin current (I_{VC}) is the current I_C that flows through the VC pin under the set conditions of V1 = V2 = 3.5 V and S1:OFF, S2:ON (normal status).
The power-down current consumption (I_{PDN}) is the current I_{SS} that flows through the VSS pin under the set conditions of V1 = V2 = 1.5 V and S1:ON, S2:OFF (overdischarge status).

6. Resistance between VM and VDD, Resistance between VM and VSS
(Test Condition 6, Test Circuit 3)

The resistance between VM and VDD (R_{VMD}) is the resistance between VM and VDD pins under the set conditions of V1 = V2 = 1.5 V and S1:OFF, S2:ON.
The resistance between VM and VSS (R_{VMS}) is the resistance between VM and VSS pins under the set conditions of V1 = V2 = 3.5 V and S1:ON, S2:OFF.

7. CO Pin H Resistance, CO Pin L Resistance
(Test Condition 7, Test Circuit 4)

The CO pin H resistance (R_{COH}) is the resistance at the CO pin under the set conditions of V1 = V2 = 3.5 V, V4 = 6.5 V.
The CO pin L resistance (R_{COL}) is the resistance at the CO pin under the set conditions of V1 = V2 = 4.5 V, V4 = 0.5 V.

8. DO Pin H Resistance, DO Pin L Resistance
(Test Condition 8, Test Circuit 4)

The DO pin H resistance (R_{DOH}) is the resistance at the DO pin under the set conditions of V1 = V2 = 3.5 V, V5 = 6.5 V.
The DO pin L resistance (R_{DOL}) is the resistance at the DO pin under the set conditions of V1 = V2 = 1.8 V, V5 = 0.5 V.

9. Overcharge Detection Delay Time, Overdischarge Detection Delay Time
(Test Condition 9, Test Circuit 2)

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to change from "H" to "L" just after the voltage V1 momentarily increases within 10 µs from overcharge detection voltage 1 (V_{CU1}) − 0.2 V to overcharge detection voltage 1 (V_{CU1}) + 0.2 V under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.
The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to change from "H" to "L" just after the voltage V1 momentarily decreases within 10 µs from overdischarge detection voltage 1 (V_{DL1}) + 0.2 V to overdischarge detection voltage 1 (V_{DL1}) − 0.2 V under the set condition of V1 = V2 = 3.5 V, V3 = 0 V.

10. Overcurrent Detection Delay Time 1, Overcurrent Detection Delay Time 2
(Test Condition 10, Test Circuit 2)

Overcurrent detection delay time 1 (t_{IOV1}) is the time needed for V_{DO} to go to "L" after the voltage V3 momentarily increases within 10 µs from 0 V to V_{IOV1} + 0.1 V under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.
Overcurrent detection delay time 2 (t_{IOV2}) is the time needed for V_{DO} to go to "L" after the voltage V3 momentarily increases within 10 µs from 0 V to 2.0 V under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

11. 0 V Charge Starting Charger Voltage (Products in Which 0 V Charge Is Available)
(Test Condition 11, Test Circuit 2)

The 0 V charge starting charger voltage (V_{0CHA}) is defined as the voltage between the VDD pin and VM pin at which V_{CO} goes to "H" (V_{VM} + 0.1 V or higher) when the voltage V3 is gradually decreased from the starting condition of V1 = V2 = V3 = 0 V.

12. 0 V Charge Inhibition Battery Voltage (Products in Which 0 V Charge Is Unavailable)
(Test Condition 12, Test Circuit 2)

The 0 V charge inhibition charger voltage (V_{0INH}) is defined as the voltage between the VDD pin and VSS pin at which V_{CO} goes to "H" (V_{VM} + 0.1 V or higher) when the voltages V1 and V2 are gradually increased from the starting condition of V1 = V2 = 0 V, V3 = –4 V.

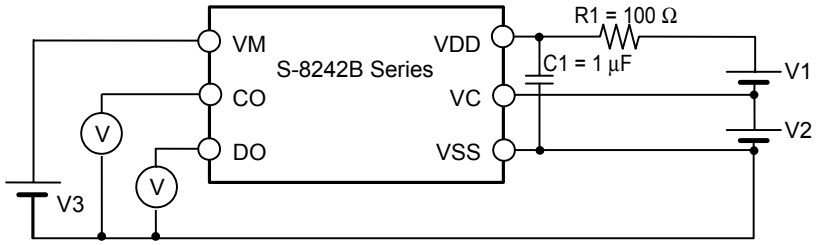


Figure 5 Test circuit 1

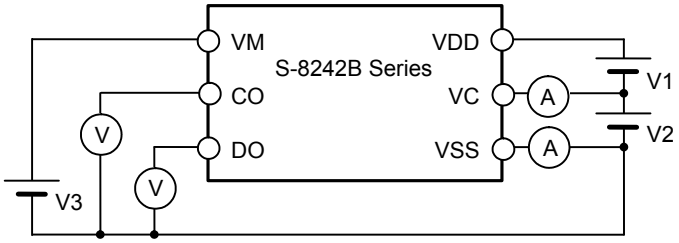


Figure 6 Test circuit 2

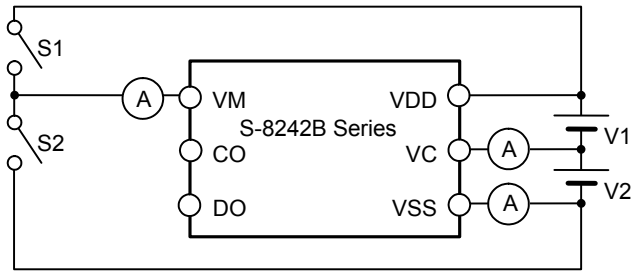


Figure 7 Test circuit 3

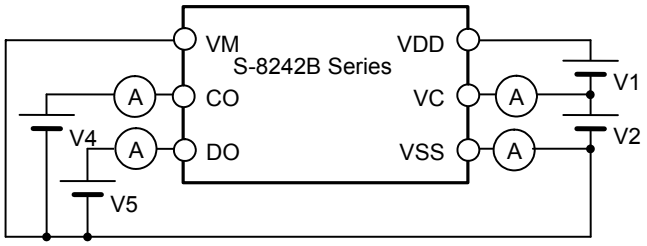


Figure 8 Test circuit 4

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Example**".

1. Normal Status

This IC monitors the voltage of the battery connected between the VDD and VSS pins and the voltage difference between the VM and VSS pins to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage n (V_{DLn}) to overcharge detection voltage n (V_{CUn}), and the VM pin voltage is in the range from the charger detection voltage (V_{CHA}) to overcurrent detection voltage 1 (V_{IOV1}), the IC turns both the charging and discharging control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.

Caution When the battery is connected for the first time, discharging may not be enabled. In this case,

Short the VM pin and VSS pin, or
Set the VM pin's voltage at the level of the charger detection voltage (V_{CHA}) or more and the overcurrent detection voltage 1 (V_{IOV1}) or less by connecting the charger

The IC returns to the normal status.

2. Overcharge Status

When the battery voltage becomes higher than overcharge detection voltage n (V_{CUn}) during charging in the normal status and detection continues for the overcharge detection delay time (t_{CU}) or longer, the S-8242B Series turns the charging control FET off to stop charging. This condition is called the overcharge status.
The overcharge status is released in the following two cases ((1) and (2)).

(1) When the battery voltage falls below overcharge release voltage n (V_{CLn}), the S-8242B Series turns the charging control FET on and returns to the normal status.
(2) When a load is connected and discharging starts, the S-8242B Series turns the charging control FET on and returns to the normal status. Just after the load is connected and discharging starts, the discharging current flows through the parasitic diode in the charging control FET. At this moment the VM pin potential becomes V_f, the voltage for the parasitic diode, higher than the V_{SS} level. When the battery voltage goes under overcharge detection voltage n (V_{CUn}) and provided that the VM pin voltage is higher than overcurrent detection voltage 1, the S-8242B Series releases the overcharge condition.

Caution 1. If the battery is charged to a voltage higher than overcharge detection voltage n (V_{CUn}) and the battery voltage does not fall below overcharge detection voltage n (V_{CUn}) even when a heavy load is connected, overcurrent 1 and overcurrent 2 do not function until the battery voltage falls below overcharge detection voltage n (V_{CUn}). Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and overcurrent 1 and overcurrent 2 function.

2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below overcharge release voltage n (V_{CLn}). The overcharge status is released when the VM pin voltage goes over the charger detection voltage (V_{CHA}) by removing the charger.

3. Overdischarge Status

When the battery voltage falls below overdischarge detection voltage n (V_{DLn}) during discharging in the normal status and detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8242B Series turns the discharging control FET off to stop discharging. This condition is called the overdischarge status. When the discharging control FET is turned off, the VM pin voltage is pulled up by the resistor between the VM and VDD pins in the IC (R_{VMD}). When the voltage difference between the VM and VSS pins is 1.3 V (typ.) or higher, the current consumption is reduced to the power-down current consumption (I_{PDN}). This condition is called the power-down status.

The power-down status is released when a charger is connected and the voltage difference between the VM and VSS pins becomes 1.3 V (typ.) or lower. Moreover, when the battery voltage becomes overdischarge detection voltage n (V_{DLn}) or higher, the S-8242B Series turns the discharging FET on and returns to the normal status.

4. Charger Detection

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than the charger detection voltage (V_{CHA}), the overdischarge hysteresis is released via the charge detection function; therefore, the S-8242B Series releases the overdischarge status and turns the discharging control FET on when the battery voltage becomes equal to or higher than overdischarge detection voltage n (V_{DLn}) since the charger detection function works. This action is called charger detection.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is not lower than the charger detection voltage (V_{CHA}), the S-8242B Series releases the overdischarge status when the battery voltage reaches overdischarge release voltage n (V_{DUn}) or higher.

5. Overcurrent Status

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or higher than the overcurrent detection voltage because the discharge current is higher than the specified value and the status lasts for the overcurrent detection delay time, the discharge control FET is turned off and discharging is stopped. This status is called the overcurrent status.

In the overcurrent status, the VM and VSS pins are shorted by the resistor between VM and VSS (R_{VMS}) in the IC. However, the voltage of the VM pin is at the V_{DD} potential due to the load as long as the load is connected. When the load is disconnected, the VM pin returns to the V_{SS} potential.

This IC detects the status when the impedance between the EB+ pin and EB− pin (Refer to **Figure 13**) increases and is equal to the impedance that enables automatic restoration and the voltage at the VM pin returns to overcurrent detection voltage 1 (V_{IOV1}) or lower and the overcurrent status is restored to the normal status.

Caution The impedance that enables automatic restoration varies depending on the battery voltage and the set value of overcurrent detection voltage 1.

6. 0 V Battery Charge Function

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ and EB− pins by connecting a charger, the charging control FET gate is fixed to the VDD pin voltage.
When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage due to the charger voltage, the charging control FET is turned on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than overdischarge release voltage n (V_{DUn}), the S-8242B Series enters the normal status.

Caution Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

7. 0 V Battery Charge Inhibition Function

This function inhibits recharging when a battery that is internally short-circuited (0 V) is connected. When the battery voltage (The voltage between VDD and VSS pins) is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charging control FET gate is fixed to the EB− pin voltage to inhibit charging. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or higher, charging can be performed.

Caution Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

8. Delay Circuit

The detection delay times are determined by dividing a clock of approximately 3.5 kHz by the counter.

Remark1. The overcurrent detection delay time 2 (t_{IOV2}) starts when the overcurrent detection voltage 1 (V_{IOV1}) is detected. When the overcurrent detection voltage 2 (V_{IOV2}) is detected over the overcurrent detection delay time 2 (t_{IOV2}) after the detection of overcurrent detection voltage 1 (V_{IOV1}), the S-8242B turns the discharging control FET off within t_{IOV2} from the time of detecting V_{IOV2}.

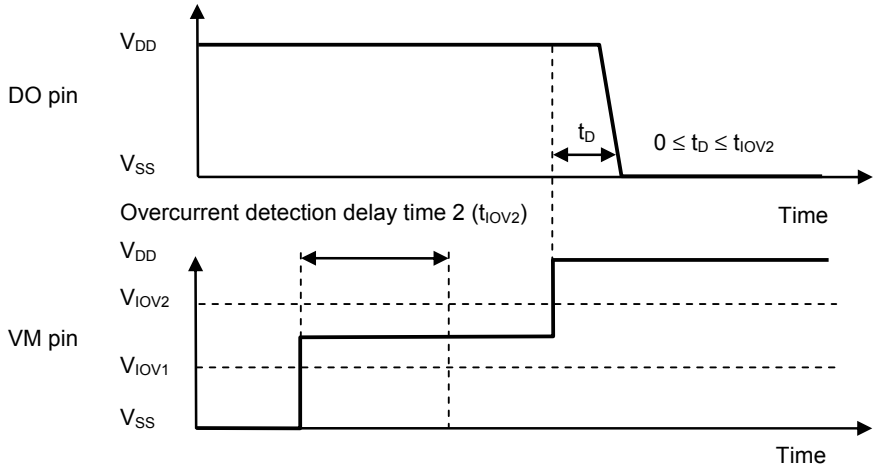
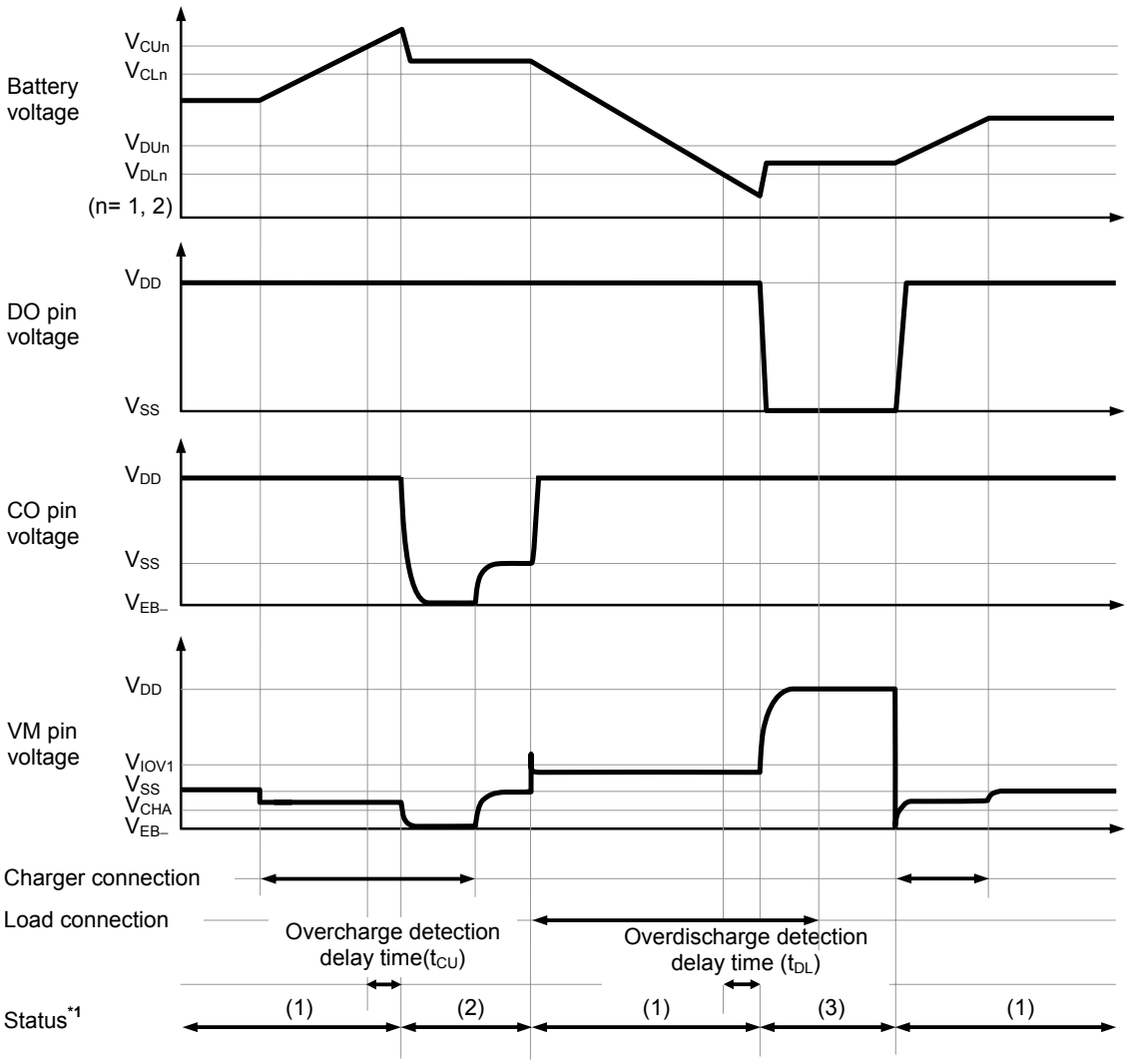


Figure 9

2. When the overcurrent is detected and continues for longer than the overdischarge detection delay time (t_{DL}) without releasing the load, the condition changes to the power-down condition when the battery voltage falls below the overdischarge detection voltage n (V_{DLn}). When the battery voltage falls below the overdischarge detection voltage n (V_{DLn}) due to the overcurrent, the S-8242B Series turns the discharging control FET off by the overcurrent detection. In this case the recovery of the battery voltage is so slow that if the battery voltage after the overdischarge detection delay time (t_{DL}) is still lower than the overdischarge detection voltage n (V_{DLn}), the S-8242B Series shifts to the power-down condition.

■ Timing Chart

1. Overcharge Detection, Overdischarge Detection

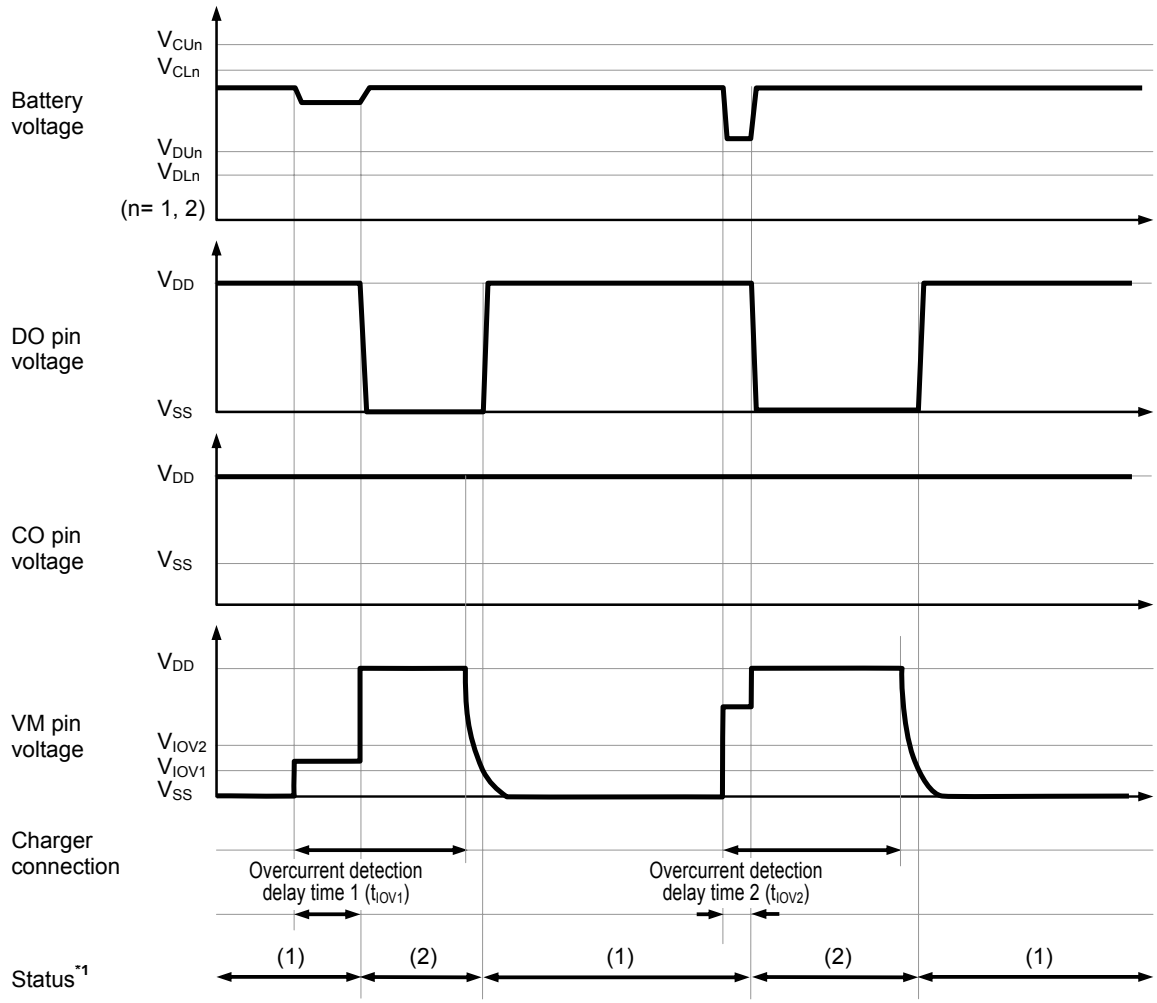


***1.** (1) : Normal status
(2) : Overcharge status
(3) : Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 10

2. Overcurrent Detection

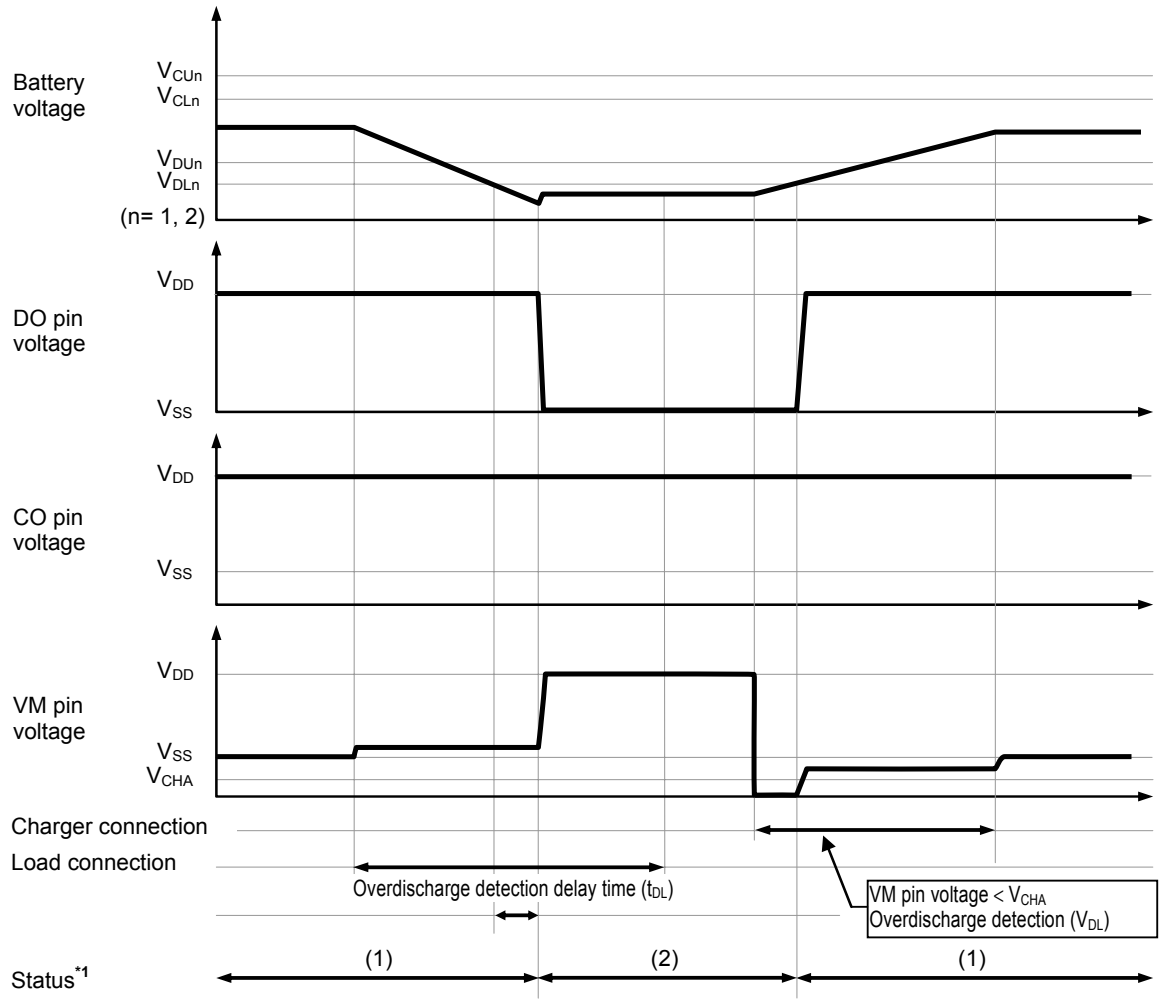


***1.** (1) : Normal status
(2) : Overcurrent status

Remark The charger is assumed to charge with a constant current.

Figure 11

3. Charger Detection



***1.** (1) : Normal status
(2) : Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 12

■ Battery Protection IC Connection Example

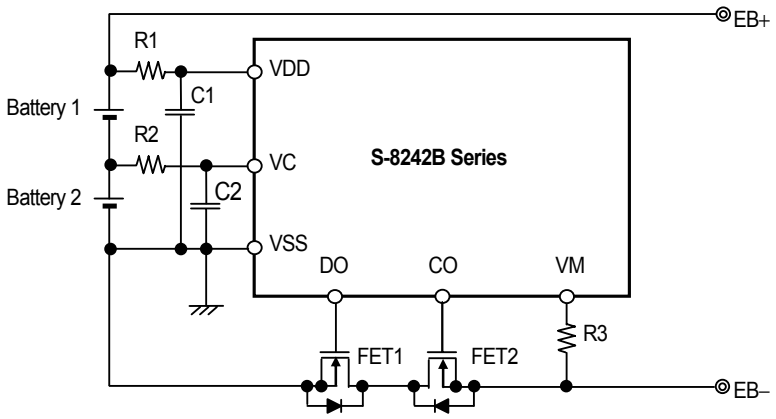


Figure 13

Table 7 Constants for External Components

Symbol	Parts	Purpose	Typ.	Min.	Max.	Remark
FET1	N-channel MOS FET	Discharge control	—	—	—	Threshold voltage≤Overdischarge detection voltage*2 Gate to source withstanding voltage≥Charger voltage*3
FET2	N-channel MOS FET	Charge control	—	—	—	Threshold voltage≤Overdischarge detection voltage*2 Gate to source withstanding voltage≥Charger voltage*3
R1	Resistor	ESD protection, For power fluctuation	100 Ω	10 Ω*1	220 Ω*1	Resistance should be as small as possible to avoid lowering the overcharge detection accuracy due to current consumption.*4
C1	Capacitor	For power fluctuation	1 μF	0.47 μF*1	10 μF*1	Connect a capacitor of 0.47 μF or higher between VDD and VSS.*5
R2	Resistor	ESD protection, For power fluctuation	1 kΩ	300 Ω*1	1 kΩ*1	—
C2	Capacitor	For power fluctuation	0.1 μF	0.022 μF*1	1.0 μF*1	—
R3	Resistor	Protection for reverse connection of a charger	2 kΩ	300 Ω	4 kΩ	Select as large a resistance as possible to prevent current when a charger is connected in reverse.*6

***1.** Please set up a filter constant to be $R2 \times C2 \geq 20\ \mu F \bullet \Omega$, and to be $R1 \times C1 = R2 \times C2$.

***2.** If the threshold voltage of a FET is low, the FET may not cut the charging current.
If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

***3.** If the withstanding voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.

***4.** If R1 has a high resistance, the voltage between VDD and VSS may exceed the absolute maximum rating when a charger is connected in reverse since the current flows from the charger to the IC.
Insert a resistor of 10 Ω or higher to R1 for ESD protection.

***5.** If a capacitor of less than 0.47 μF is connected to C1, DO pin may oscillate when load short-circuiting is detected. Be sure to connect a capacitor of 0.47 μF or higher to C1.

***6.** If R3 has a resistance higher than 4 kΩ, the charging current may not be cut when a high-voltage charger is connected.

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform through evaluation using the actual application to set the constant.

■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- When connecting a battery and the protection circuit, the output voltage of the DO pin (V_{DO}) may become “L” (initial state). In this case,

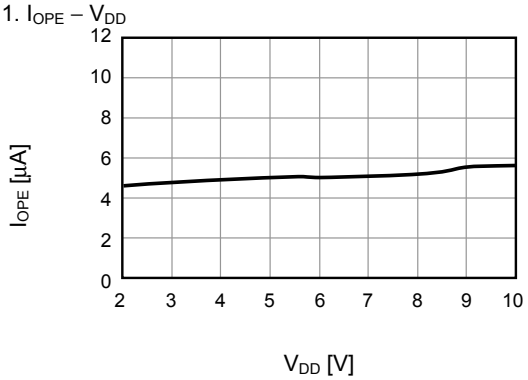
  Short the VM and VSS pins or,
  Set the VM pin’s voltage at the level of the charger detection voltage (V_{CHA}) or more and the overcurrent detection voltage 1 (V_{IOV1}) or less by connecting the charger

  The output voltage of the DO pin (V_{DO}) is set to “H” (normal status).
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

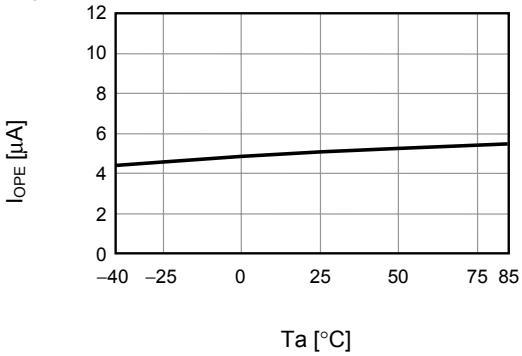
■ Characteristics (Typical Data)

(1) Current consumption

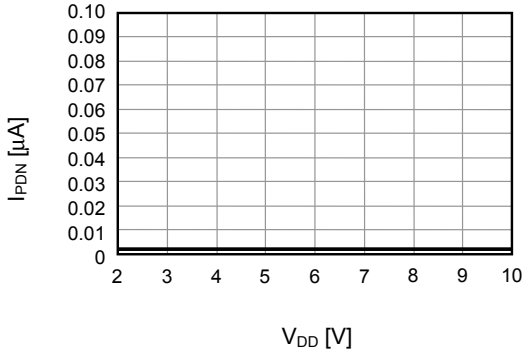
1. I_{OPE} – V_{DD}



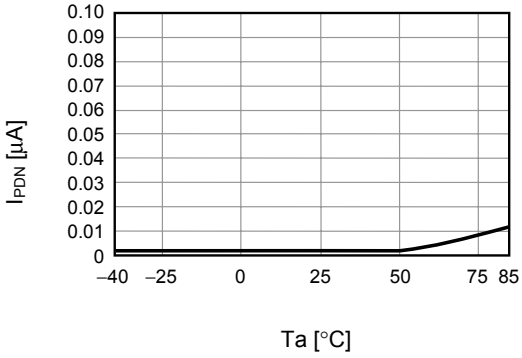
2. I_{OPE} – Ta



3. I_{PDN} – V_{DD}

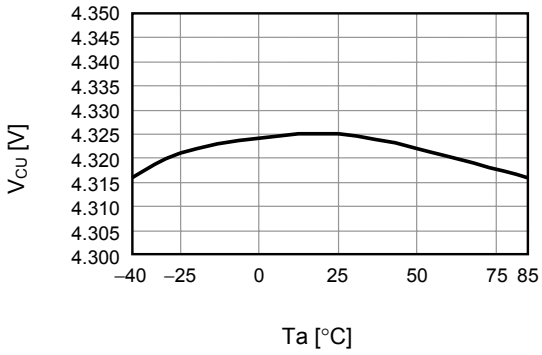


4. I_{PDN} – Ta

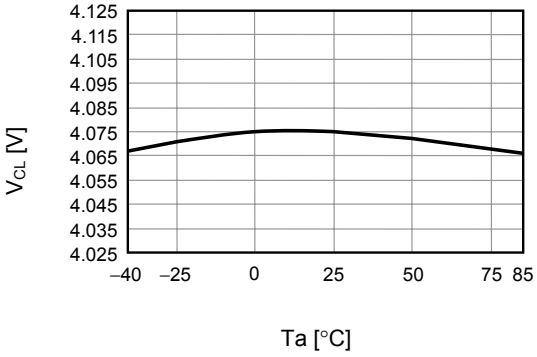


(2) Overcharge detection/release voltage, overdischarge detection/release voltage, overcurrent detection voltage, and delay time

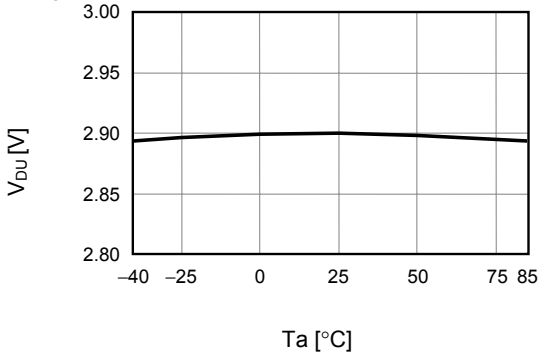
1. V_{CU} – Ta



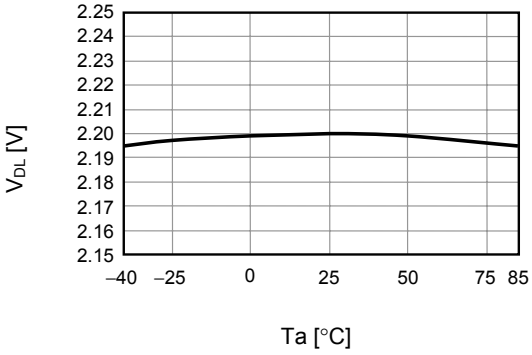
2. V_{CL} – Ta



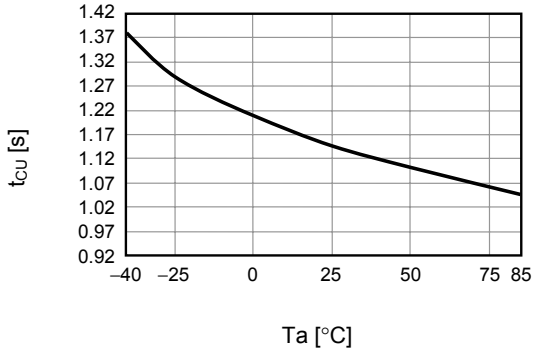
3. V_{DU} – Ta



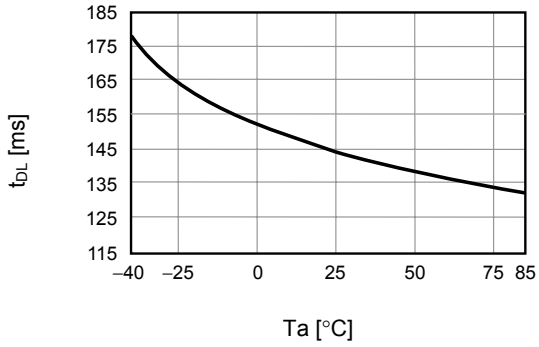
4. V_{DL} – Ta



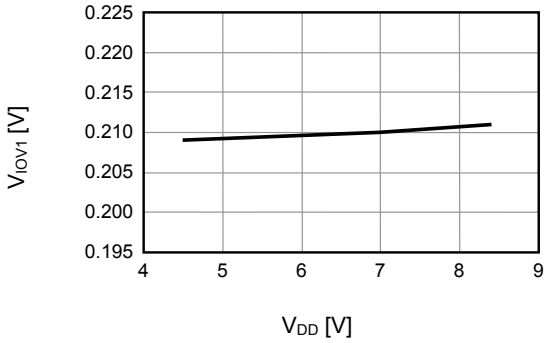
5. t_{CU} – Ta



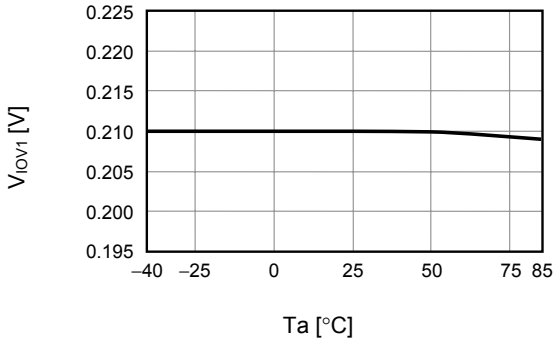
6. t_{DL} – Ta



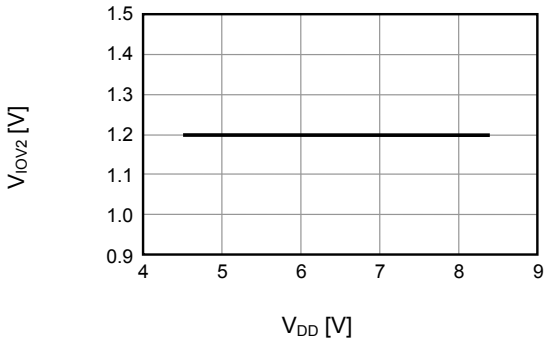
7. V_{IOV1} – V_{DD}



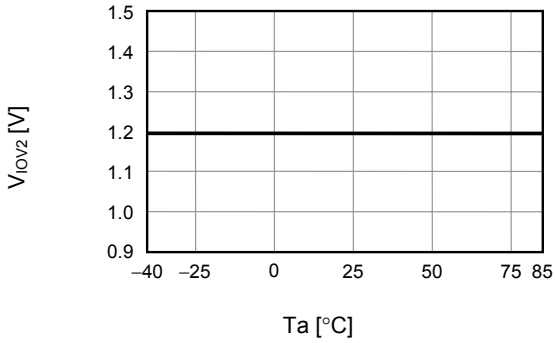
8. V_{IOV1} – Ta



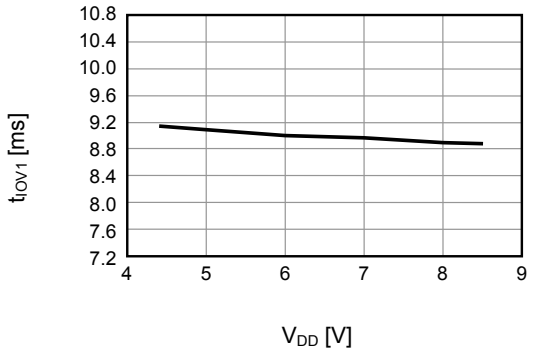
9. V_{IOV2} – V_{DD}



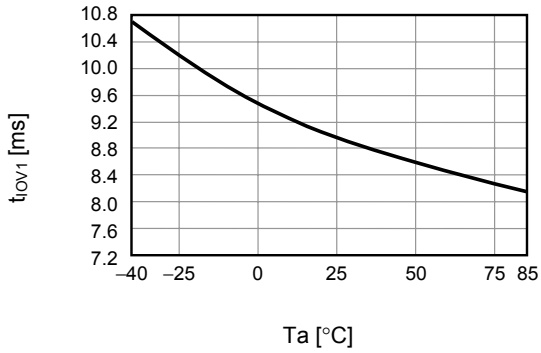
10. V_{IOV2} – Ta



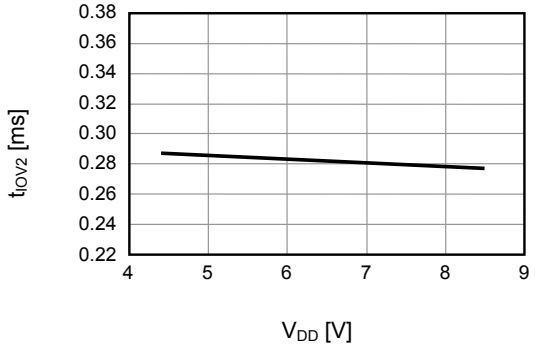
11. t_{IOV1} – V_{DD}



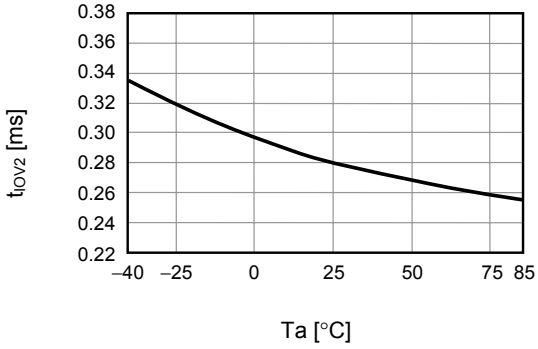
12. t_{IOV1} – Ta



13. t_{IOV2} – V_{DD}

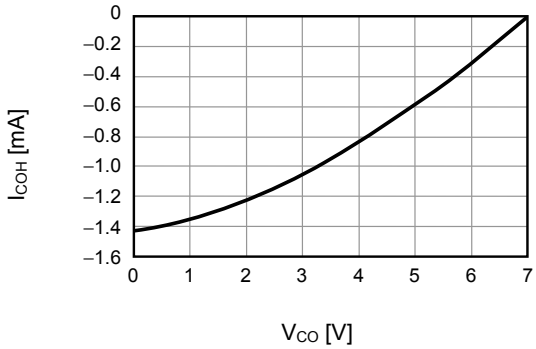


14. t_{IOV2} – Ta

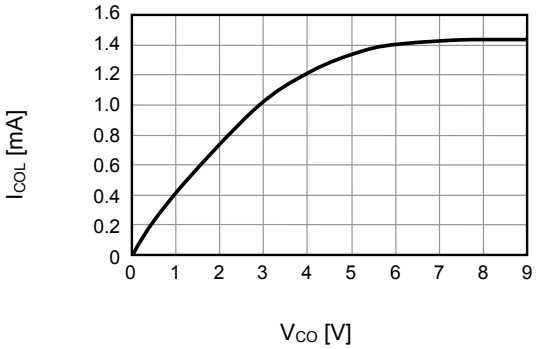


(3) CO/DO pin

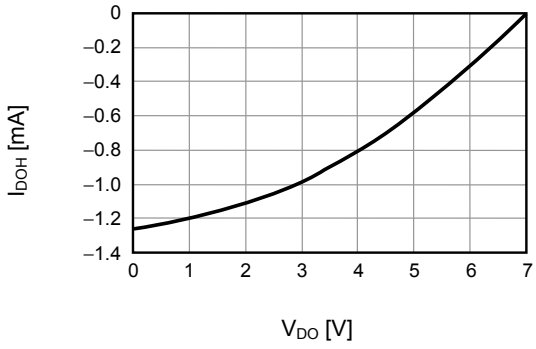
1. I_{COH} – V_{CO}



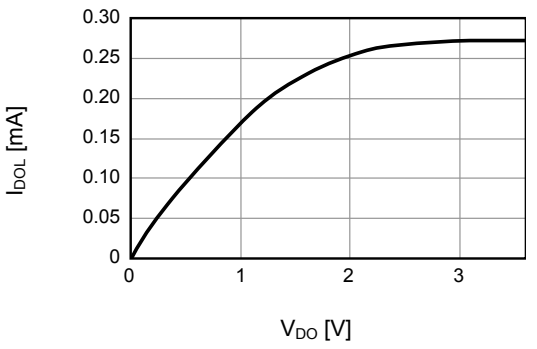
2. I_{COL} – V_{CO}



3. I_{DOH} – V_{DO}



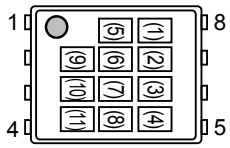
4. I_{DOL} – V_{DO}



■ Marking Specifications

(1) SNT-8A

SNT-8A
Top view



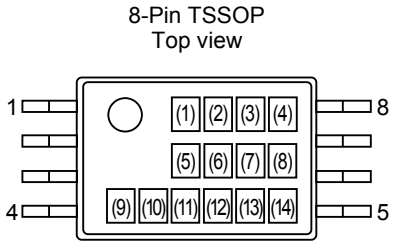
(1)	Blank
(2) to (4)	Product code (Refer to **Product name vs. Product code**)
(5), (6)	Blank
(7) to (11)	Lot number

Product Name vs. Product Code

Product Name	Product Code		
	(2)	(3)	(4)
S-8242BAB-I8T1G	Q	N	B
S-8242BAC-I8T1G	Q	N	C
S-8242BAD-I8T1G	Q	N	D
S-8242BAE-I8T1G	Q	N	E
S-8242BAF-I8T1G	Q	N	F
S-8242BAH-I8T1G	Q	N	H
S-8242BAI-I8T1G	Q	N	I
S-8242BAM-I8T1G	Q	N	M
S-8242BAN-I8T1G	Q	N	N
S-8242BAO-I8T1G	Q	N	O
S-8242BAQ-I8T1G	Q	N	Q
S-8242BAR-I8T1G	Q	N	R
S-8242BAU-I8T1G	Q	N	U
S-8242BAV-I8T1G	Q	N	V
S-8242BAW-I8T1G	Q	N	W
S-8242BAX-I8T1G	Q	N	X
S-8242BAY-I8T1G	Q	N	Y
S-8242BAZ-I8T1G	Q	N	Z
S-8242BBA-I8T1G	Q	O	A
S-8242BBB-I8T1G	Q	O	B
S-8242BBC-I8T1G	Q	O	C
S-8242BBD-I8T1G	Q	O	D
S-8242BBF-I8T1G	Q	O	F
S-8242BBI-I8T1G	Q	O	I

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

(2) 8-Pin TSSOP

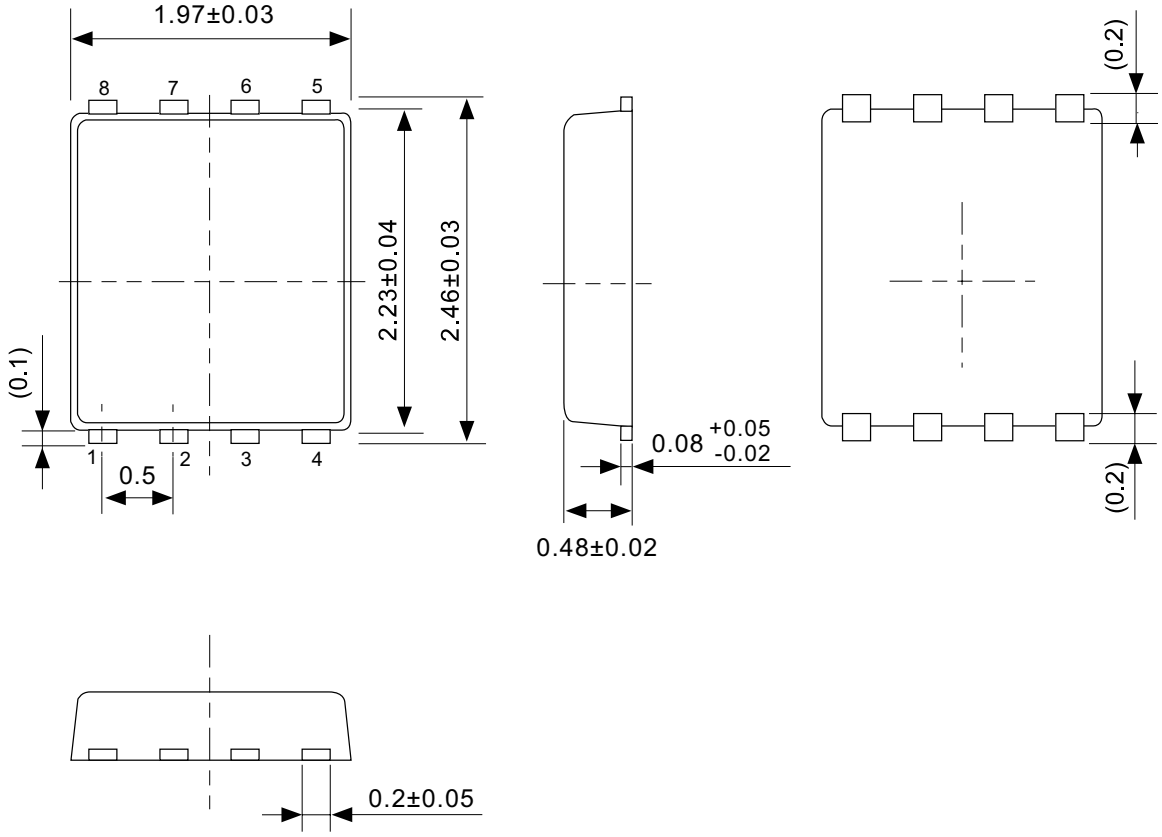


(1) to (5): Product Name : S8242 (Fixed)
(6) to (8): Function Code
(refer to **Product Name vs. Function Code**)
(9) to (14): Lot number

Product Name vs. Function Code

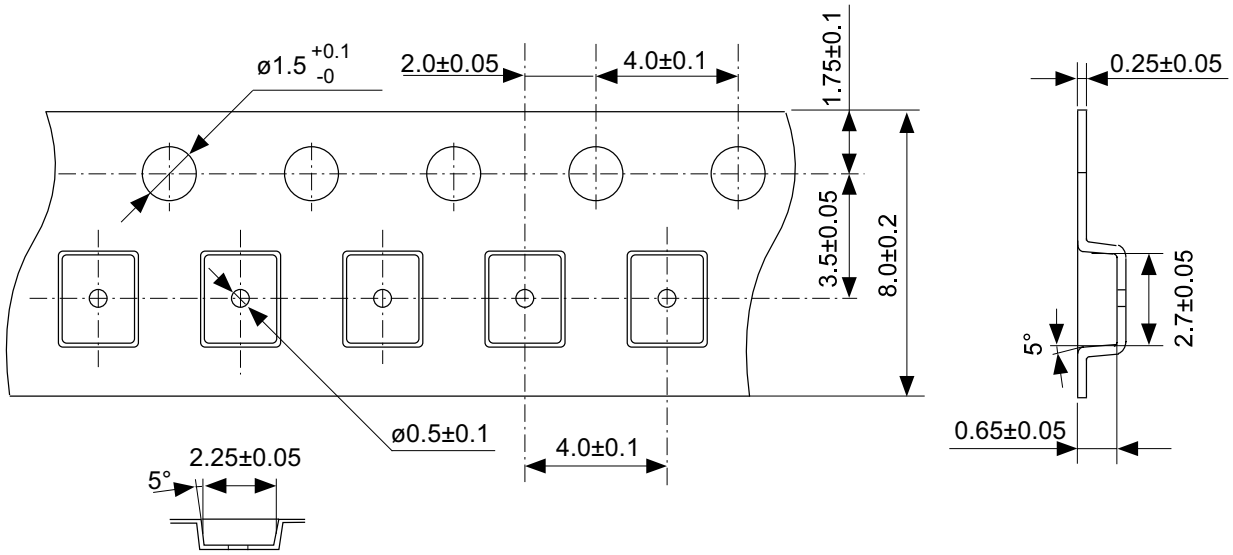
Product Name	Function Code		
	(6)	(7)	(8)
S-8242BAC-T8T1G	B	A	C
S-8242BAH-T8T1G	B	A	H
S-8242BAI-T8T1G	B	A	I
S-8242BAP-T8T1G	B	A	P
S-8242BAR-T8T1G	B	A	R
S-8242BAU-T8T1G	B	A	U
S-8242BAV-T8T1G	B	A	V
S-8242BAW-T8T1G	B	A	W
S-8242BAX-T8T1G	B	A	X
S-8242BBE-T8T1G	B	B	E
S-8242BBF-T8T1G	B	B	F
S-8242BBG-T8T1G	B	B	G

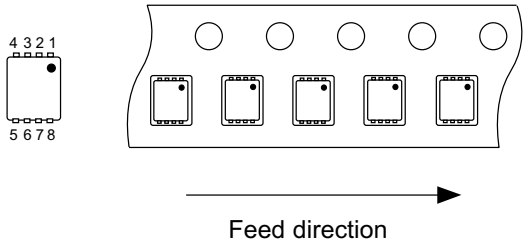
Remark Please contact our sales office for the products with detection voltage value other than those specified above.



No. PH008-A-P-SD-2.0

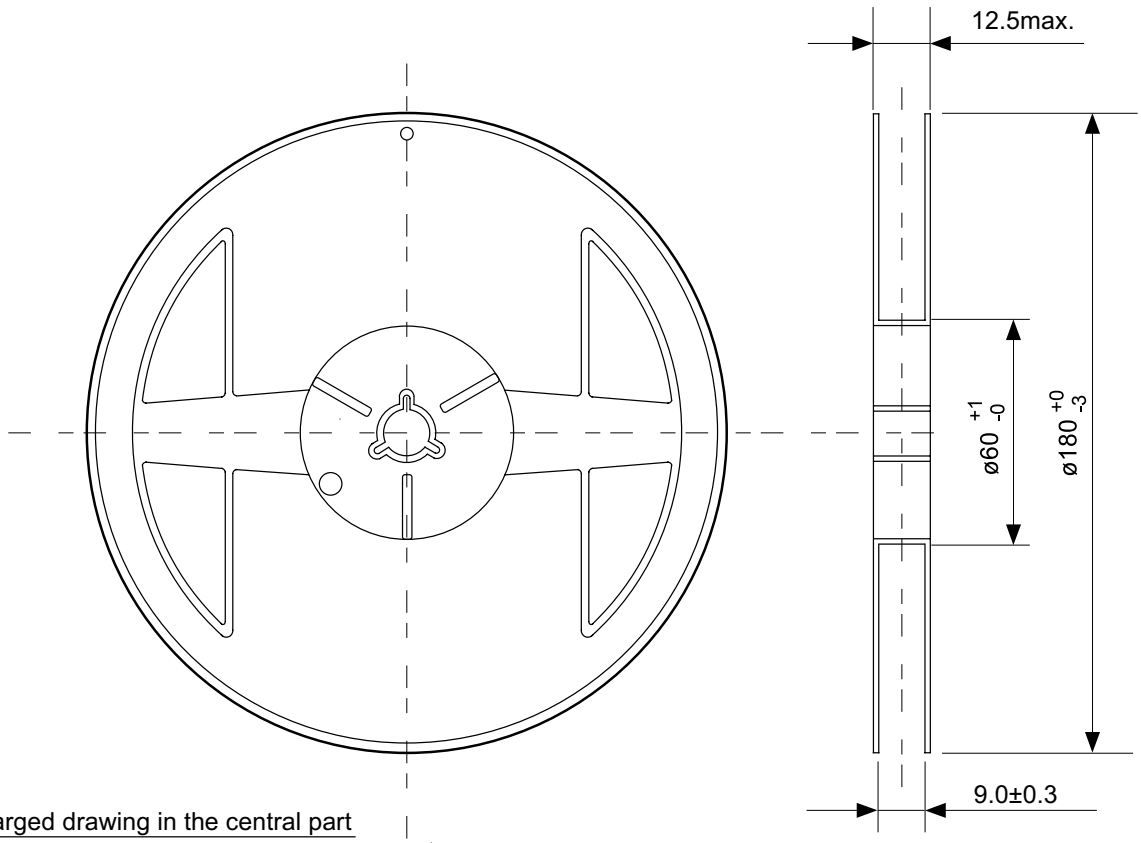
TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



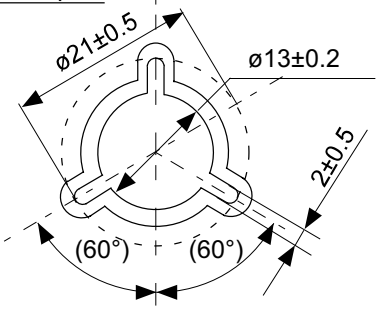


No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

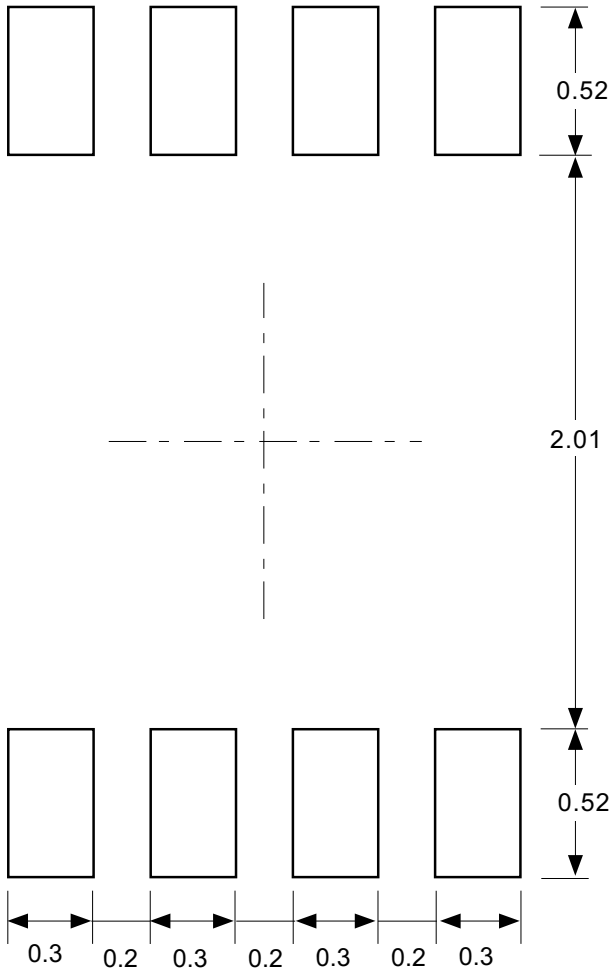


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
Seiko Instruments Inc.			

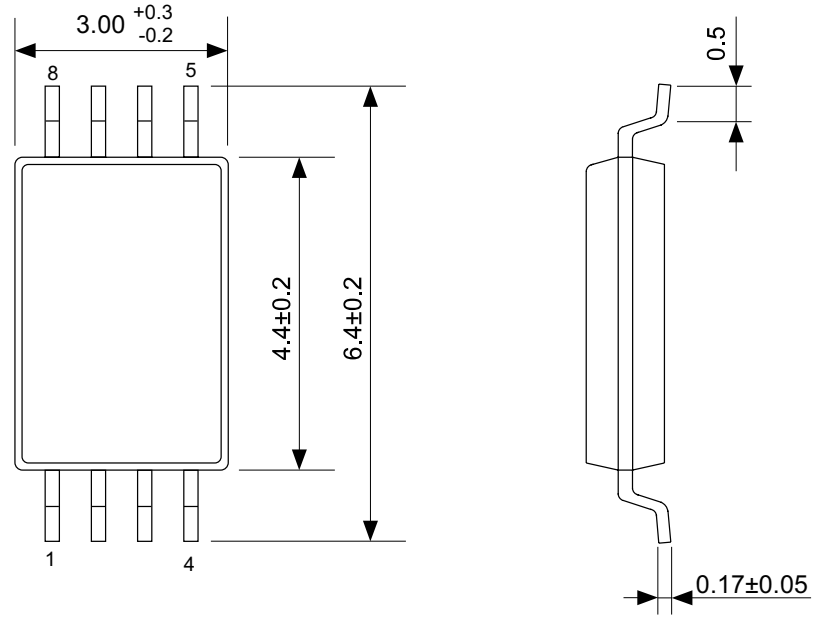


Caution Making the wire pattern under the package is possible. However, note that the package may be upraised due to the thickness made by the silk screen printing and of a solder resist on the pattern because this package does not have the standoff.

注意 パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフが無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージが持ち上がることがありますのでご配慮ください。

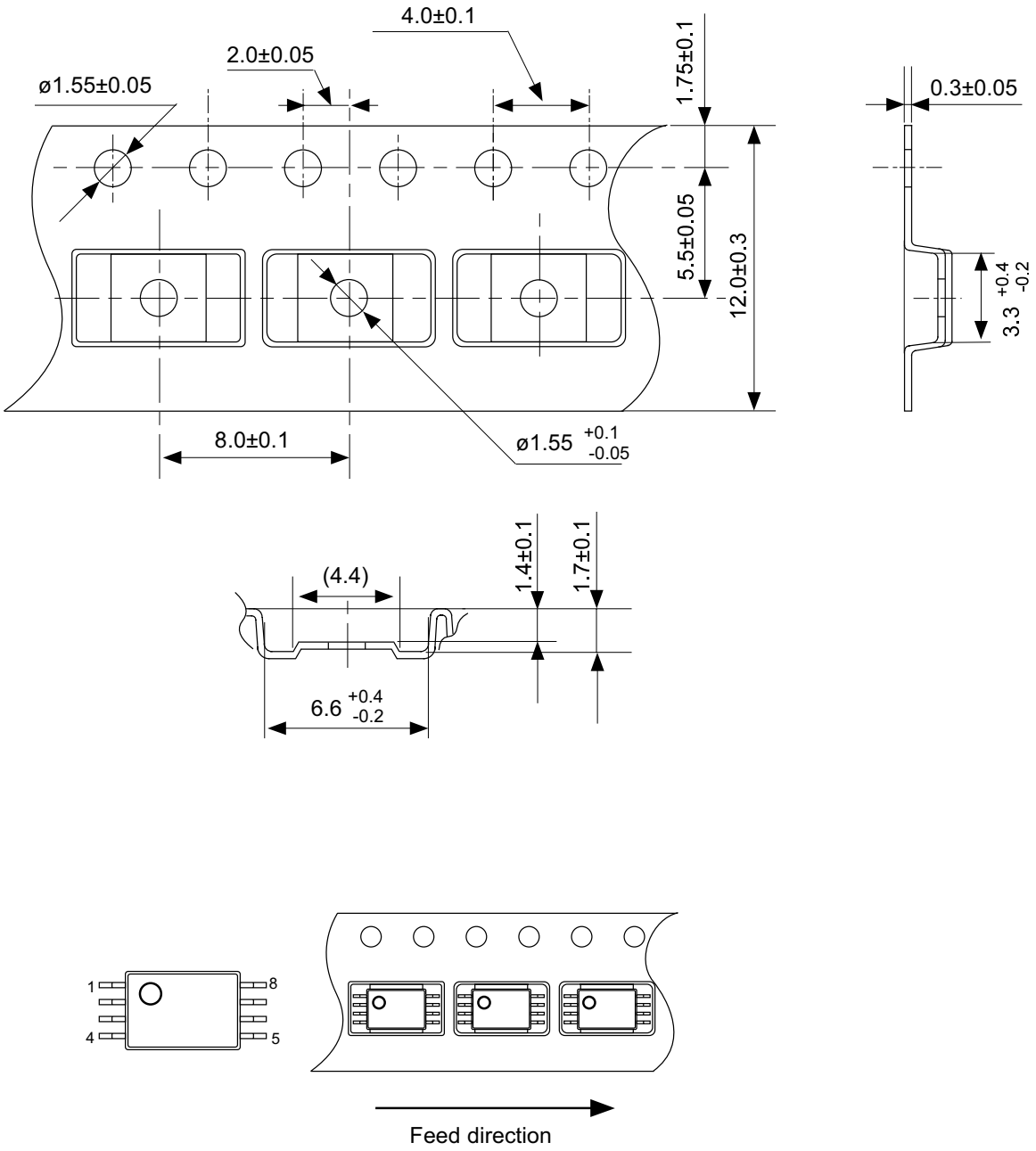
No. PH008-A-L-SD-3.0

TITLE	SNT-8A-A-Land Recommendation
No.	PH008-A-L-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



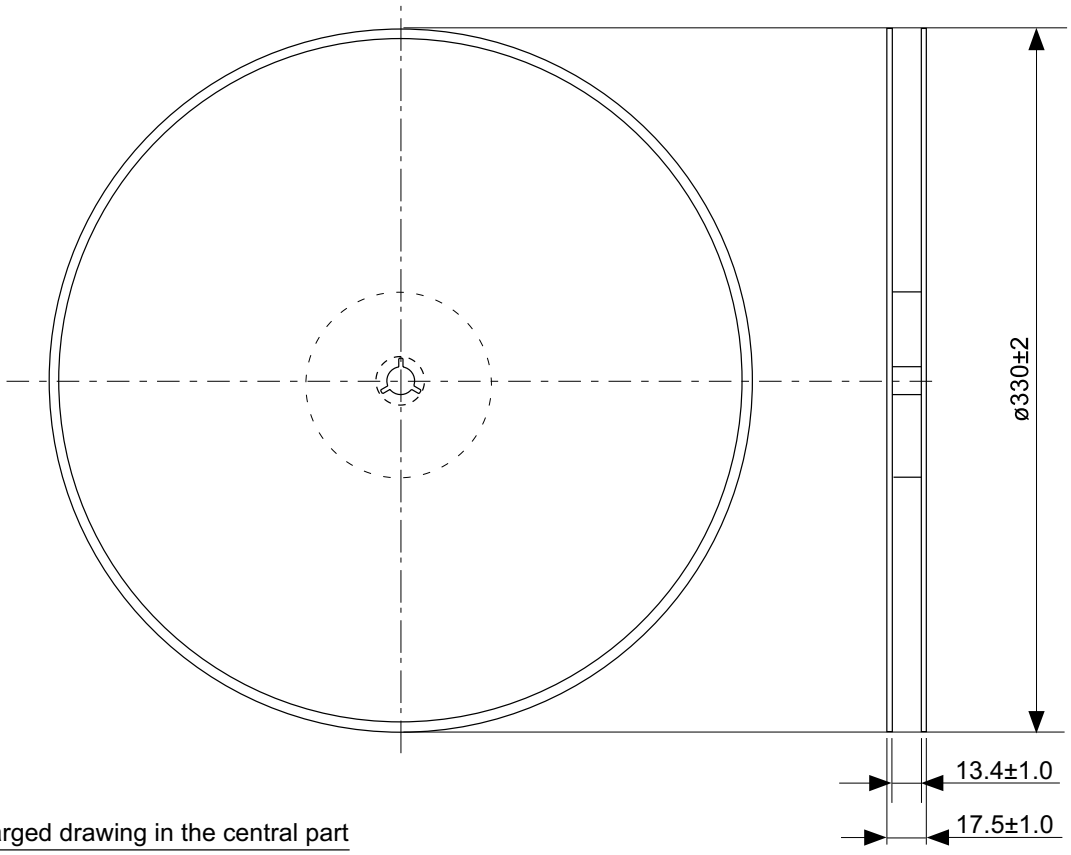
No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

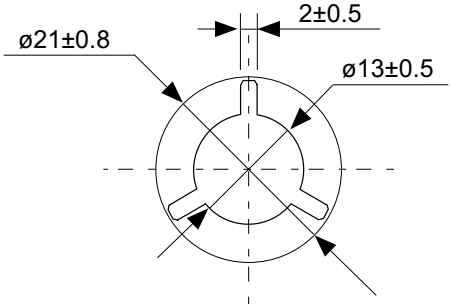


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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