BATTERY PROTECTION IC FOR 1-SERIAL TO 4-SERIAL-CELL PACK (SECONDARY PROTECTION)

S-8244 Series

The S-8244 Series is used for secondary protection of lithium-ion batteries with from one to four cells, and incorporates a high-precision voltage detector circuit and a delay circuit.   Short-circuits between cells accommodate series connection of one to four cells.

■ Features

(1) Internal high-precision voltage detector circuit
- Overcharge detection voltage range : 3.700 V to 4.500 V : Accuracy of $\pm$ 25 mV (at +25°C)
  (at a 5 mV/step)   Accuracy of $\pm$ 50 mV (at −40°C to +85°C)
- Hysteresis :   5 types
  0.38 $\pm$ 0.1 V, 0.25 $\pm$ 0.07 V, 0.13 $\pm$ 0.04 V, 0.045 $\pm$ 0.02 V, None
(2) High withstand voltage device :   Absolute maximum rating : 26 V
(3) Wide operating voltage range :   3.6 V to 24 V (refers to the range in which the delay circuit can operate normally after overvoltage is detected)
(4) Delay time during detection :   Can be set by an external capacitor.
(5) Low current consumption :   At 3.5 V for each cell :   3.0 μA max. (+25°C)
                                         At 2.3 V for each cell :   2.4 μA max. (+25°C)
(6) Output logic and form :   5 types
                                         CMOS output active "H"
                                         CMOS output active "L"
                                         Pch open drain output active "L"
                                         Nch open drain output active "H"
                                         Nch open drain output active "L"
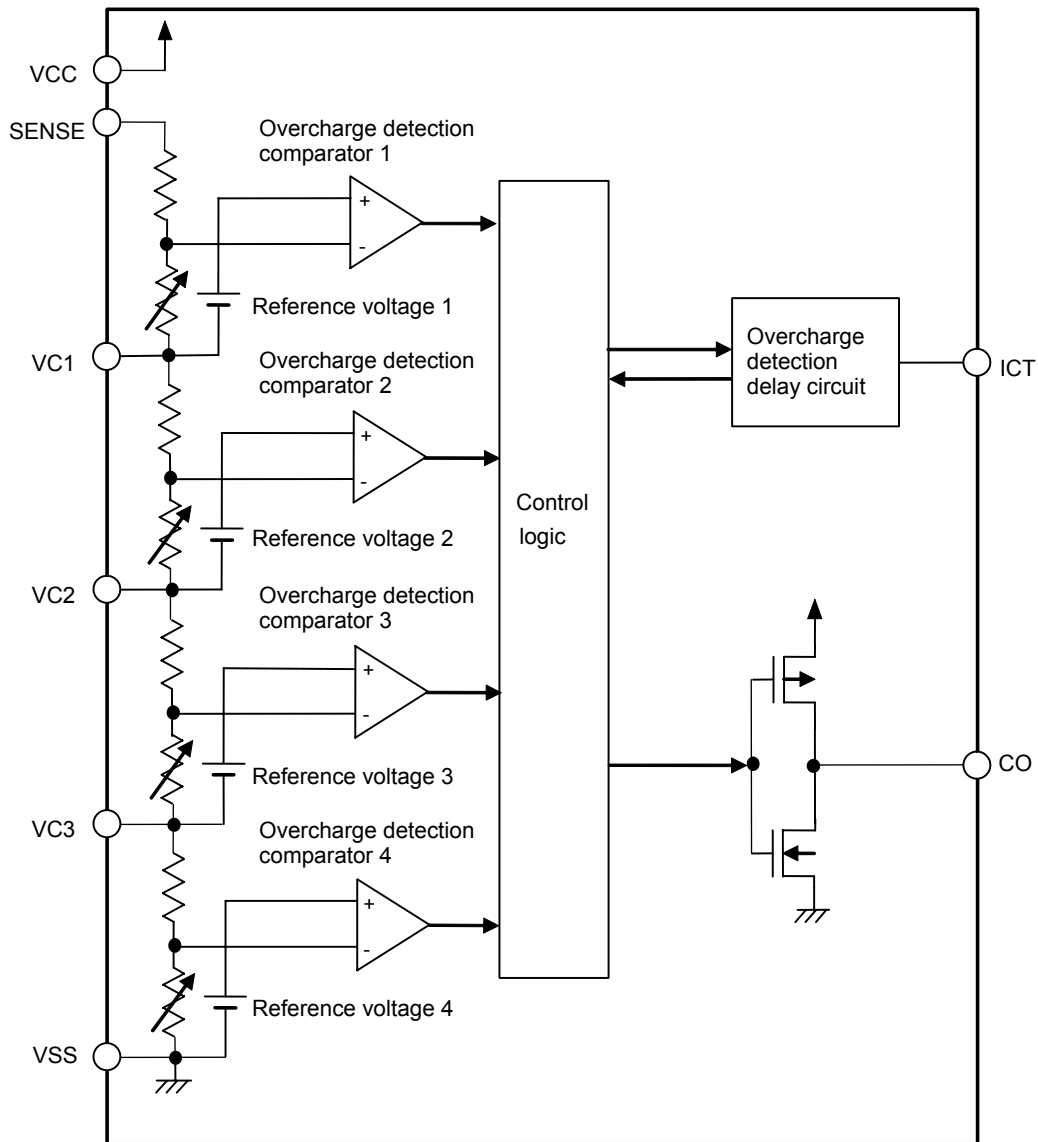   (CMOS / Nch open drain output for 0.045 V hysteresis models)
(7) Lead-free products

■ Applications

- Lithium ion rechargeable battery packs (secondary protection)

■ Packages

Package name	Drawing code			
	Package	Tape	Reel	Land
SNT-8A	PH008-A	PH008-A	PH008-A	PH008-A
8-Pin MSOP	FN008-A	FN008-A	FN008-A	—

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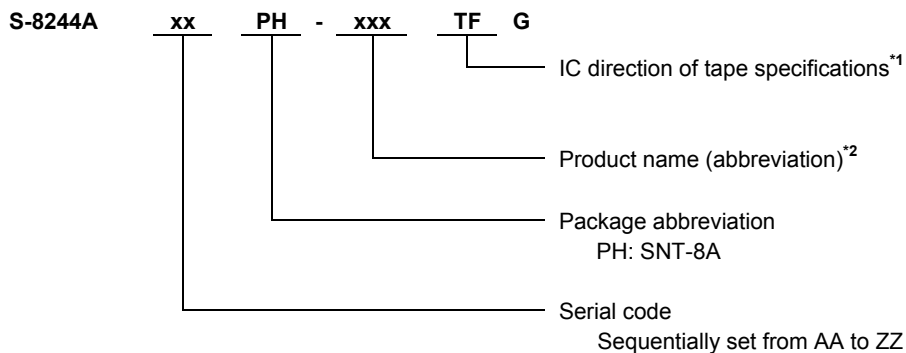
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■ **Block Diagram**

Remark In the case of Nch open-drain output, only the Nch transistor will be connected to the CO pin.
In the case of Pch open-drain output, only the Pch transistor will be connected to the CO pin.

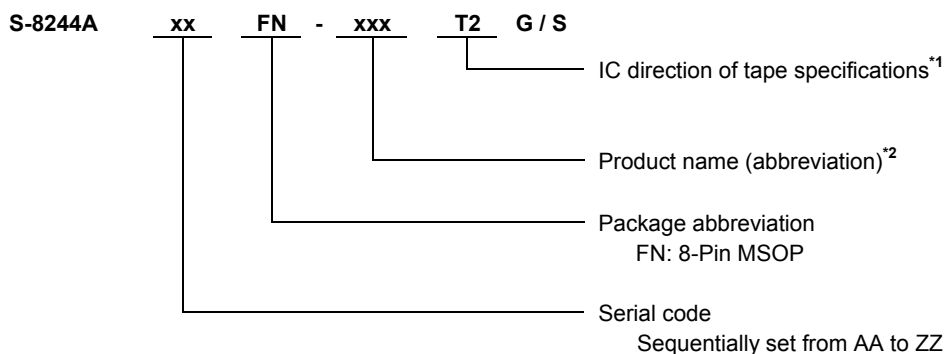**Figure 1**

■ Product Name Structure

1. Product Name

(1) SNT-8A

S-8244A __xx__ __PH__ - __xxx__ __TF__ __G__

IC direction of tape specifications[1]

Product name (abbreviation)[2]

Package abbreviation
PH: SNT-8A

Serial code
Sequentially set from AA to ZZ

[1]. Refer to the tape specifications at the end of this book.
[2]. Refer to the **Product Name List**.

(2) 8-Pin MSOP

S-8244A __xx__ __FN__ - __xxx__ __T2__ __G / S__

IC direction of tape specifications[1]

Product name (abbreviation)[2]

Package abbreviation
FN: 8-Pin MSOP

Serial code
Sequentially set from AA to ZZ

[1]. Refer to the tape specifications at the end of this book.
[2]. Refer to the **Product Name List**.

2. Product Name List

(1) SNT-8A

Table 1

Product name/Item	Overcharge detection voltage [V_{CU}]	Overcharge hysteresis voltage [V_{CD}]	Output form
S-8244AAAPH-CEATFG	4.450 ± 0.025 V	0.38 ± 0.1 V	CMOS output active "H"
S-8244AABPH-CEBTFG	4.200 ± 0.025 V	0 V	Nch open drain active "H"
S-8244AADPH-CEDTFG	4.200 ± 0.025 V	0 V	Pch open drain active "L"
S-8244AAFPH-CEFTFG	4.350 ± 0.025 V	0.045 ± 0.02 V	CMOS output active "H"
S-8244AAGPH-CEGTFG	4.450 ± 0.025 V	0.045 ± 0.02 V	CMOS output active "H"
S-8244AAJPH-CEJTFG	4.500 ± 0.025 V	0.38 ± 0.1 V	CMOS output active "H"
S-8244AASPH-CESTFG	4.350 ± 0.025 V	0.38 ± 0.1 V	CMOS output active "H"
S-8244AAVPH-CEVTFG	4.275 ± 0.025 V	0.045 ± 0.02 V	CMOS output active "H"
S-8244AAYPH-CEYTFG	4.300 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244AAZPH-CEZTFG	4.280 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244ABBPH-CFBTFG	4.380 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244ABDPH-CFDTFG	4.150 ± 0.025 V	0.045 ± 0.02 V	CMOS output active "L"
S-8244ABEPH-CFETFG	4.215 ± 0.025 V	0 V	Nch open drain active "L"
S-8244ABHPH-CFHTFG	4.280 ± 0.025 V	0.045 ± 0.02 V	CMOS output active "H"

Remark   Please contact our sales office for the products with the detection voltage value other than those specified above.

(2) 8-Pin MSOP

Table 2

Product name/Item	Overcharge detection voltage [V_{CU}]	Overcharge hysteresis voltage [V_{CD}]	Output form
S-8244AAAFN-CEAT2G	4.450 ± 0.025 V	0.38 ± 0.1 V	CMOS output active "H"
S-8244AABFN-CEBT2G	4.200 ± 0.025 V	0 V	Nch open drain active "H"
S-8244AACFN-CECT2G	4.115 ± 0.025 V	0.13 ± 0.04 V	CMOS output active "H"
S-8244AADFN-CEDT2G	4.200 ± 0.025 V	0 V	Pch open drain active "L"
S-8244AAEFN-CEET2G	4.225 ± 0.025 V	0 V	Nch open drain active "H"
S-8244AAFFN-CEFT2G	4.350 ± 0.025 V	0.045 ± 0.02 V	CMOS output active "H"
S-8244AAGFN-CEGT2G	4.450 ± 0.025 V	0.045 ± 0.02 V	CMOS output active "H"
S-8244AAHFN-CEHT2G	4.300 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244AAIFN-CEIT2G	4.400 ± 0.025 V	0.045 ± 0.02 V	CMOS output active "H"
S-8244AAJFN-CEJT2G	4.500 ± 0.025 V	0.38 ± 0.1 V	CMOS output active "H"
S-8244AAKFN-CEKT2G	4.475 ± 0.025 V	0.38 ± 0.1 V	CMOS output active "H"
S-8244AALFN-CELT2G	4.350 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244AAMFN-CEMT2G	4.300 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "L"
S-8244AANFN-CENT2G	4.150 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244AAOFN-CEOT2G	4.250 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244AAPFN-CEPT2G	4.050 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244AAQFN-CEQT2G	4.150 ± 0.025 V	0 V	Nch open drain active "H"
S-8244AARFN-CERT2G	4.300 ± 0.025 V	0.25 ± 0.07 V	Nch open drain active "H"
S-8244AATFN-CETT2G	4.200 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244AAUFN-CEUT2G	3.825 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244AAWFN-CEWT2G	4.500 ± 0.025 V	0.38 ± 0.1 V	CMOS output active "L"
S-8244AAXFN-CEXT2G	4.025 ± 0.025 V	0.25 ± 0.07 V	CMOS output active "H"
S-8244ABAFN-CFAT2G	4.220 ± 0.025 V	0.045 ± 0.02 V	CMOS output active "H"
S-8244ABGFN-CFGT2S	4.225 ± 0.025 V	0.045 ± 0.02 V	Nch open drain active "L"
S-8244ABIFN-CFIT2S	4.100 ± 0.025 V	0 V	Nch open drain active "L"
S-8244ABJFN-CFJT2S	4.325 ± 0.025 V	0.045 ± 0.02 V	Nch open drain active "L"
S-8244ABKFN-CFKT2S	4.175 ± 0.025 V	0 V	Nch open drain active "L"

Remark   Please contact our sales office for the products with the detection voltage value other than those specified above.
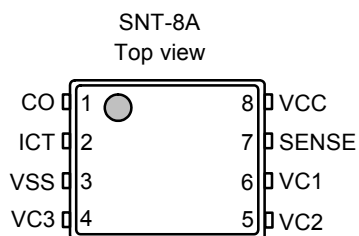
■ Pin Configurations

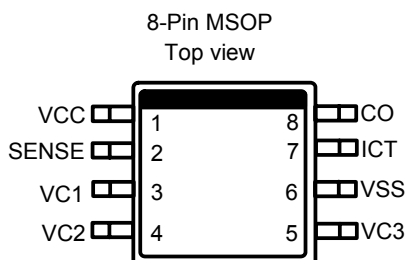SNT-8A
Top view

CO ▯1 ⬤   8 ▯ VCC
ICT ▯2   7 ▯ SENSE
VSS ▯3   6 ▯ VC1
VC3 ▯4   5 ▯ VC2

Figure 2

Table 3

Pin No.	Symbol	Description
1	CO	FET gate connection pin for charge control
2	ICT	Capacitor connection pin for overcharge detection delay
3	VSS	Input pin for negative power supply, Connection pin for battery 4's negative voltage
4	VC3	Connection pin for battery 3's negative voltage, Connection pin for battery 4's positive voltage
5	VC2	Connection pin for battery 2's negative voltage, Connection pin for battery 3's positive voltage
6	VC1	Connection pin for battery 1's negative voltage, Connection pin for battery 2's positive voltage
7	SENSE	Connection pin for battery 1's positive voltage
8	VCC	Input pin for positive power supply

8-Pin MSOP
Top view

VCC ▭   1   8   ▭ CO
SENSE ▭   2   7   ▭ ICT
VC1 ▭   3   6   ▭ VSS
VC2 ▭   4   5   ▭ VC3

Figure 3

Table 4

Pin No.	Symbol	Description
1	VCC	Input pin for positive power supply
2	SENSE	Connection pin for battery 1's positive voltage
3	VC1	Connection pin for battery 1's negative voltage, Connection pin for battery 2's positive voltage
4	VC2	Connection pin for battery 2's negative voltage, Connection pin for battery 3's positive voltage
5	VC3	Connection pin for battery 3's negative voltage, Connection pin for battery 4's positive voltage
6	VSS	Input pin for negative power supply, Connection pin for battery 4's negative voltage
7	ICT	Capacitor connection pin for overcharge detection delay
8	CO	FET gate connection pin for charge control

■ Absolute Maximum Ratings

Table 5

(Ta = 25°C unless otherwise specified)

Item		Symbol	Applied pin	Rating	Unit
Input voltage between VCC and VSS		V_{DS}	VCC	V_{SS}−0.3 to V_{SS}+26	V
Delay capacitor connection pin voltage		V_{ICT}	ICT	V_{SS} −0.3 to V_{CC} +0.3	V
Input pin voltage		V_{IN}	SENSE, VC1, VC2, VC3	V_{SS} −0.3 to V_{CC} +0.3	V
CO output pin voltage	(CMOS output)	V_{CO}	CO	V_{SS} −0.3 to V_{CC} +0.3	V
	(Nch open drain output)			V_{SS} −0.3 to 26	V
	(Pch open drain output)			V_{CC} −26 to V_{CC} +0.3	V
Power dissipation	SNT-8A	P_D	—	450[*1]	mW
	8-Pin MSOP			500[*1]	mW
Operating ambient temperature		T_{opr}	—	−40 to +85	°C
Storage temperature		T_{stg}	—	−40 to +125	°C

*1. When mounted on board

   [Mounted board]

   (1) Board size :   114.3 mm × 76.2 mm × t1.6 mm

   (2) Name :   JEDEC STANDARD51-7

Caution   **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**
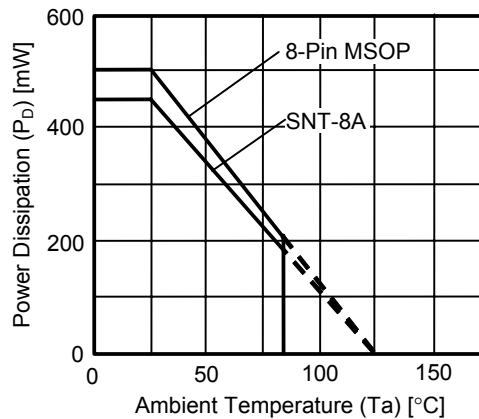
Figure 4   Power Dissipation of Package (When Mounted on Board)

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■ Electrical Characteristics

Table 6

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test conditions	Test circuit
DETECTION VOLTAGE								
Overcharge detection voltage 1 [*1]	V_{CU1}	3.7 V to 4.5 V Adjustment	V_{CU1} −0.025	V_{CU1}	V_{CU1} +0.025	V	1	1
Overcharge detection voltage 2 [*1]	V_{CU2}	3.7 V to 4.5 V Adjustment	V_{CU2} −0.025	V_{CU2}	V_{CU2} +0.025	V	2	1
Overcharge detection voltage 3 [*1]	V_{CU3}	3.7 V to 4.5 V Adjustment	V_{CU3} −0.025	V_{CU3}	V_{CU3} +0.025	V	3	1
Overcharge detection voltage 4 [*1]	V_{CU4}	3.7 V to 4.5 V Adjustment	V_{CU4} −0.025	V_{CU4}	V_{CU4} +0.025	V	4	1
Overcharge hysteresis voltage 1 [*2]	V_{CD1}	—	0.28	0.38	0.48	V	1	1
Overcharge hysteresis voltage 2 [*2]	V_{CD2}	—	0.28	0.38	0.48	V	2	1
Overcharge hysteresis voltage 3 [*2]	V_{CD3}	—	0.28	0.38	0.48	V	3	1
Overcharge hysteresis voltage 4 [*2]	V_{CD4}	—	0.28	0.38	0.48	V	4	1
Detection voltage temperature coefficient [*3]	T_{COE}	Ta = −40°C to +85°C[*4]	−0.4	0.0	+0.4	mV/°C	—	—
DELAY TIME								
Overcharge detection delay time	t_{CU}	C = 0.1 μF	1.0	1.5	2.0	s	5	2
OPERATING VOLTAGE								
Operating voltage between VCC and VSS [*5]	V_{DSOP}	—	3.6	—	24	V	—	—
CURRENT CONSUMPTION								
Current consumption during normal operation	I_{OPE}	V1 = V2 = V3 = V4 = 3.5 V	—	1.5	3.0	μA	6	3
Current consumption at power down	I_{PDN}	V1 = V2 = V3 = V4 = 2.3 V	—	1.2	2.4	μA	6	3
VC1 sink current	I_{VC1}	V1 = V2 = V3 = V4 = 3.5 V	−0.3	—	0.3	μA	6	3
VC2 sink current	I_{VC2}	V1 = V2 = V3 = V4 = 3.5 V	−0.3	—	0.3	μA	6	3
VC3 sink current	I_{VC3}	V1 = V2 = V3 = V4 = 3.5 V	−0.3	—	0.3	μA	6	3
OUTPUT VOLTAGE[*6]								
CO "H" voltage	$V_{CO(H)}$	at I_{OUT} = 10 μA	V_{CC} −0.05	—	—	V	7	4
CO "L" voltage	$V_{CO(L)}$	at I_{OUT} = 10 μA	—	—	V_{SS} +0.05	V	7	4

*1. ± 50 mV when Ta = −40°C to +85°C.

*2. 0.25 ± 0.07 V, 0.13 ± 0.04 V, 0.045 ± 0.02 V except for 0.38 V hysteresis models.

*3. Overcharge detection voltage or overcharge hysteresis voltage.

*4. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

*5. After detecting the overcharge, the delay circuit operates normally in the range of operating voltage.

*6. Output logic and CMOS or open drain output can be selected.

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■ Test Circuits

(1) Test Condition 1, Test Circuit 1

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active "H", Nch open drain output active "H"

The overcharge detection voltage 1 (V_{CU1}) is a voltage at V1; when the CO pin's voltage is set to "H" by increasing V1 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V1's voltage to set CO = "L", and the difference of this V1's voltage and V_{CU1} is the overcharge hysteresis voltage 1 (V_{CD1}).

- Product with CMOS output active "L", Nch open drain output active "L", Pch open drain output active "L"

The overcharge detection voltage 1 (V_{CU1}) is a voltage at V1; when the CO pin's voltage is set to "L" by increasing V1 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V1's voltage to set CO = "H", and the difference of this V1's voltage and V_{CU1} is the overcharge hysteresis voltage 1 (V_{CD1}).

(2) Test Condition 2, Test Circuit 1

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active "H", Nch open drain output active "H"

The overcharge detection voltage 2 (V_{CU2}) is a voltage at V2; when the CO pin's voltage is set to "H" by increasing V2 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V2's voltage to set CO = "L", and the difference of this V2's voltage and V_{CU2} is the overcharge hysteresis voltage 2 (V_{CD2}).

- Product with CMOS output active "L", Nch open drain output active "L", Pch open drain output active "L"

The overcharge detection voltage 2 (V_{CU2}) is a voltage at V2; when the CO pin's voltage is set to "L" by increasing V2 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V2's voltage to set CO = "H", and the difference of this V2's voltage and V_{CU2} is the overcharge hysteresis voltage 2 (V_{CD2}).

(3) Test Condition 3, Test Circuit 1

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active "H", Nch open drain output active "H"

The overcharge detection voltage 3 (V_{CU3}) is a voltage at V3; when the CO pin's voltage is set to "H" by increasing V3 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V3's voltage to set CO = "L", and the difference of this V3's voltage and V_{CU3} is the overcharge hysteresis voltage 3 (V_{CD3}).

- Product with CMOS output active "L", Nch open drain output active "L", Pch open drain output active "L"

The overcharge detection voltage 3 (V_{CU3}) is a voltage at V3; when the CO pin's voltage is set to "L" by increasing V3 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V3's voltage to set CO = "H", and the difference of this V3's voltage and V_{CU3} is the overcharge hysteresis voltage 3 (V_{CD3}).

(4) Test Condition 4, Test Circuit 1

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active "H", Nch open drain output active "H"

  The overcharge detection voltage 4 (V_{CU4}) is a voltage at V4; when the CO pin's voltage is set to "H" by increasing V4 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V4's voltage to set CO = "L", and the difference of this V4's voltage and V_{CU4} is the overcharge hysteresis voltage 4 (V_{CD4}).

- Product with CMOS output active "L", Nch open drain output active "L", Pch open drain output active "L"

  The overcharge detection voltage 4 (V_{CU4}) is a voltage at V4; when the CO pin's voltage is set to "L" by increasing V4 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V4's voltage to set CO = "H", and the difference of this V4's voltage and V_{CU4} is the overcharge hysteresis voltage 4 (V_{CD4}).

(5) Test Condition 5, Test Circuit 2

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active "H", Nch open drain output active "H"

  Rise V1 to 4.7 V momentarily within 10 µs after setting V1 = V2 = V3 = V4 = 3.5 V. The period from V1 having reached 4.7 V to CO = "H" is the overcharge detection delay time (t_{CU}).

- Product with CMOS output active "L", Nch open drain output active "L", Pch open drain output active "L"

  Rise V1 to 4.7 V momentarily within 10 µs after setting V1 = V2 = V3 = V4 = 3.5 V. The period from V1 having reached 4.7 V to CO = "L" is the overcharge detection delay time (t_{CU}).

(6) Test Condition 6, Test Circuit 3

Measure current consumption (I1) setting V1 = V2 = V3 = V4 = 2.3 V. This I1 is current consumption at power-down (I_{PDN}).
Measure current consumption (I1) setting V1 = V2 = V3 = V4 = 3.5 V. This I1 is current consumption during normal operation (I_{OPE}), I2 is the VC1 sink current (I_{VC1}), I3 is the VC2 sink current (I_{VC2}), I4 is the VC3 sink current (I_{VC3}).

(7) Test Condition 7, Test Circuit 4

Measure setting switch 1 to OFF and switch 2 to ON.
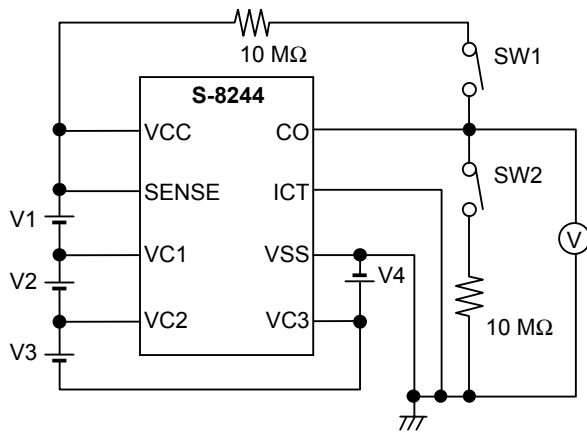
- Product with CMOS output active "H"

  Decrease V6 from V_{CC} gradually after setting V1 = V2 = V3 = V4 = 4.6 V, the V6's voltage when flowing I2 = −10 μA is the $V_{CO(H)}$ voltage.
 Increase V6 from 0 V gradually after setting V1 = V2 = V3 = V4 = 3.5 V, the V6's voltage when flowing I2 = 10 μA is the $V_{CO(L)}$ voltage.
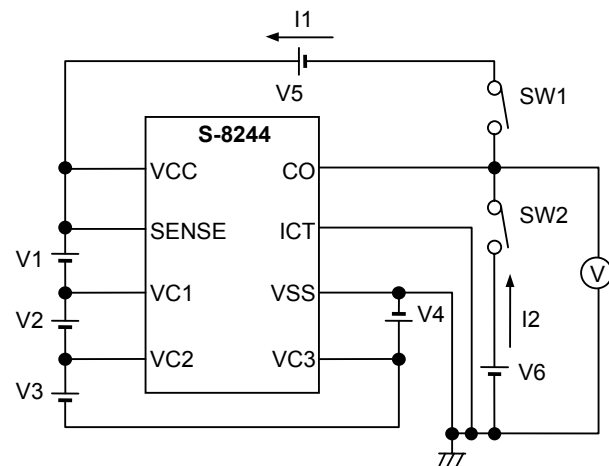
- Product with CMOS output active "L"

  Decrease V6 from V_{CC} gradually after setting V1 = V2 = V3 = V4 = 3.5 V, the V6's voltage when flowing I2 = −10 μA is the $V_{CO(H)}$ voltage.
  Increase V6 from 0 V gradually after setting V1 = V2 = V3 = V4 = 4.6 V, the V6's voltage when flowing I2 = 10 μA is the $V_{CO(L)}$ voltage.

- Product with Pch open drain output active "L"

  Decrease V6 from V_{CC} gradually after setting V1 = V2 = V3 = V4 = 3.5 V, the V6's voltage when flowing I2 = −10 μA is the $V_{CO(H)}$ voltage.

- Product with Nch open drain output active "H"

  Increase V6 from 0 V gradually after setting V1 = V2 = V3 = V4 = 3.5 V, the V6's voltage when flowing I2 = 10 μA is the $V_{CO(L)}$ voltage.

- Product with Nch open drain output active "L"

  Increase V6 from 0 V gradually after setting V1 = V2 = V3 = V4 = 4.6 V, the V6's voltage when flowing I2 = 10 μA is the $V_{CO(L)}$ voltage.

Test Circuit   1
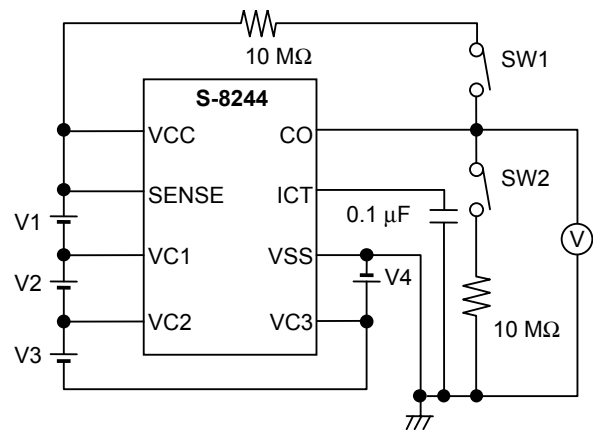
Test Circuit   2
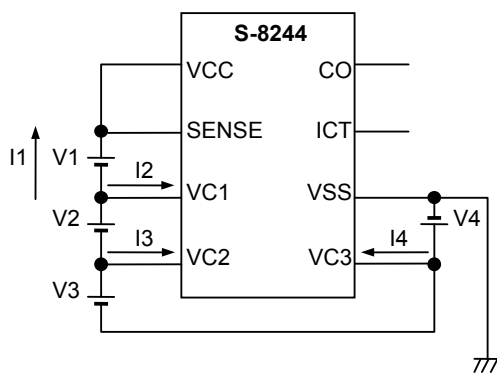
Test Circuit   3

Test Circuit   4

Figure 5

■ Operation

Remark Refer to " ■ **Battery Protection IC Connection Example**".

1. Overcharge Detection

- Product with CMOS output active "H", Nch open drain output active "H"

During charging in the normal status, any of battery voltages exceeds overcharge detection voltage (V_{CU}), and this status is maintained for overcharge detection delay time (t_{CU}) or longer, CO gets "H". This is overcharge status. Connecting an FET to the CO pin enables charge-control and the second protect.
In this case, the IC maintains the overcharge status until all battery voltages decreases, to the overcharge hysteresis voltage (V_{CD}) from the overcharge detection voltage (V_{CU}).

- Product with CMOS output active "L", Nch open drain output active "L", Pch open drain output active "L"

During charging in the normal status, any of battery voltages exceeds overcharge detection voltage (V_{CU}), and this status is maintained for overcharge detection delay time (t_{CU}) or longer, CO gets "L". This is overcharge status. Connecting an FET to the CO pin enables charge-control and the second protect.
In this case, the IC maintains the overcharge status until all battery voltages decreases, to the overcharge hysteresis voltage (V_{CD}) from the overcharge detection voltage (V_{CU}).

2. Delay Circuit

The delay circuit rapidly charges the capacitor connected to the delay capacitor connection pin up to a specified voltage when the voltage of one of the batteries exceeds the overcharge detection voltage (V_{CU}).   Then, the delay circuit gradually discharges the capacitor at 100 nA and inverts the CO output when the voltage at the delay capacitor connection pin goes below a specified level.   Overcharge detection delay time (t_{CU}) varies depending upon the external capacitor.

Each delay time is calculated using the following equation.

$$\text{Min.} \quad \text{Typ.} \quad \text{Max.}$$
$$t_{CU}[s] = \text{Delay Coefficient } (10, \quad 15, \quad 20) \times C_{ICT} \, [\mu F]$$

Because the delay capacitor is rapidly charged, the smaller the capacitance, the larger the difference between the maximum voltage and the specified value of delay capacitor pin (ICT pin).   This will cause a deviation between the calculated delay time and the resultant delay time.   Also, delay time is internally set in this IC to prevent the CO output from inverting until the charge to delay capacitor pin is reached to the specified voltage.   If large capacitance is used, output may be enabled without delay time because charge is disabled within the internal delay time.
Please note that the maximum capacitance connected to the delay capacitor pin (ICT pin) is 1 μF.
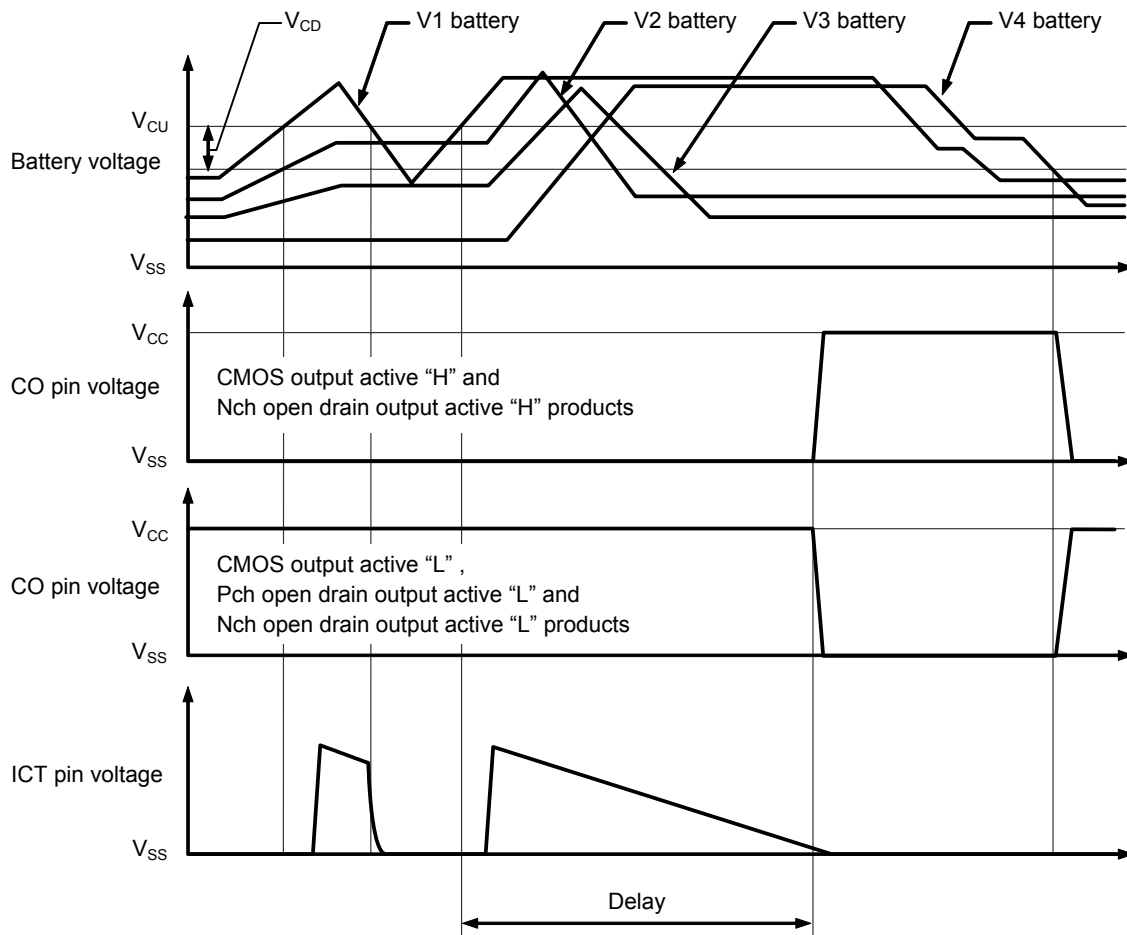
■ Timing Chart

Figure 6

■ Battery Protection IC Connection Example
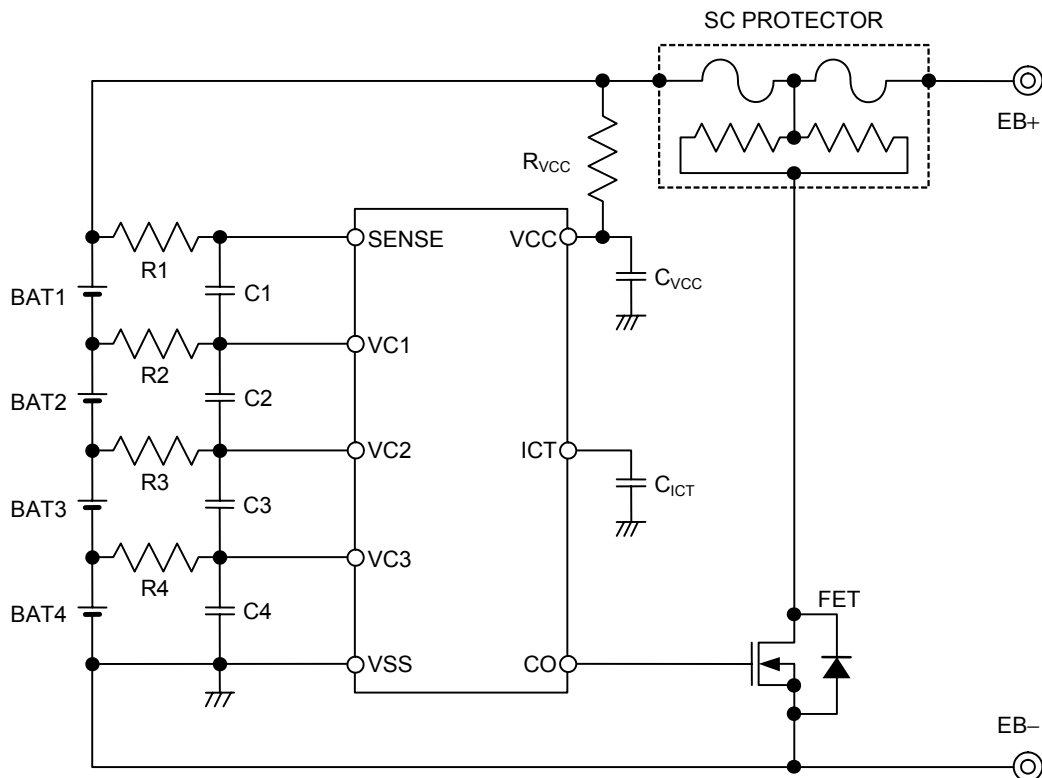
(1)   Connection Example 1

Figure 7

Table 7   Constants for External Components 1

Symbol	Min.	Typ.	Max.	Unit
R1 to R4	0	1 k	10 k	Ω
C1 to C4	0	0.1	1	μF
R_{VCC}	0	100	1 k	Ω
C_{VCC}	0	0.1	1	μF
C_{ICT}	0	0.1	1	μF

Caution1.   The above constants may be changed without notice.
  2.   It has not been confirmed whether the operation is normal or not in circuits other than the above
       example of connection.   In addition, the example of connection shown above and the constant
       do not guarantee proper operation. Perform through evaluation using the actual application to set
       the constant.
  3.   In the case of Nch open drain output, pull up CO pin by external resistor.

[For SC PROTECTOR, contact]
 Sony Chemical & Information Device Corporation, Electronic Device Marketing & Sales Dept.
  Gate City Osaki East Tower 8F, 1-11-2
  Osaki, Shinagawa-ku, Tokyo, 141-0032 Japan
  TEL +81-3-5435-3943
  Contact Us: http://www.sonycid.jp/en/

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(2) Connection Example 2
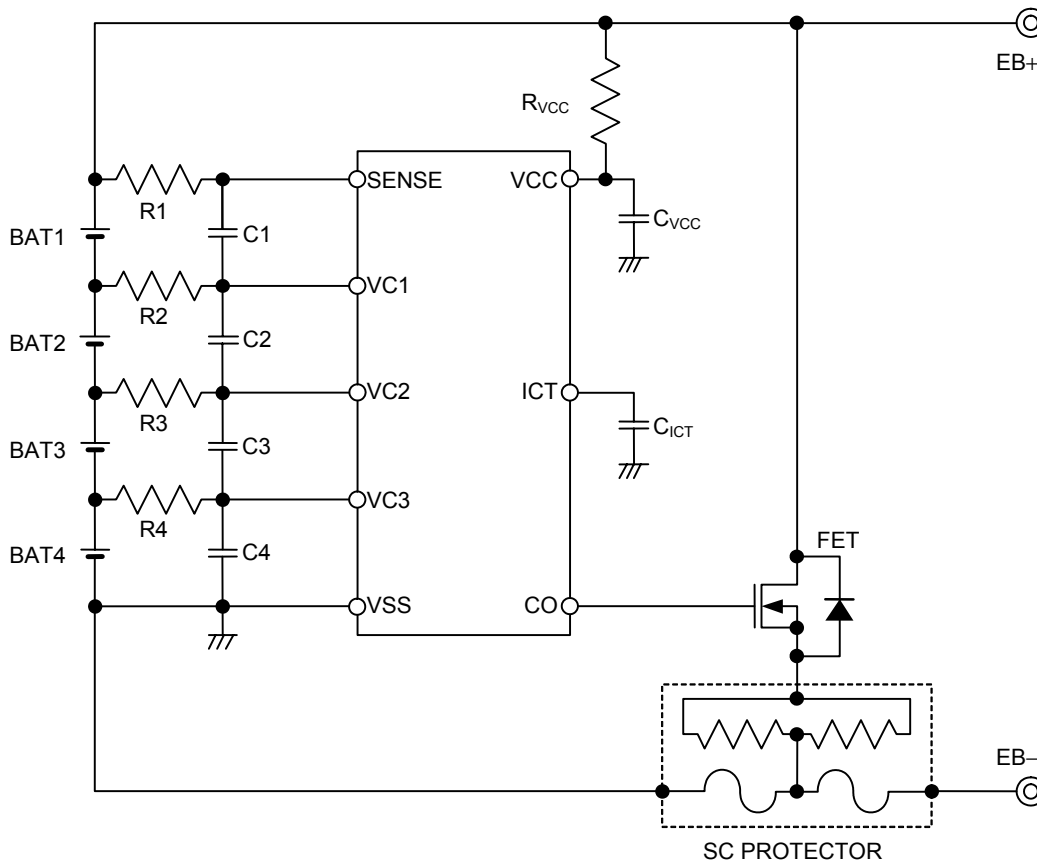
Figure 8

Table 8   Constants for External Components 2

Symbol	Min.	Typ.	Max.	Unit
R1 to R4	0	1 k	10 k	Ω
C1 to C4	0	0.1	1	μF
R_{VCC}	0	100	1 k	Ω
C_{VCC}	0	0.1	1	μF
C_{ICT}	0	0.1	1	μF

Caution1. The above constants may be changed without notice.
       2. It has not been confirmed whether the operation is normal or not in circuits other than the above
           example of connection.   In addition, the example of connection shown above and the constant
           do not guarantee proper operation. Perform through evaluation using the actual application to
           set the constant.
       3. In the case of Nch open drain output, pull up CO pin by external resistor.

(3)   Connection Example 3 (for 3-cells)
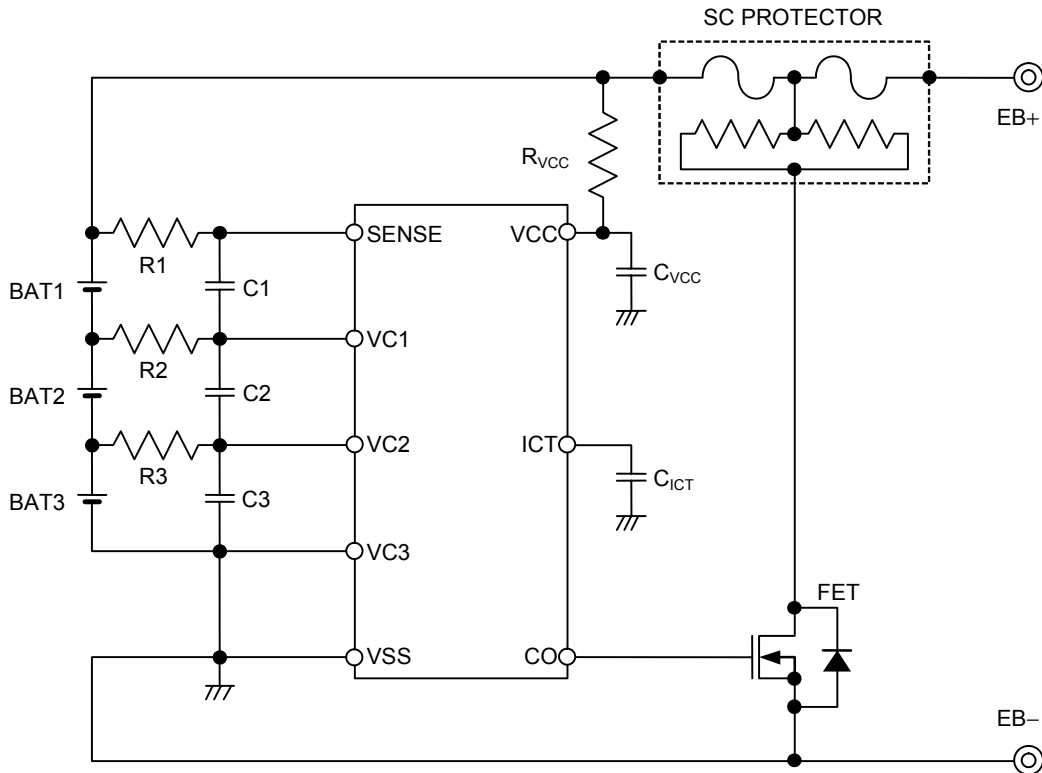

Figure 9

Table 9   Constants for External Components 3

Symbol	Min.	Typ.	Max.	Unit
R1 to R3	0	1 k	10 k	Ω
C1 to C3	0	0.1	1	μF
R_{VCC}	0	100	1 k	Ω
C_{VCC}	0	0.1	1	μF
C_{ICT}	0	0.1	1	μF

Caution1. The above constants may be changed without notice.
      2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection.   In addition, the example of connection shown above and the constant do   not guarantee proper operation. Perform through evaluation using the actual application to set the constant.
      3. In the case of Nch open drain output, pull up CO pin by external resistor.

(4) Connection Example 4 (for 2-cells)
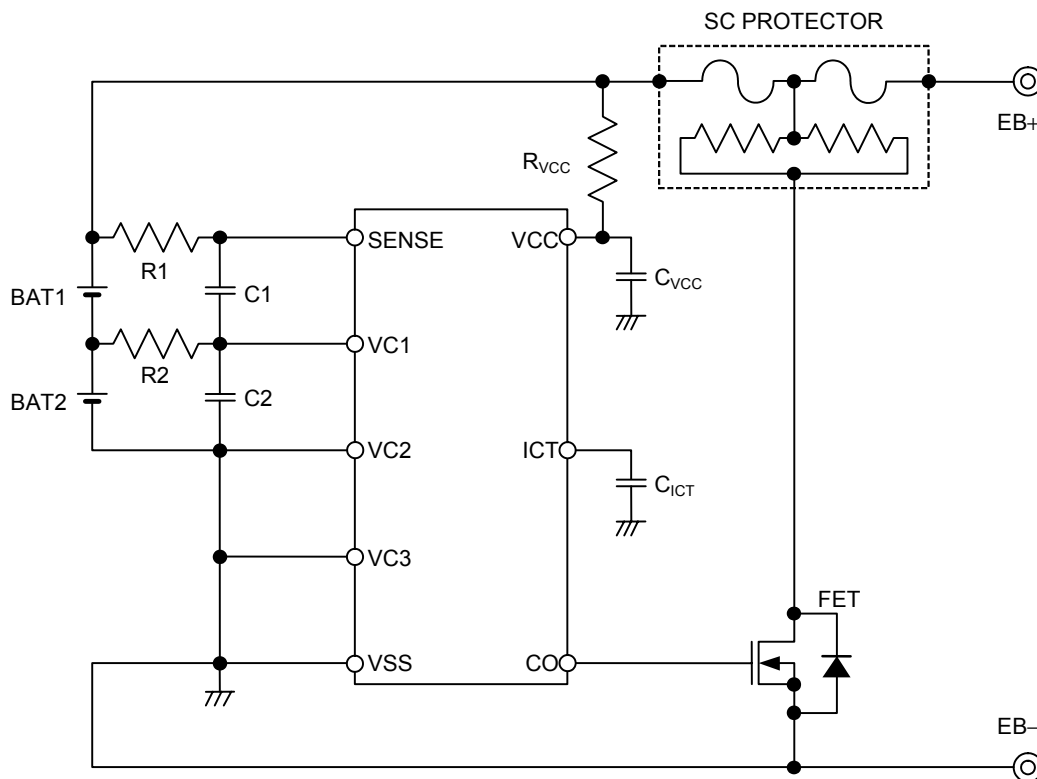
Figure 10

Table 10 Constants for External Components 4

Symbol	Min.	Typ.	Max.	Unit
R1, R2	0	1 k	10 k	Ω
C1, C2	0	0.1	1	μF
R_{VCC}	0	100	1 k	Ω
C_{VCC}	0	0.1	1	μF
C_{ICT}	0	0.1	1	μF

Caution1. **The above constants may be changed without notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform through evaluation using the actual application to set the constant.**
3. **In the case of Nch open drain output, pull up CO pin by external resistor.**

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(5)   Connection Example 5 (for 1-cell)
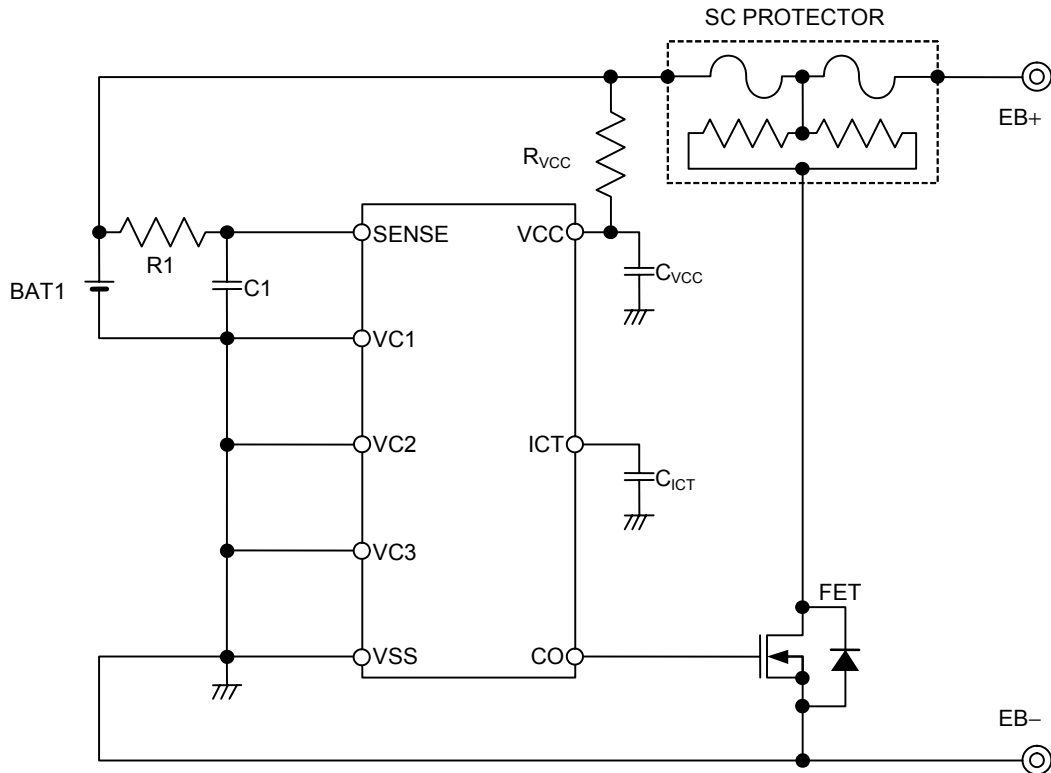
Figure 11

Table 11   Constants for External Components 5

Symbol	Min.	Typ.	Max.	Unit
R1	0	1 k	10 k	Ω
C1	0	0.1	1	µF
R_{VCC}	0	100	1 k	Ω
C_{VCC}	0	0.1	1	µF
C_{ICT}	0	0.1	1	µF

Caution1. The above constants may be changed without notice.
**   2. It has not been confirmed whether the operation is normal or not in circuits other than the above**
**   example of connection.   In addition, the example of connection shown above and the constant**
**   do not guarantee proper operation. Perform through evaluation using the actual application to set**
**   the constant.**
**   3. In the case of Nch open drain output, pull up CO pin by external resistor.**

■ Precautions

- This IC charges the delay capacitor through the delay capacitor pin (ICT pin) immediately when the voltage of one of batteries V1 to V4 reaches the overcharge voltage.   Therefore, setting the resistor connected to the VCC pin to any value greater than the recommended level causes a reduction in the IC power supply voltage because of charge current of the delay capacitor.   This may lead to a malfunction.   Set up the resistor NOT to exceed the typical value. If you change the resistance, please consult us.

- DO NOT connect any of overcharged batteries.   Even if only one overcharged battery is connected to this IC, the IC detects overcharge, then charge current flows to the delay capacitor through the parasitic diode between pins where the battery is not connected yet.   This may lead to a malfunction.   Please perform sufficient evaluation in the case of use.   Depending on an application circuit, even when the fault charge battery is not contained, the connection turn of a battery may be restricted in order to prevent the output of CO detection pulse at the time of battery connection.

CMOS output active "H" and Nch open drain output active "H" products
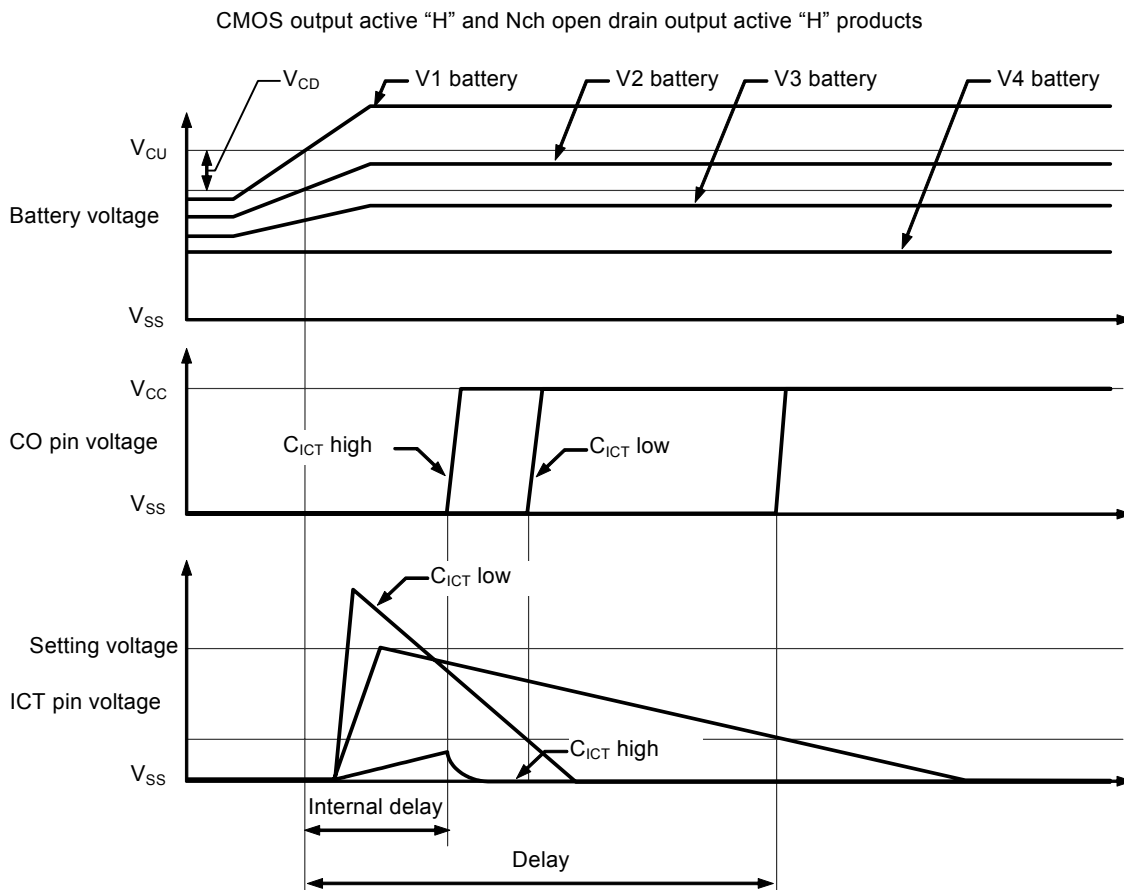
- In this IC, the output logic of the CO pin is inverted after several milliseconds of internal delay if this IC is under the overcharge condition even ICT pin is either "V_{SS}–short circuit," "V_{DD}–short circuit" or "Open" status.

- Any position from V1 to V4 can be used when applying this IC for a one to three-cell battery. However, be sure to short circuit between pins not in use (SENSE–VC1, VC1–VC2, VC2–VC3, or VC3–VSS).

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.
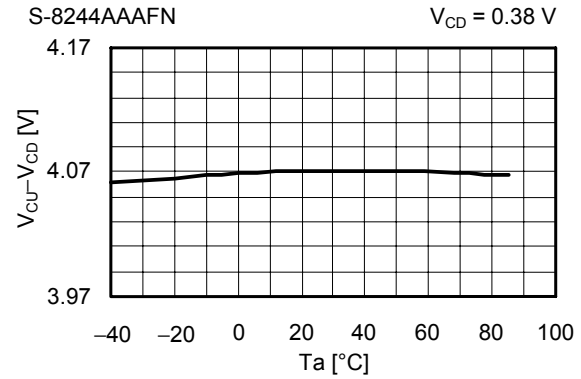
■ Characteristics (Typical Data)

1. Detection Voltage vs. Temperature

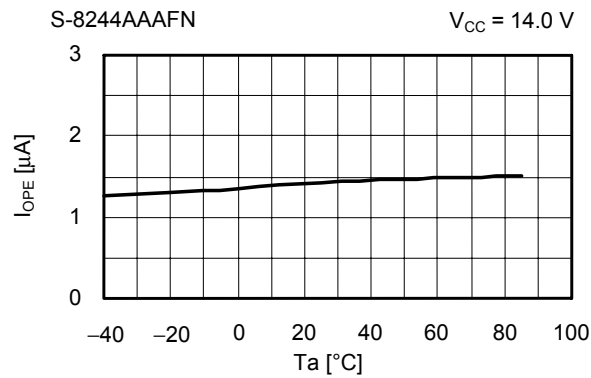Overcharge Detection Voltage vs. Temperature

S-8244AAAFN V_{CU} = 4.45 V
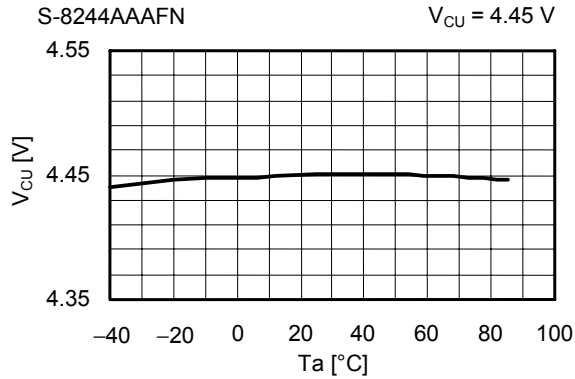
Overcharge Release Voltage vs. Temperature

S-8244AAAFN V_{CD} = 0.38 V

2. Current Consumption vs. Temperature

Current Consumption during Normal Operation vs. Temperature

S-8244AAAFN V_{CC} = 14.0 V

Current Consumption at Power Down vs. Temperature

S-8244AAAFN V_{CC} = 9.2 V
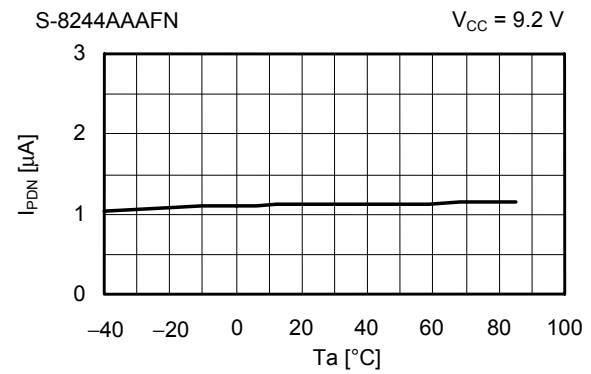
3. Delay Time vs. Temperature

Overcharge Detection Delay Time vs. Temperature

S-8244AAAFN V_{CC} = 15.2 V
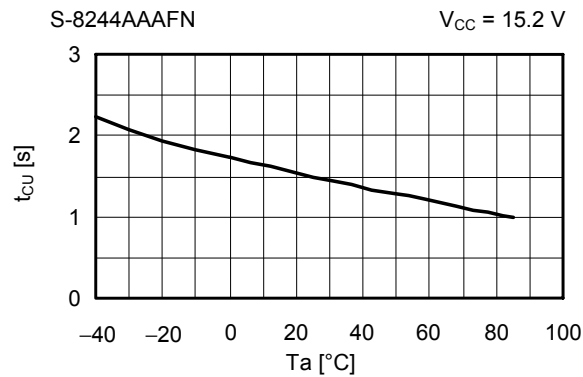
Caution   Please design all applications of the S-8244 Series with safety in mind.

1.97±0.03

8 7 6 5

(0.1)

1 2 3 4

0.5

2.23±0.04

2.46±0.03

(0.2)

(0.2)

$0.08 \, ^{+0.05}_{-0.02}$

0.48±0.02

0.2±0.05
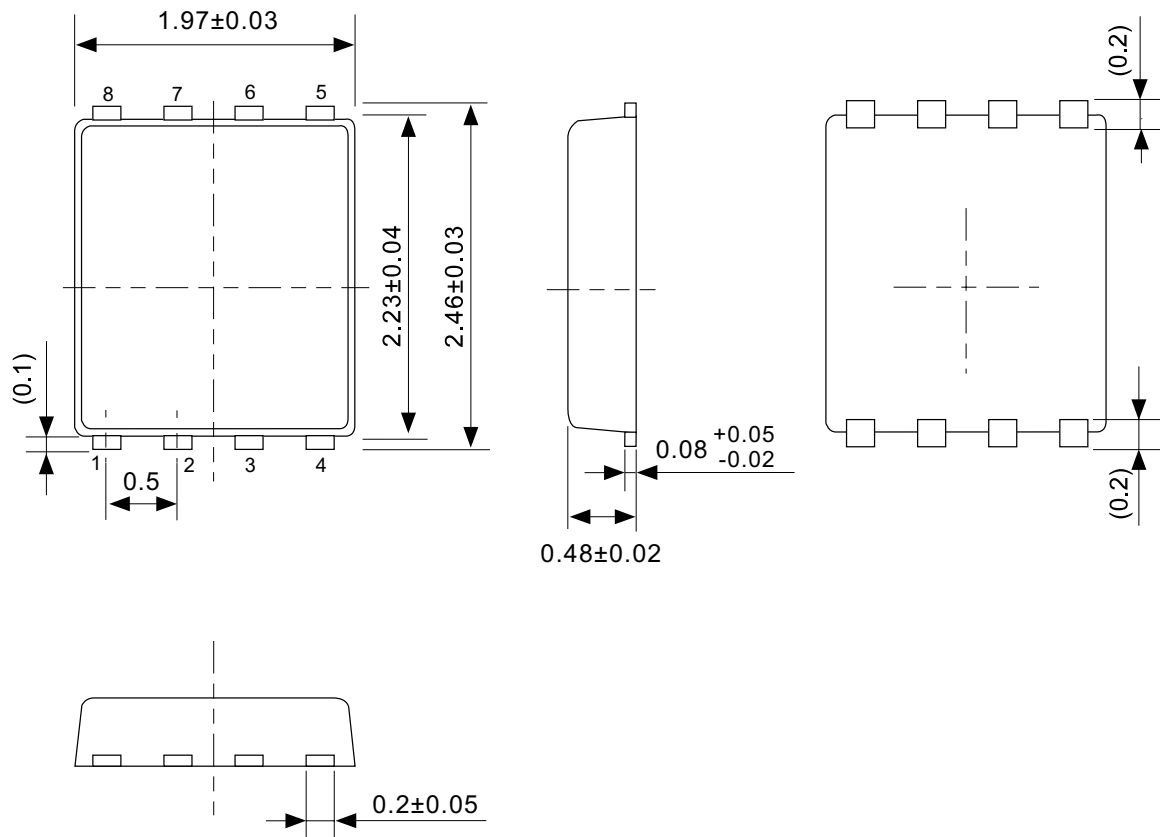
No. PH008-A-P-SD-2.0

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.0
SCALE	
UNIT	mm

Seiko Instruments Inc.

ø1.5 $^{+0.1}_{-0}$ 2.0±0.05   4.0±0.1   1.75±0.1   0.25±0.05

3.5±0.05   8.0±0.2   2.7±0.05

5°

0.65±0.05

ø0.5±0.1   4.0±0.1

2.25±0.05

5°
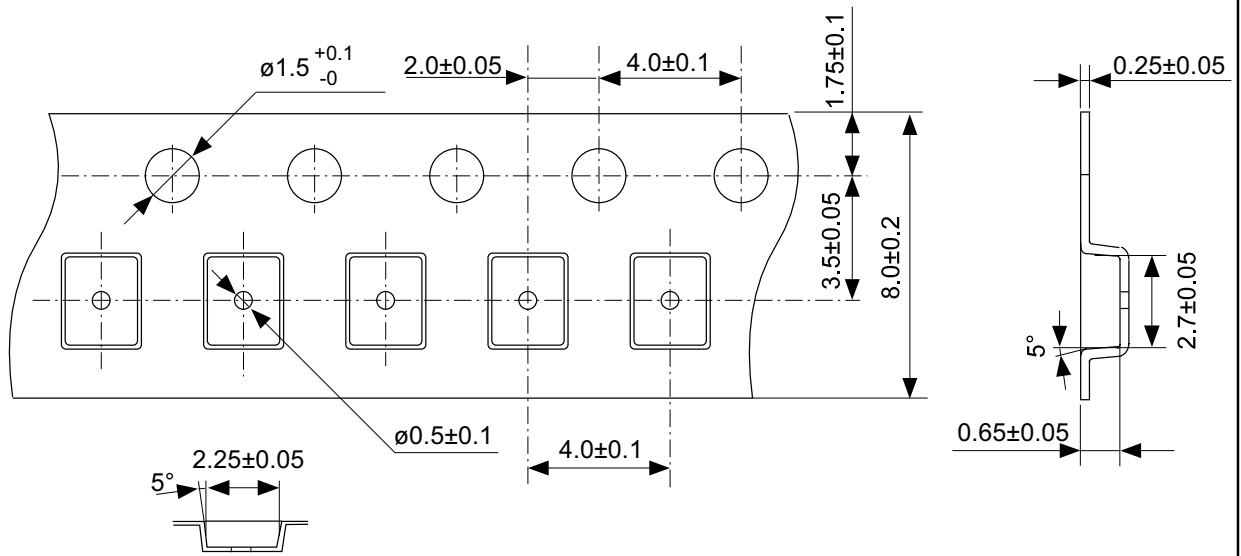
4 3 2 1

5 6 7 8
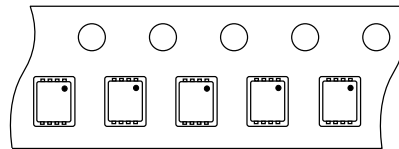
Feed direction

No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

12.5max.

$\phi 60 \; ^{+1}_{-0}$

$\phi 180 \; ^{+0}_{-3}$

9.0±0.3

Enlarged drawing in the central part

$\phi 21 \pm 0.5$

$\phi 13 \pm 0.2$

2±0.5

(60°) (60°)
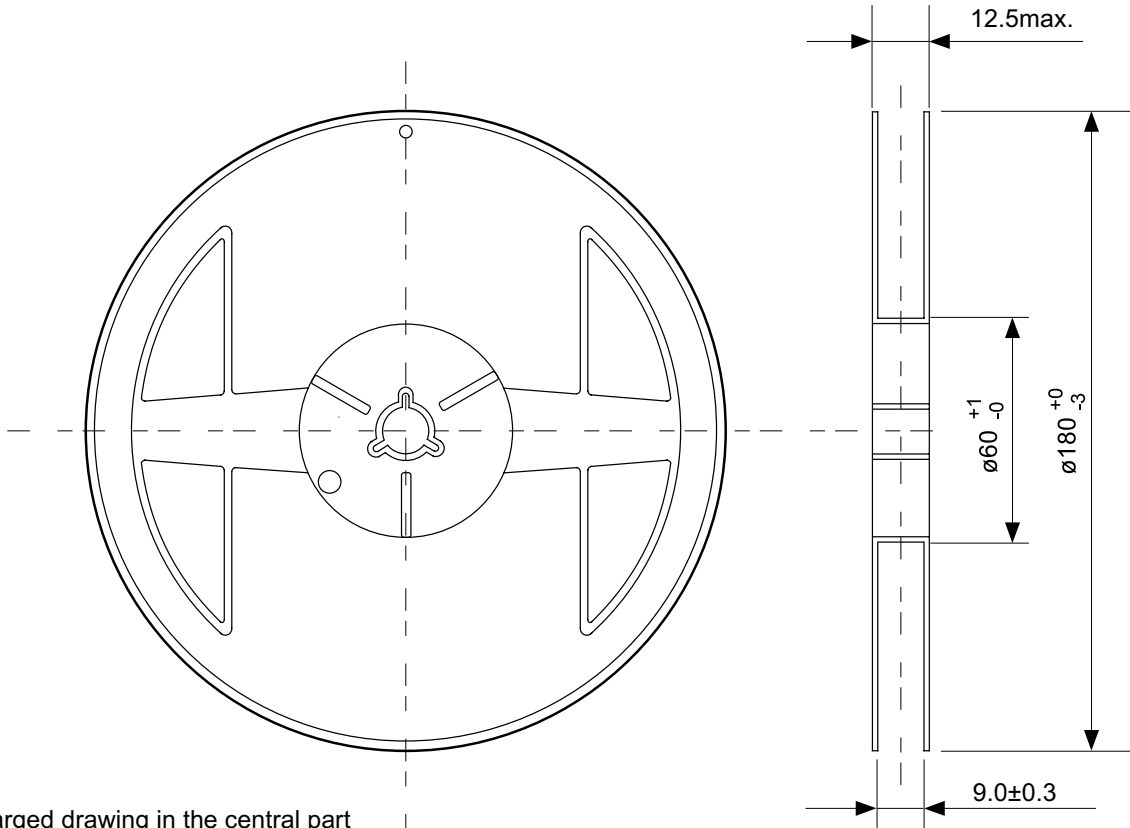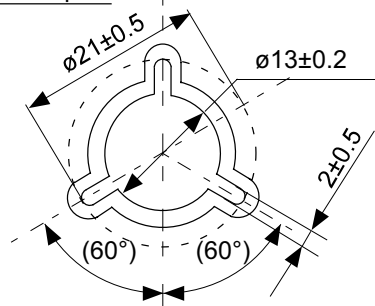
No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		

Seiko Instruments Inc.

0.52

2.01

0.52

0.3 0.2 0.3 0.2 0.3 0.2 0.3
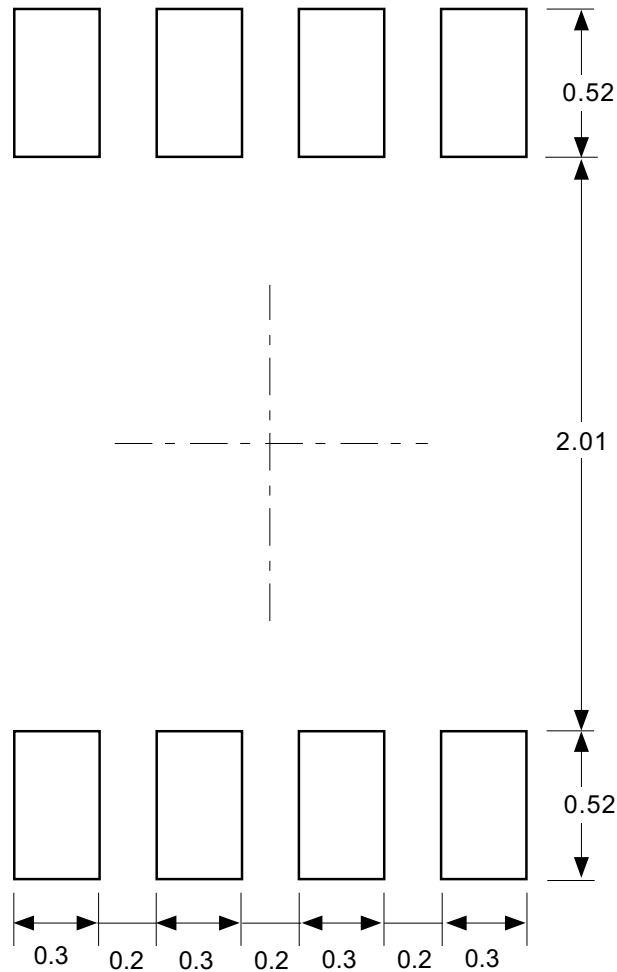
Caution   Making the wire pattern under the package is possible. However, note that the package
may be upraised due to the thickness made by the silk screen printing and of a solder
resist on the pattern because this package does not have the standoff.

注意　パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフ
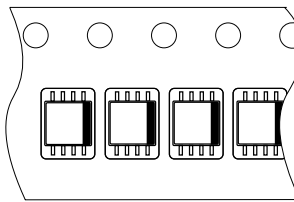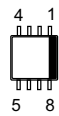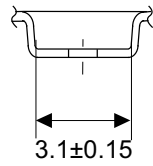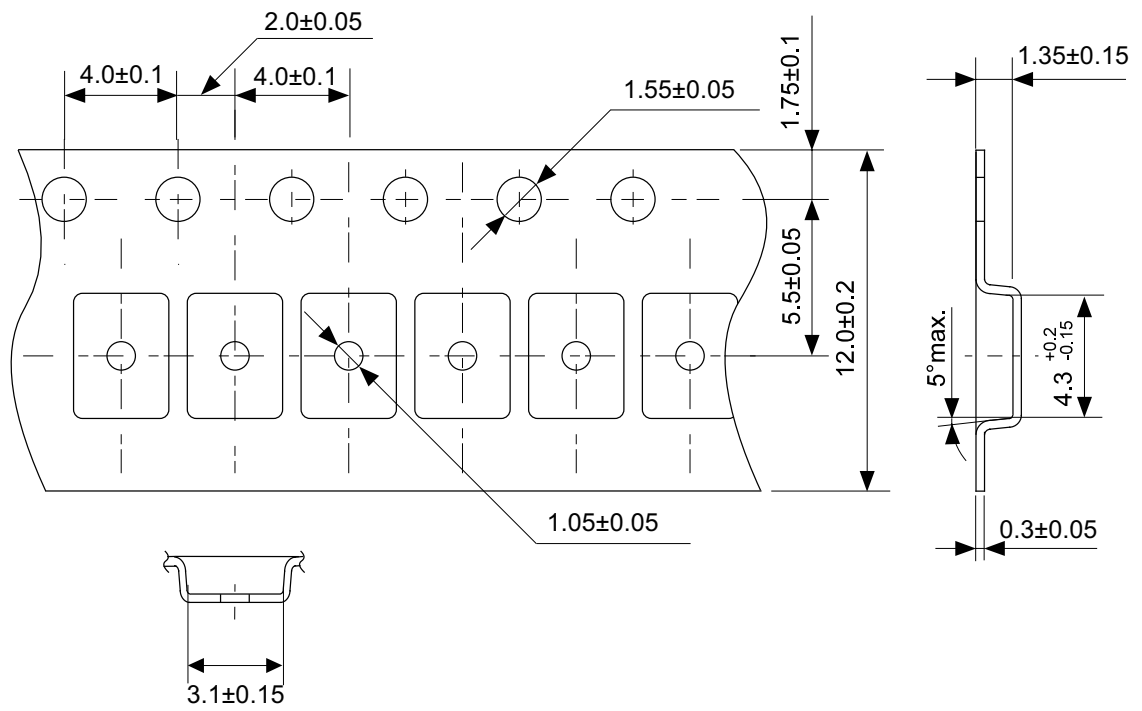が無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージ
が持ち上がることがありますのでご配慮ください。

No. PH008-A-L-SD-3.0

TITLE	SNT-8A-A-Land Recommendation
No.	PH008-A-L-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

2.95±0.2

8   5

2.8±0.2

4.0±0.3

1   4

0.45±0.2

0.13±0.1

1.1±0.1

1.3max.

0.2±0.1

0.65±0.1

$0.1 \, ^{+0.05}_{-0.10}$
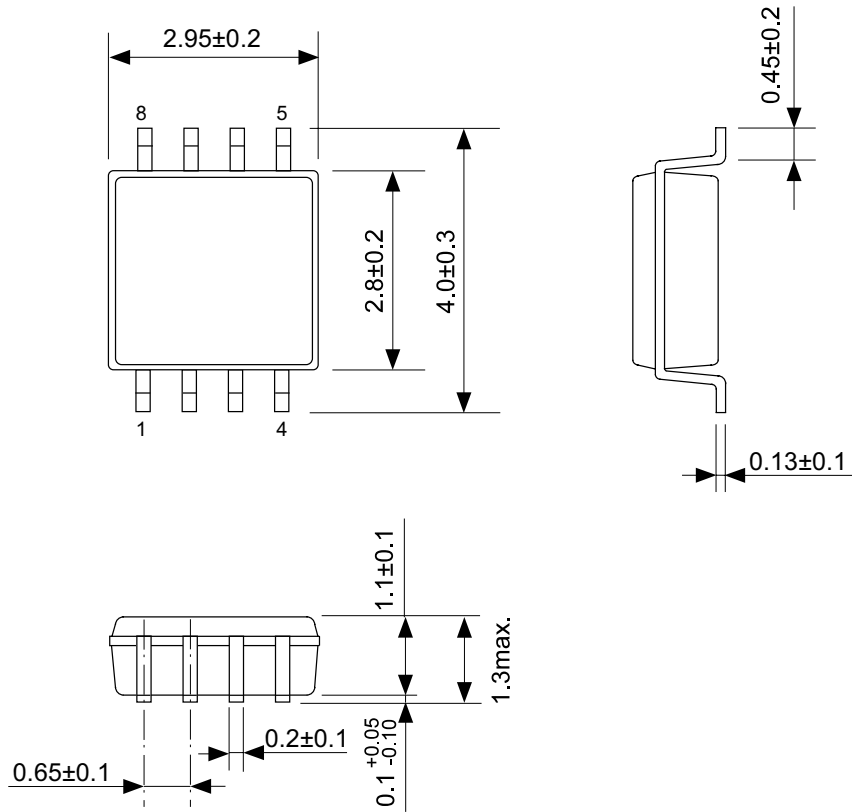
No. FN008-A-P-SD-1.1

TITLE	MSOP8-A-PKG Dimensions
No.	FN008-A-P-SD-1.1
SCALE	
UNIT	mm
	Seiko Instruments Inc.

2.0±0.05

4.0±0.1 4.0±0.1

1.55±0.05

1.75±0.1

1.35±0.15

5.5±0.05

12.0±0.2

5°max.

$4.3^{+0.2}_{-0.15}$

1.05±0.05

0.3±0.05

3.1±0.15

4   1

5   8

Feed direction

No. FN008-A-C-SD-1.1

TITLE	MSOP8-A-Carrier Tape
No.	FN008-A-C-SD-1.1
SCALE	
UNIT	mm
	Seiko Instruments Inc.

16.5max.

ø60 $^{+1}_{-0}$ ø180 $^{+0}_{-3}$

13.0±0.3

Enlarged drawing in the central part

21±0.5   13±0.2

2±0.2

(60°)   (60°)
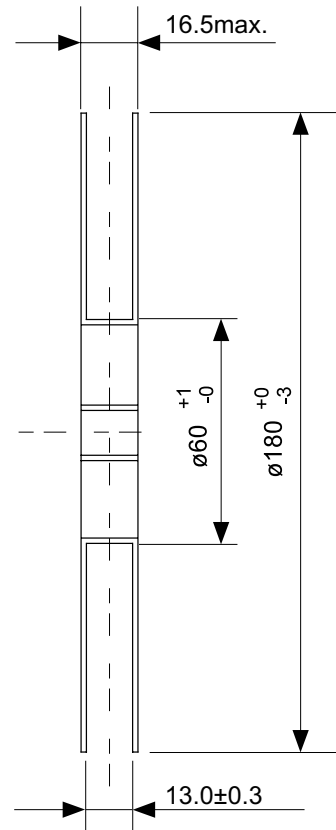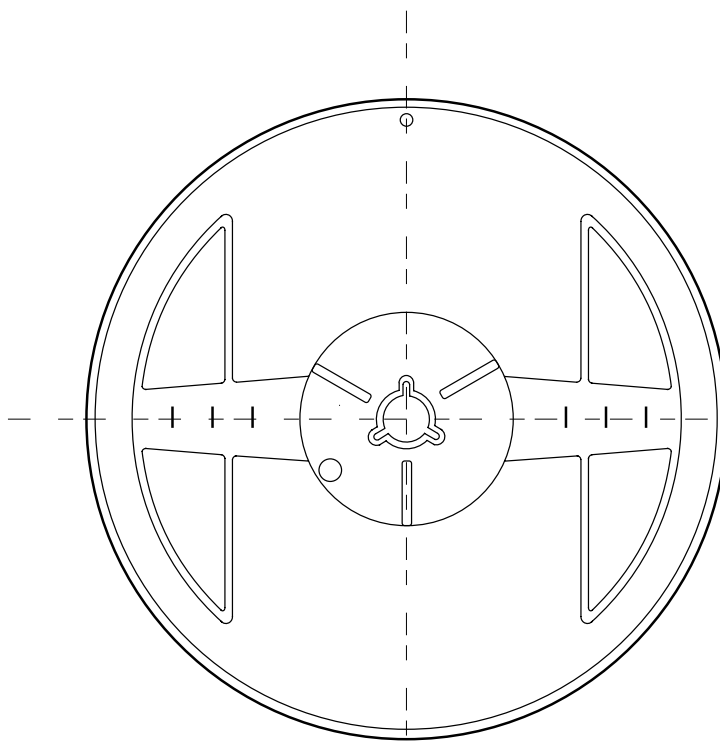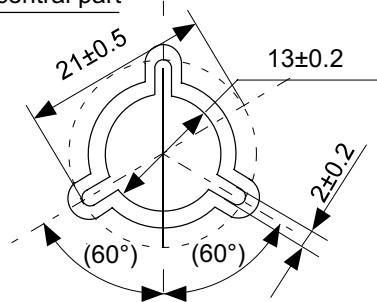
No. FN008-A-R-SD-1.1

TITLE	MSOP8-A-Reel		
No.	FN008-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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