Dual 800mA Step-Down Switching Regulator with Power-On Reset and Watchdog Timer

FEATURES

- **Wide Input Range: Operation from 3.8V to 36V**
- **Low Ripple (<25mV$_{P-P}$) Burst Mode Operation: I_Q = 115µA at 12V$_{IN}$ to 3.3V and 5V**
- **Programmable, Defeatable Window Watchdog Timer**
- **Two Independently Programmable Power-On-Reset Timers**
- **Synchronizable, Adjustable 350kHz-2.2MHz Switching Frequency**
- Two 800mA Output Switching Regulators with Internal Power Switches
- Programmable Input Undervoltage Lockout with Hysteresis
- Thermally Enhanced 24-Pin TSSOP and 4mm × 4mm QFN Packages

APPLICATIONS

- Automotive Electronic Control Units
- Industrial Power Supplies
- High-Reliability µProcessor Systems

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DESCRIPTION

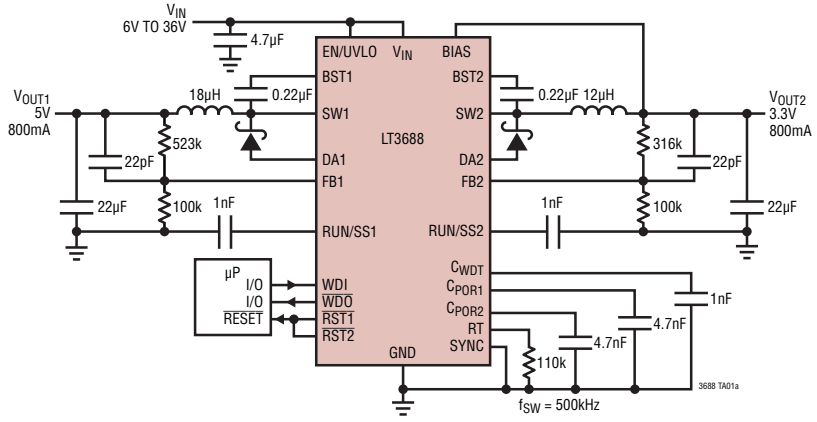
The LT®3688 is an adjustable frequency (350kHz to 2.2MHz) dual monolithic step-down switching regulator with two power-on reset timers and a watchdog timer. The regulator operates off inputs up to 36V. Low ripple Burst Mode® operation maintains high efficiency at low output current while keeping output ripple below 25mV in a typical application, with input quiescent current of just 115µA. Shutdown circuitry reduces input supply current to less than 1µA while EN/UVLO is pulled low.

The reset and watchdog timeout periods are both adjustable using external capacitors. Tight accuracy specifications and glitch immunity ensure reliable reset operation without false triggering. The open collector $\overline{RST}$ pins will pull down if the monitored output voltage drops 10% below the programmed value. The LT3688 watchdog timer monitors for watchdog falling edges grouped too close together or too far apart.

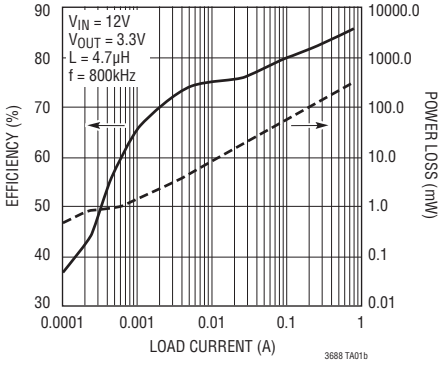
The LT3688 is available in 24-Pin TSSOP and 4mm × 4mm QFN packages, each with an exposed pad for low thermal resistance.

TYPICAL APPLICATION

5V and 3.3V Regulator with Power-On Reset and Watchdog Timers



Efficiency



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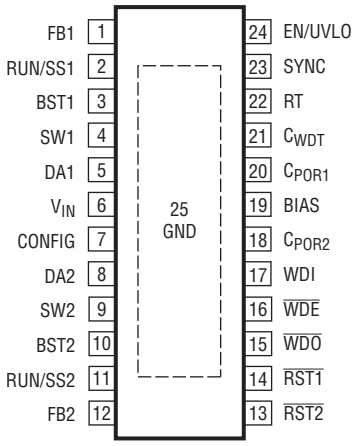
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO, CONFIG Voltage (Note 2).....36V
BST Voltage 55V
BST above SW Voltage 30V
BIAS Voltage.....30V
$\overline{WDE}$, WDI, $\overline{RST}$, $\overline{WDO}$ Voltage 6V
FB, RT, SYNC, RUN/SS Voltage 6V
C_{WDT}, C_{POR} Voltage 3V

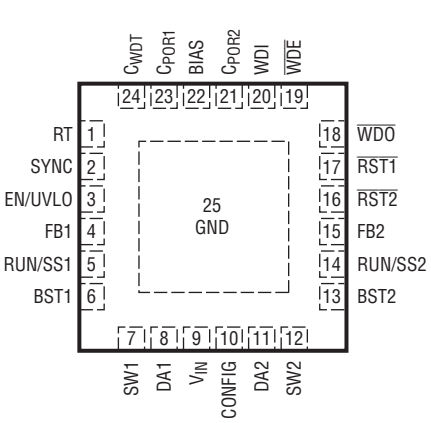
Operating Junction Temperature Range (Note 3)
LT3688E, LT3688I .....–40°C to 125°C
LT3688H .....–40°C to 150°C
Maximum Junction Temperature
LT3688E, LT3688I .....125°C
LT3688H .....150°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Package .....300°C

PIN CONFIGURATION



FE PACKAGE
24-LEAD PLASTIC TSSOP

θ_{JA} = 38°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE ELECTRICALLY CONNECTED TO PCB



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

θ_{JA} = 37°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE ELECTRICALLY CONNECTED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3688EFE#PBF	LT3688EFE#TRPBF	LT3688FE	24-Lead Plastic TSSOP	–40°C to 125°C
LT3688IFE#PBF	LT3688IFE#TRPBF	LT3688FE	24-Lead Plastic TSSOP	–40°C to 125°C
LT3688HFE#PBF	LT3688HFE#TRPBF	LT3688FE	24-Lead Plastic TSSOP	–40°C to 150°C
LT3688EUF#PBF	LT3688EUF#TRPBF	3688	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LT3688IUF#PBF	LT3688IUF#TRPBF	3688	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{IN} Undervoltage Lockout		●	3	3.5	3.8	V
	Quiescent Current from V_{IN}	$V_{EN/UVLO}$ = 0.3V V_{BIAS} = 5V, Not Switching V_{BIAS} = 0V, Not Switching	 ● 		0.01 65 235	1 105 310	µA µA µA
	Quiescent Current from BIAS	$V_{EN/UVLO}$ = 0.3V V_{BIAS} = 5V, Not Switching V_{BIAS} = 0V, Not Switching	 ● 		0.01 155 –5	1 200 –20	µA µA µA
	FB Voltage		 ●	0.790 0.784	0.800	0.810 0.814	V V
	FB Pin Bias Current	V_{FB} = 0.800V	●		–3	–50	nA
	FB Voltage Line Regulation	5V < V_{IN} < 36V			0.002		%/V
	Switching Frequency	R_T = 20k, V_{BST} = 12V R_T = 110k, V_{BST} = 12V	● ●	1.85 460	2.1 500	2.35 540	MHz kHz
	Minimum Off-Time (Note 4)	V_{BST} = 12V	●		115	180	ns
	Switch Current Limit (Note 5)	DC = 15%	●	1.2	1.7	2.2	A
	Switch V_{CESAT}	I_{SW} = 0.8A			280		mV
	Switch Leakage Current (Note 8)				–0.01	–1	µA
	DA Current Limit		●	0.9	1.2	1.6	A
	Boost Schottky Reverse Leakage	V_{BIAS} = 0V			0.01	2	µA
	Minimum BST Voltage above SW				2.15	2.5	V
	BST Pin Current	I_{SW} = 0.8A			15	25	mA
	EN/UVLO Threshold Voltage		●	1.15	1.25	1.35	V
	EN/UVLO Input Current	$V_{EN/UVLO}$ = 1.35V $V_{EN/UVLO}$ = 1.15V		 2.5	0.3 4	 6	µA µA
	Threshold Current Hysteresis			2.5	3.7	5.5	µA
	RUN/SS Pin Current	$V_{RUN/SS}$ = 0V		–1.4	–2.8	–4	µA
	RUN/SS Switching Threshold			0.15	0.8	1	V
	SYNC Threshold Voltage			0.4	0.8	1.3	V
V_{UV}	Reset Threshold	% of FB Voltage, V_{FB} Falling	●	88	90	92	%
t_{RST}	Reset Timeout Period	C_{POR} = 4700pF	●	21.2	23.5	25.8	ms
t_{WDU}	Watchdog Window Upper Boundary	C_{WDT} = 1000pF	●	18	20	22	ms
t_{WDL}	Watchdog Window Lower Boundary	C_{WDT} = 1000pF	●	0.8	1.25	1.6	ms
t_{WDTO}	Watchdog Timeout Period	C_{WDT} = 1000pF			2.5		ms
	$\overline{RST}$ Output Voltage Low	I_{SINK} = 2.5mA, V_{FB} = 0.6V I_{SINK} = 100µA, V_{FB} = 0.6V	● ●		0.2 0.01	0.4 0.3	V V
t_{UV}	UV Detect to $\overline{RST}$ Asserted	V_{FB} Set to 0.680V	●	4	10	30	µs
	WDI Input Threshold		●	0.4	0.95	1.3	V
	WDI Input Pull-Up Current				–2		µA
	WDI Input Pulse Width		●	300			ns
	$\overline{WDE}$ Threshold Voltage		●	0.4	0.65	1	V
	$\overline{WDE}$ Input Pull-Down Current	$V_{\overline{WDE}}$ = 1.2V			3.5		µA
	$\overline{WDO}$ Output Voltage Low	I_{SINK} = 2.5mA I_{SINK} = 100µA	● ●		0.2 0.01	0.4 0.3	V V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	$\overline{RST}$ Pull-Up Current (Note 6)			–1.5	–2.5		µA
	$\overline{WDO}$ Pull-Up Current (Note 6)			–1.5	–2.5		µA
	CONFIG Low Level Input Voltage		●			0.2	V
	CONFIG High Level Input Voltage		●	1.4			V
	CONFIG Pin Voltage When Open				0.64		V
	Maximum CONFIG Input Current in Open State		●			±1	µA
	CONFIG Pin Bias Current	V_{CONFIG} = 0V, V_{IN}	●			±20	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute Maximum Voltage at the V_{IN}, CONFIG and EN/UVLO pins is 36V for continuous operation.

Note 3: The LT3688 is tested under pulsed load conditions such that $T_J = T_A$. The LT3688E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3688I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3688H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (PD, in Watts) according to the formula:

$T_J = T_A + (PD\ \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 4: The LT3688 contains circuitry that extends the maximum duty cycle if the BST voltage is 2V greater than the SW voltage. See the Applications Information section for more details.

Note 5: Current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

Note 6: The outputs of $\overline{RST}$ and $\overline{WDO}$ have a weak pull-up to V_{BIAS} of typically 2.5µA. However, external pull-up resistors may be used when faster rise times are required or for V_{OH} higher than V_{BIAS}.

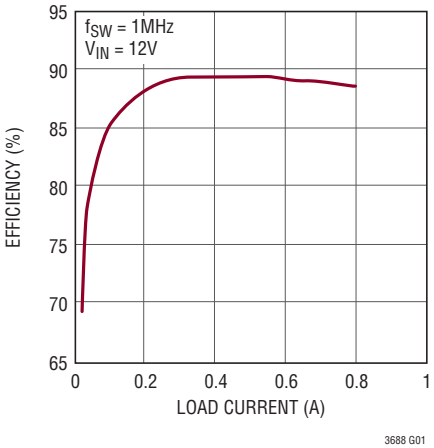
Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 8: All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

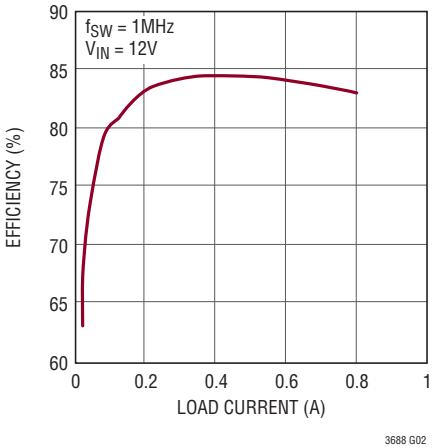
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted.

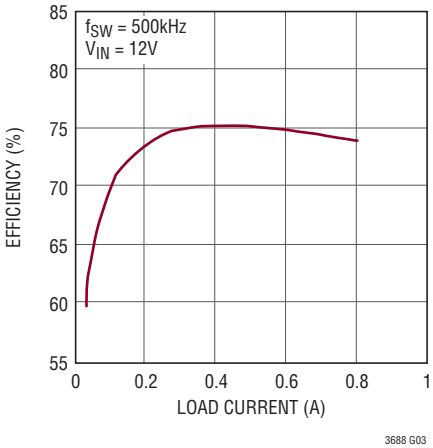
Efficiency, V_{OUT} = 5V



Efficiency, V_{OUT} = 3.3V



Efficiency, V_{OUT} = 1.8V



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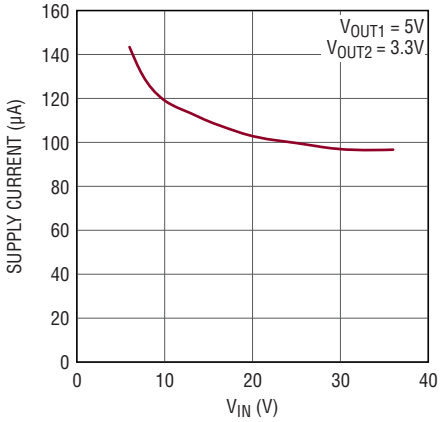
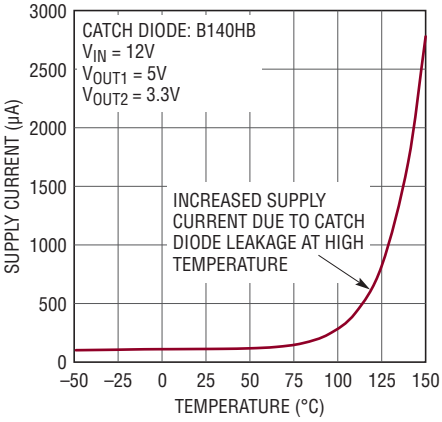
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

No-Load Supply Current (Input)



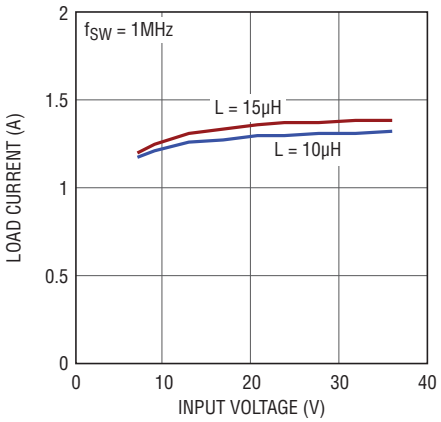
3688 G04

No-Load Supply Current (Temperature)



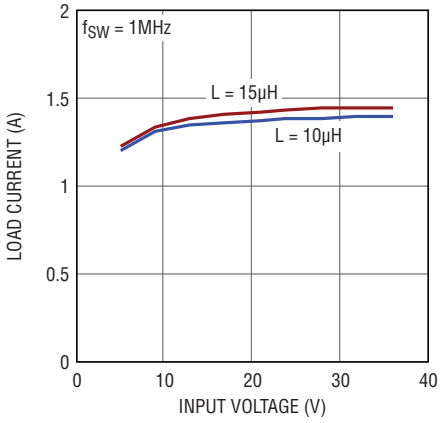
3688 G05

Maximum Load Current (5V)



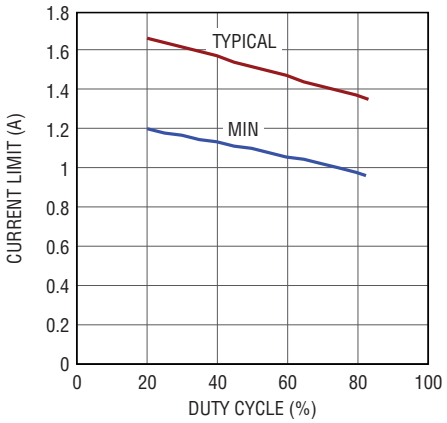
3688 G06

Maximum Load Current (3.3V)



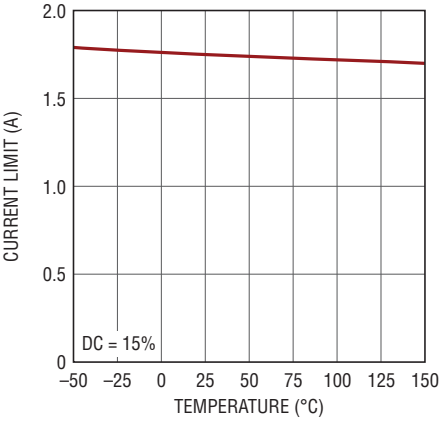
3688 G07

Switch Current Limit vs Duty Cycle



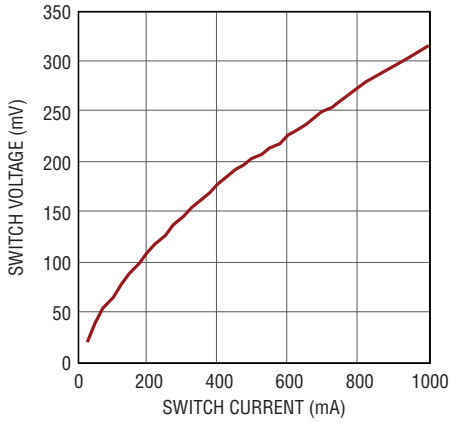
3688 G08

Switch Current Limit vs Temperature



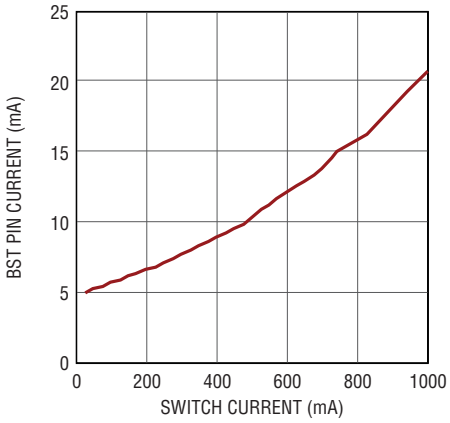
3688 G09

Switch Voltage Drop



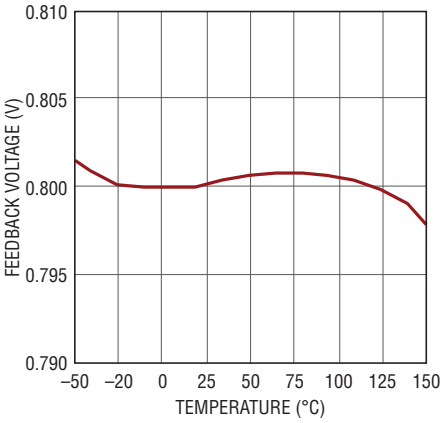
3688 G10

BST Pin Current



3688 G11

Feedback Voltage



3688 G12

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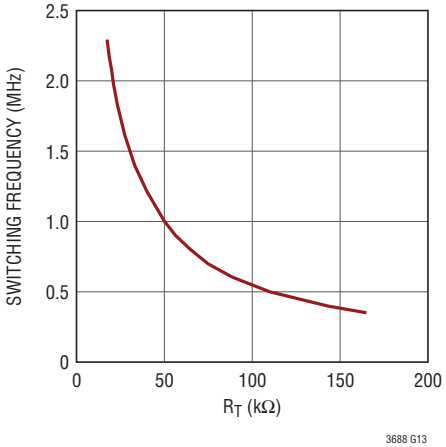
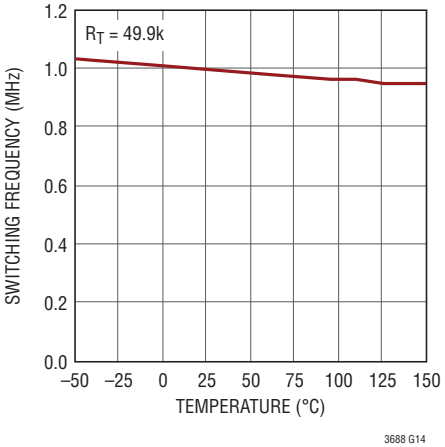
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

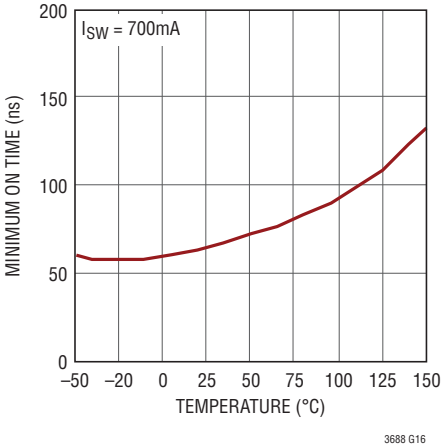
Switching Frequency vs R_T



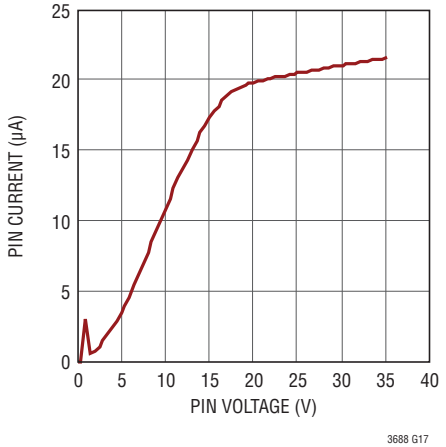
Switching Frequency vs Temperature



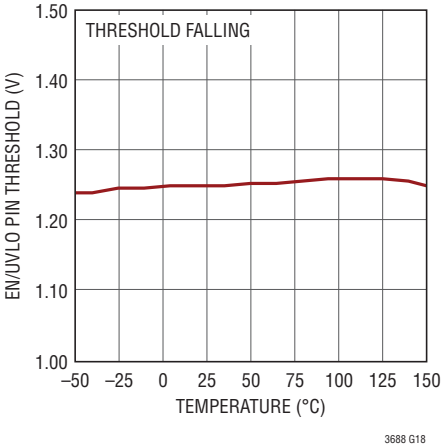
Minimum Switch On-Time



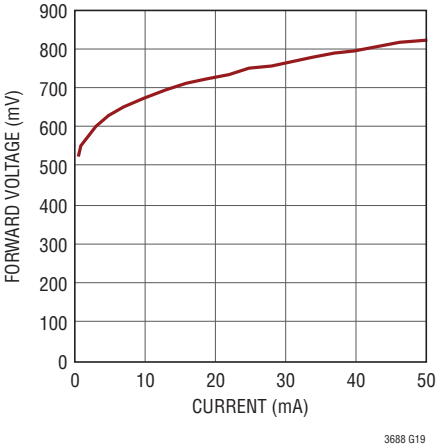
EN/UVLO Pin Current



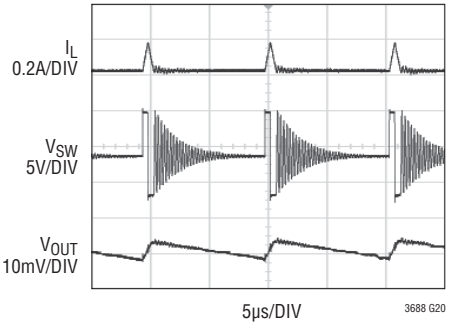
EN/UVLO Pin Threshold



Boost Diode Forward Voltage

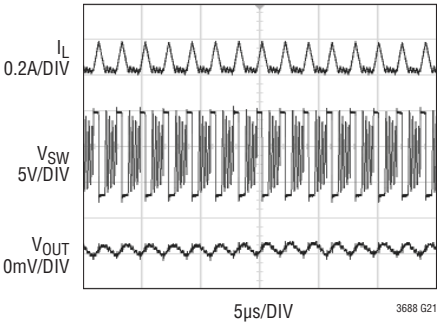


Switching Waveforms, Burst Mode Operation



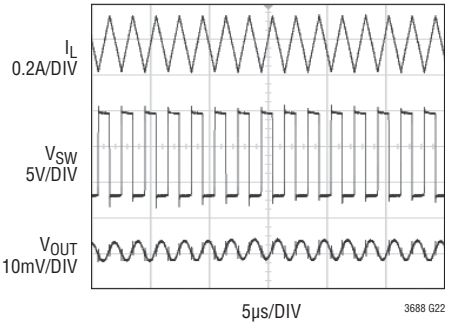
V_{IN} = 12V; FRONT PAGE APPLICATION
I_{LOAD} = 7mA

Switching Waveforms, Transition from Burst Mode to Full Frequency



V_{IN} = 12V; FRONT PAGE APPLICATION
I_{LOAD} = 40mA

Switching Waveforms, Full Frequency Continuous Operation



V_{IN} = 12V; FRONT PAGE APPLICATION
I_{LOAD} = 160mA

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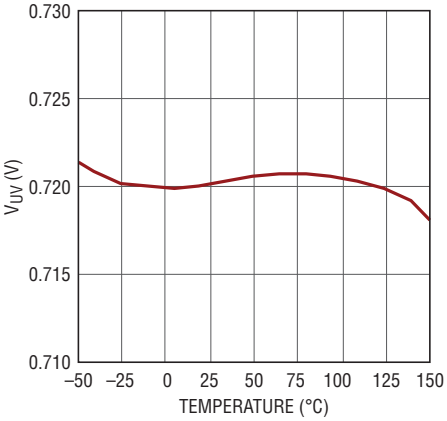
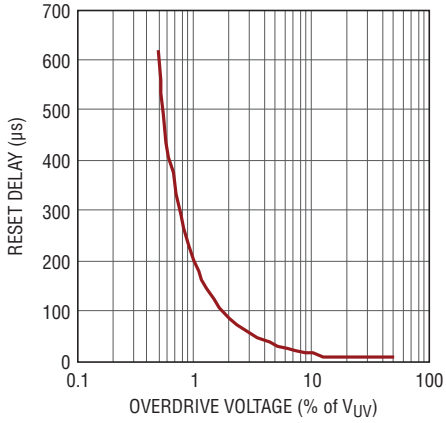
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted.

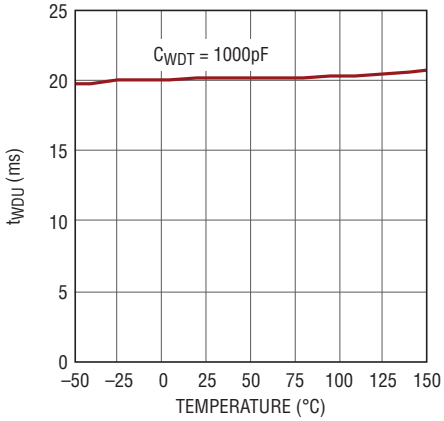
Power-On Reset Threshold vs Temperature



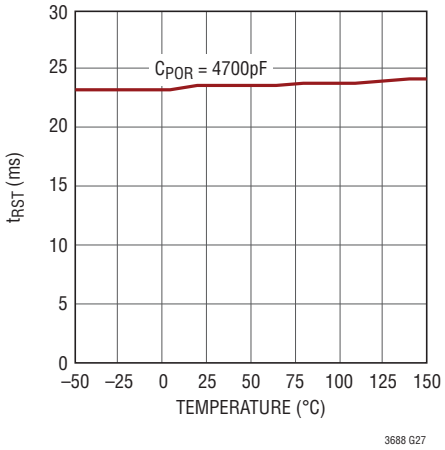
Typical Transient Duration vs Comparator Overdrive



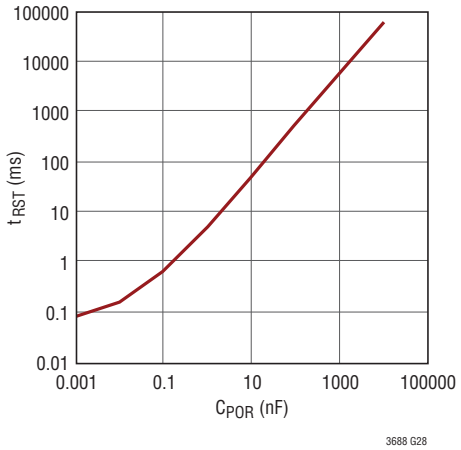
Watchdog Window Mode Period vs Temperature



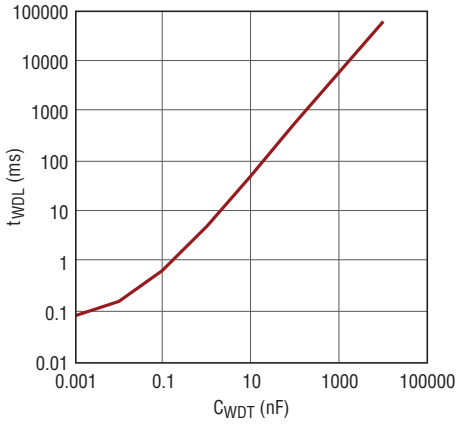
Reset Timeout Period (t_{RST}) vs Temperature



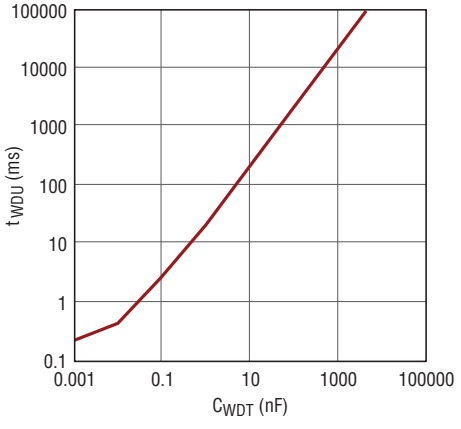
Reset Timeout Period (t_{RST}) vs Capacitance



Watchdog Window Lower Boundary (t_{WDL}) vs Capacitance



Watchdog Window Upper Boundary (t_{WDU}) vs Capacitance



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PIN FUNCTIONS (QFN/TSSOP)

RT (Pin 1/Pin 22): The RT pin is used to set the internal oscillator frequency. Tie a resistor from RT to GND to set the switching frequency.

SYNC (Pin 2/Pin 23): Drive the SYNC pin with a logic-level signal with positive and negative pulse widths of at least 150ns. Do not float this pin. Tie to GND if the SYNC feature is not used.

EN/UVLO (Pin 3/Pin 24): The EN/UVLO pin is used to put the LT3688 in shutdown mode. Pull the pin below 0.3V to shut down the LT3688. The 1.25V threshold can function as an accurate undervoltage lockout (UVLO), preventing the regulator from operating until the input voltage has reached the programmed level.

FB1, FB2 (Pins 4, 15/Pins 1, 12): The LT3688 regulates the feedback pins to 0.800V. Connect the feedback resistor divider taps to this pin.

RUN/SS1, RUN/SS2 (Pins 5, 14/Pins 2, 11): Place a capacitor from RUN/SS to GND to program the soft start period. Use a 1000pF or larger capacitor at these pins. To ensure the SS capacitors are discharged, internal circuitry pulls the RUN/SS pins low and disables switching during startup before initiating the soft-start sequence. Once the RUN/SS pins fall below 0.2V, the pull down turns off, the SS capacitors start charging again, and switching is enabled. Do not drive these pins directly. Use an open drain or collector to pull them low, if necessary.

BST1, BST2 (Pins 6, 13/Pins 3, 10): The BST pins are used to provide drive voltage, higher than the input voltage, to the internal NPN power switches.

SW1, SW2 (Pins 7, 12/Pins 4, 9): The SW pins are the outputs of the internal power switches. Connect these pins to the inductors, catch diodes and boost capacitors.

DA1, DA2 (Pins 8, 11/Pins 5, 8): Tie the DA pin to the anode of the external catch Schottky diode. If the DA pin current exceeds 1.2A, which could occur in an overload or short-circuit condition, switching is disabled until the DA pin current falls below 1.2A.

V_{IN} (Pin 9/Pin 6): The V_{IN} pin supplies current to the LT3688's internal circuitry and to the internal power switches and must be locally bypassed.

CONFIG (Pin 10/Pin 7): The CONFIG pin programs the start-up sequence of the two voltage regulators and the behavior of the power-on reset and watchdog timers. To select one of three configuration options, tie the CONFIG pin to V_{IN}, tie the CONFIG pin to GND or leave the CONFIG pin floating. With the CONFIG pin tied to V_{IN}, each reset output depends on its respective FB pin. Channel 2 only starts when FB1 rises above 0.72V, and the watchdog timer only starts when both $\overline{RST}$ pins go high. With the CONFIG pin tied to GND, both $\overline{RST}$ pins pull low until both FB pins rise above 0.72V and the POR timer programmed by C_{POR1} expires. Again, channel 2 only starts when FB1 rises above 0.72V, and the watchdog timer only starts when both $\overline{RST}$ pins go high. Tie C_{POR2} to GND if the CONFIG pin is tied low. With the CONFIG pin floating, both channels start coincidentally, each reset output depends on its respective FB pin, and the watchdog timer starts when $\overline{RST1}$ goes high.

$\overline{RST1}$, $\overline{RST2}$ (Pins 17, 16/Pins 14, 13): The $\overline{RST}$ pins are active low, open-drain logic outputs with a weak pull-up to BIAS. After V_{FB} rises above 0.72V, the reset remains asserted for the period set by the capacitor on the C_{POR} pin. Tie the $\overline{RST}$ pins to BIAS with a 100k resistor for a stronger pull-up.

$\overline{WDO}$ (Pin 18/Pin 15): $\overline{WDO}$ will go low if the microprocessor fails to drive the WDI pin of the LT3688 with the appropriate signal. Tie the $\overline{WDO}$ pin to BIAS with a 100k resistor for a stronger pull-up. Keep capacitive loading on this pin below 1000pF.

$\overline{WDE}$ (Pin 19/Pin 16): The watchdog timer enable pin disables the watchdog timer if the $\overline{WDE}$ voltage exceeds 1V. Float this pin or tie to ground for normal operation.

WDI (Pin 20/Pin 17): The watchdog timer input pin receives the watchdog signal from the microprocessor. If two or more negative edges occur on WDI before the programmed fast timer period or no negative edge occurs within the slow timer period, the part will pulse $\overline{WDO}$ low with a pulse width of 1/8th of the slow timer period. Drive the WDI pin with a pulse width of at least 300ns.

BIAS (Pin 22/Pin 19): The BIAS pin supplies current to the internal circuitry when BIAS is above 3V, helping reduce input quiescent current. The internal Schottky diodes are connected from BIAS to BST, providing the charging path for the boost capacitors.

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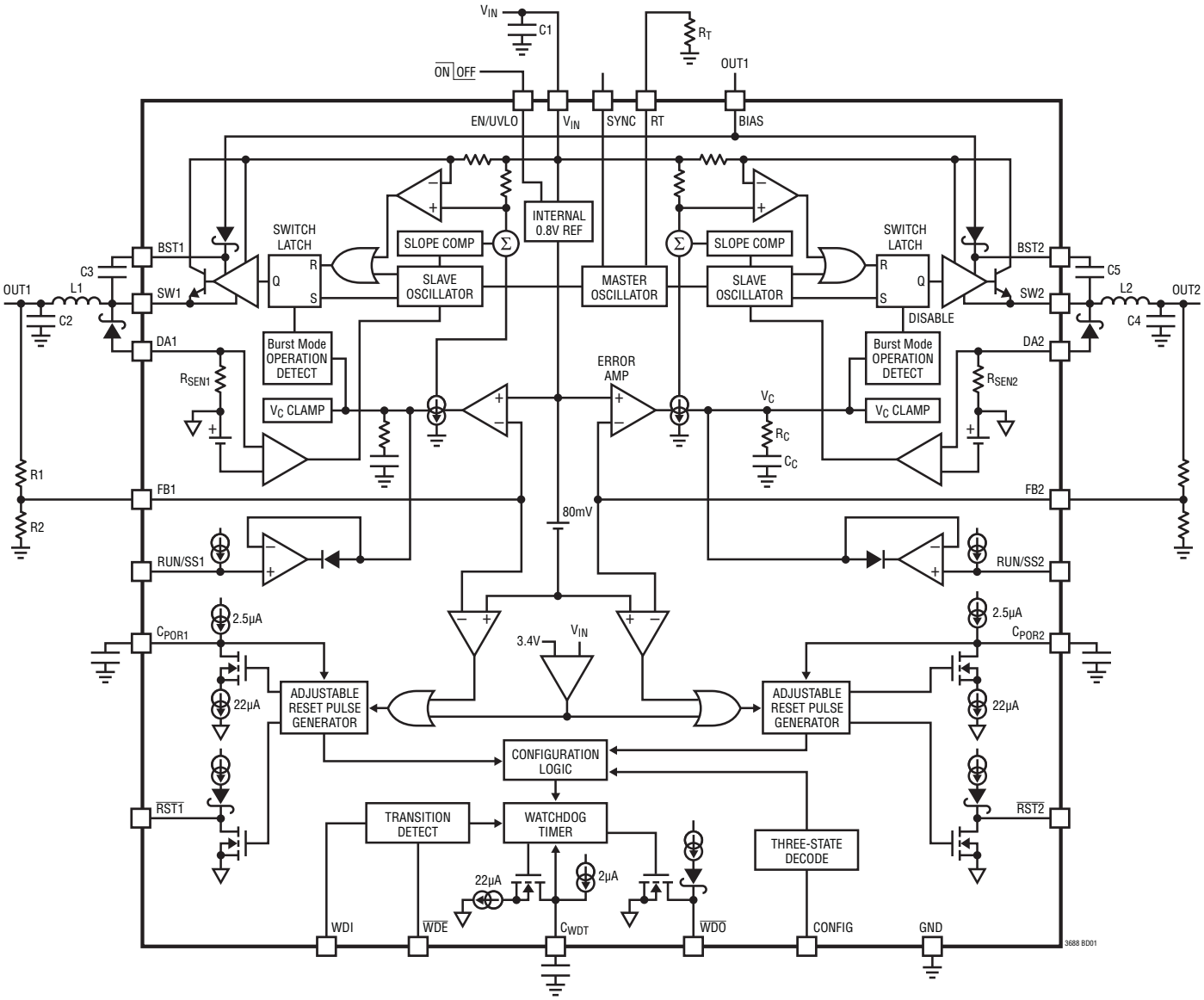
PIN FUNCTIONS (QFN/TSSOP)

C_{POR1}, C_{POR2} (Pins 23, 21/Pins 20, 18): Place a capacitor between this pin and ground to set the power-on-reset timeout period.

C_{WDT} (Pin 24/Pin 21): Place a capacitor between this pin and ground to set the fast and slow watchdog timer periods.

Exposed Pad (Pin 25/Pin 25): Ground. Tie the exposed pad directly to the ground plane. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The device must be soldered to the circuit board for proper operation.

BLOCK DIAGRAM



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OPERATION

The LT3688 is a constant-frequency, current mode step-down regulator with two reset timers and a watchdog timer that perform microprocessor supervisory functions. Operation can be best understood by referring to the Block Diagram. Keeping the EN/UVLO pin at ground completely shuts off the part drawing minimal current from the V_{IN} source. To turn on the internal bandgap and the rest of the logic circuitry, raise the EN/UVLO pin above the accurate threshold of 1.25V. Also, V_{IN} needs to be higher than 3.5V for the part to start switching.

Switching Regulator Operation

An oscillator, with frequency set by R_T, enables an RS flip flop, turning on the internal power switch. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C. An error amplifier measures the output voltage through an external resistor divider tied to the FB pin and servos the V_C voltage. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp on the V_C voltage provides current limit. The V_C voltage is also controlled by the internal soft-start circuit during start-up or after a fault condition takes place.

An internal regulator provides power to the control circuitry. The internal regulator normally draws current from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 3V, bias current will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The BIAS pin also provides a current path to the internal boost diode that charges up the boost capacitor. The switch driver operates either from the V_{IN} or from the BST pin. An external capacitor is used to generate a voltage at the BST pin that is higher than the V_{IN} supply. This allows the driver to fully saturate the internal NPN power switch for efficient operation. To further optimize efficiency, the LT3688 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 115µA in a typical application.

A comparator monitors the current flowing through the catch diode via the DA pin. This comparator delays switching if the diode current goes higher than 1.2A (typical) during a fault condition such as a shorted output with high input voltage. Switching will only resume once the diode current has fallen below the 1.2A limit. This way the DA comparator regulates the valley current of the inductor to 1.2A during short circuit. This will ensure that the part will survive a short-circuit event.

Power-On Reset and Watchdog Timer Operation

The LT3688 has two power-on reset comparators that monitor the regulated output voltages. If V_{OUT} is 10% below the regulation value, the $\overline{RST}$ pin is pulled low. Once the output voltage crosses over 90% of the regulation value, a reset timer is started and $\overline{RST}$ is released after the programmed reset delay time. The reset delay is programmable through the C_{POR} pin.

The watchdog typically monitors a microprocessor's activity. The watchdog can be enabled or disabled by applying a logic signal to the $\overline{WDE}$ pin. The watchdog timer requires successive negative edges on the WDI pin to come within a programmed time window to keep $\overline{WDO}$ from going low. If the time between the two negative WDI edges is too short or too long, then the $\overline{WDO}$ pin will be pulled low. When the $\overline{WDO}$ pin goes low, it stays low for a time period equivalent to 1/8th of the watchdog window upper boundary. The $\overline{WDO}$ pin will go high again once the timer expires or if the $\overline{RST}$ pin goes low. The watchdog window upper and lower boundaries can be set through the C_{WDT} pin.

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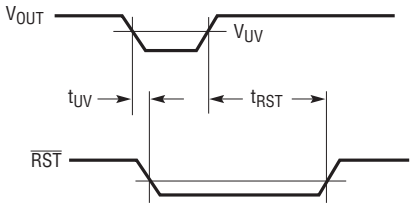
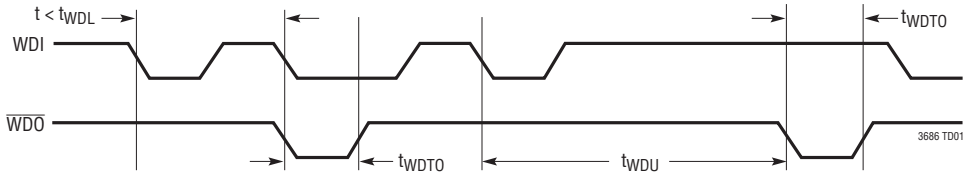
TIMING DIAGRAMS

Power-On Reset Timing



Watchdog Timing



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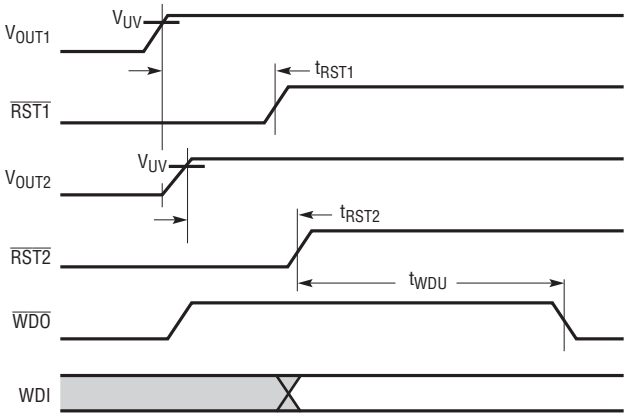
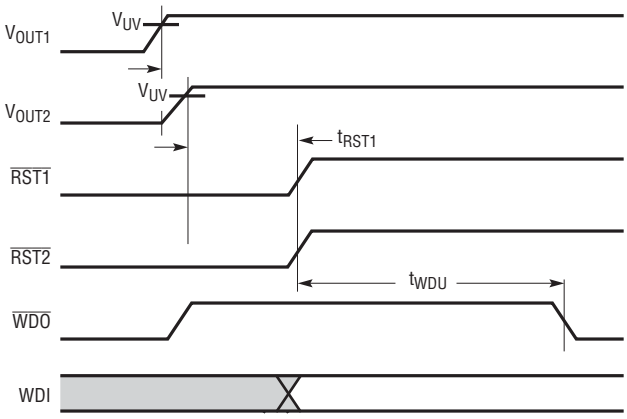
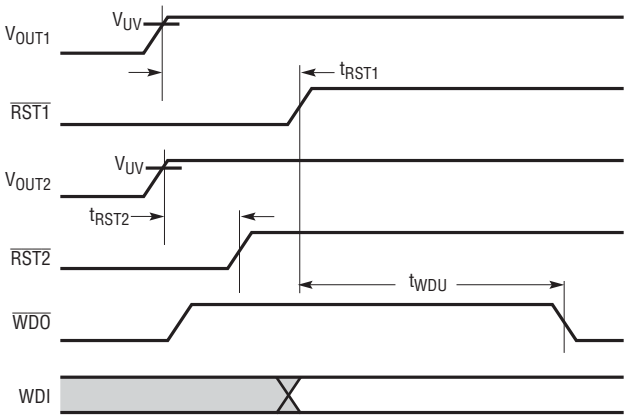
TIMING DIAGRAMS



STARTUP TIMING (V_{CONFIG} = HIGH)



STARTUP TIMING (V_{CONFIG} = LOW)



STARTUP TIMING (V_{CONFIG} = OPEN)

t_{RST1} = PROGRAMMED RESET PERIOD (C_{POR1})
t_{RST2} = PROGRAMMED RESET PERIOD (C_{POR2})
t_{WDU} = WATCHDOG WINDOW UPPER BOUNDRY
V_{UV} = RESET THRESHOLD

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Setting the Output Voltage

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the 1% resistors according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

For reference designators, refer to the Block Diagram.

Setting the Switching Frequency

The LT3688 uses a constant-frequency PWM architecture that can be programmed to switch from 350 kHz to 2.2 MHz by using a resistor tied from the RT pin to ground. Table 1 shows the R_T values for various switching frequencies

Table 1. Switching Frequency vs R_T

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
0.35	165
0.5	110
0.6	88.7
0.7	75
0.8	64.9
0.9	56.2
1	49.9
1.2	40.2
1.4	33.2
1.6	27.4
1.8	23.2
2.1	20
2.3	17.4

Operating Frequency Tradeoffs

Selection of the operating frequency is a tradeoff between efficiency, component size and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, and narrower input voltage range at constant-frequency. The highest constant-switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_F}{t_{ON(MIN)}\left(V_{IN} + V_F - V_{SW}\right)}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, V_F is the catch diode drop (~0.5V) and V_{SW} is the internal switch drop (~0.3V at maximum load). If the LT3688 is programmed to operate at a frequency higher than $f_{SW(MAX)}$ for a given input voltage, the LT3688 enters pulse skip mode, where it skips switching cycles to maintain regulation. At frequencies higher than $f_{SW(MAX)}$, the LT3688 no longer operates with constant frequency. The LT3688 enters pulse skip mode at frequencies higher than $f_{SW(MAX)}$ because of the limitation on the LT3688's minimum on time of 140ns (180ns for $T_J > 125°C$). As the switching frequency is increased above $f_{SW(MAX)}$, the part is required to switch for shorter periods to maintain the same duty cycle. Delays associated with turning off the power switch dictate the minimum on-time of the part. When the required on-time decreases below the minimum on-time of 140ns, the switch pulse width remains fixed at 140ns (instead of becoming narrower) to accommodate the same duty cycle requirement. The inductor current ramps up to a value exceeding the load current and the output ripple increases. The part then remains off until the output voltage dips below the programmed value before it begins switching again.

Maximum Operating Voltage Range

The maximum input voltage for LT3688 applications depends on switching frequency, the absolute maximum ratings of the V_{IN} and BST pins, and by the minimum duty cycle (DC_{MIN}). The LT3688 can operate from input voltages up to 36V.

$$DC_{MIN} = t_{ON(MIN)} \bullet f_{SW}$$

where $t_{ON(MIN)}$ is equal to 140ns and f_{SW} is the switching frequency. Running at a lower switching frequency allows a lower minimum duty cycle. The maximum input voltage before pulse-skipping occurs depends on the output voltage and the minimum duty cycle:

$$V_{IN(PS)} = \frac{V_{OUT} + V_F}{DC_{MIN}} - V_F + V_{SW}$$

Example: f = 2.1MHz, V_{OUT} = 3.3V

$$DC_{MIN} = 140ns \bullet 2.1MHz = 0.294$$

$$V_{IN(PS)} = \frac{3.3V + 0.5V}{0.294} - 0.5V + 0.3V = 12.7V$$

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The LT3688 will regulate the output voltage at input voltages greater than $V_{IN(PS)}$. For example, an application with an output voltage of 3.3V and switching frequency of 2.1MHz has a $V_{IN(PS)}$ of 12.7V, as shown in Figure 1. Figure 2 shows operation at 27V. Output ripple and peak inductor current have significantly increased. A saturating inductor may further reduce performance. In pulse skip mode, the LT3688 skips switching pulses to maintain output regulation. The LT3688 will also skip pulses at very low load currents. $V_{IN(PS)}$ vs load current is plotted in the Typical Performance section.

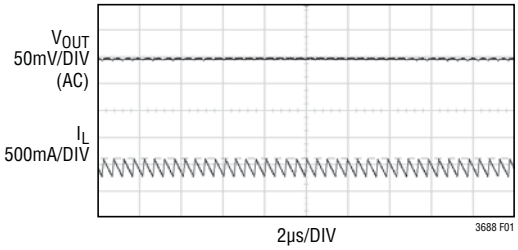

Figure 1. Operation Below Pulse-Skipping Voltage. V_{OUT} = 3.3V and f_{SW} = 2.1MHz

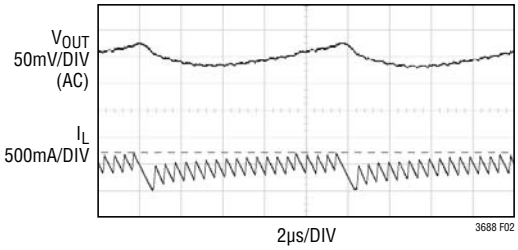

Figure 2. Operation Above $V_{IN(ps)}$. V_{IN} = 27V, V_{OUT} = 3.3V and f_{SW} = 2.1MHz. Output Ripple and Peak Inductor Current Increase

Minimum Operating Voltage Range

The minimum input voltage is determined either by the LT3688's minimum operating voltage of ~3.6V or by its maximum duty cycle. The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltages:

$$DC = \frac{V_{OUT} + V_F}{V_{IN} - V_{SW} + V_F}$$

Unlike many fixed frequency regulators, the LT3688 can extend its duty cycle by remaining on for multiple cycles. The LT3688 will not switch off at the end of each clock cycle if there is sufficient voltage across the boost capacitor (C3 in the Block Diagram). Eventually, the voltage on the boost capacitor falls and requires refreshing. Circuitry detects this condition and forces the switch to turn off, allowing the inductor current to charge up the boost capacitor. This places a limitation on the maximum duty cycle as follows:

$$DC_{MAX} = 90\%$$

This leads to a minimum input voltage of:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_F}{DC_{MAX}} - V_F + V_{SW}$$

where V_F is the forward voltage drop of the catch diode (~0.4V) and V_{SW} is the voltage drop of the internal switch (~0.3V at maximum load).

Example: I_{SW}=0.8A and V_{OUT} = 3.3V

$$V_{IN(MIN)} = \frac{3.3V + 0.4V}{90\%} - 0.4 + 0.3V = 4V$$

For best performance in dropout, use a 1µF or larger boost capacitor.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is

$$L = (V_{OUT} + V_F) \bullet \frac{1.8MHz}{f_{SW}}$$

where V_F is the voltage drop of the catch diode (~0.4V), f_{SW} is in MHz, and L is in µH. The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be at least 30% higher. For robust operation in fault conditions (start-up or short-circuit) and high input voltage (>30V), use an 8.2µH or greater inductor with a saturation rating of 2.2A, or higher. For highest efficiency, the series resistance (DCR) should be less than 0.1Ω. Table 2 lists several vendors and types that are suitable.

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Table 2. Inductor Vendors

VENDOR	PART SERIES	TYPE	URL
Murata	LQH55D	Open	www.murata.com
TDK	SLF7045 SLF10145	Shielded Shielded	www.component.tdk.com
Toko	DC62CB D63CB D75C D75F	Shielded Shielded Shielded Open	www.toko.com
Sumida	CR54 CDRH74 CDRH6D38 CR75	Open Shielded Shielded Open	www.sumida.com

The optimum inductor for a given application may differ from the one indicated by this simple design guide. A larger value inductor provides a higher maximum load current, and reduces the output voltage ripple. If your load is lower than the maximum load current, then you can relax the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that if the inductance differs from the simple rule above, then the maximum load current will depend on input voltage. In addition, low inductance may result in discontinuous mode operation, which further reduces maximum load current. Discontinuous operation occurs when I_{OUT} is less than ΔI_L / 2. For details of maximum output current and discontinuous mode operation, see Linear Technology's Application Note AN44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillations:

$$L_{MIN} = (V_{OUT} + V_F) \bullet \frac{1.2MHz}{f_{SW}}$$

where V_F is the voltage drop of the catch diode (~0.4V), f_{SW} is in MHz, and L_{MIN} is in µH.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT3688 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3688 will deliver depends on the switch current limit, the inductor value, and the input and output voltages.

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor

$$\Delta I_L = \frac{(1-DC)(V_{OUT} + V_F)}{L \bullet f}$$

where f is the switching frequency of the LT3688 and L is the value of the inductor. The peak inductor and switch current is

$$I_{SW(PK)} = I_{L(PK)} = I_{OUT} + \frac{\Delta I_L}{2}$$

To maintain output regulation, this peak current must be less than the LT3688's switch current limit I_{LIM}. I_{LIM} is at least 1.25A for at low duty cycles and decreases linearly to 0.9A at DC = 0.9. The maximum output current is a function of the chosen inductor value:

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

$$= 1.25A \bullet (1 - 0.3DC) - \frac{\Delta I_L}{2}$$

Choosing an inductor value so that the ripple current is small will allow a maximum output current near the switch current limit.

One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors, and choose one to meet cost or space goals. Then use these equations to check that the LT3688 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous.

Input Capacitor

Bypass the input of the LT3688 circuit with a ceramic capacitor of an X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 2.2µF to 4.7µF ceramic capacitor is adequate to bypass the LT3688 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables,

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additional bulk capacitance may be necessary. This can be provided with a lower performance electrolytic capacitor. Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3688 input and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 2.2µF capacitor is capable of this task, but only if it is placed close to the LT3688 and the catch diode (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3688. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3688 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3688's voltage rating. See Linear Technology's Application Note 88 for details.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3688 to produce the DC output. In this role it determines the output ripple, and low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3688's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{50}{V_{OUT} \bullet f_{SW}}$$

where f_{SW} is in MHz and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types, which will provide low output ripple and good transient response. Transient performance can be improved with a high value capacitor, but a phase lead capacitor across the feedback resistor R1 may be required to get the full benefit (see the Compensation section).

High performance electrolytic capacitors can be used for the output capacitor. Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be specified by the supplier and should be 0.1Ω or less. Such a capacitor will be larger than a ceramic capacitor and will have a larger capacitance because the capacitor must be large to achieve low ESR. Table 3 lists several capacitor vendors.

Table 3. Capacitor Vendors

VENDOR	PART SERIES	COMMENTS
Panasonic	Ceramic Polymer Tantalum	EEEF Series
Kemet	Ceramic Tantalum	T494, T495
Sanyo	Ceramic Polymer Tantalum	POSCAP
Murata	Ceramic	
AVX	Ceramic Tantalum	TPS Series
Taiyo Yuden	Ceramic	

Catch Diode

The catch diode conducts current only during switch-off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}$$

where I_{OUT} is the output load current. The only reason to consider a diode with a larger current rating than necessary for nominal operation is for the worst-case condition of shorted output. The diode current will then increase to the typical peak switch current limit. Peak reverse voltage is equal to the regulator input voltage. Use a Schottky diode with a reverse voltage rating greater than the input voltage. Table 4 lists several Schottky diodes and their manufacturers.

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Table 4. Capacitor Vendors

Part Number	V_R (V)	I_{AVE} (A)	V_F at 1A (mV)
On Semiconductor			
MBR0520L	20	0.5	
MBR0540	40	0.5	620
MBRM120E	20	1	530
MBRM140	40	1	550
Diodes Inc.			
B0530W	30	0.5	
B120	20	1	500
B130	30	1	500
B140HB	40	1	
DFLS140	40	1.1	510

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT3688 due to their piezoelectric nature. When in Burst Mode operation, the LT3688's switching frequency depends on the load current, and at very light loads the LT3688 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT3688 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

Frequency Compensation

The LT3688 uses current mode control to regulate the output, which simplifies loop compensation. In particular, the LT3688 does not require the ESR of the output capacitor for stability, allowing the use of ceramic capacitors to achieve low output ripple and small circuit size. Figure 3 shows an equivalent circuit for the LT3688 control loop. The error amp is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C node. Note that the output capacitor, C1, integrates this current, and that the capacitor on the V_C node (C_C) integrates the error amplifier output current, resulting in two poles in the loop. R_C provides a zero. With the recommended output capacitor, the loop crossover occurs above the R_CC_C zero. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. With a larger ceramic capacitor (very low ESR), crossover may be lower and a phase lead capacitor (C_{PL}) across the feedback divider may improve the phase margin and transient response. At minimum, use a 10pF phase lead capacitor to reduce noise injection to the FB pin. If the output capacitor is different than the recommended capacitor, stability should be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load. Figure 4 shows the transient response when the load current is stepped from 300mA to 600mA and back to 300mA.

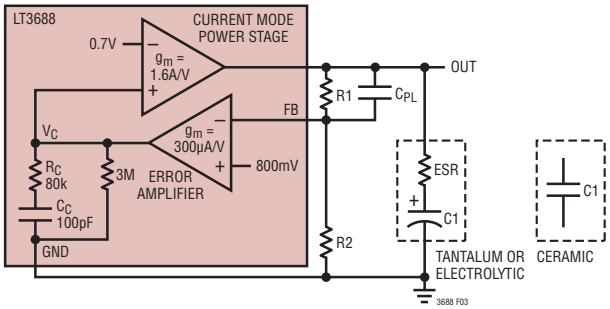

Figure 3. Model for the Loop Response

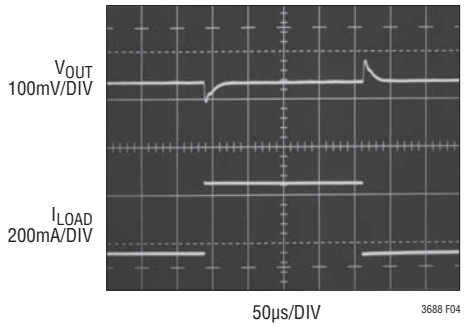

Figure 4. Transient Load Response of the LT3688 Front Page Application as the Load Current is Stepped from 300mA to 600mA

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Low Ripple Burst Mode Operation

To enhance efficiency at light loads, the LT3688 operates in low ripple Burst Mode operation that keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LT3688 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. Because the LT3688 delivers power to the output with single, low current pulses, the output ripple is kept below 25mV for a typical application. In addition, V_{IN} and BIAS quiescent currents are reduced to typically 65µA and 155µA, respectively, during the sleep time. As the load current decreases towards a no-load condition, the percentage of time that the LT3688 operates in sleep mode increases and the average input current is greatly reduced, resulting in high efficiency even at very low loads (see Figure 5). At higher output loads the LT3688 will be running at the frequency programmed by the R_T resistor, and will be operating in standard PWM mode. The transition between PWM and low ripple Burst Mode operation is seamless, and will not disturb the output voltage. The front page application circuit will switch at full frequency at output loads higher than about 60mA.

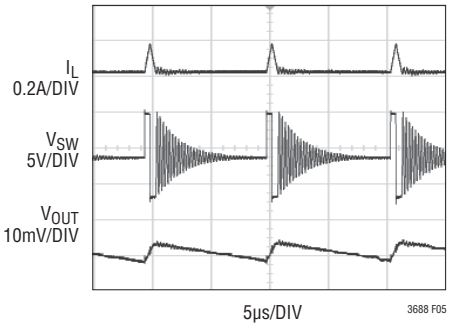
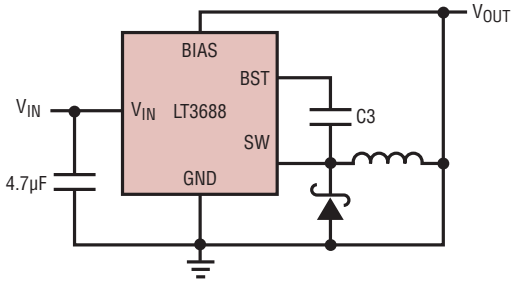


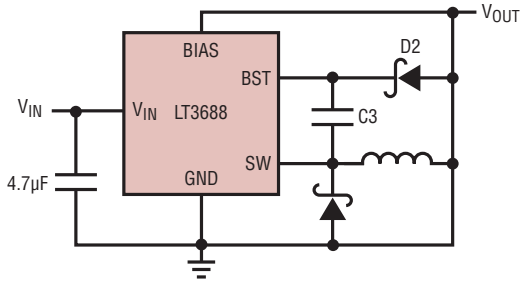
Figure 5. Burst Mode Operation

BST and BIAS Pin Considerations

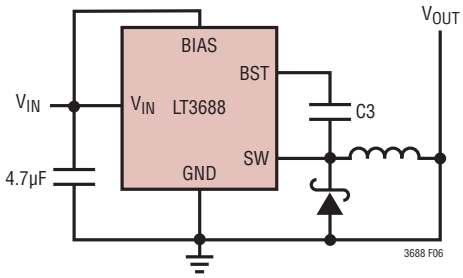
Capacitor C3 and the internal boost Schottky diodes (see the Block Diagram) are used to generate boost voltages that are higher than the input voltage. In most cases, a 0.22µF capacitor will work well. For the best performance in dropout, use a 1µF or larger capacitor. Figure 6 shows three ways to arrange the boost circuit. The BST pin must be more than 2.3V above the SW pin for best efficiency. For outputs of 3V and above, the standard circuit (Figure 6a) is best. For outputs between 2.8V and 3V, use a 1µF boost capacitor. A 2.5V output presents a special case because it is marginally adequate to support the boosted drive stage while using the internal boost diode. For reliable BST pin operation with 2.5V outputs, use a good external Schottky diode (such as the ON semi MBR0540), and a 1µF boost capacitor (see Figure 6b). For lower output voltages, the boost diode can be tied to the input (Figure 6c), or to another supply greater than 2.8V. The circuit in Figure 6a is more efficient because the BST pin current and BIAS pin quiescent current comes from a lower volt-



(6a) For V_{OUT} > 2.8V



(6b) For 2.5V < V_{OUT} < 2.8V



(6c) For V_{OUT} < 2.5V; $V_{IN(MAX)}$ = 30V

Figure 6. Three Circuits for Generating the Boost Voltage

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age source. However, the full benefit of the BIAS pin is not realized unless it is at least 3V. Ensure that the maximum voltage ratings of the BST and BIAS pins are not exceeded.

The minimum operating voltage of an LT3688 application is limited by the minimum input voltage (3.6V) and by the maximum duty cycle, as outlined in a previous section. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT3688 is turned on with its EN/UVLO pin when the output is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. Figure 7 shows a plot of minimum load to start and to run as a function of input voltage. In many cases, the discharged output capacitor will present a load to the switcher, which will allow it to start. The plots show the worst-case situation where V_{IN} is ramping very slowly. For lower start-up voltage, the boost diode can be tied to V_{IN}; however, this restricts the input range to one-half of the absolute maximum rating of the BST pin. At light loads, the inductor current becomes discontinuous and the effective duty cycle can be very high. This reduces the minimum input voltage to approximately 300mV above V_{OUT}. At higher load currents, the inductor current is continuous and the duty cycle is limited by the maximum duty cycle of the LT3688, requiring a higher input voltage to maintain regulation.

There is one particular issue to note if sequencing is used. If the BIAS pin is tied to V_{OUT2}, it will be low during the startup of V_{OUT1}. This will prevent the boost circuit from working on V_{OUT1} until it has risen to 90% of its programmed value, increasing the required startup voltage. Using circuit in Figure 6b for V_{OUT1} will reduce the startup voltage to its normal value. An alternative is to tie BIAS to V_{OUT1}, if it is greater than 2.8V.

Soft-Start and Individual Channel Shutdown

The RUN/SS (Run/Soft-Start) pins are used to place the individual switching regulators in shutdown mode. They also provide a soft-start function. To shut down either

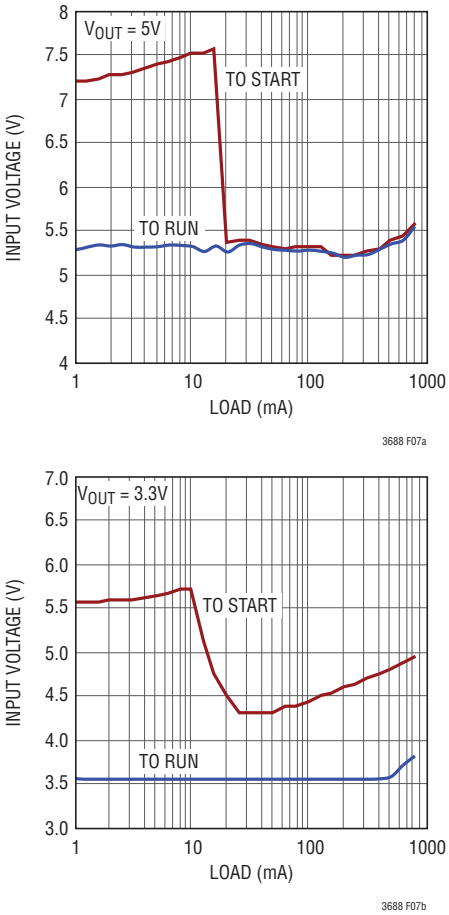

Figure 7. The Minimum Input Voltage Depends on Output Voltage, Load Current and Boost Circuit

regulator, pull the RUN/SS pin to ground with an open-drain or collector. Note that if CONFIG is tied high or low (not open), shutting down Channel 1 will also shut down Channel 2 because of the sequencing function (See the Configuration and Sequencing section for more details). 2.5µA current sources pull up on each pin. If the RUN/SS pin reaches ~0.2V, the channel will begin to switch

If a capacitor is tied from the RUN/SS pin to ground, then the internal pull-up current will generate a voltage ramp on this pin. This voltage clamps the V_C pin, limiting the peak switch current and therefore input current during start up. A good value for the soft-start capacitor is C_{OUT}/10,000, where C_{OUT} is the value of the output capacitor.

The RUN/SS pins can be left floating if the Soft-Start feature is not used. They can also be tied together with a single capacitor providing soft-start. The internal current sources

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will charge these pins to ~2V. The RUN/SS pins provide a soft-start function that limits peak input current to the circuit during start-up. This helps to avoid drawing more current than the input source can supply or glitching the input supply when the LT3688 is enabled. The RUN/SS pins do not provide an accurate delay to start or an accurately controlled ramp at the output voltage, both of which depend on the output capacitance and the load current.

Synchronization

Synchronizing the LT3688 oscillator to an external frequency can be done by connecting a square wave (with positive and negative pulse width > 150ns) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks that are above 1.3V (up to 6V). The LT3688 may be synchronized over a 350kHz to 2.5MHz range. The R_T resistor should be chosen to set the LT3688 switching frequency 20% below the lowest synchronization input. For example, if the synchronization signal will be 350kHz and higher, R_T should be chosen for 280kHz. To assure reliable and safe operation, the LT3688 will only synchronize when the output voltage is above 90% of its regulated voltage. It is therefore necessary to choose a large enough inductor value to supply the required output current at the frequency set by the R_T resistor (see the Inductor Selection section). It is also important to note that the slope compensation is set by the R_T value. When the sync frequency is much higher than the one set by R_T, the slope compensation will be significantly reduced, which may require a larger inductor value to prevent subharmonic oscillation.

Shutdown and Undervoltage Lockout

Figure 8 shows how to add undervoltage lockout (UVLO) to the LT3688. Typically, UVLO is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions.

UVLO prevents the regulator from operating at source voltages where the problems might occur. An internal comparator will force the part into shutdown below the minimum V_{IN} of 3.5V. This feature can be used to prevent excessive discharge of battery-operated systems. If an adjustable UVLO threshold is required, the EN/UVLO pin can be used. The threshold voltage of the EN/UVLO pin comparator is 1.25V. Current hysteresis is added above the EN threshold. This can be used to set voltage hysteresis of the UVLO using the following:

$$R3 = \frac{V_H - V_L}{3.7\mu A}$$

$$R4 = \frac{R3 \bullet 1.25V}{V_H - 1.25V - R3 \bullet 0.3\mu A}$$

Example: switching should not start until the input is above 4.40V, and is to stop if the input falls below 4V.

$$V_H = 4.40V,\ V_L = 4V$$

$$R3 = \frac{4.40V - 4V}{3.7\mu A} = 107k$$

$$R4 = \frac{107k \bullet 1.25V}{4.40V - 1.25V - 107k \bullet 0.3\mu A} = 43.2k$$

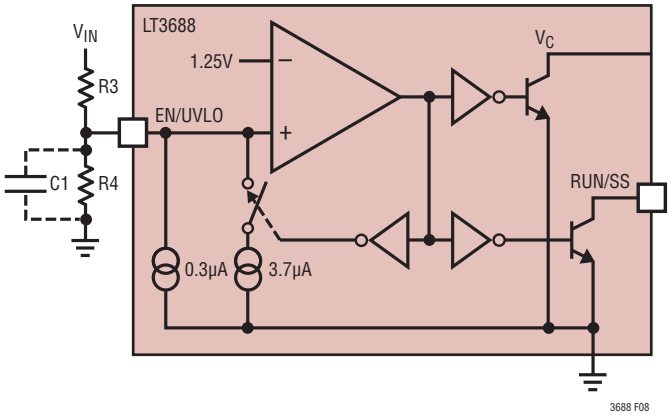

Figure 8. Undervoltage Lockout

Keep the connection from the resistor to the EN/UVLO pin short and make sure the interplane or surface capacitance to switching nodes is minimized. If high resistor values are used, the EN/UVLO pin should be bypassed with a 1nF capacitor to prevent coupling problems from the switch node.

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Output Voltage Monitoring

The LT3688 provides power supply monitoring for microprocessor-based systems. The features include power-on reset (POR) and watchdog timing.

A precise internal voltage reference and glitch immune precision POR comparator circuits monitor the LT3688 output voltages. Each channel's output voltage must be above 90% of the programmed value for $\overline{RST}$ not to be asserted (refer to the Timing Diagram). The LT3688 will assert $\overline{RST}$ during power-up, power-down and brownout conditions. Once the output voltage rises above the $\overline{RST}$ threshold, the adjustable reset timer is started and $\overline{RST}$ is released after the reset timeout period. On power-down, once the output voltage drops below $\overline{RST}$ threshold, $\overline{RST}$ is held at a logic low. The reset timer is adjustable using external capacitors. This capability helps hold the microprocessor in a stable shutdown condition. The $\overline{RST}$ pin has weak pull-up to the BIAS pin.

The above discussion is concerned only with the DC value of the monitored supply. Real supplies also have relatively high-frequency variation, from sources such as load transients, noise, and pickup. These variations should not be considered by the monitor in determining whether a supply voltage is valid or not. The variations may cause spurious outputs at $\overline{RST}$, particularly if the supply voltage is near its trip threshold.

Two techniques are used to combat spurious reset without sacrificing threshold accuracy. First, the timeout period helps prevent high-frequency variation whose frequency is above $1/t_{RST}$ from appearing at the $\overline{RST}$ output. When the voltage at FB goes below the threshold, the $\overline{RST}$ pin asserts low. When the supply recovers past the threshold, the reset timer starts (assuming it is not disabled), and $\overline{RST}$ does not go high until it finishes. If the supply becomes invalid any time during the timeout period, the timer resets and starts fresh when the supply next becomes valid. While the reset timeout is useful for preventing toggling of the reset output in most cases, it is not effective at preventing nuisance resets due to short glitches (due to load transients or other effects) on a valid supply. To reduce sensitivity to these short glitches, the comparator has additional anti-glitch circuitry. Any transient at the input of the comparator needs to be of sufficient magnitude and duration (t_{UV}) before it can change the monitor state. The combination of the reset timeout and anti-glitch circuitry prevents spurious changes in output state without sacrificing threshold accuracy.

Watchdog Timer

The LT3688 includes an adjustable watchdog timer that monitors a µP's activity. If a code execution error occurs in a µP, the watchdog will detect this error and will set the $\overline{WDO}$ low. This signal can be used to interrupt a routine or to reset a µP.

The watchdog circuitry is triggered by negative edges on the WDI pin. The window mode restricts the WDI pin's negative going pulses to appear inside a programmed time window (see the Timing Diagram) to prevent $\overline{WDO}$ from going low. If more than two pulses are registered in the window's fast period, the $\overline{WDO}$ is forced to go low. The $\overline{WDO}$ also goes low if no negative edge is supplied to the WDI pin in the window's slow timer period. During a code execution error, the microprocessor will output WDI pulses that would be either too fast or too slow. This condition will assert $\overline{WDO}$ and force the microprocessor to reset the program. In window mode, the WDI signal frequency is bounded by an upper and lower limit for normal operation. The WDI input frequency period should be higher than the window mode's fast period and lower than the window mode's slow period to keep $\overline{WDO}$ high under normal conditions. The window mode's fast and slow times have a fixed ratio of 16 between them. These times can be increased or decreased by adjusting an external capacitor on the C_{WDT} pin.

When $\overline{WDO}$ is asserted, a timer is enabled for a time equivalent to 1/8th of the watchdog window upper boundary. Any WDI pulses that appear while the reset timer is running are ignored. When the timer expires, the $\overline{WDO}$ is allowed to go high again. Therefore, if no input is applied to the WDI pin, then the watchdog circuitry produces a train of pulses on the $\overline{WDO}$ pin. The high time of this pulse train is equal to the watchdog window upper boundary, and low time is equal to the 1/8th of the watchdog window upper boundary.

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If $\overline{WDO}$ is low and $\overline{RST}$ goes low, then $\overline{WDO}$ will go high. The $\overline{WDE}$ pin allows the user to turn on and off the watchdog function. Leaving this pin open is okay and will automatically enable the watchdog. It has an internal weak pull-down to ground. The WDI pin has an internal weak pull-up that keeps the WDI pin high. If watchdog is disabled, leaving this pin open is acceptable.

Configuration and Sequencing

Use the CONFIG pin to adjust the sequencing and the behavior of the power-on reset and watchdog timers. The table below shows all of the configuration options.

Table 5. Configuration Options

	CONFIG		
CONDITION	**HIGH**	**LOW**	**OPEN**
Channel 1 starts before Channel 2	×	×	
Channel 1 and Channel 2 start simultaneously			×
Watchdog operates only if Reset 1 Expires			×
Watchdog operates only if Reset 1 and Reset 2 Expire	×	×	
$\overline{RST1}$ and $\overline{RST2}$ high only if Timer 1 Expires		×	
$\overline{RST1}$ and $\overline{RST2}$ use independent timers	×		×

With the CONFIG pin tied high, V_{OUT1} will rise first, as shown in Figure 9a. After V_{OUT1} reaches V_{UV}, V_{OUT2} will start increasing. In addition, the reset timer for Channel 1 starts. Once V_{OUT2} reaches V_{UV}, the reset timer for Channel 2 starts. Once the reset timers for both Channel 1 and Channel 2 have expired, the Watchdog will start operation.

With the CONFIG pin tied low, V_{OUT1} will rise first. After V_{OUT1} reaches V_{UV}, V_{OUT2} will start increasing. The reset timer will only start if both V_{OUT1} and V_{OUT2} are above V_{UV}, as shown in Figure 9b. Once the reset timer programmed by C_{POR1} expires, both RST1 and RST2 can pull high, and the Watchdog will start operation. In this mode, tie C_{POR2} to GND.

With the CONFIG pin open, V_{OUT1} and V_{OUT2} can rise simultaneously, as shown in figure 9c. After V_{OUT1} reaches V_{UV} the reset timer for Channel 1 starts. Once V_{OUT2} reaches V_{UV}, the reset timer for Channel 2 starts. Once the reset timer for Channel 1 has expired, the Watchdog will start operation.

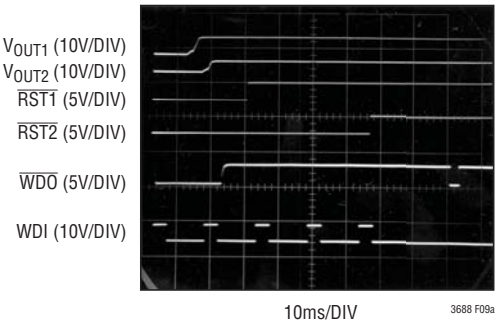

Figure 9a. CONFIG = HIGH

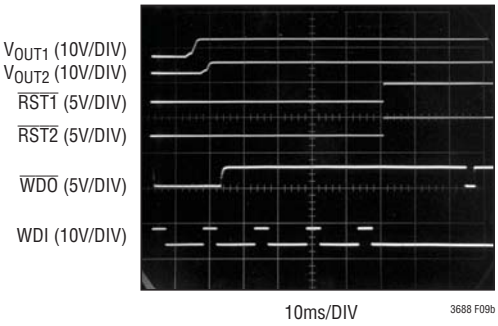

Figure 9b. CONFIG = LOW

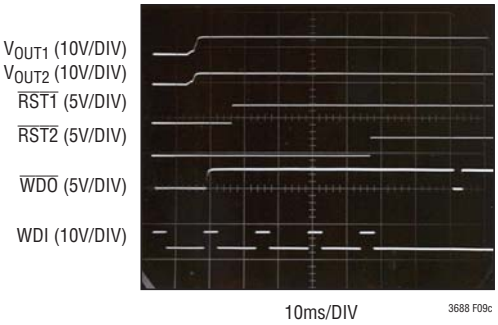

Figure 9c. CONFIG = OPEN

Figure 9. Startup Waveforms with the Three Configuration Settings

Selecting the Reset Timing Capacitors

The reset timeout period is adjustable in order to accommodate a variety of microprocessor applications. The reset timeout period, t_{RST}, is adjusted by connecting a capacitor, C_{POR}, between the C_{POR} pin and ground. The value of this capacitor is determined by:

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$$C_{POR} = t_{RST} \bullet 200\left(\frac{pF}{ms}\right)$$

This equation is accurate for reset timeout periods of 1ms, or greater. To program faster timeout periods, see the Reset Timeout Period vs Capacitance graph in the Typical Characteristics section. Leaving the C_{POR} pin unconnected will generate a minimum reset timeout of approximately 65µs. Maximum reset timeout is limited by the largest available low leakage capacitor. The accuracy of the timeout period will be affected by capacitor leakage (the nominal charging current is 2.5µA), capacitor tolerance and temperature coefficient. A low leakage, low tempco, capacitor is recommended.

Selecting the Watchdog Timing Capacitor

The watchdog timeout period is adjustable and can be optimized for software execution. The watchdog window upper boundary, t_{WDU} is adjusted by connecting a capacitor, C_{WDT}, between the C_{WDT} pin and ground. Given a specified watchdog timeout period, the capacitor is determined by:

$$C_{WDT} = t_{WDU} \bullet 50\left(\frac{pF}{ms}\right)$$

The window lower boundary (t_{WDL}) and the watchdog timeout (t_{WDTO}) have a fixed relationship to t_{WDU} for a given capacitor. The window lower boundary is related to t_{WDU} by the following:

$$t_{WDL} = \frac{1}{16} \bullet t_{WDU}$$

The watchdog timeout is related to t_{WDU} by the following:

$$t_{WDTO} = \frac{1}{8} \bullet t_{WDU}$$

Leaving the C_{WDT} pin unconnected will generate a minimum watchdog window upper boundary of approximately 200µs. Maximum window upper boundary is limited by the largest available low leakage capacitor. The timing accuracy of the reset and watchdog signals depends on the initial accuracy and stability of the programing capacitors. Use capacitors with specified accuracy, leakage and voltage and temperature coefficients. For surface mount ceramic capacitors C0G and NP0 types are superior to alternatives such as X5R and X7R.

Shorted and Reversed Input Protection

If an inductor is chosen to prevent excessive saturation, the LT3688 will tolerate a shorted output. When operating in short-circuit condition, the LT3688 will reduce its frequency until the valley current is at a typical value of 1.2A (see Figure 12). There is another situation to consider in systems where the output will be held high when the input to the LT3688 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LT3688's output. If the V_{IN} pin is allowed to float and the EN/UVLO pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT3688's internal circuitry will pull its quiescent current through its SW pin. This is fine if the system can tolerate a few mA in this state. If the EN/UVLO pin is grounded, the SW pin current will drop to essentially zero.

However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT3688 can pull large currents from the output through the SW pin and the V_{IN} pin. Figure 13 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

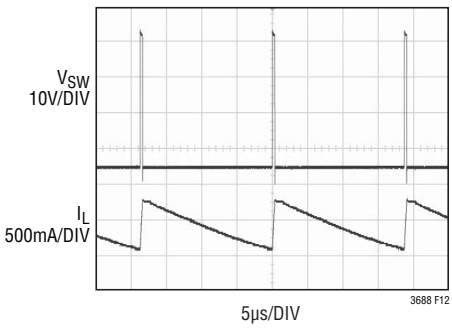

Figure 12. The LT3688 Reduces Its Frequency to Below 70kHz to Protect Against Shorted Output with 36V Input

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 14 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3688's V_{IN}, DA and SW pins, the catch diode (D1) and the input capacitor (C1). The loop formed by

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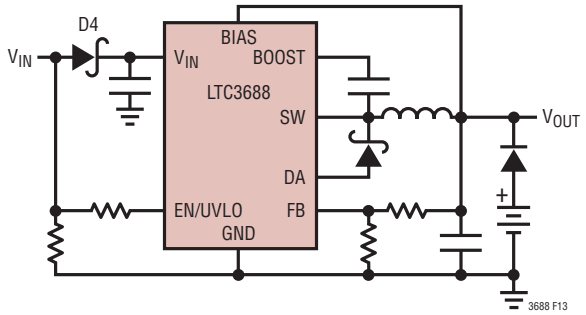

Figure 13. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output; It Also Protects the Circuit from a Reversed Input. The LT3688 Runs Only When the Input Is Present

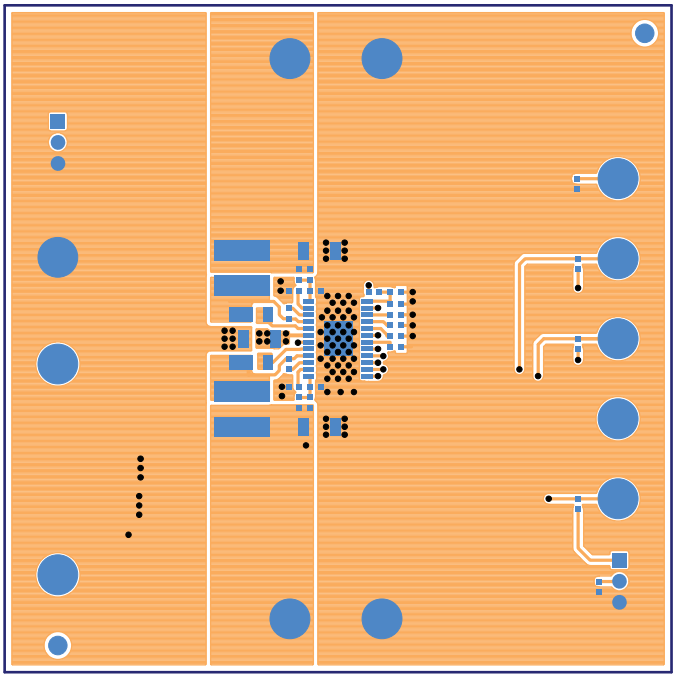

Figure 14. Top Layer PCB Layout in the LT3688 Demonstration Board

these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board.

Place a local, unbroken ground plane below these components. The SW and BST nodes should be as small as possible. Finally, keep the FB node small so that the ground traces will shield them from the SW and BST nodes.

The exposed pad on the bottom of the package must be soldered to ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT3688 to additional ground planes within the circuit board and on the bottom side.

High Temperature Considerations

The PCB must provide heat sinking to keep the LT3688 cool. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3688. Placing additional vias can reduce thermal resistance further. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to θ_{JA} = 40°C/W or less. With 100 LFPM airflow, this resistance can fall by another 25%. Further increases in airflow will lead to lower thermal resistance. Because of the large output current capability of the LT3688, it is possible to dissipate enough heat to raise the junction temperature beyond the absolute maximum of 125°C (150°C for H Grade). When operating at high ambient temperatures, the maximum load current should be derated as the ambient temperature approaches 125°C (150°C for H Grade). Power dissipation within the LT3688 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode loss. The die temperature is calculated by multiplying the LT3688 power dissipation by the thermal resistance from junction-to-ambient. Thermal resistance depends on the layout of the circuit board, but values from 30°C/W to 60°C/W are typical. Die temperature rise was measured on a 4-layer, 5cm • 7.5cm circuit board in still air at a load current of 0.8A (f_{SW} = 800kHz). For a 12V input to 3.3V output the die temperature elevation above ambient was 14°C; for $12V_{IN}$ to $5V_{OUT}$ the rise was 15°C and for $12V_{IN}$ to $5V_{OUT}$ and $3.3V_{OUT}$ the rise was 30°C.

Other Linear Technology Publications

Application Notes 19, 35 and 44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 318 shows how to generate a bipolar output supply using a buck regulator.

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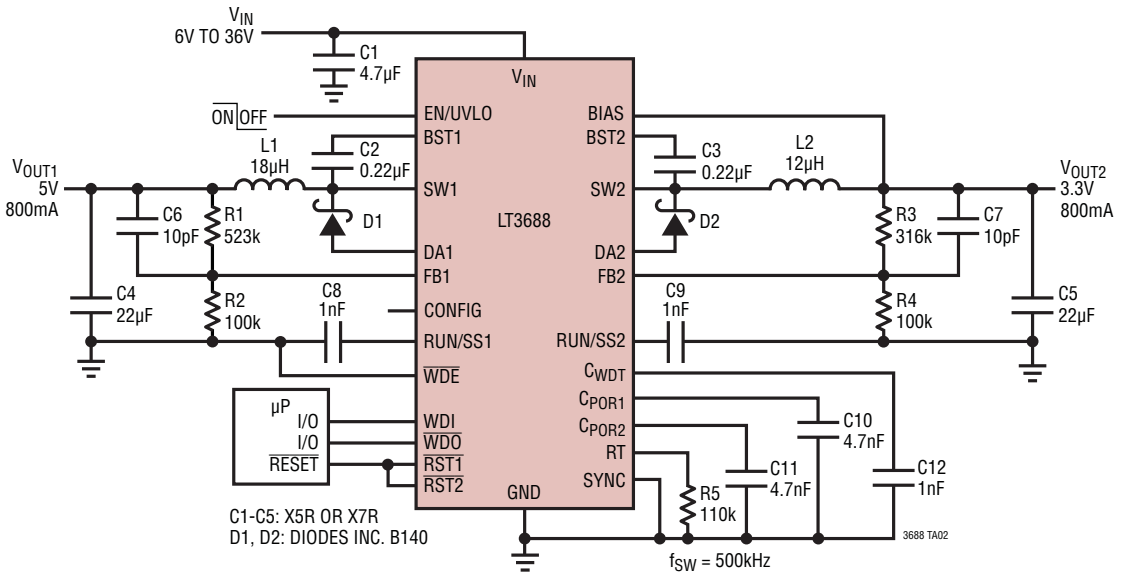
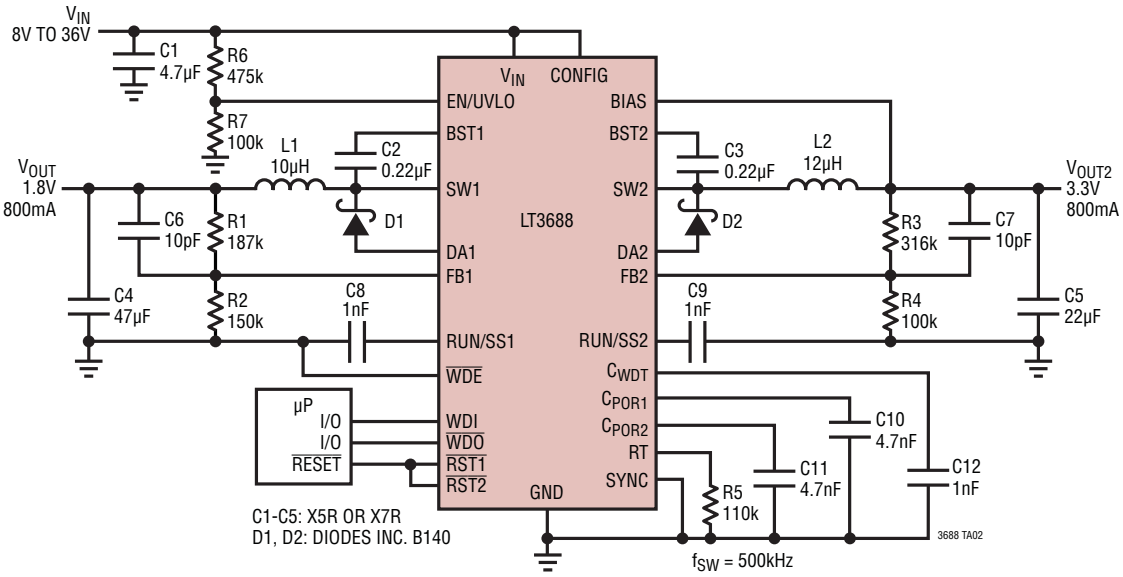
TYPICAL APPLICATIONS



5V and 3.3V Regulator with Power-On Reset and Watchdog Timers



3.3V and 1.8V Regulator with Power-On Reset and Watchdog Timers and Input Under Voltage Lockout

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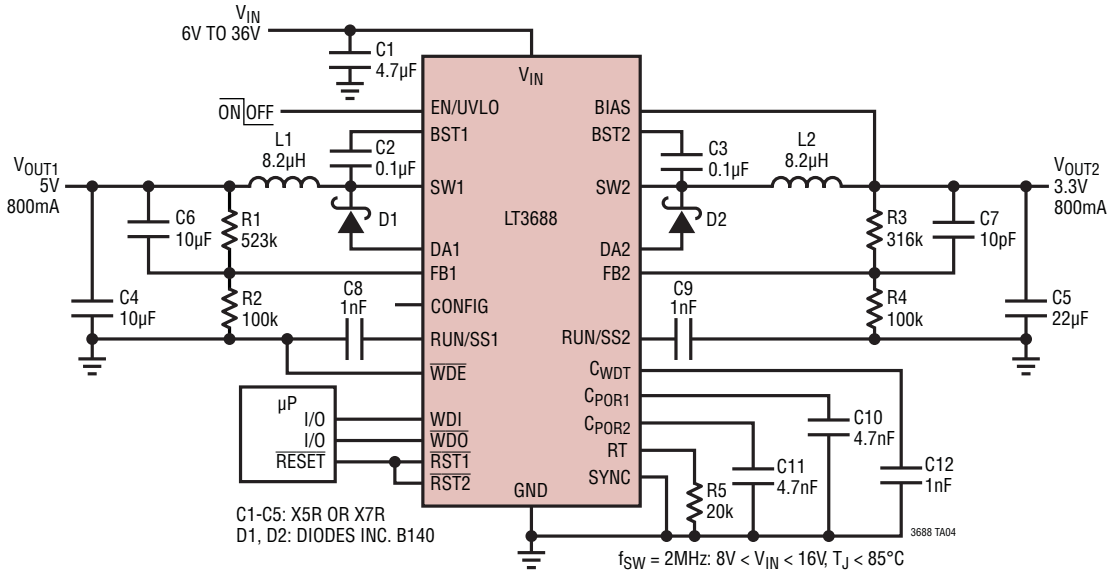
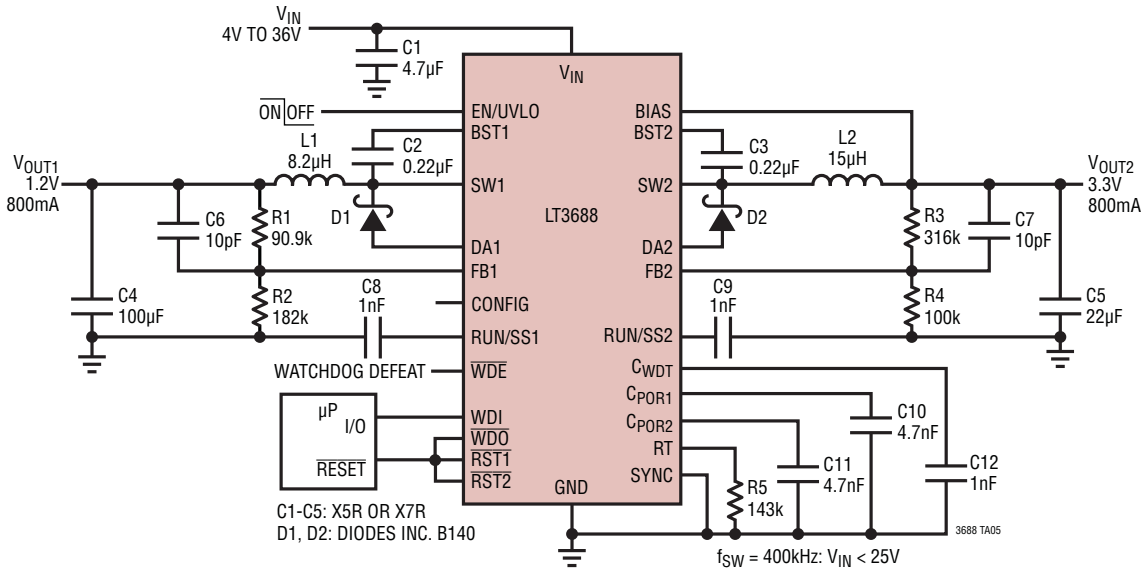
TYPICAL APPLICATIONS



2MHz Switching Frequency, 5V and 3.3V Regulator with Power-On Reset and Watchdog Timers



3.3V and 1.2V Regulator with Power-On Reset Timer and Defeatable Watchdog, Timing Error Resets Microprocessor

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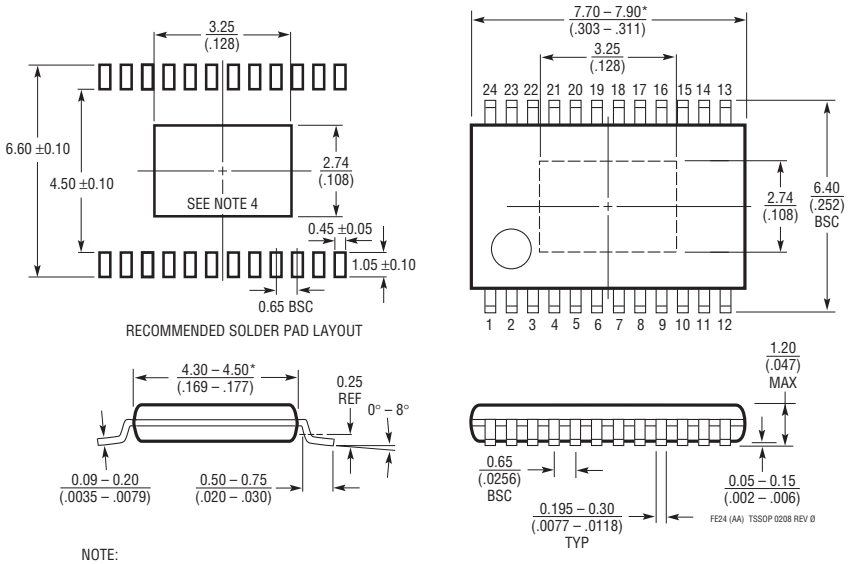
PACKAGE DESCRIPTION

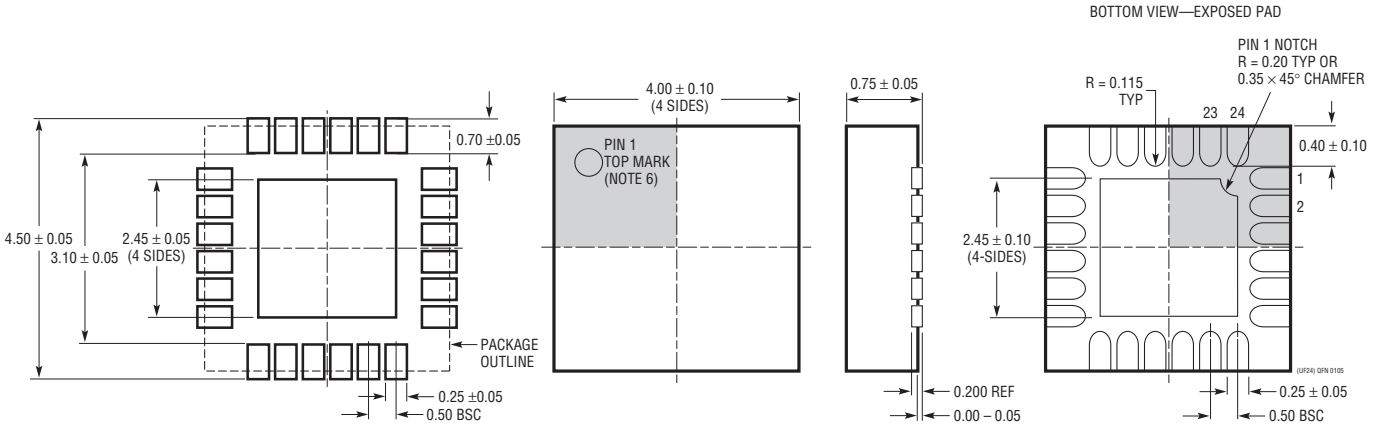
FE Package
24-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1771 Rev Ø)

Variation AA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

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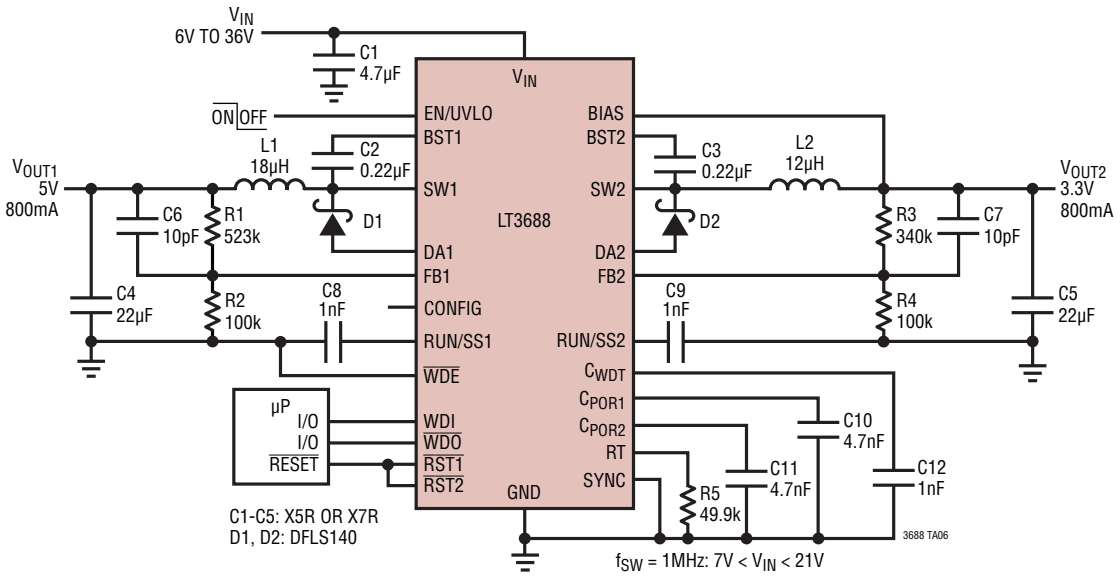
TYPICAL APPLICATION



1MHz 5V and 3.3V Regulator with Power-On Reset and Watchdog Timers

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3640	35V, 55V MAX, Dual (1.3A, 1.1A), 2.5MHz High Efficiency Step-Down DC/DC Converter with POR Reset and Watchdog Timer	V_{IN} Min = 4V, V_{IN} Max = 35V, Transient to 55V, $V_{OUT(MIN)}$ = 0.6V, I_Q = <290µA, I_{SD} = <1µA, 4mm × 5mm QFN-28 TSSOP-28E Package
LT3689/LT3689–5	36V, 60V Transient Protection, 800mA, 2.2MHz High Efficiency MicroPower Step-Down DC/DC Converter with POR Reset and Watchdog Timer	V_{IN} Min = 3.6V, V_{IN} Max = 36V, Transient to 60V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} = <1µA, 3mm × 3mm QFN-16 Package
LT3686	37V, 55Vmax, 1.2A, 2.5MHz High Efficiency Step-Down DC/DC Converter	V_{IN} Min = 3.6V, V_{IN} Max = 37V, Transient to 55V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 1.1mA, I_{SD} = <1µA, 3mm × 3mm DFN-10 Package
LT3682	36V, 60Vmax, 1A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter	V_{IN} Min = 3.6V, V_{IN} Max = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} = <1µA, 3mm × 3mm DFN-12 Package
LT3971	38V, 1.2A (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with only 2.8uA of Quiescent Current	V_{IN} Min = 4.2V, V_{IN} Max = 38V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.8µA, I_{SD} = <1µA, 3mm × 3mm DFN-10, MSOP-10E Package
LT3991	55V, 1.2A (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with only 2.8uA of Quiescent Current	V_{IN} Min = 4.2V, V_{IN} Max = 55V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.8µA, I_{SD} = <1µA, 3mm × 3mm DFN-10, MSOP-10E Package
LT3970	40V, 350mA (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with only 2.5uA of Quiescent Current	V_{IN} Min = 4.2V, V_{IN} Max = 40V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5µA, I_{SD} = <1µA, 2mm × 3mm DFN-10, MSOP-10E Package
LT3990	60V, 350mA (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with only 2.5uA of Quiescent Current	V_{IN} Min = 4.2V, V_{IN} Max = 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5µA, I_{SD} = <1µA, 3mm × 3mm DFN-10, MSOP-16E Package

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