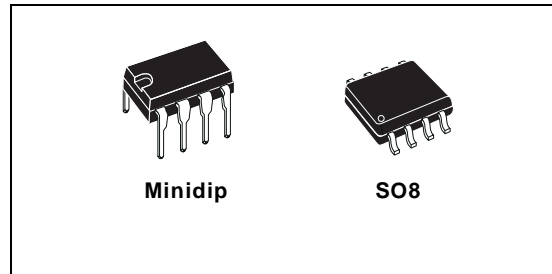




# UC3842T UC3843T UC3844T UC3845T

## HIGH PERFORMANCE CURRENT MODE PWM CONTROLLER

- TRIMMED OSCILLATOR FOR PRECISE FREQUENCY CONTROL
- OSCILLATOR FREQUENCY GUARANTEED AT 250kHz
- CURRENT MODE OPERATION TO 500kHz
- AUTOMATIC FEED FORWARD COMPENSATION
- LATCHING PWM FOR CYCLE-BY-CYCLE CURRENT LIMITING
- INTERNALLY TRIMMED REFERENCE WITH UNDERVOLTAGE LOCKOUT
- HIGH CURRENT TOTEM POLE OUTPUT
- UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LOW START-UP AND OPERATING CURRENT



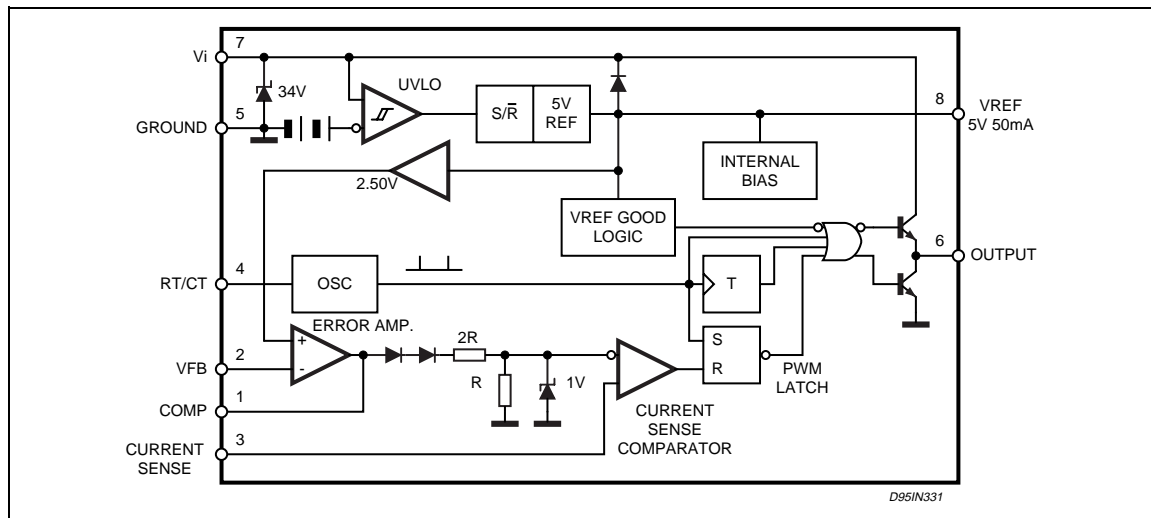
comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842T and UC3844T have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC3843T and UC3845T are 8.5 V and 7.9 V. The UC3842T and UC3843T can operate to duty cycles approaching 100%. A range of zero to < 50 % is obtained by the UC3844T and UC3845T by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

### DESCRIPTION

The UC384XT family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise DUTY CYCLE CONTROL under voltage lock-out featuring start-up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM

### BLOCK DIAGRAM (toggle flip flop used only in UC3844T and UC3845T)



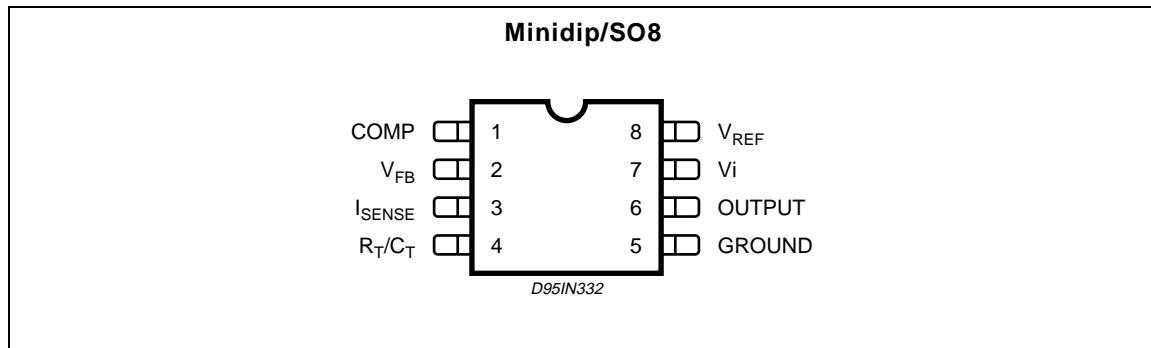
## UC3842T - UC3843T - UC3844T - UC3845T

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_i$	Supply Voltage (low impedance source)	30	V
$V_i$	Supply Voltage ( $I_i < 30\text{mA}$ )	Self Limiting	
$I_o$	Output Current	$\pm 1$	A
$E_o$	Output Energy (capacitive load)	5	$\mu\text{J}$
	Analog Inputs (pins 2, 3)	- 0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
$P_{\text{tot}}$	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (Minidip)	1.25	W
$P_{\text{tot}}$	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (SO8)	800	mW
$T_{\text{stg}}$	Storage Temperature Range	- 65 to 150	$^\circ\text{C}$
$T_L$	Lead Temperature (soldering 10s)	300	$^\circ\text{C}$

\* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

### PIN CONNECTION (top view)



### PIN FUNCTIONS

No	Function	Description
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	$V_{\text{FB}}$	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	$I_{\text{SENSE}}$	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	$R_T/C_T$	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor $R_T$ to $V_{\text{ref}}$ and capacitor $C_T$ to ground. Operation to 500kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	$V_{\text{CC}}$	This pin is the positive supply of the control IC.
8	$V_{\text{ref}}$	This is the reference output. It provides charging current for capacitor $C_T$ through resistor $R_T$ .

### ORDERING NUMBERS

SO8	Minidip
UC3842TD	UC3842TN
UC3843TD	UC3843TN
UC3844TD	UC3844TN
UC3845TD	UC3845TN

**THERMAL DATA**

Symbol	Description	Minidip	SO8	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient.	max. 100	150	°C/W

**ELECTRICAL CHARACTERISTICS** ( [note 1] Unless otherwise stated, these specifications apply for  $0 \leq T_{amb} \leq 105^{\circ}\text{C}$ ;  $V_i = 15\text{V}$  (note 5);  $R_T = 10\text{K}$ ;  $C_T = 3.3\text{nF}$ )

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>REFERENCE SECTION</b>						
$\Delta V_{REF}$	Line Regulation	$12\text{V} \leq V_i \leq 25\text{V}$		2	20	mV
$\Delta V_{REF}$	Load Regulation	$1 \leq I_o \leq 20\text{mA}$		3	25	mV
$\Delta V_{REF}/\Delta T$	Temperature Stability	(Note 2)		0.2		mV/°C
	Total Output Variation	Line, Load, Temperature	4.85		5.15	V
$e_N$	Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}$ $T_j = 25^{\circ}\text{C}$ (note 2)		50		$\mu\text{V}$
	Long Term Stability	$T_{amb} = 125^{\circ}\text{C}$ , 1000Hrs (note 2)		5	25	mV
$I_{SC}$	Output Short Circuit		-30	-100	-180	mA
<b>OSCILLATOR SECTION</b>						
$f_{osc}$	Frequency	$T_j = 25^{\circ}\text{C}$ $T_A = T_{low}$ to $T_{high}$ $T_j = 25^{\circ}\text{C}$ ( $R_T = 6.2\text{K}$ , $C_T = 1\text{nF}$ )	49 48 225	52 – 250	55 56 275	KHz KHz KHz
$\Delta f_{osc}/\Delta V$	Frequency Change with Volt.	$V_{CC} = 12\text{V}$ to $25\text{V}$	–	0.2	1	%
$\Delta f_{osc}/\Delta T$	Frequency Change with Temp.	$T_A = T_{low}$ to $T_{high}$	–	1	–	%
$V_{OSC}$	Oscillator Voltage Swing	(peak to peak)	–	1.6	–	V
$I_{dischg}$	Discharge Current ( $V_{OSC} = 2\text{V}$ )	$T_A = T_{low}$ to $T_{high}$	7.3	–	8.8	mA
<b>ERROR AMP SECTION</b>						
$V_2$	Input Voltage	$V_{PIN1} = 2.5\text{V}$	2.42	2.50	2.58	V
$I_b$	Input Bias Current	$V_{FB} = 5\text{V}$		-0.1	-2	$\mu\text{A}$
	$A_{VOL}$	$2\text{V} \leq V_o \leq 4\text{V}$	65	90		dB
BW	Unity Gain Bandwidth	$T_j = 25^{\circ}\text{C}$	0.7	1		MHz
PSRR	Power Supply Rejec. Ratio	$12\text{V} \leq V_i \leq 25\text{V}$	60	70		dB
$I_o$	Output Sink Current	$V_{PIN2} = 2.7\text{V}$ $V_{PIN1} = 1.1\text{V}$	2	12		mA
$I_o$	Output Source Current	$V_{PIN2} = 2.3\text{V}$ $V_{PIN1} = 5\text{V}$	-0.5	-1		mA
	$V_{OUT}$ High	$V_{PIN2} = 2.3\text{V}$ ; $R_L = 15\text{K}\Omega$ to Ground	5	6.2		V
	$V_{OUT}$ Low	$V_{PIN2} = 2.7\text{V}$ ; $R_L = 15\text{K}\Omega$ to Pin 8		0.8	1.1	V
<b>CURRENT SENSE SECTION</b>						
$G_V$	Gain	(note 3 & 4)	2.85	3	3.15	V/V
$V_3$	Maximum Input Signal	$V_{PIN1} = 5\text{V}$ (note 3)	0.9	1	1.1	V
SVR	Supply Voltage Rejection	$12 \leq V_i \leq 25\text{V}$ (note 3)		70		dB
$I_b$	Input Bias Current			-2	-10	$\mu\text{A}$
	Delay to Output			100	300	ns



## UC3842T - UC3843T - UC3844T - UC3845T

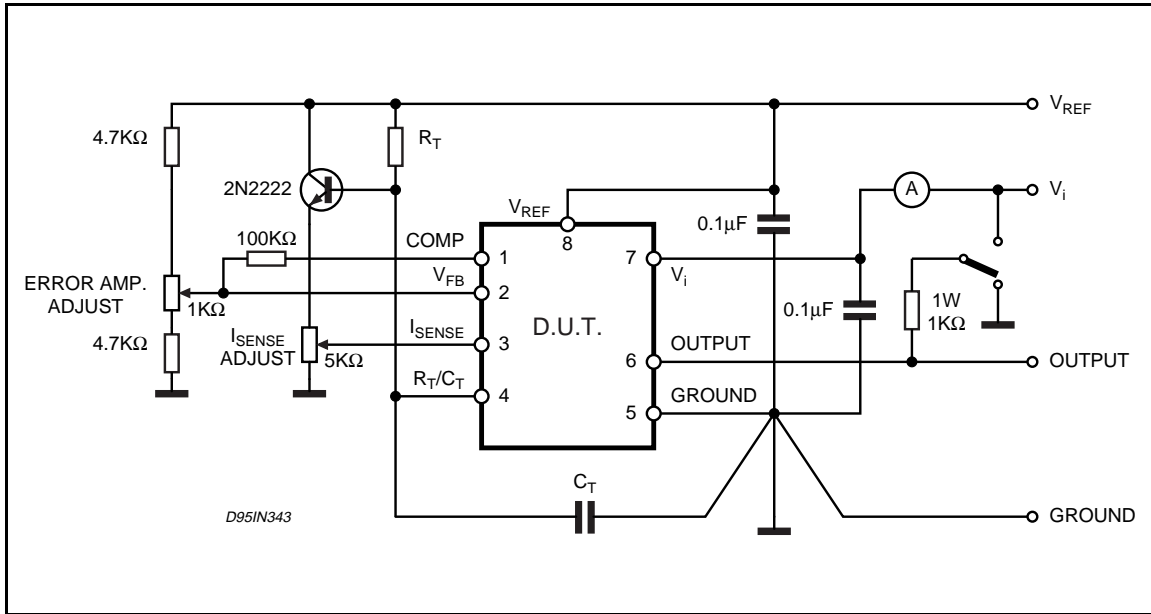
### ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>OUTPUT SECTION</b>						
V <sub>OL</sub>	Output Low Level	I <sub>SINK</sub> = 20mA		0.1	0.4	V
		I <sub>SINK</sub> = 200mA		1.6	2.2	V
V <sub>OH</sub>	Output High Level	I <sub>SOURCE</sub> = 20mA	13	13.5		V
		I <sub>SOURCE</sub> = 200mA	12	13.5		V
V <sub>OLS</sub>	UVLO Saturation	VCC = 6V; I <sub>SINK</sub> = 1mA		0.1	1.1	V
t <sub>r</sub>	Rise Time	T <sub>J</sub> = 25°C C <sub>L</sub> = 1nF (2)		50	150	ns
t <sub>f</sub>	Fall Time	T <sub>J</sub> = 25°C C <sub>L</sub> = 1nF (2)		50	150	ns
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>						
	Start Threshold	UC3842T/4T	15	16	17	V
		UC3843T/5T	7.8	8.4	9.0	V
	Min Operating Voltage After Turn-on	UC3842T/4T	9	10	11	V
		UC3843T/5T	7.0	7.6	8.2	V
<b>PWM SECTION</b>						
	Maximum Duty Cycle	UC3842T/3T	94	96	100	%
		UC3844T/5T	47	48	50	%
	Minimum Duty Cycle			0	%	
<b>TOTAL STANDBY CURRENT</b>						
I <sub>st</sub>	Start-up Current	V <sub>i</sub> = 6.5V for UC3843T/45T		0.3	0.5	mA
		V <sub>i</sub> = 14V for UC3842T/44T		0.3	0.5	mA
I <sub>i</sub>	Operating Supply Current	V <sub>PIN2</sub> = V <sub>PIN3</sub> = 0V		12	17	mA
V <sub>iz</sub>	Zener Voltage	I <sub>i</sub> = 25mA	30	36		V

- Notes :**
1. Max package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T<sub>J</sub> as close to T<sub>amb</sub> as possible.
  2. These parameters, although guaranteed, are not 100% tested in production.
  3. Parameter measured at trip point of latch with V<sub>PIN2</sub> = 0.
  4. Gain defined as :  

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} ; 0 \leq V_{PIN3} \leq 0.8 \text{ V}$$
  5. Adjust V<sub>i</sub> above the start threshold before setting at 15 V.

Figure 1: Open Loop Test Circuit.



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close

to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 2: Timing Resistor vs. Oscillator Frequency

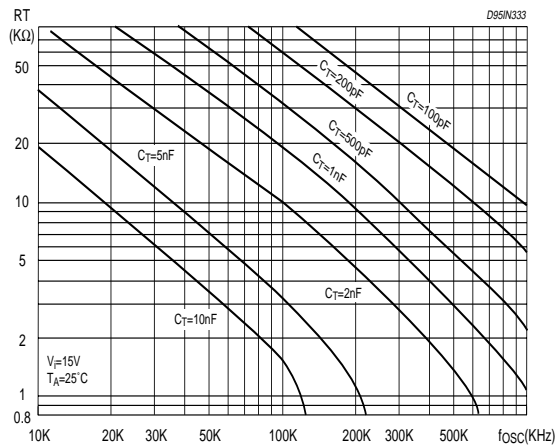
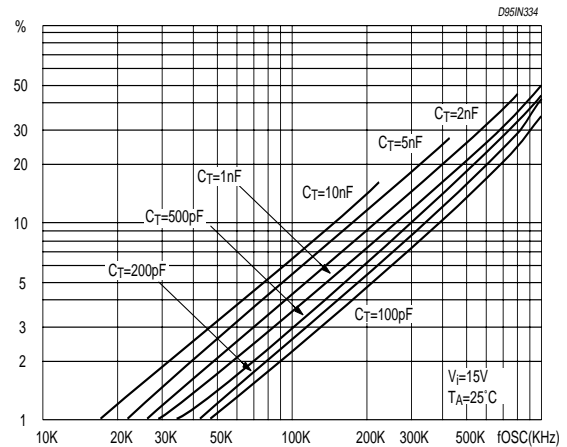
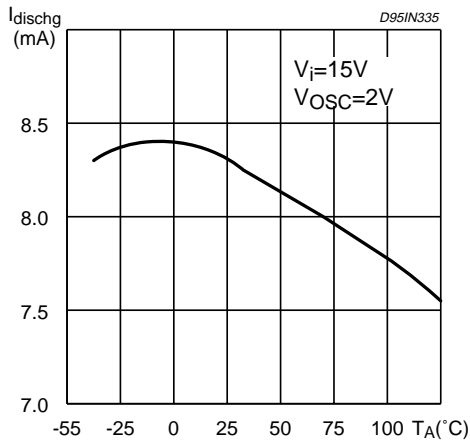


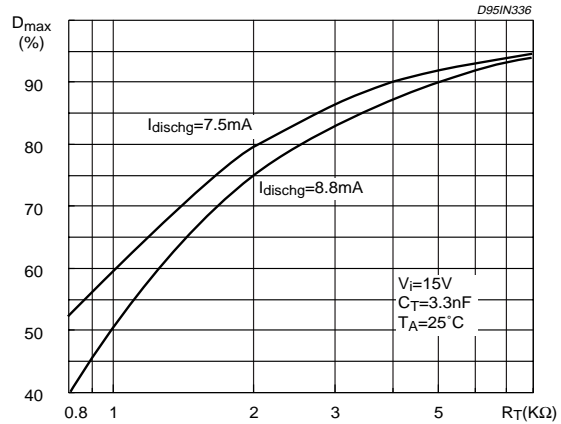
Figure 3: Output Dead-Time vs. Oscillator Frequency



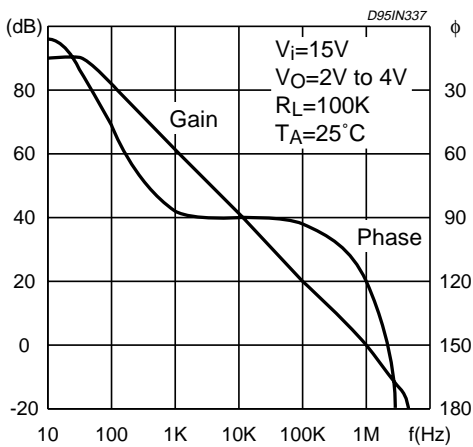
**Figure 4:** Oscillator Discharge Current vs. Temperature.



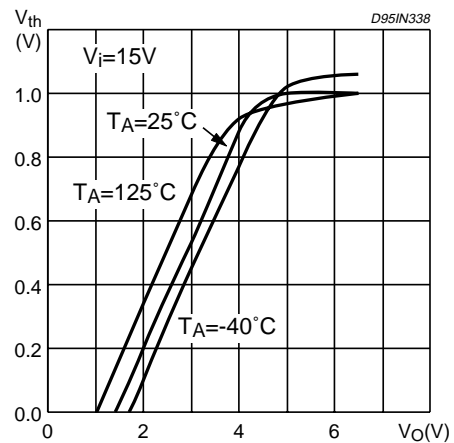
**Figure 5:** Maximum Output Duty Cycle vs. Timing Resistor.



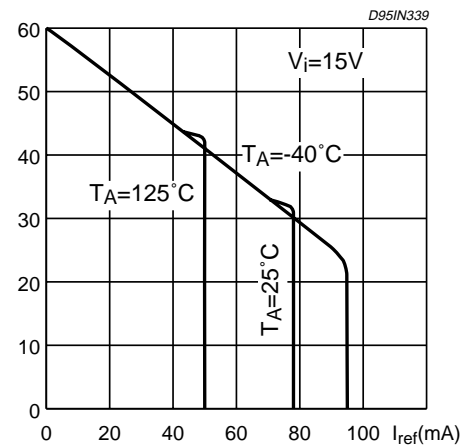
**Figure 6:** Error Amp Open-Loop Gain and Phase vs. Frequency.



**Figure 7:** Current Sense Input Threshold vs. Error Amp Output Voltage.



**Figure 8:** Reference Voltage Change vs. Source Current.



**Figure 9:** Reference Short Circuit Current vs. Temperature.

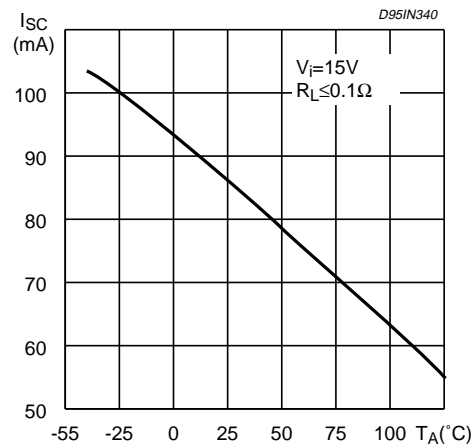


Figure 10: Output Saturation Voltages vs. Load Current.

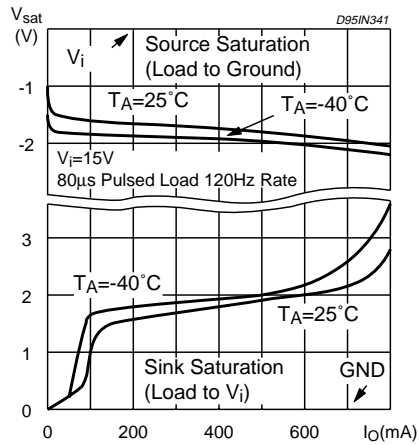


Figure 12: Output Waveform.

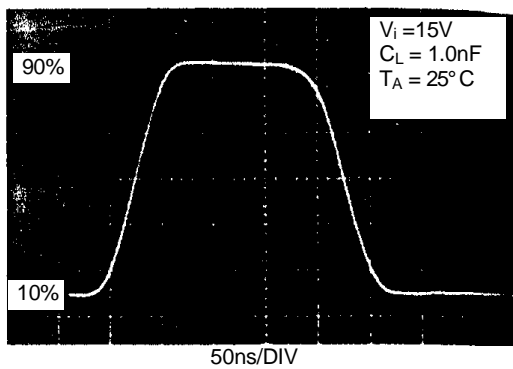


Figure 11: Supply Current vs. Supply Voltage.

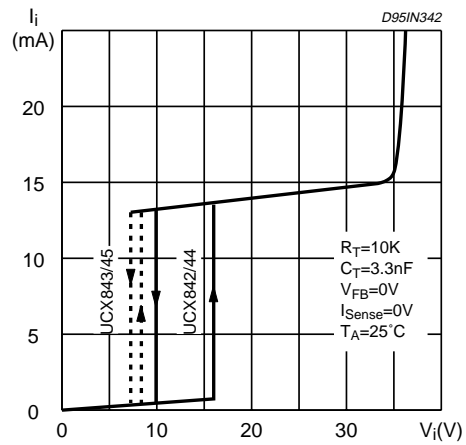


Figure 13: Output Cross Conduction

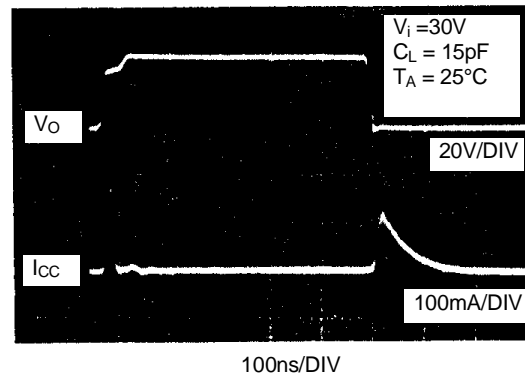
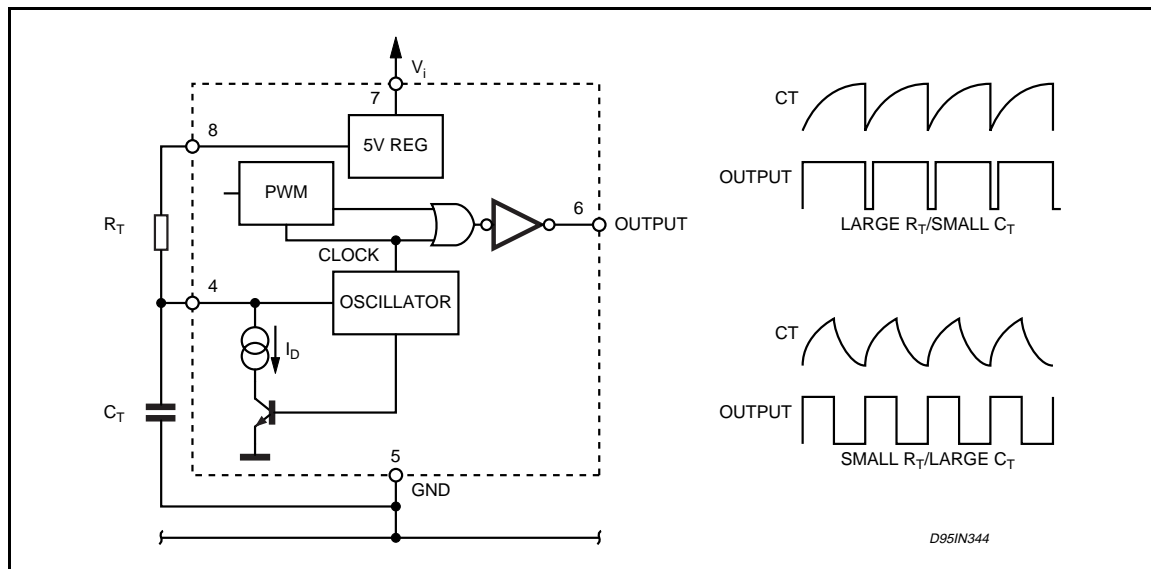


Figure 14: Oscillator and Output Waveforms.



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Figure 15 : Error Amp Configuration.

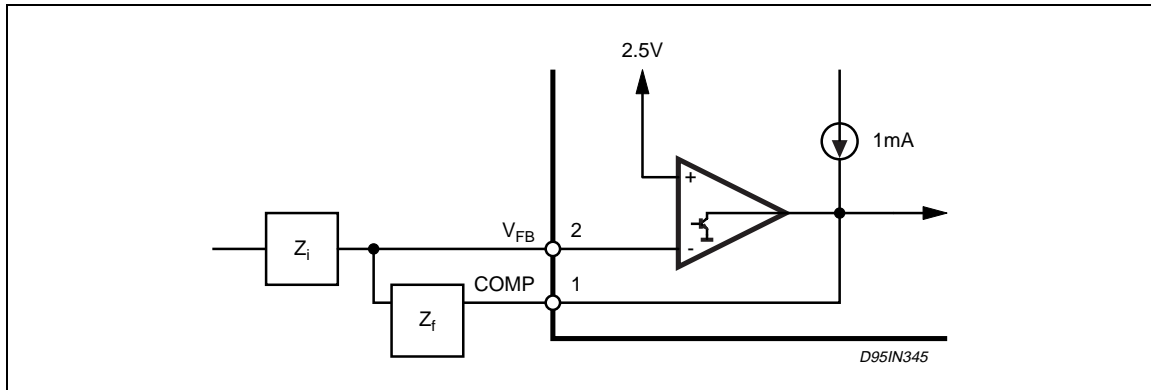


Figure 16 : Under Voltage Lockout.

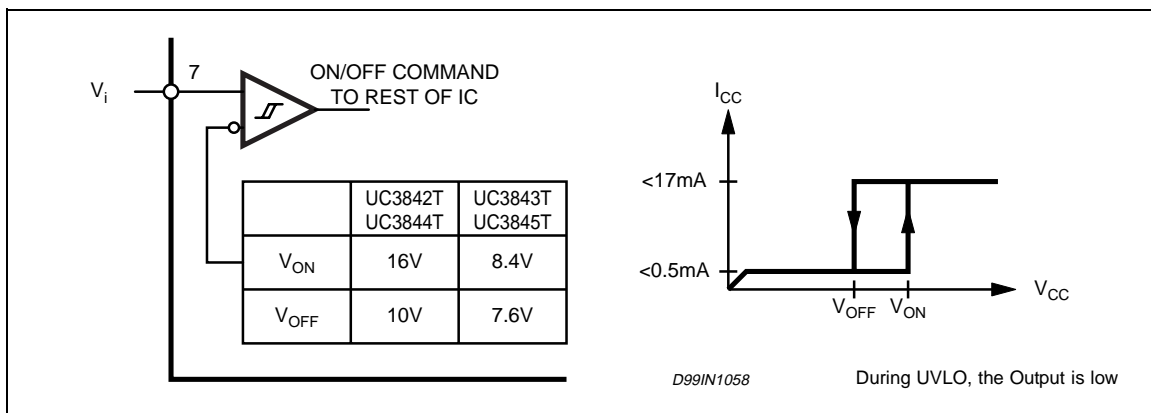
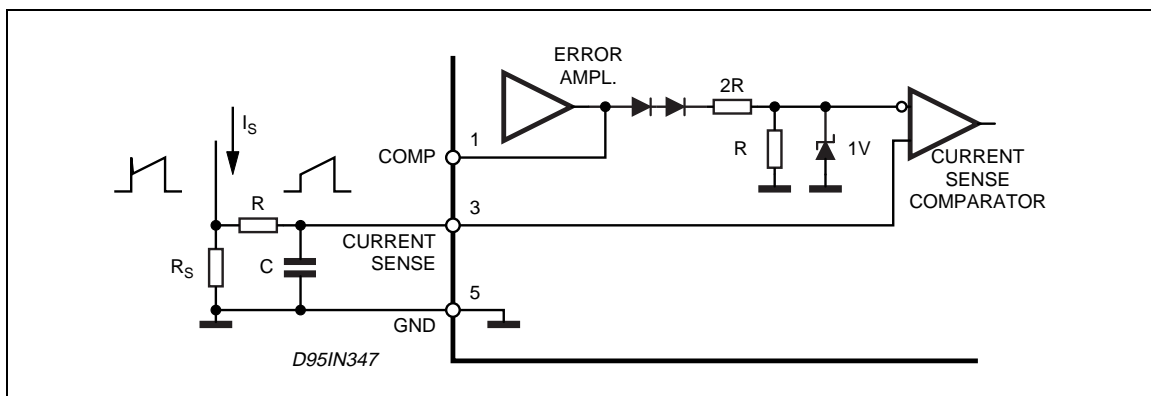


Figure 17 : Current Sense Circuit .



Peak current ( $i_s$ ) is determined by the formula

$$I_{S \max} \approx \frac{1.0 \text{ V}}{R_s}$$

A small RC filter may be required to suppress switch transients.



Figure 18 : Slope Compensation Techniques.

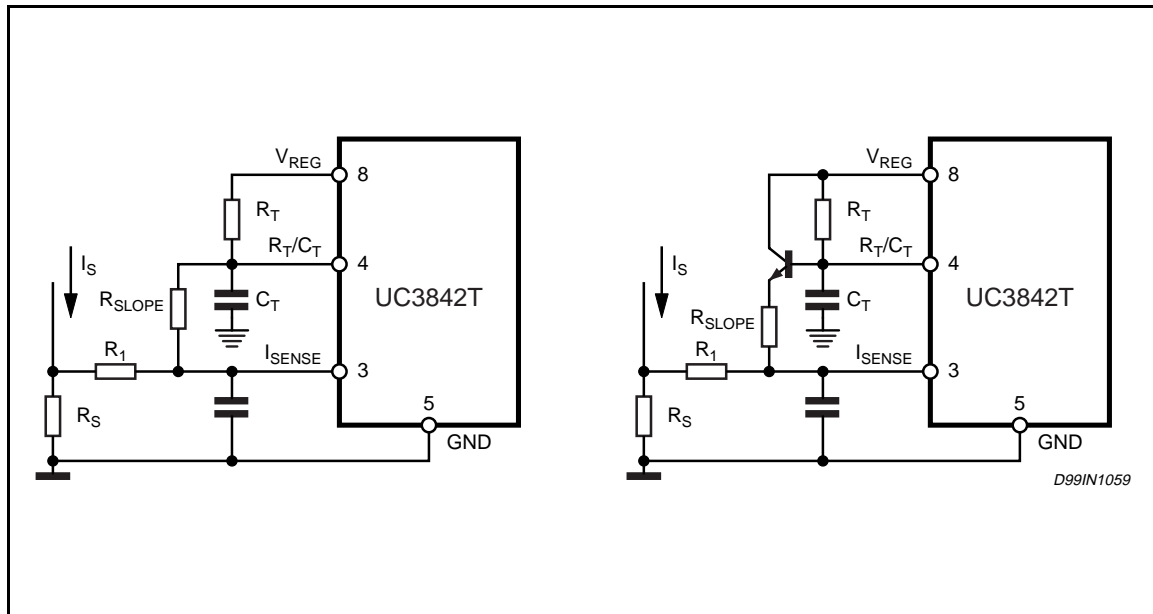


Figure 19 : Isolated MOSFET Drive and Current Transformer Sensing.

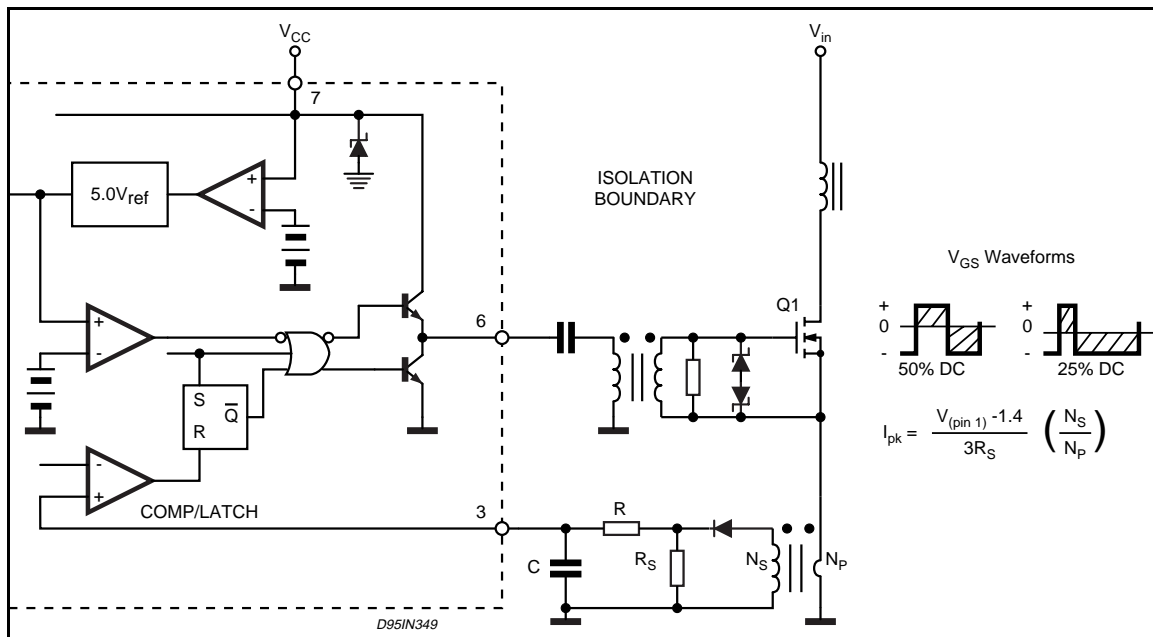


Figure 20 : Latched Shutdown.

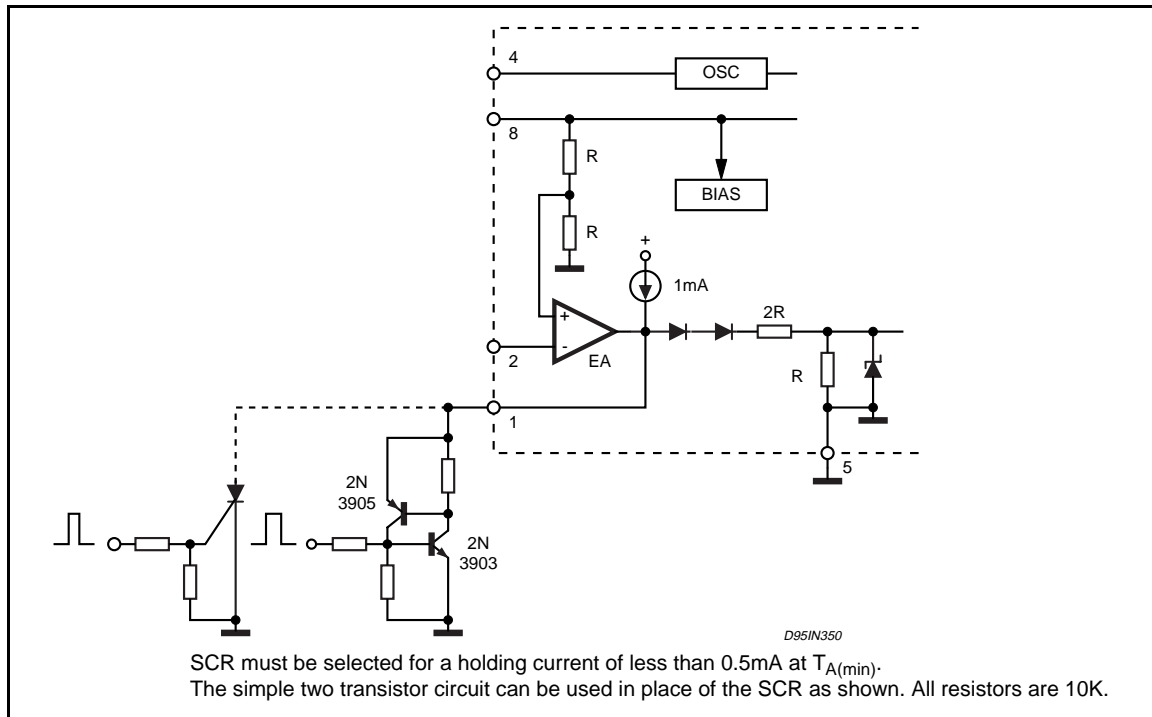


Figure 21: Error Amplifier Compensation

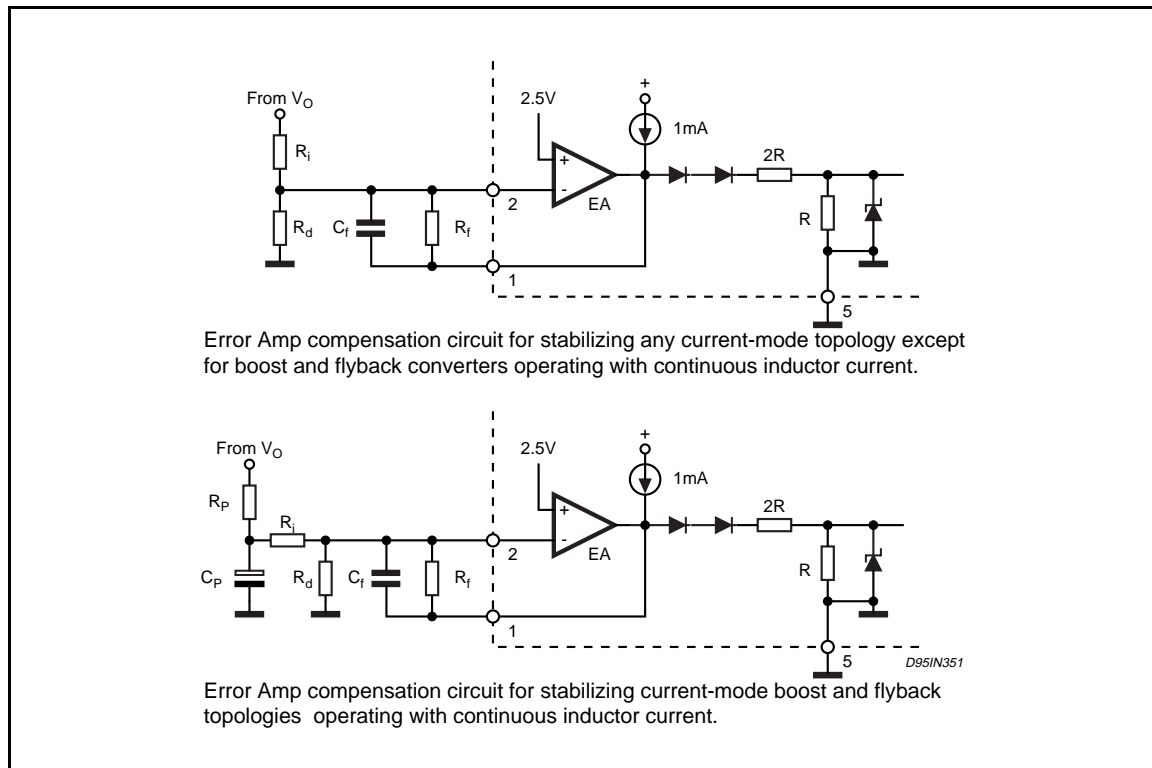


Figure 22: External Clock Synchronization.

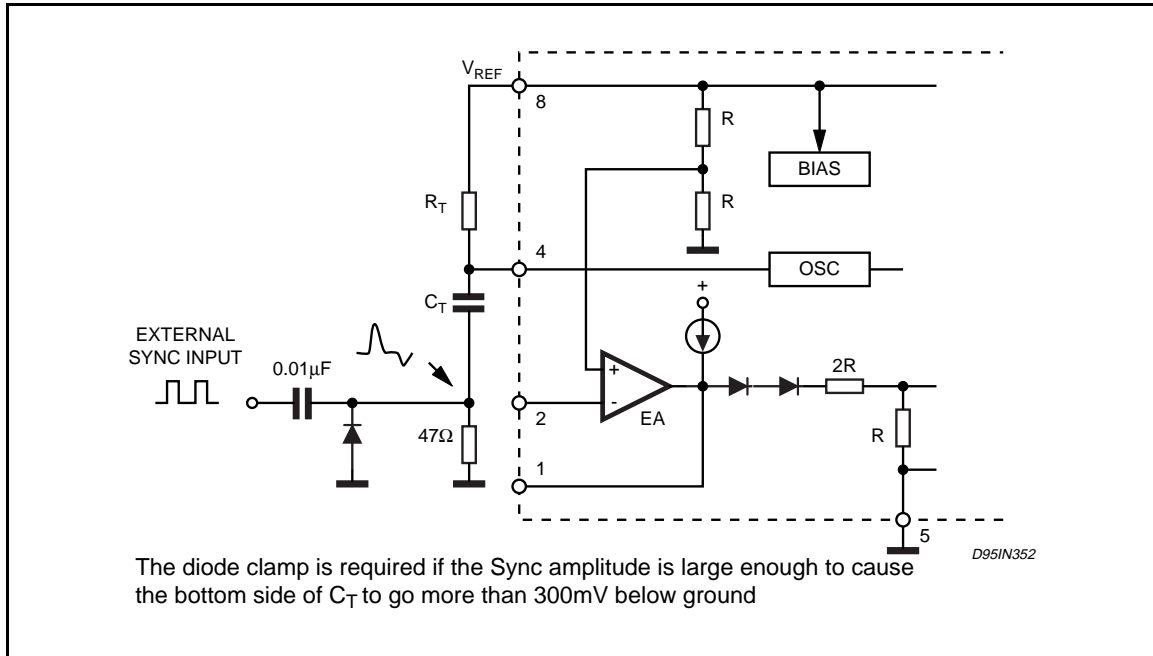


Figure 23: External Duty Cycle Clamp and Multi Unit Synchronization.

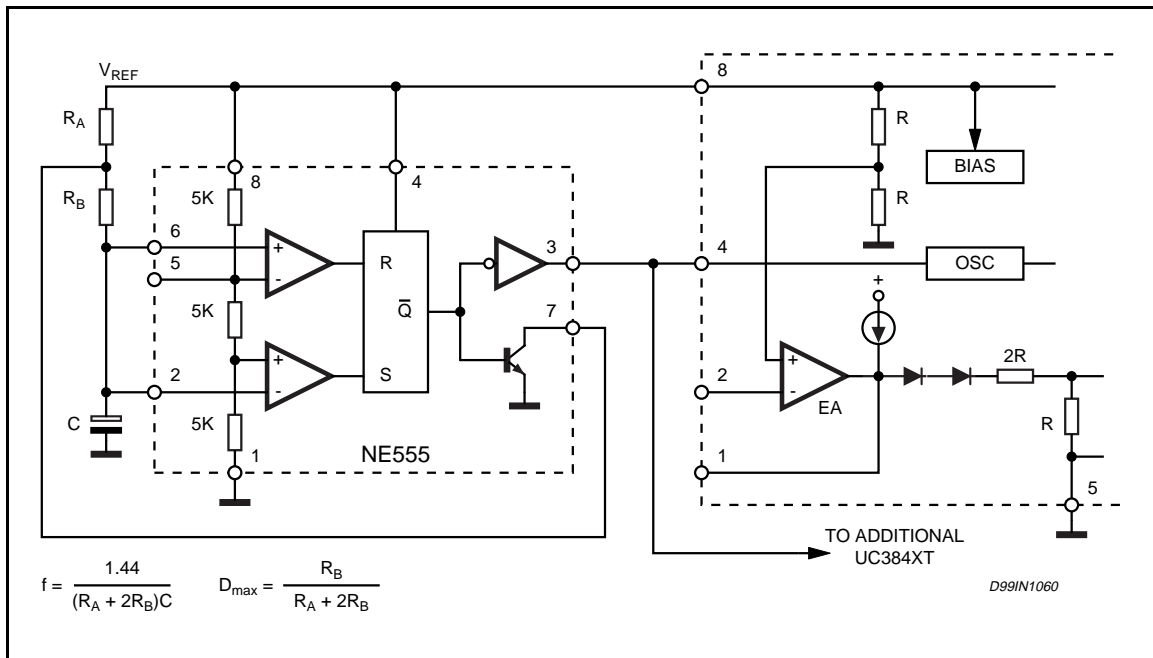


Figure 24: Soft-Start Circuit

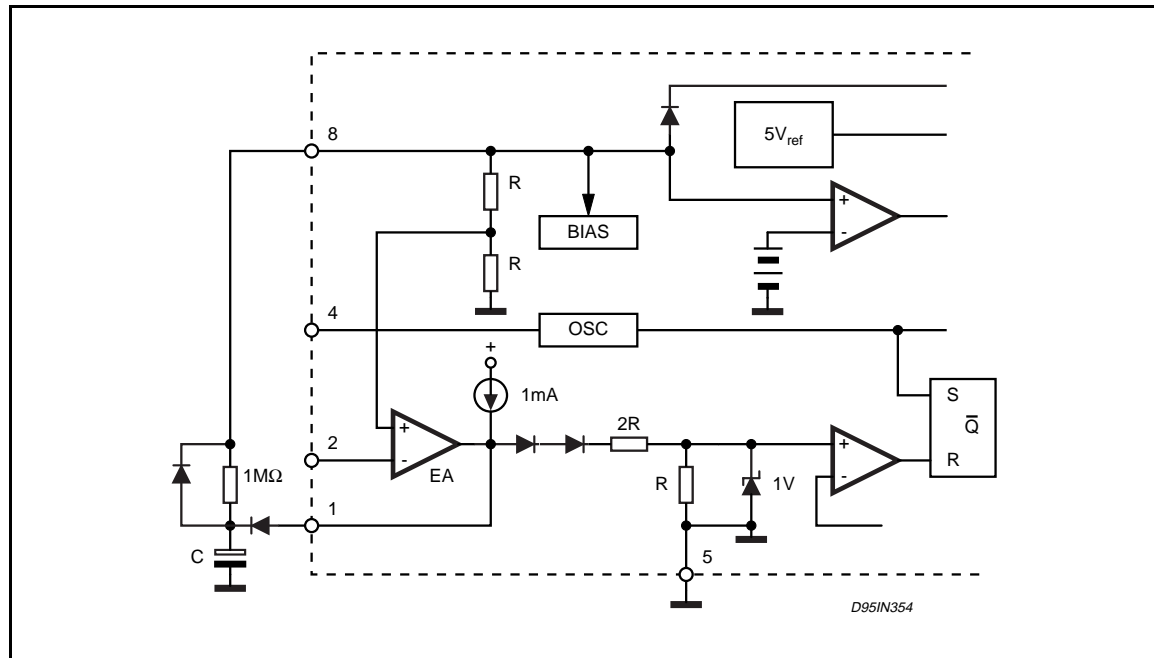
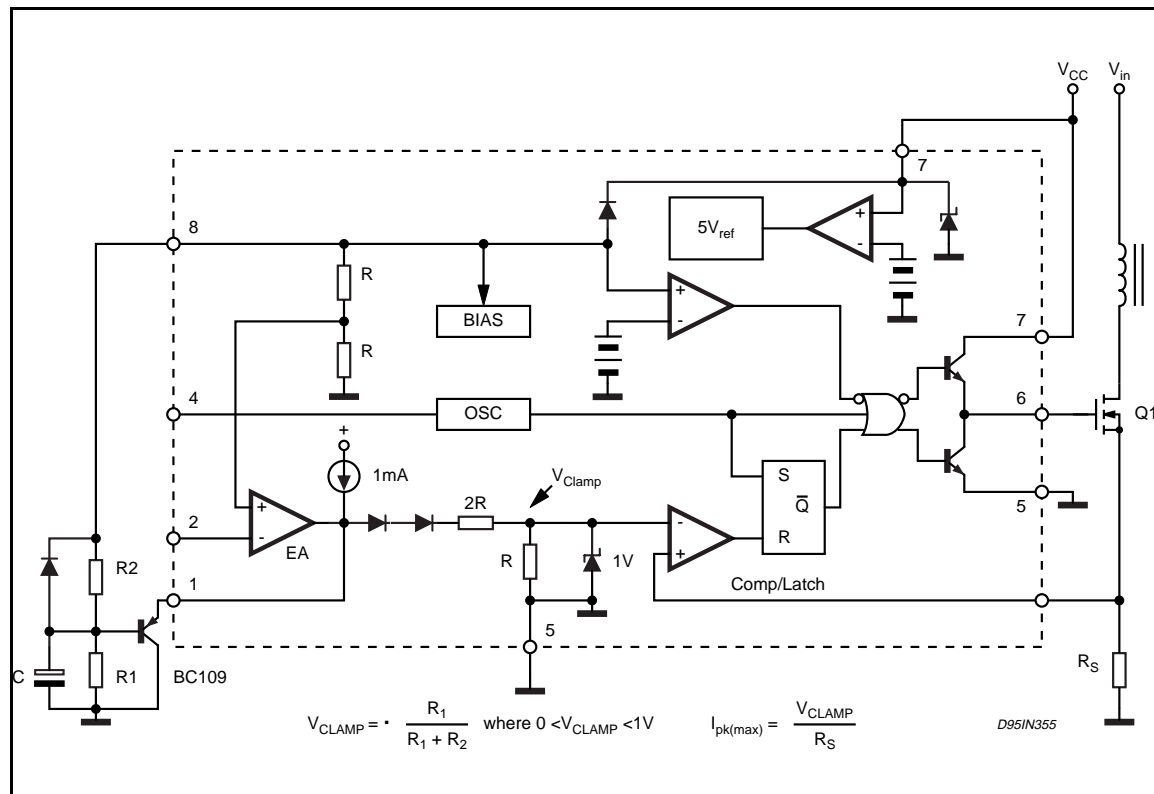
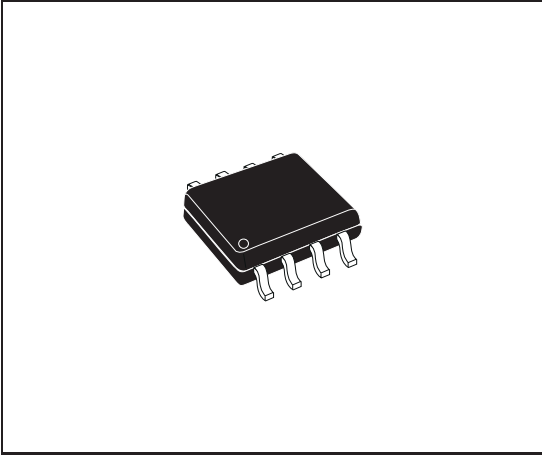


Figure 25: Soft-Start and Error Amplifier Output Duty Cycle Clamp.



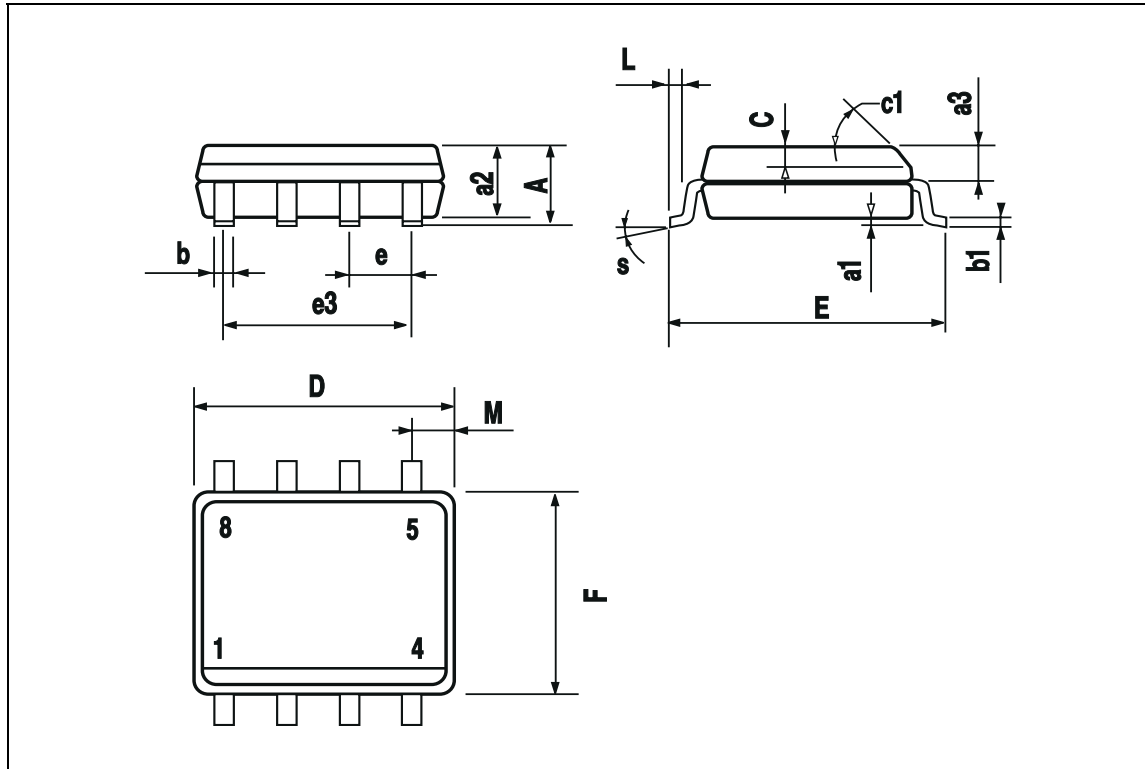
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

**OUTLINE AND MECHANICAL DATA**



**SO8**

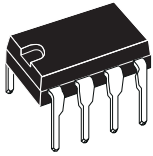
(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).



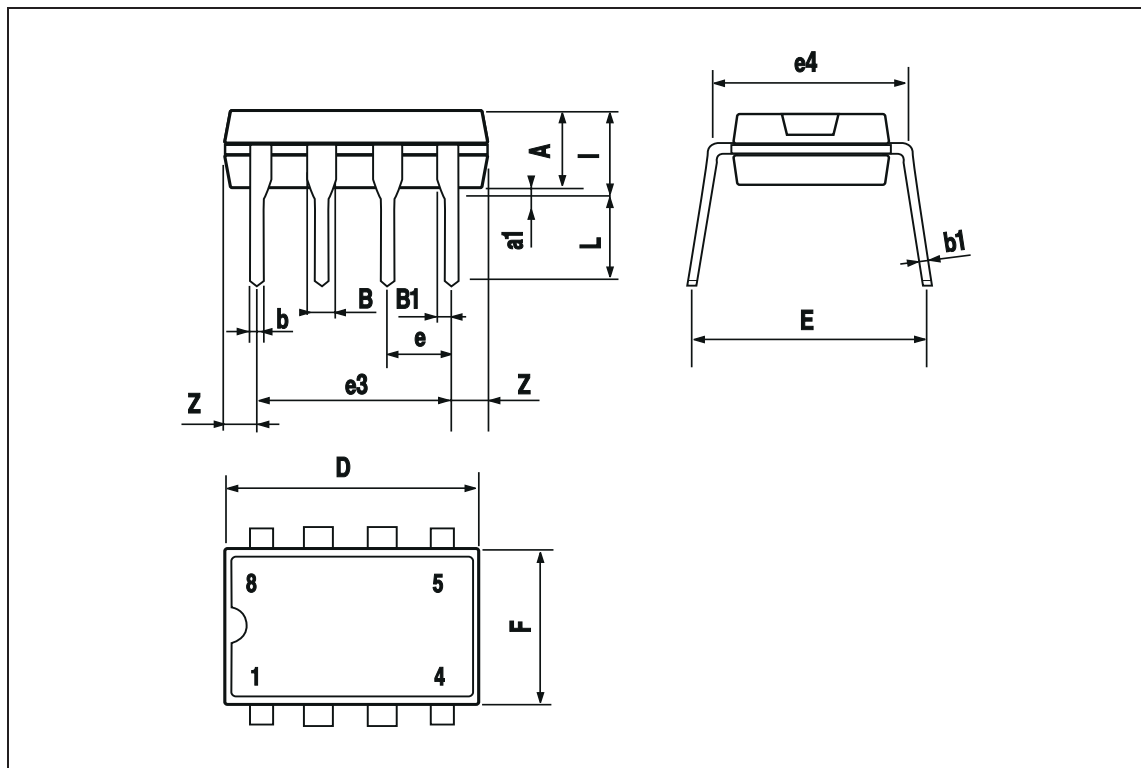
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DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

**OUTLINE AND MECHANICAL DATA**



**Minidip**



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